1. Calculation (2 points)

1）Obtain the 1s and 2s complements of the following unsigned binary numbers.

00011101

1s:11100010

2s:11100011

2）Perform the indicated substraction with the following unsigned binary numbers by taking the 2s complement of the substrahend(减数).

101 – 001000

A:101+111000=111101

1	0	I_2
1	1	I_3

$$Y = \overline{S}_1\overline{S}_0 I_0 + \overline{S}_1 S_0 I_1 + S_1\overline{S}_0 I_2 + S_1 S_0 I_3$$

2） Please write a verilog description for the circuit by using a process containing case statement.

A:

```
module 1_MUX4TO1(S, I, Y);
input wire [1:0] S;
input wire [3:0] I;
output reg       Y;

always @ (*) begin
    case (s)
        2'b00: Y = I[0];
        2'b01: Y = I[1];
        2'b10: Y = I[2];
        2'b11: Y = I[3];
    endcase
end
endmodule
```

```
endmodule
```

3） Please write a verilog description for the circuit by using a process containing if- else statement.

A:

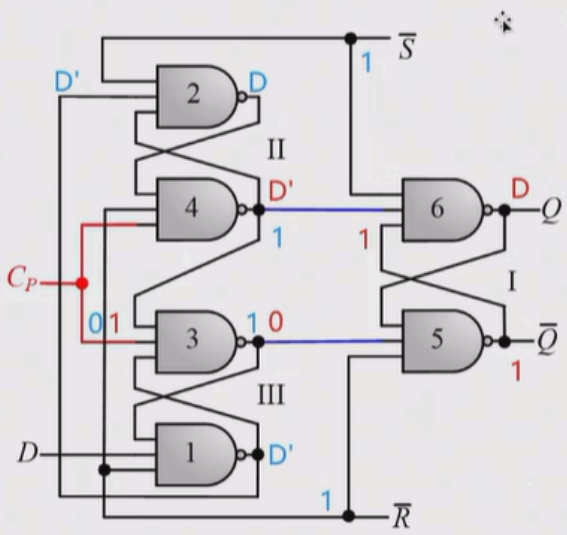
```
module 1_MUX4TO1(S, I, Y);
input wire [1:0] S;
input wire [3:0] I;
output reg       Y;

always @ (*) begin
    if      (s==2'b00) Y = I[0];
    else if (s==2'b01) Y = I[1];
    else if (s==2'b10) Y = I[2];
    else               Y = I[3];
end
endmodule
```

4) Which function does this circuit accomplish? What is the difference between the circuits implemented by the two methods in 2) and 3)? (2points)

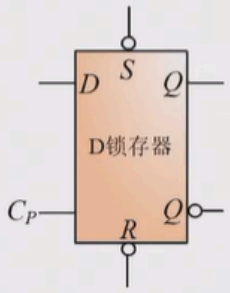
A: 4-to-1 1bit Multiplexer

circuit in 3） have priorities

正边沿维持阻塞型D触发器



异步控制		上升沿触发			
$\overline{R}$	$\overline{S}$	C_P	D	Q	$\overline{Q}$
0	1	×	×	0	1
1	0	×	×	1	0
1	1	↑	0	0	1
1	1	↑	1	1	0

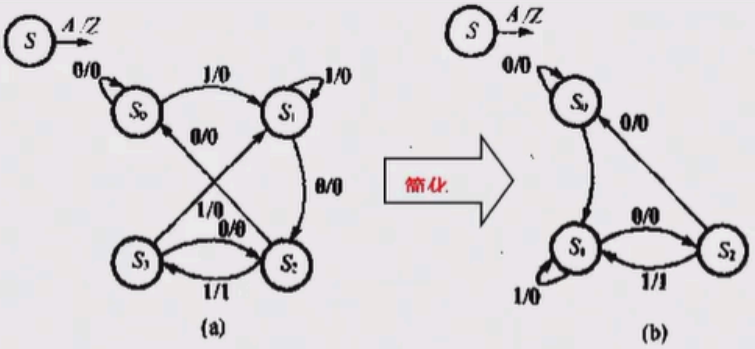


4. Analysis states (10 points)

Please draw the state diagram of "101" sequential detector（simplified as far as possible） and the input、output as following:

(1) Input A: 0 1 0 1 0 1 1 0 1

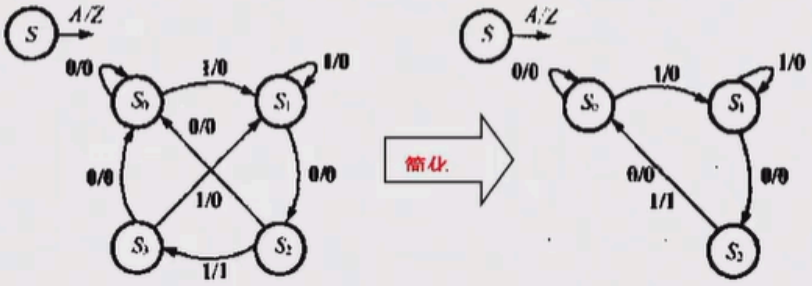
Output Z: 0 0 0 1 0 1 0 0 1



(2) Input A: 0 1 0 1 0 1 1 0 1 0

Output Z: 0 0 0 1 0 0 0 0 1 0

A:

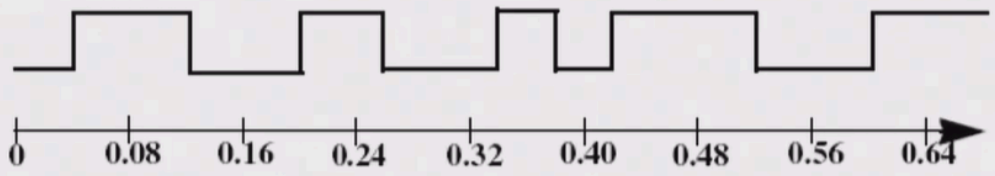


5. Sequential Circuits analysis (20 points)

1)A sequential circuit with two D lip- lops A and B, two inputs X and Y, and one output Z. The state table
following:

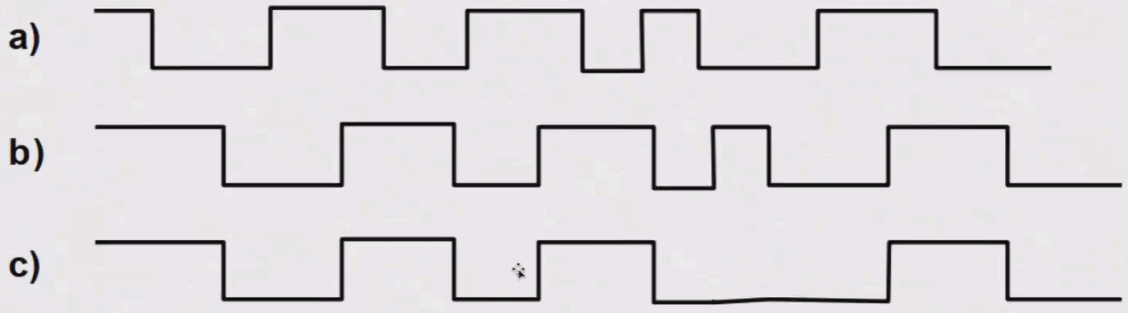
Present state		Inputs		Next state		Output
A	B	X	Y	A	B	Z
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	1	0	1
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	1	0	1	1	0
1	1	1	1	1	1	0

(c) it has an inertial delay of 0.06 ns with a reject time of 0.06 ns. (10 points)



0 0.08 0.16 0.24 0.32 0.40 0.48 0.56 0.64

A:

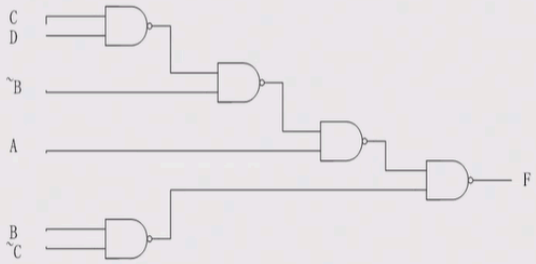


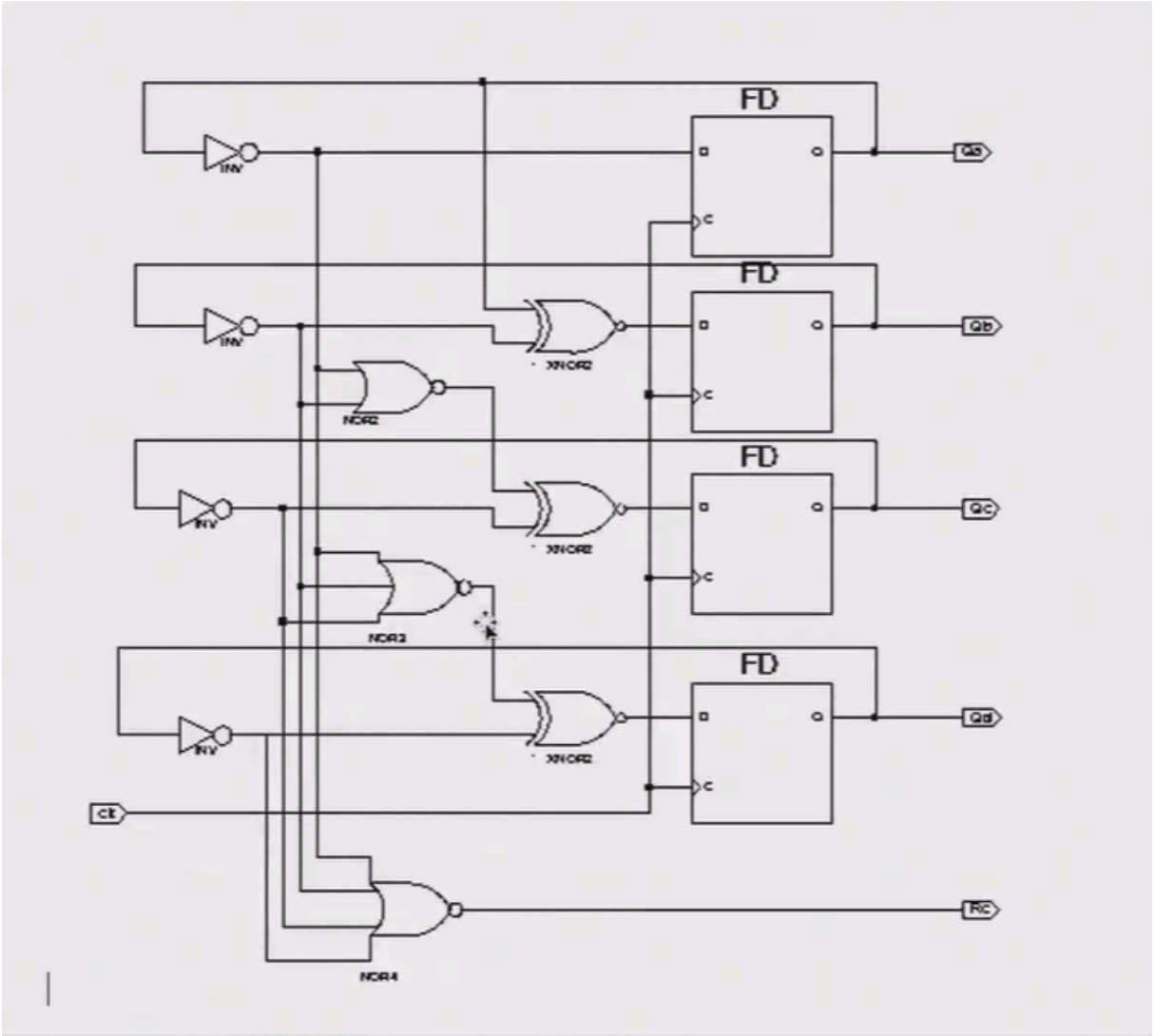
2. Find the delay from each input to the output.

(a) Finding t_{PHL} and t_{PLH} for each path, assuming t_{PHL} = 0.30ns and t_{PLH} = 0.50ns for each gate. From these values, find t_{pd} for each path.

(b) Using t_{pd} = 0.40ns for each gate.

(c) Compare your answers in (a) and (b) and discuss the differences. (10 points)




FD
FD
FD
FD
INV
INV
INV
INV
XNOR2
XNOR2
XNOR2
NOR2
NOR3
NOR4
C
C
C
C
Qa
Qb
Qc
Qd
clk
RC

(a) Please write the state table.

	Q_A	Q_B	Q_C	Q_D	D_A	D_B	D_C	D_D
0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	1	0	0
2	0	1	0	0	1	1	0	0
3	1	1	0	0	0	0	1	0
4	0	0	1	0	1	0	1	0
5	1	0	1	0	0	1	1	0
6	0	1	1	0	1	1	1	0
7	1	1	1	0	0	0	0	1
8	0	0	0	1	1	0	0	1