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有问题可以找我 😎

填空

1. 十进制 529.625 求 二进制 八进制 16 进制
2. 给一个 8bit signed 二进制 求反码 补码
3. the index of minterm $\overline{A}\overline{B}C$ is

the index of maxterm $\overline{A}+\overline{B}+C$ is

4. DRAM 有 12 位的地址线,16 位的数据线。 存多少 MB （具体数忘了）
5. R_1R_2 都是 8 位二进制码

   经过 two icrooierations

   a）$R_1 \leftarrow \text{sr}R_1$

   b）$R_1 \leftarrow \overline{R_1} \oplus R_2$

   问你R_1是啥
6. 做一个 128MB 的 需要几个 2M×8bit 的 ROM
7. 给一个表达式， input 是 A B C， 用 二选一多路选择器做，其中 A = S_1 B = S_0 ， 问$I_0I_1I_2I_3$是啥

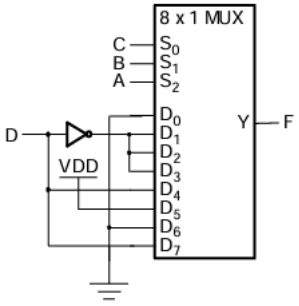
   会这题考试题必然会了

   Implement the following Boolean function with an 8–to–1-line multiplexer and a single inverter with variable D as its input:

   $$F(A, B, C, D) = \Sigma m(2, 4, 6, 9, 10, 11, 15)$$

3-46.

A	B	C	D	F	
0	0	0	0	0	F = 0
0	0	0	1	0	
0	0	1	0	1	F = $\bar{D}$
0	0	1	1	0	
0	1	0	0	1	F = $\bar{D}$
0	1	0	1	0	
0	1	1	0	1	F = $\bar{D}$
0	1	1	1	0	
1	0	0	0	0	F = D
1	0	0	1	1	
1	0	1	0	1	F = 1
1	0	1	1	1	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	0	F = D
1	1	1	1	1	



8. 求 Gate input cost 和 Gate input cost with NOTs (GN)

类似这个

3. 求 GN(with NOT): $F = AB + \overline{C}(BC + \overline{A}D)$

9. n 个三态门, 其中最多有 _____ 个三态门的 $\overline{EN}$ 引脚可以等于 _____(0/1), 其他的三态门的 $\overline{EN}$ 引脚应为 _____(0/1).

10. 求 even parity code （校验的 bit 放在给定序列的左边）

11. _____模型的 output 是关于 state 和 input 的函数

选择

12. 4，5 用 BCD 编码 4+5 的结果 是 4+5 得到的 BCD 码修正，还是就是这个结果

13. SRAM 和 DROM 特性比较 应该是 SRAM 更快

14. 延时问题 类似这个

4-59. *A sequential circuit is shown in Figure 4-49. The timing parameters for the gates and flip-flops are as follows:

Inverter: $t_{pd} = 0.01$ ns
XOR gate: $t_{pd} = 0.04$ ns
Flip-flop: $t_{pd} = 0.08$ ns, $t_s = 0.02$ ns, and $t_h = 0.01$ ns

(a) Find the longest path delay from an external circuit input passing through gates only to an external circuit output.

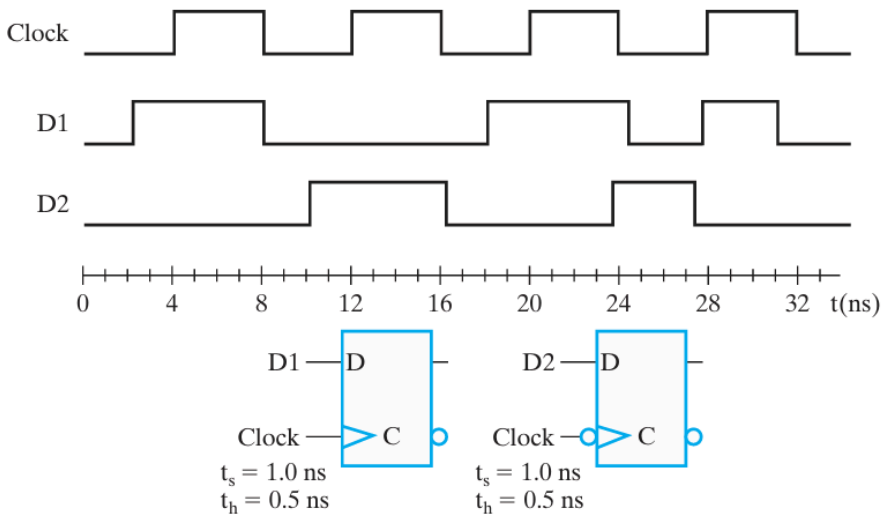


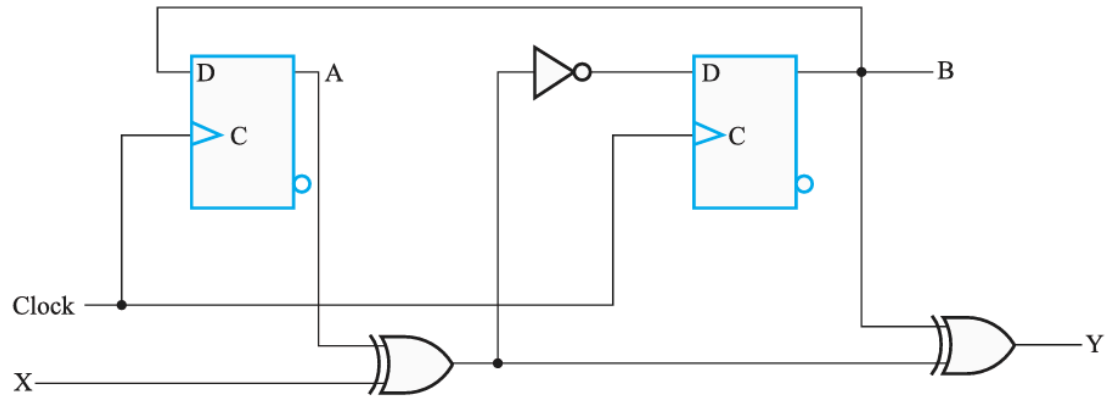
FIGURE 4-56
Circuit for Problem 4-58.

(b) Find the longest path delay in the circuit from an external input to positive clock edge.

(c) Find the longest path delay from positive clock edge to output.

(d) Find the longest path delay from positive clock edge to positive clock edge.

(e) Determine the maximum frequency of operation of the circuit in megahertz (MHz).



Problem Solutions – Chapter 4

4-59.*

a) The longest direct path delay is from input X through the two XOR gates to the output Y.

$$t_{delay} = t_{pdXOR} + t_{pdXOR} = 0.04 + 0.04 = 0.08 \text{ ns}$$

b) The longest path from an external input to a positive clock edge is from input X through the XOR gate and the inverter to the B Flip-flop.

$$t_{delay} = t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.04 + 0.01 + 0.02 = 0.07 \text{ ns}$$

c) The longest path delay from the positive clock edge is from Flip-flop A through the two XOR gates to the output Y.

$$t_{delay} = t_{pdFF} + 2\,t_{pdXOR} = 0.08 + 2(0.04) = 0.16 \text{ ns}$$

d) The longest path delay from positive clock edge to positive clock edge is from clock on Flip-flop A through the XOR gate and inverter to clock on Flip-flop B.

$$t_{delay\text{-clock edge to clock edge}} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF} = 0.08 + 0.04 + 0.01 + 0.02 = 0.15 \text{ ns}$$

e) The maximum frequency is $1/t_{delay\text{- clock edge to clock edge}}$. For this circuit, $t_{delay\text{-clock edge to clock edge}}$ is 0.15 ns, so the maximum frequency is 1/0.15 ns = 6.67 GHz.

Comment: The clock frequency may need to be lower due to other delay paths that pass outside of the circuit into its environment. Calculation of this frequency cannot be performed in this case since data for paths through the environment is not provided.

这个题会了那考试题必然会了

15. $F(A,B,C) = \sum m(2,5,6,7)$ 考转化成 pom 形式的选项是什么
16. PLA AND 阵列_____; , OR 阵列_____ (Fixed/Programmable
17. 4-bit counter 是 module 7 的计数器 clear = _____（我觉得是$Q_2Q_1Q_0$）
18. the gate costs of 16bit Lookahead Carry Adder:

    A. 2 XOR and 15 OR-AND

    B. 2 XOR and 16 OR-AND

大题

19. 给一个电路图，写他的 verilog，一个 structral model，一个 dataflow model（非常简单的）

20. 化简表达式 用布尔代数化简 每一步要写上他的名字
21. 给一个布尔方程 要卡诺图化简 带 don't care

    写他的卡诺图 Essential Prime Implicant 还有最后化简的表达式
22. 给一个电路图 求次态方程、状态表、状态图

    可以参考这个题

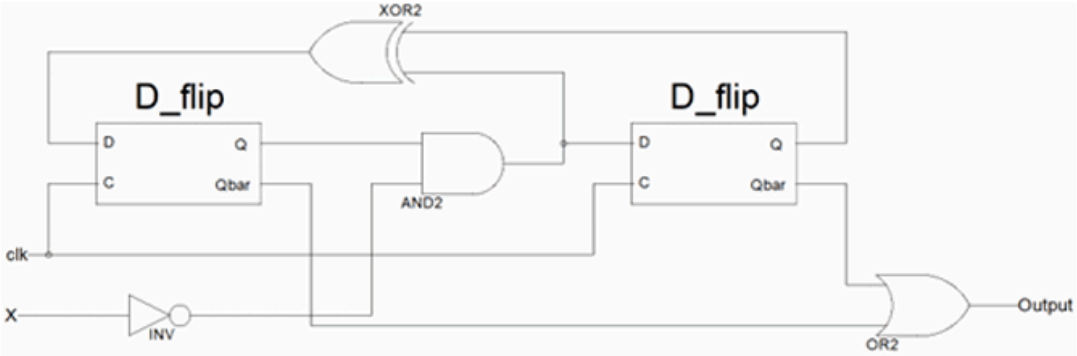


图 5: 20 题图

23. 做个一位的全减器，

    input： X ,Y ,C_{in}

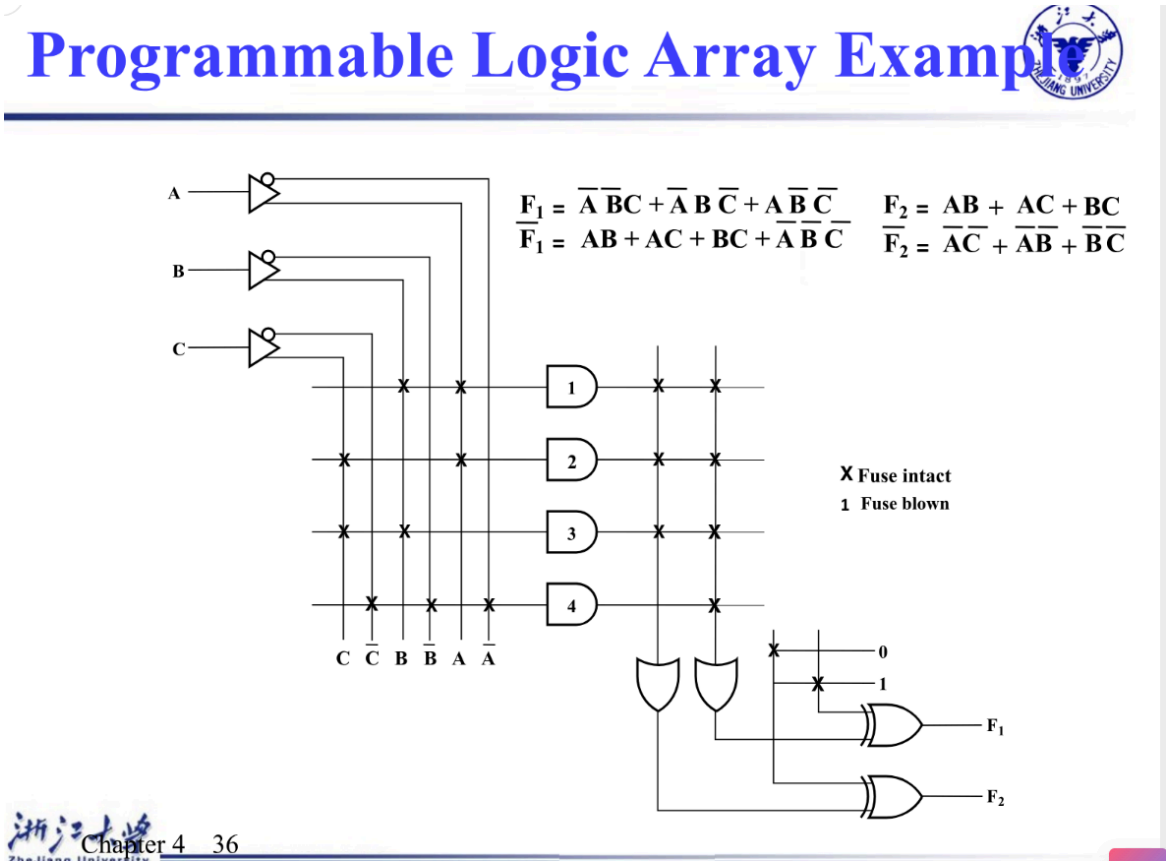
    output： diff 和C_{out}

    diff = $X - Y - C_{in}$

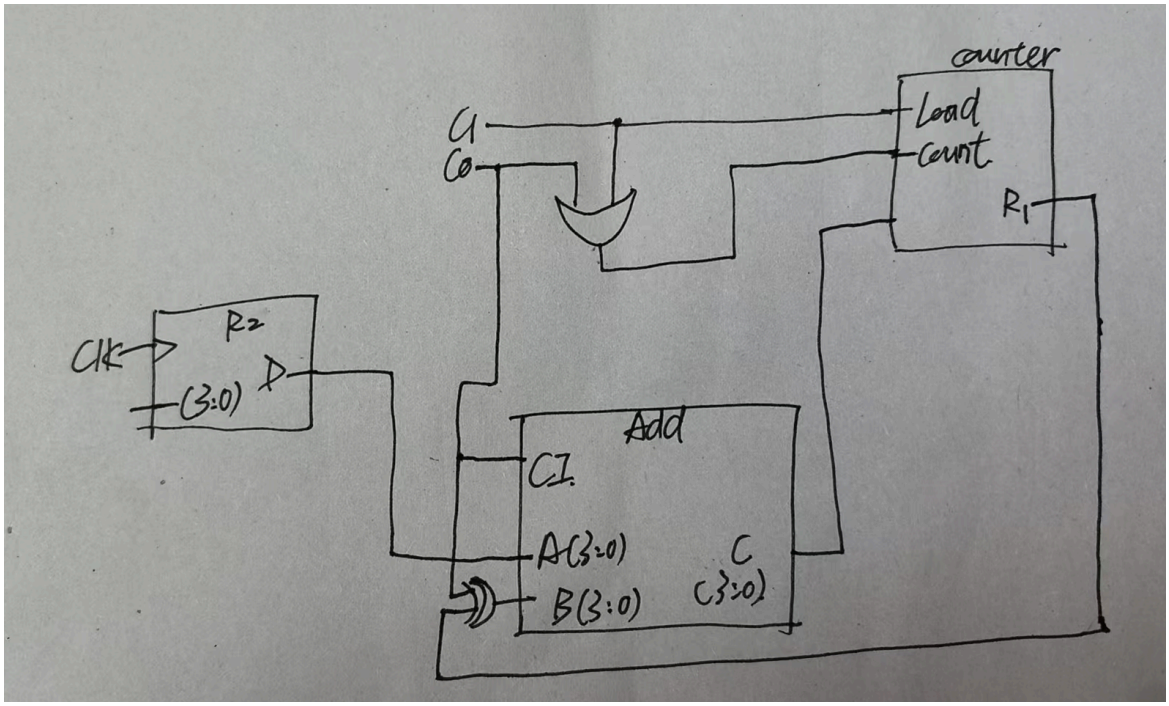
    C_{in} 是之前位的借位

    如果算的时候发生了借位 C_{out} = 1 否则为 0

    写他的真值表 output 的布尔方程 画电路图
24. 可编程电路（md 老师 ppt 里有例子）



25. 给一个时序电路图 填表格 LOAD R_1 还有实现的是什么功能 （ 大概长这样？ 总之我从我的答案推出来的）



C_1	C_0	Load	R_1寄存器传输语言	功能
0	0			
0	1			

1	0			
1	1			

6-27. *Two register transfer statements are given (otherwise, $R1$ is unchanged):

$$C1\text{: } R1 \leftarrow R1 + R2 \quad \text{Add } R2 \text{ to } R1$$
$$\overline{C1}\,C2\text{: } R1 \leftarrow R1 + 1 \quad \text{Increment } R1$$

(a) Using a 4-bit counter with parallel load as in Figure 6-14 and a 4-bit adder as in Figure 4-5, draw the logic diagram that implements these register transfers.

和这个有点像

这是作业题 你可以找找看

26. 两个信号

（input）brake

（output）LED

L=1 亮 ; L=0 不亮

brake = 1 的时候 LED 这样变化： on off on off on off 然后一直保持 on

在任何时候 brake =0 了 LED 就 reset initial state

画 state table， state diagram 状态和 ouput 的布尔方程式 再自己设计电路图