New AC-based capacitance tomography system

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Abstract: Electrical capacitance tomography (ECT) is a new technology that is used to visualise the internal behaviour of industrial processes comprising dielectric components. A particular difficulty with capacitance measurement for tomography is that the stray capacitance to earth of an ECT sensor is large (~150pF) compared with the interelectrode capacitance to be measured (usually <0.5pF), and the measurement range is wide (0.01–2pF). The authors present a highly sensitive AC-based capacitance measuring circuit, which has been specially designed for this purpose, and a PC-based ECT system with this circuit. Experimental results show that this ECT system can measure as small as 0.01pF capacitance with 0.0002pF error, and could collect tomographic image data at more than 100 frames per second.

1 Introduction

In the last decade, process tomography techniques have been developed rapidly for visualising the internal behaviour of industrial processes, e.g. gas/oil flows in oil pipelines [1], gas/solid flows in pneumatic conveyors [2], and separation/mixing processes in chemical vessels [3]. Electrical capacitance tomography (ECT) involves the measurement of changes in capacitance from a multielectrode sensor due to the change in permittivity of materials being imaged, and the reconstruction of cross-sectional images using the measured data and a suitable algorithm [1, 4].

A typical ECT pipeline sensor consists of a set of measurement electrodes mounted symmetrically around the circumference of an insulating pipe (see Fig. 1). An earthed screen, which surrounds the measurement electrodes, minimises external electrical noise. Radial earthed screens are fitted between the electrodes to reduce the interelectrode capacitance external to the sensor pipe, particularly the standing capacitance between adjacent electrode pairs. For a sensor with N electrodes there are $N(N-1)/2$ single-electrode pairs and hence $N(N-1)/2$ independent capacitance measurements.

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The interelectrode capacitance of an ECT sensor depends mainly on the electrode size. For a given number of electrodes, the capacitance is proportional to the axial length of electrodes. To obtain wide-spatial-bandwidth signals, short electrodes are preferable [5]. However, short electrodes result in small capacitance values. Typically, the length of electrodes is selected as 10cm [1, 4]. Fig. 2 shows a set of capacitance measurements which have been obtained from a typical ECT sensor with 12 electrodes, using an impedance analyser (HP4192A). These include the standing capacitance when the sensor is empty ($\varepsilon_r = 1.0$), and the changes in capacitance when the sensor is completely filled with polystyrene beads ($\varepsilon_r = 1.8$). Note that, although polystyrene has a permittivity of 2.56 [6], the effective permittivity of polystyrene beads is smaller due to gaps between beads. It is clear that the standing capacitance values are small, from 0.01pF to 0.5pF, and the changes in capacitance are even smaller, from 0.005pF to 0.08pF.

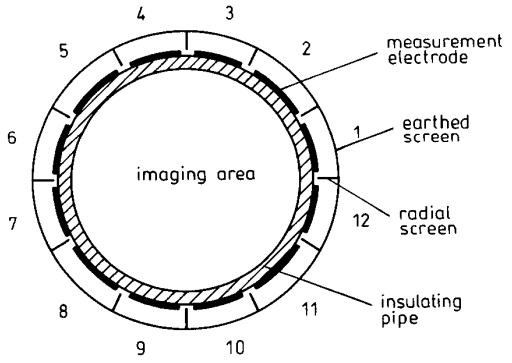

Fig. 1 *Cross sectional view of typical ECT sensor with 12 measurement electrodes*

In an ECT sensor stray capacitance arises mainly from three sources:

(i) the capacitance between the measurement electrode and the earthed screen (see Fig. 1);

(ii) the capacitance of the shielding cable connecting the electrode to a capacitance measuring circuit, typically 1pF/cm (i.e. 100pF for a cable of 1m); and

(iii) the input capacitance of the CMOS switches in the capacitance measuring circuit (to be discussed in Section 3.2).

The total stray capacitance is around 150pF. Therefore the capacitance measuring circuit must be insensitive to stray capacitance, i.e. stray-immune. In addition, it should have high signal-to-noise ratio (SNR), low drift and wide bandwidth to enable a high data sampling rate. Of many different capacitance measuring circuits,

the charge/discharge circuit [7] and the AC-based circuit [8–10] are the most suitable for use in ECT systems because of their stray-immunity. The charge/discharge circuit, however, suffers from charge injection problems [11]. In this paper a new ECT system, which employs a highly sensitive AC-based capacitance measuring circuit, is described.

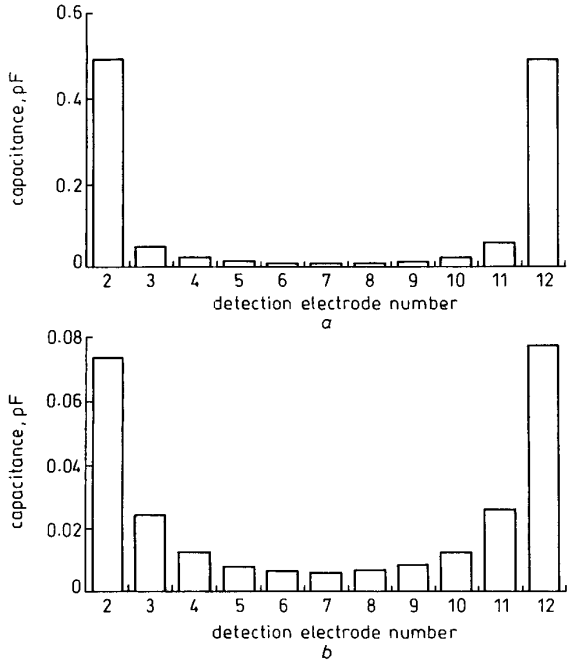

Fig.2 *Capacitance values of typical 12-electrode ECT sensor*
a Standing capacitance
b Changes in capacitance

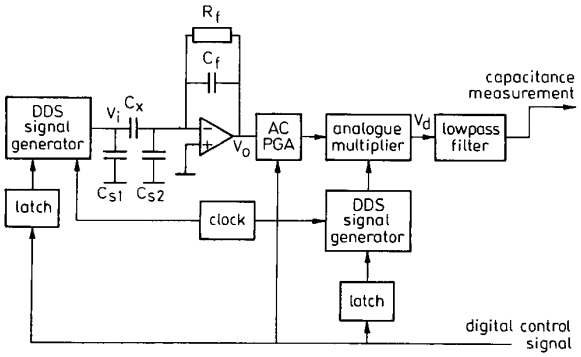

Fig.3 *AC-based capacitance measuring circuit, showing stray capacitance*

2 AC-based capacitance measuring circuit

The AC-based capacitance measuring circuit shown in Fig. 3 employs sine-wave excitation. Two DDS (direct-digital-synthesiser) integrated circuit chips (AD7008) are used to generate two 500 kHz sine-wave signals of 18 V peak to peak. One is used as an excitation voltage source and the other as a reference signal. The amplitude, frequency and phase of the signals can be programmed digitally. To keep the two signal generators synchronous, a common clock of 50 MHz together with two latches (74HC273) are used.

The excitation voltage V_i is applied to the unknown capacitance C_x. A wide bandwidth operational amplifier (LM6263), with a feedback capacitance C_f and a feedback resistance R_f, converts the current into an AC voltage V_o given by

$$V_o = -\frac{j\omega C_x R_f}{j\omega C_f R_f + 1} V_i \tag{1}$$

where ω is the angular frequency of the excitation voltage.

When capacitance feedback is selected to be dominant, i.e. $1/\omega C_f << R_f$, eqn. 1 becomes

$$V_o = -\frac{C_x}{C_f} V_i \tag{2}$$

This AC signal is amplified further by an AC programmable-gain amplifier (PGA) constructed from operational amplifiers (LM6263) and CMOS switches (ADG201), which provides gains of 10 and 100, to accommodate a large range of capacitance values (see Fig. 2), and to ensure that the AC signal to be demodulated is of the order of volts; otherwise the following circuit will produce significant noise and errors.

The AC signal is demodulated using an analogue multiplier (MPY634). The reference signal is approximately in phase with the excitation signal and can be adjusted digitally in steps corresponding to 0.1°, to accommodate small changes in the phase delay of the measurement signal due to the amplifiers. The multiplier performs demodulation as follows:

$$\begin{aligned} V_d &= \frac{1}{S} A \sin(\omega t + \alpha) B \sin(\omega t + \beta) \\ &= \frac{AB}{2S} \{\cos(\alpha - \beta) - \cos(2\omega t + \alpha + \beta)\} \end{aligned} \tag{3}$$

where A and B are, respectively, the amplitudes of the AC signals from the AC PGA and the reference sine wave, α and β are the angles of the two signals with respect to the excitation voltage, and S is the scale factor of the multiplier.

When the two signals are adjusted to be exactly in phase, the multiplier output becomes

$$V_d = \frac{AB}{2S} \{1 - \cos 2(\omega t + \alpha)\} \tag{4}$$

The demodulated signal consists of DC and 1 MHz sine-wave components. A 4th-order Butterworth low-pass filter, which is constructed from operational amplifiers, with a cut-off frequency of 5 kHz, is used to reject the AC signal. The resultant DC signal represents the capacitance measurement.

Table 1: Circuit parameters

Parameter	Symbol	Unit	Value
Excitation voltage	V_i	V_{n-n}	18
Reference voltage	B	V_{n-n}	18
Feedback capacitance	C_f	pF	10
AC PGA gain	G	V_{n-n}/V_{n-n}	10 or 100
Scale factor of multiplier	F	V	10

Table 1 lists the chosen circuit parameters. From these parameters the circuit sensitivity can be calculated as 0.2 V/pF or 2.0 V/pF, depending on the gain of the AC PGA.

In Fig. 3 two stray capacitances between the two measurement electrodes and earth are shown as C_{s1} and C_{s2}. Since C_{s1} is directly driven by the voltage

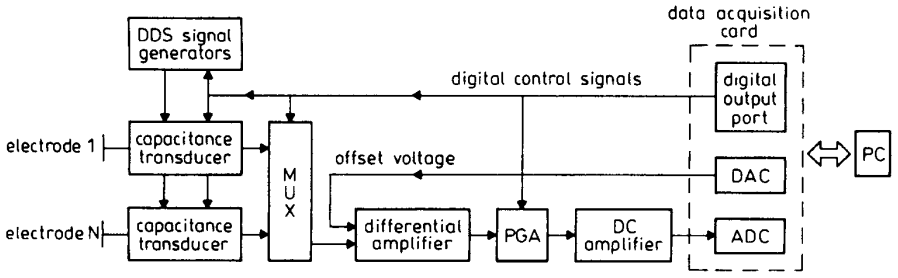

Fig. 4 *Schematic diagram of ECT system*

source, it does not affect the voltage applied to the unknown capacitance and hence has no effect on the capacitance measurement. Because the invert input of the operational amplifier is held at virtual earth by feedback and the potential difference across C_{s2} is close to zero, there is nearly zero current passing through C_{s2}, and hence it does not affect the capacitance measurement, either. Therefore this capacitance measuring circuit is not sensitive to the stray capacitance, i.e. it is stray-immune.

3 ECT system design

3.1 General description

The overall ECT system is shown in Fig. 4. One measurement channel using an AC-based capacitance measuring circuit shown in Fig. 3 is employed for each electrode. The N capacitance measurements which are DC signals are sent, in turn, to a common signal conditioning circuit, via a 16-to-1 multiplexer (MUX) (ADG526). An offset signal is subtracted using a unity-gain differential amplifier (INA105) to balance the standing capacitance (to be discussed further in Section 3.3). The resultant signal represents the change in capacitance. It is amplified first by a DC PGA (ADG526) with selectable gains of 1, 2, 4, 8 and 16 to deal with the large measurement range, and then by a DC amplifier with a gain of 10. The final analogue signal is digitised by a 12-bit ADC (AD547) on a data-acquisition card (PCL711) which is embedded in a PC.

The offset signal, which is used to balance the standing capacitance, comes from a 12-bit DAC (DAC7541) which is also on the data-acquisition card. The offset signal can vary from 0 to 5V in 4096 steps, and is expressed as

$$V_{offset} = V_{ref}\frac{D}{2^{12}} \tag{5}$$

where, V_{ref} is the the reference voltage for the DAC and D is the digital input.

The ADC is configured for offset bipolar operation. Its digital reading is

$$E = \frac{V_{in} + \frac{1}{2}F}{F}(2^{12} - 1) \tag{6}$$

where F is the full range of the ADC.

System operation is controlled by the digital output port on the data acquisition card and provides the following functions:

(i) control of CMOS switches to select the excitation and detection electrodes (see Section 3.2);

(ii) control of the amplitude and frequency of the excitation and the reference signals and the phase difference between them;

(iii) control of the MUX to select the DC signals, in turn, from the capacitance measuring circuits; and

(iv) control the PGA gain to make full use of the measurement range of the ADC.

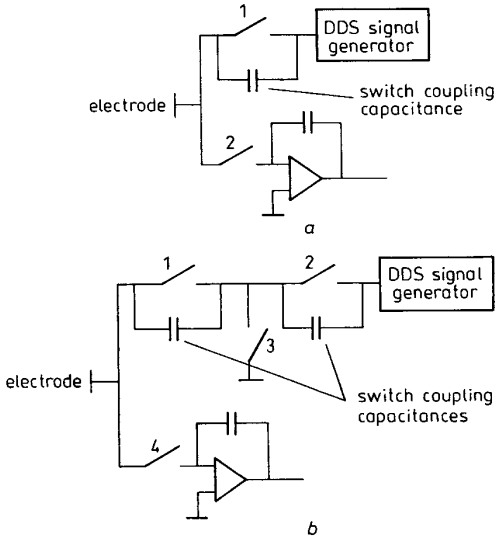

Fig. 5 *Switch arrangement*
a Circuit in principle
b Practical circuit

3.2 Switch arrangement

In Fig. 3 only the basic capacitance measuring circuit is shown, with the left-side electrode used for excitation and the right-side electrode for detection. In an actual situation, each electrode can be used for either excitation or detection, the modes being selected via CMOS switches. In principle, only two switches per electrode are required as shown in Fig. 5*a*. However, this arrangement is unsatisfactory because in the detection mode (switch 1 open and switch 2 closed) the coupling capacitance of switch 1 is effectively in parallel with the measured interelectrode capacitance. Note that the interelectrode capacitance can vary from 0.01pF (opposing electrodes) to 0.5pF (adjacent electrodes) whilst the switch capacitance is about 0.5pF [12] and nonconstant. With this two-switch configuration, the measurement accuracy would be seriously degraded because the driven signal is directly coupled to the detection amplifier when the electrode is used in the detection mode.

In practice a four-switch arrangement is necessary as shown in Fig. 5*b*. In the excitation mode, switches 1 and 2 are closed while switches 3 and 4 are open. In the detection mode, switches 1 and 2 are open while switches 3 and 4 are closed, connecting the coupling

capacitance of switch 1 to earth and thus eliminating its effect on the interelectrode capacitance measurement. This arrangement reduces the effect of the coupling capacitance of the CMOS switches significantly.

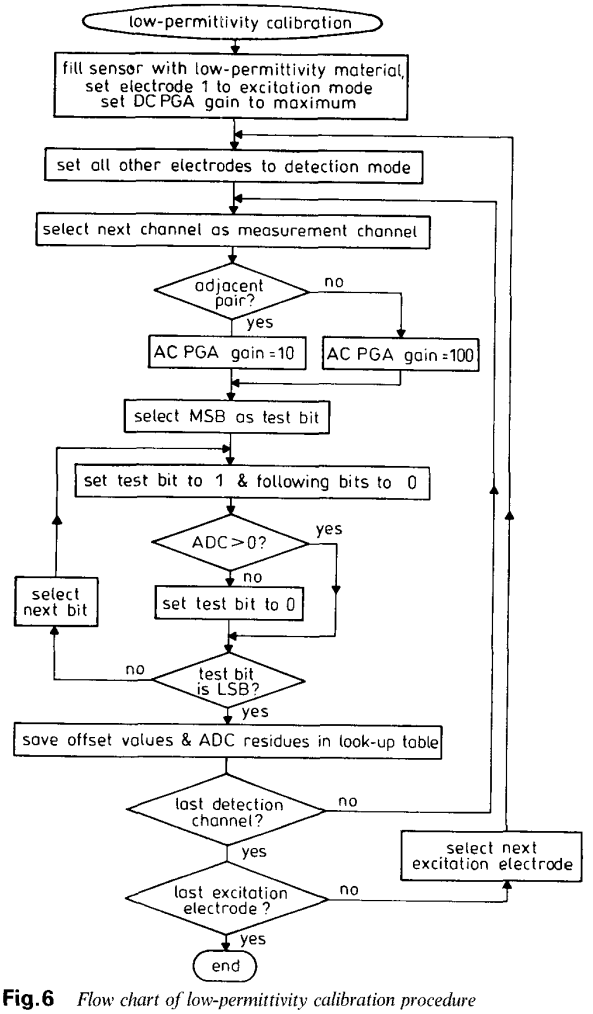

Fig.6 *Flow chart of low-permittivity calibration procedure*

3.3 System calibration

Since the standing capacitance of an ECT sensor is relatively large and the changes in capacitance to be measured are very small [7], the standing capacitance signals have to be balanced using the offset signal as shown in Fig. 4. For a specific electrode pair, an appropriate offset value can be found which matches the DC voltage due to the standing capacitance, so that the standing capacitance is balanced. Since the standing capacitances vary significantly for different electrode pairs, as shown in Fig. 2*a*, a set of offset values must be obtained for all electrode pairs, when the sensor is empty or full of a low-permittivity material. This process is called 'low-permittivity calibration' or 'zero-point calibration'. Essentially, the calibration procedure is similar to the successive-approximation process in an ADC and is shown in Fig. 6. The digital offset values which have been found are saved in the memory of the PC as a look-up table. When the capacitance of a specific electrode pair is measured, the corresponding digital value is sent back from the PC to the offset DAC to balance the standing capacitance.

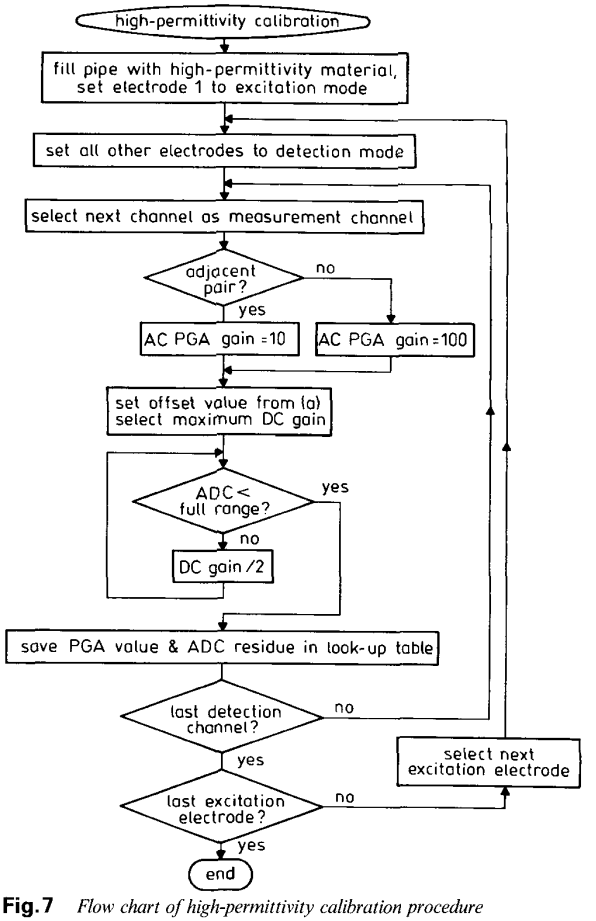

Fig.7 *Flow chart of high-permittivity calibration procedure*

Since the changes in capacitance vary significantly for different electrode pairs, as shown in Fig. 2*b*, the capacitance change signal from the differential amplifier (see Fig. 4) is conditioned by a DC PGA with five different gains. A set of appropriate gain values can be found for all the electrode pairs, when the sensor is full of a high-permittivity material. This process is called 'high-permittivity calibration' or 'full-scale calibration'. The digital gain values are saved in the memory of the PC as another look-up table. A digital value is sent from the PC to the PGA for a specific electrode pair, to keep the maximum capacitance change signal close to the full range of the ADC. The calibration procedure for the PGA is similar to that for the offset and is shown in Fig. 7. The low- and high-permittivity calibration procedures are summarised in Table 2.

Table 2: System calibration to find offset and PGA values

Procedure	Sensor state	Offset	PGA gain	Criterion
Low-permittivity calibration	Empty or full of a low-permittivity material	Adjusted during procedure	At maximum	Keep ADC reading > 0
High-permittivity calibration	Full of a high-permittivity material	At the values found during low-permittivity calibration	Adjusted during procedure	Keep ADC reading close to but less than full range

3.4 Capacitance measurement with ECT system

From Fig. 4, a complete measurement channel of the ECT system can be modelled as shown in Fig. 8, where C_x is the measured capacitance in picofarads; C_p is the parasitic capacitance in picofarads (note that although the capacitance measuring circuit is stray-immune, the parasitic capacitance, which is in parallel with the measured capacitance, is inevitable, e.g. due to PCB layout); K_c is the sensitivity of the AC-based capacitance measuring circuit, 0.2 or 2.0V/pF, depending on the AC PGA gain; D is the digital input to the offset DAC; V_{ref} is the reference voltage for the DAC (5V); K_g is the DC PGA gain (1, 2, 4, 8 and 16V/V); K_d is the gain of the DC amplifier (10V/V); F is the full range of the ADC (5V); and E is the digital reading of the ADC.

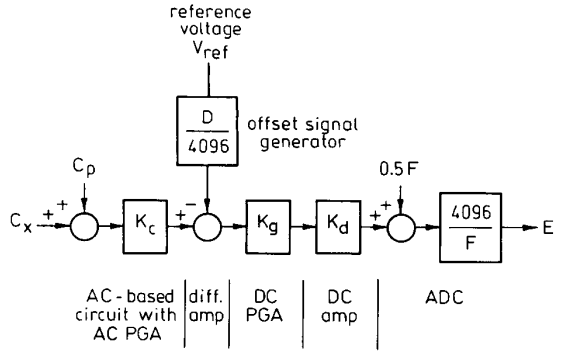

Fig. 8 *Block diagram of complete measurement channel*

Note that in Fig. 8, the bipolar function of the ADC is modelled as an offset, 0.5F. From Fig. 8, the capacitance value can be calculated:

$$C_x + C_p = \frac{1}{K_c}\left(\frac{\frac{E}{4096}F - 0.5F}{K_g K_d} + V_{ref}\frac{D}{4096}\right) \quad (7)$$

The parasitic capacitance C_p can be found by connecting the excitation electrode to earth (i.e. the earthed shield) so that C_x is not measured. Once C_p has been found and $C_x + C_p$ has been measured, C_x can be obtained simply by subtraction. As confirmed experimentally, C_p is very stable and needs to be measured only once during system calibration. The measured value is used for compensation of the parasitic capacitance during system operation.

4 Experimental results

To evaluate the new ECT system, experiments were carried out. At first, 12 parasitic capacitances, each corresponding to one measurement channel, were measured as listed in Table 3. The capacitance values are around 0.06pF, which is relatively large compared with the typical changes in capacitance that are shown in Fig. 2*b*. Therefore it is important to measure and compensate the parasitic capacitances.

An ECT sensor (12 electrodes, 10cm long and 50mm in diameter), was used for the following tests. Fig. 9 shows a set of capacitance values measured by the new ECT system with electrode 1 selected as the excitation electrode and the others as the detection electrodes. These capacitance values were compared with those measured by the impedance analyser (see Fig. 2*a*). Fig. 10 shows the comparison and suggests very good linearity. Table 4 lists the detailed comparison results, showing that the maximum absolute error is 1.8fF (between an adjacent electrode pair) and the maximum relative error is 2.3% (between the opposing electrode pair).

Table 4: Capacitance values measured by the ECT system and the impedance analyser

Electrode pair	Capacitance measured by impedance analyser (pF)	Capacitance measured by ECT (pF)	Absolute error (pF)	Relative error (%)
1–2	0.492	0.4938	0.0018	0.37
1–3	0.049	0.0490	0.0000	0.0
1–4	0.022	0.0221	0.0001	0.45
1–5	0.013	0.0133	0.0003	2.3
1–6	0.011	0.0106	−0.0004	−1.3
1–7	0.010	0.0098	−0.0002	2.0

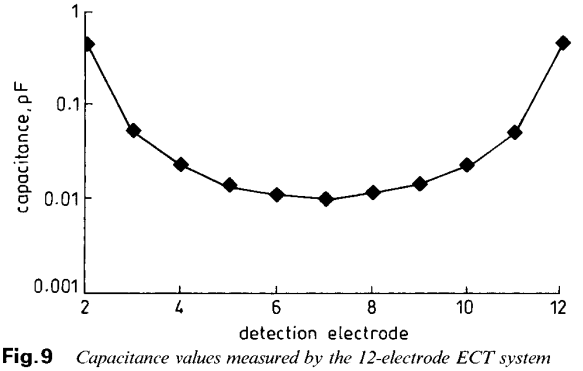

Fig. 9 *Capacitance values measured by the 12-electrode ECT system*

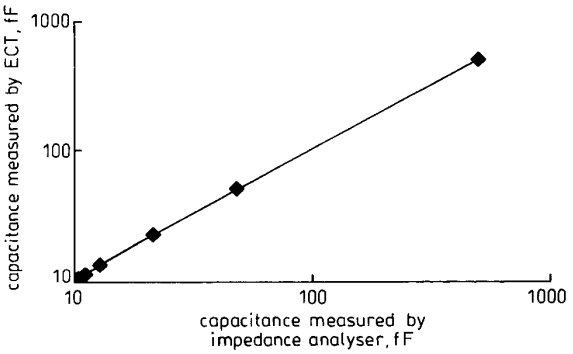

Fig. 10 *ECT measurements against impedance analyser measurements*

For image reconstruction, it is common practice to use normalised capacitance which is defined by

$$\lambda = \frac{C_m - C_l}{C_h - C_l} \quad (8)$$

where, C_m is the measured capacitance when object(s)

Table 3: Measured parasitic capacitance values

Channel	1	2	3	4	5	6	7	8	9	10	11	12
Parasitic capacitance (× 0.001pF)	64	54	62	58	58	55	57	58	57	56	55	52

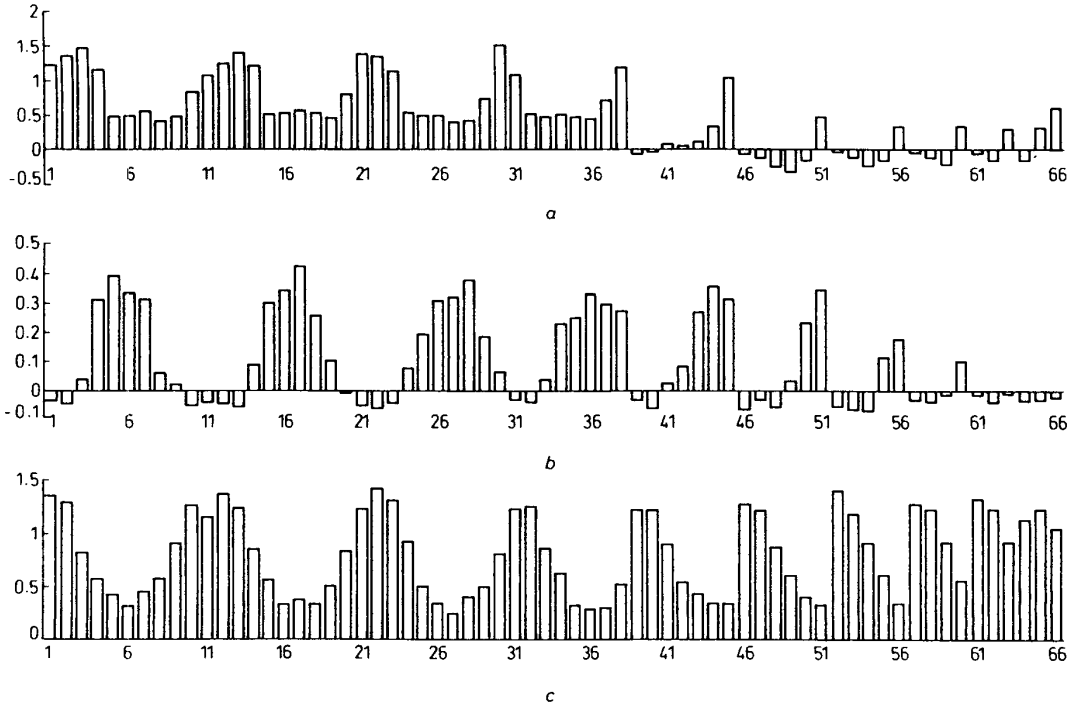

Fig. 11 *Normalised capacitance measurements*
a Stratified distribution
b Core distribution
c Annular distribution

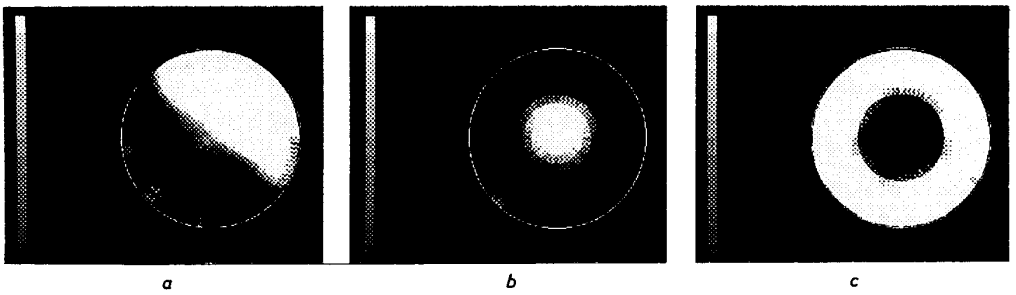

Fig. 12 *Reconstructed images*
a Stratified distribution
b Core distribution
c Annular distribution

present in the sensor, and C_l, C_h are the capacitance values when the sensor is completely filled with a low-permittivity material and a high-permittivity material, respectively.

Three typical flow distributions (stratified, core and annular) were modelled physically with air and polystyrene beads as the low- and high-permittivity materials. Fig. 11 shows three sets of normalised capacitance measurements for the three typical flow regimes, each set having 66 capacitance measurements between electrodes 1–2, 1–3, ... 1–12, 2–3, 2–4, ... 2–12, up to 11–12 [7]. Note that the electric field is the so-called 'soft field'. Some of the normalised capacitance values are larger than '1' and some less than '0' when the sensor is not uniformly filled.

Using these normalised capacitance data, images were reconstructed using an iterative feedback algorithm [13] as shown in Fig. 12.

5 Conclusions and discussion

A new ECT system is being developed at UMIST which is suitable for both research and laboratory applications. It employs a stray-immune AC-based circuit. Because the standing capacitance is relatively large, the system has been designed to be able to cancel standing capacitance by a programmable offset signal. The circuit gain is also programmable, in both AC and DC parts, to deal with a large dynamic measurement range. The methods of standing capacitance cancellation and circuit-gain adjustment are two key features of the ECT system. Without these two functions, it would not be able to measure so small a capacitance varying in so large a dynamic range.

The other features of the ECT system include:

(*a*) multiplying demodulation with a high SNR and high harmonics rejection;

(*b*) four-switch configuration to eliminate the coupling capacitance of CMOS switches;

(*c*) software-controlled calibration; and

(*d*) self measurement of parasitic capacitance.

The experiments show that the ECT system can measure small capacitance accurately. For adjacent electrode pairs, the capacitance of which is relatively large,

about 0.5pF, the relative error is 0.37%. For all other electrode pairs, the capacitance of which is less than a tenth of that of adjacent electrode pairs, the maximum absolute error is 0.0004pF and the maximum relative error is 2.3%. This accuracy is hardly achieved with the previous ECT systems. Combined with a new image-reconstruction algorithm, the ECT system produces very promising images.

The main limitation on the data acquisition speed of an ECT system lies in the capacitance measuring circuits; in particular, the frequency of the excitation signal and the cut-off frequency of the low-pass filter. For 500kHz excitation and 5kHz cut-off frequency, the transient time of the capacitance measuring circuit is about 200μs. Since the electrodes are energised sequentially, the total time taken by the capacitance measuring circuits is $N \times 200\mu s$, where N is the number of electrodes. This corresponds to 2.4ms for a 12-electrode sensor. Simulation studies have shown that, after taking the conditioning circuit response and the data transmission into account, the system data acquisition speed could be much higher than 100 frames per second [14].

6 Acknowledgments

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