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Differential capacitive sensing circuit for a multi-electrode capacitive force sensor

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ABSTRACT

A multi-electrode differential capacitive sensing circuit is designed and realized for the read-out of a multi-axis capacitive force–torque sensor. The sensing circuit is based on a differential relaxation oscillator, to which multiple capacitances can be connected. For selecting the capacitances, reprogrammable asynchronous logic can be used, such that any desired combination of differential or single-ended capacitance can be determined. The noise performance of the oscillator in the system is analysed and measured, revealing the influence of individual component values on the noise performance of the system. Capacitance measurements show that a deviation of 0.9 fF is obtained at an acquisition rate of 225 Hz including auto-calibration, which is mainly limited by the quantization noise due to the frequency counter. The lowest obtained deviation is 0.12 fF at an acquisition rate of 3.5 Hz. The system is successfully interfaced to the multi-axis capacitive force–torque for the read-out of six capacitor configurations at an acquisition rate of 38 Hz.

1. Introduction

Capacitive sensing technology is widely used for sensor systems which require high sensitivity and low power consumption. In a differential configuration, capacitive sensing principles offer effective reduction of common-mode noise and parasitic effects [1,2]. Differential capacitive sensing can therefore be found in many sensor systems such as accelerometers [3–5], gyroscopes [6–8], pressure sensors [9], flow sensors [10,11] and force sensors [12–14]. For the read-out of a differential capacitor pair various sensing techniques can be used in which the difference in capacitance is converted to a voltage, duty cycle or frequency. If the sensor consists of multiple electrode pairs, e.g. for the detection of multiple-degrees of freedom acceleration, angular acceleration, flow or force, each individual pair of electrodes needs to be interfaced. For a limited number of electrodes, each differential pair can be provided with an individual sensing circuit, referred to as space division multiplexing (SDM). When the number of electrodes increases, for example an array of differential capacitor pairs, techniques such as frequency division multiplexing (FDM) or time division multiplexing (TDM) can be used [15].

Capacitive read-out interfaces in which square-wave signals are used to determine the capacitance are an attractive candidate to combine with TDM since standard logic components can be used. Meijer et al. [16–19] presented an elegant low-cost and high resolution single-ended capacitive read-out system based on a relaxation oscillator and a TDM approach by multiplexing square wave signals. Several improvements to this circuit were presented later with, e.g. a high tolerance for a parasitic parallel conductance [20] and lower power consumption [21]. The resulting output of the sensing circuit is a square-wave signal with a frequency proportional to the measured capacitance that can easily be interfaced to a microcontroller to determine the frequency. Previously, successful read-out of a capacitive 1-D force sensor comprising of 16 single-ended capacitors using this system is demonstrated by Wiegerink et al. [22].

For a sensor application which we presented in [14,23], a capacitive read-out system is required which can measure both single-ended and differential capacitance to a common node with an accuracy better than 0.1% of the full scale, i.e. better than 1 fF accuracy, at an acquisition rate of 200 Hz per capacitor configuration. For this sensor a direct differential measurement is required; subtracting two single ended measurements can result in large errors if the measurements are not performed exactly at the same moment while the capacitances are changing in time due to a dynamic load. Commercially available capacitance to digital

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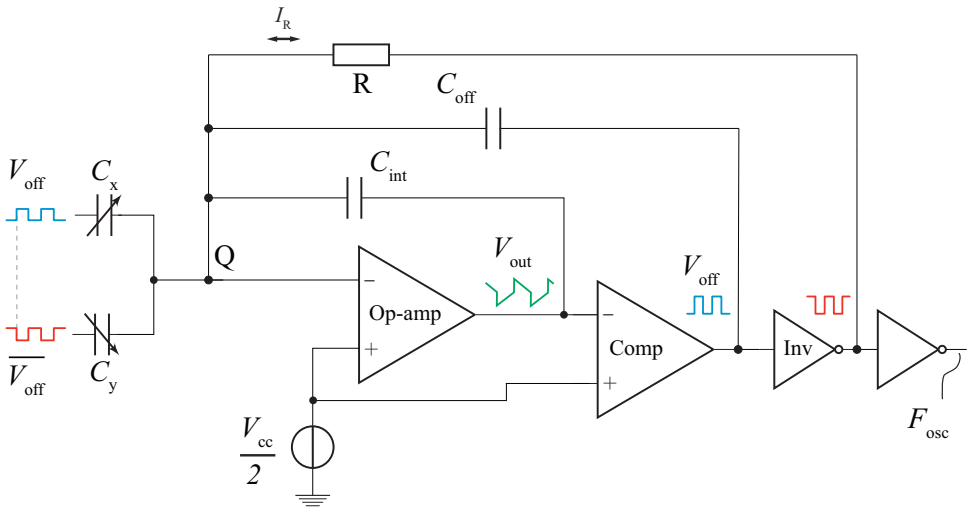

Fig. 1. Relaxation oscillator schematic with differential capacitor pair C_x and C_y.

converters (CDCs), such as [24–26] have excellent resolution, but are not suitable for multiple differential capacitance pairs to a common node. Furthermore, for optimal sensitivity of the force sensor, the same electrode must be combined in multiple differential configurations. CDCs that are capable of measuring multiple differential capacitance pairs to a common node, e.g. [27,28], are not intended for high accuracy capacitance measurements at relatively high acquisition rates.

The requirements described above make commercially available CDCs not suitable, which initiated the research described in this paper. We modified the measurement system presented by Meijer et al. [16–19] such that the oscillation period is proportional to differential capacitance with the capability to determine any combination of differential or single-ended capacitance [29]. In this work, the basic measurement principle is shown and the noise performance of the proposed system is analysed. To prove and assess its functionality and performance we interface the circuit to the force sensor in [14] and perform force and moment measurements.

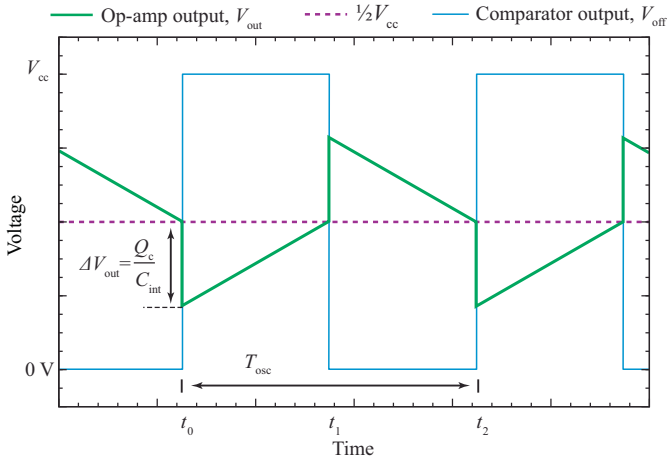

Fig. 2. Oscillator signals of the op-amp output and the comparator output.

2. Theory and modelling

2.1. Differential relaxation oscillator

The proposed differential capacitive read-out system is based on a relaxation oscillator presented by Martin [30] and modified by Meijer et al. [16–19]. We adapted the oscillator such that the oscillation period is proportional to differential capacitance. The circuit of the relaxation oscillator is illustrated in Fig. 1 and the oscillator signals are shown in Fig. 2. The basic circuit consists of an op-amp, comparator, inverter, two capacitors and a resistor. The op-amp in the circuit regulates the voltage at point Q such that it is kept at a constant level of $V_{cc}/2$ by regulating its output voltage V_{out}. When the circuit oscillates, charge is transferred from C_{off} to C_{int} and vice versa. The charge transfer occurs when voltage V_{off} at the right-hand side of capacitor C_{off} switches between 0 V and V_{cc}, which is controlled by the output of the comparator. When V_{off} switches from 0 V to V_{cc} (t_0 in Fig. 2), an amount of charge equal to $Q_c = V_{cc}C_{off}$ will flow into node Q. Because the op-amp regulates the voltage at this point such that it kept constant, this charge will go into C_{int}. The change in voltage at the output of the op-amp is equal to $\Delta V_{out} = Q_c/C_{int}$. The current I_R through resistance R will discharge capacitance C_{int}. This discharge current is constant, since the voltage drop over R is constant. The discharging current results in a decrease in voltage over C_{int} and hence an increase in voltage at the output of the op-amp ($t_0 - t_1$ in Fig. 2). When V_{out} crosses the threshold level of the comparator ($V_{cc}/2$), the output of the comparator switches from V_{cc} to 0 V (t_1 in Fig. 2). This voltage swing will transfer charge from C_{int} to C_{off}, resulting in a voltage jump ΔV_{out} at the output of the op-amp in opposite direction (t_1 in Fig. 2). Because the comparator switches to low-state, the output of the inverter will switch to high-state, which changes the direction of the current through R such that it will discharge C_{int} again. Since the discharge current is constant, the time duration before C_{int} is discharged and V_{out} crosses the threshold level again is $Q_c/I_R = 2RC_{off}$. Since this discharging occurs twice per period, the total oscillation period is given by

$$T_{off} = 2\frac{Q_c}{I_R} = 4RC_{off}. \quad (1)$$

As can be seen from (1), the oscillation time is proportional to the amount of charge Q_c transferred to and from C_{int}. If additional capacitors are connected in parallel to C_{off}, this will increase the amount of transferred charge and hence the oscillation time. This is the basic principle for measuring an unknown capacitance as demonstrated by Toth et al. [19]. We propose to extend the principle for the measurement of differential capacitance by switching capacitors in-phase and out-of-phase with respect to the comparator output. Doing so, the oscillation period becomes proportional to the net resulting charge from the capacitors which are switched

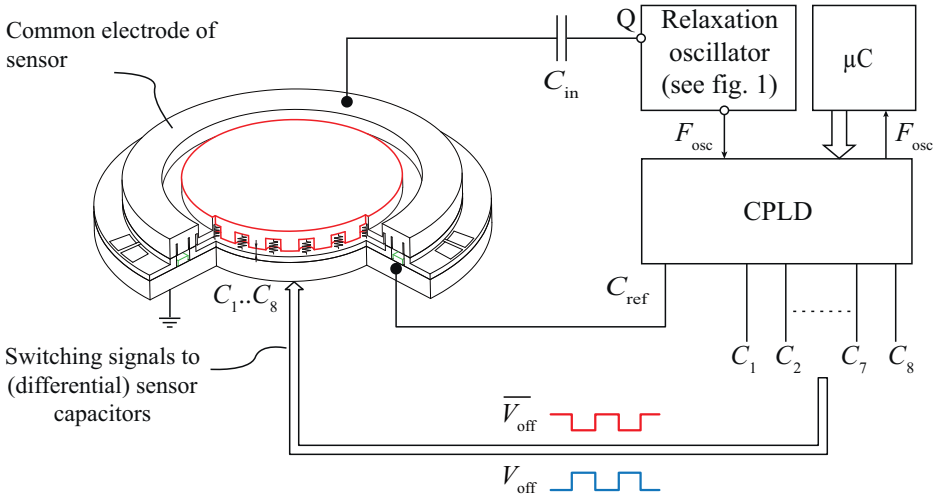

Fig. 3. Differential relaxation oscillator circuit in combination with the force sensor. The CPLD switches sensor capacitances in- and out-of-phase. A microcontroller is used for selecting the connection states and to measure the resulting oscillator frequency. In case there is a parasitic resistance parallel to the sensor capacitances, input capacitor C_{in} can be used to mitigate the influence of this resistance.

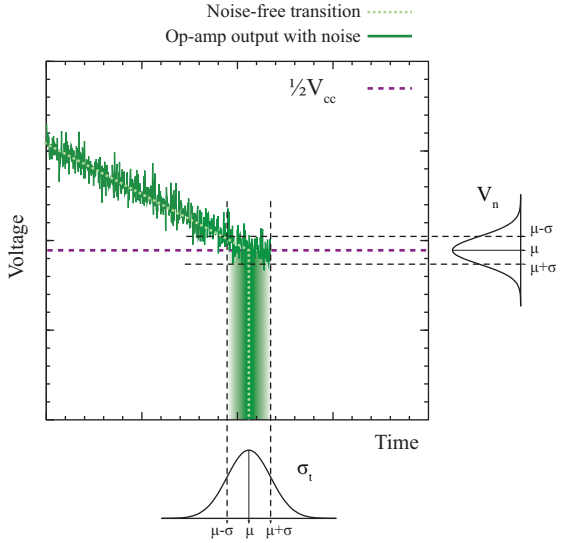

Fig. 4. Effect of noise in the op-amp signal on the switching moment of the comparator.

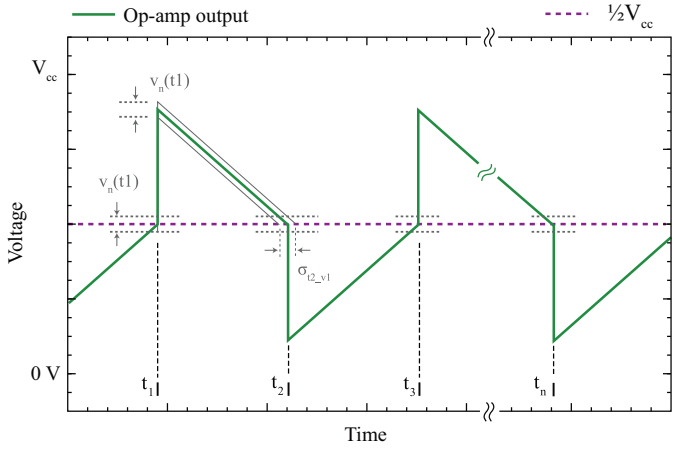

Fig. 5. Effect of noise in the op-amp signal on the switching moment of the comparator.

in-phase (Q_{in}) and out-of-phase (Q_{out}) and hence to the difference in capacitance:

$$T_{osc}(\Delta C) = 2\frac{(Q_{in} - Q_{out})}{I_R} = 4RC_{off} + 4R\Delta C, \quad (2)$$

with

$$\Delta C = C_x - C_y, \quad (3)$$

where C_x is the total capacitance switched in-phase (parallel to C_{off}) and C_y is the total capacitance which is switched out-of-phase with respect to the output of the comparator. Here, it is assumed that the peak-to-peak value of the switching voltage at the capacitors (V_x, V_y and V_{off}) is equal and $C_y < (C_{off} + C_x)$. As can be seen from (2) the absolute change in oscillation period due to a varying differential capacitance ΔC is also determined by the resistance R. The relative change in oscillation period is only determined by the ratio of the differential capacitance and the offset capacitance:

$$\frac{\Delta T_{osc}}{T_{osc}} = \frac{T_{osc}(\Delta C) - T_{off}}{T_{off}} = \frac{\Delta C}{C_{off}}. \quad (4)$$

To implement the in-phase and out-of-phase switching of the capacitors we use a complex programmable logic device (CPLD). A CPLD allows to freely define and reconfigure multiple connection states which can select any combination of the connected capacitors. This gives the possibility to determine the differential capacitance of any possible capacitor combination. Also, asynchronous logic has the potential to be faster than synchronous logic, and therefore minimal delay times can be obtained. Moreover, the outputs of the CPLD are only triggered by the output of the relaxation oscillator and not to an external clock signal. If the outputs would be triggered by a clock signal, this might lead to quantization effects in the oscillator. A micro-controller is used to select the capacitor configuration and to measure the resulting output frequency of the oscillator. Fig. 3 shows the proposed implementation of the relaxation oscillator in combination with the CPLD, micro-controller and the force sensor. The force sensor has 8 internal capacitances connected to a single node from which the sum and/or difference is measured to determine the applied force (represented by C_1 to C_8 in Fig. 3). An additional reference capacitor (C_{ref}) that is integrated at the side of the sensor chip is used for auto-calibration of the measurement.

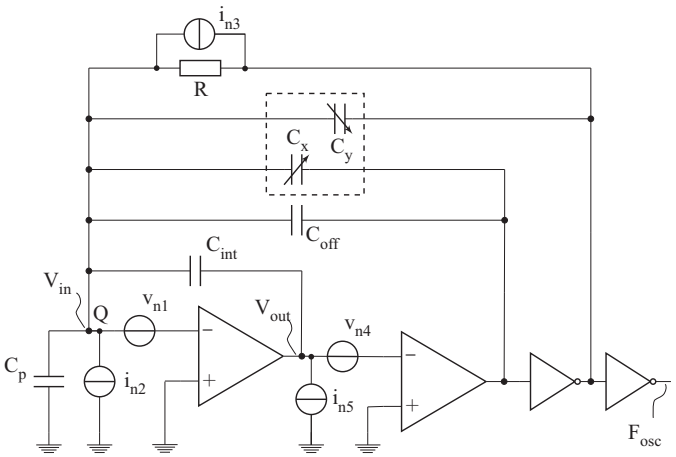

Fig. 6. Differential relaxation oscillator with the main noise sources.

Table 1
Properties of the relaxation oscillator.

Property	Symbol	Value
Noise sources and bandwidth		
Input voltage noise	v_{n1}, v_{n4}	7 nV $\sqrt{\text{Hz}^{-1}}$
Input current noise	i_{n2}, i_{n5}	0.6 fA $\sqrt{\text{Hz}^{-1}}$
Resistor current noise (T = 300 K)	i_{n3}	372 fA $\sqrt{\text{Hz}^{-1}}$
Unity-gain bandwidth of op-amp	BW_1	145 MHz
Comparator bandwidth	BW_{comp}	3 MHz
Effective rms-noise contributions at input of comparator ($BW = BW_{comp}$)		
Op-amp, v_{n1}	$V_{out\text{-}n1}$	25 μV
Op-amp, V_{n2}	$V_{out\text{-}n2}$	3.7 nV
Resistor, V_{n3}	$V_{out\text{-}n3}$	2.3 μV
Comparator voltage noise, v_{n4}	v_{n4}	12 μV

Table 2
Properties of the relaxation oscillator.

Property	Symbol	Value
Component values		
Capacitor	C_{off}	39 pF
Capacitor	C_{int}	500 pF
Resistor	R	120 kΩ
Power supply	V_{cc}	5 V
Other		
Oscillation frequency (theoretical)	F_{osc}	53 kHz
Counter frequency of micro-controller	F_{clk}	32 MHz
Op-amp, comparator	–	AD8066
Microcontroller	–	AVR ATMega32
CPLD	–	Altera EPM7064S

2.2. Auto-calibration of capacitance measurement

To compensate for errors due to drift in the interface circuit and common-mode parasitic capacitance, an auto-calibration method is used [17,31]. This method calculates the ratio of the oscillator periods of T_{off}, $T_{osc}(C_{ref})$ and $T_{osc}(\Delta C)$ to determine ratio between the unknown capacitance ΔC and a known reference capacitor:

$$\frac{\Delta C}{C_{ref}} = \frac{T_{osc}(\Delta C) - T_{off}}{T_{osc}(C_{ref}) - T_{off}}, \tag{5}$$

where C_{ref} is a stable and known reference capacitor. Assuming that parasitic capacitance and sensor drift is stable within these three measurements, this method eliminates all additive and multiplicative errors [19,32].

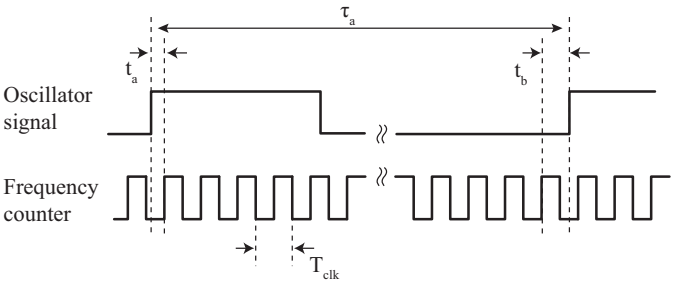

Fig. 7. Quantization noise in the frequency measurement (image modified from [40]).

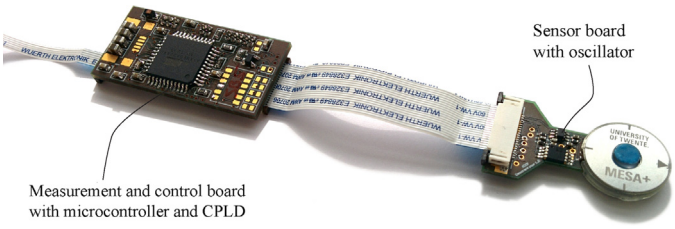

Fig. 8. Implementation of the capacitive read-out system.

3. Noise analysis

3.1. Relaxation oscillator jitter

For investigation of the noise, we define the normalized period jitter σ_{jn} in terms of the standard deviation of the period length σ_{tp} and the mean of the period length μ_{tp} resulting in [33,34]

$$\sigma_{jn} = \frac{\sigma_{tp}}{\mu_{tp}} = \frac{\sigma_{tp}}{T_{osc}}. \tag{6}$$

The square-wave oscillation signal is generated at the output of the comparator, as a result of comparing the output signal of the op-amp with $V_{cc}/2$. Noise in the voltage signal around this decision point can cause the output of the comparator to switch earlier or later in time, resulting in jitter in the oscillation period. This effect is visualized in Fig. 4, which shows a noisy op-amp signal around the ideal decision point of the comparator. The noise distribution is shown at the right of the graph, the resulting distribution in the switching moment of the comparator is shown below the graph.

The width of this distribution is dependent on the slope S of the op-amp signal; for a steep slope the time window where noise has influence on the moment of switching is small compared to a gradual slope. The switching time jitter σ_t as a result of the noise in the voltage signal around the threshold level can be approximated by [35]

$$\sigma_t = \frac{V_n}{S} \quad \text{with} \quad V_n = v_n\sqrt{BW}. \tag{7}$$

Here, V_n is the rms-voltage of the virtual noise-source in series with the op-amp, seen at the input of the comparator and is assumed to be white noise with a flat spectral density V_n with bandwidth BW. The slope S of the signal at the output of the op-amp can be found by dividing the voltage jump over half of the period length:

$$S = \frac{V_{cc}(C_{off} + \Delta C)}{C_{int}} \frac{1}{2R(C_{off} + \Delta C)} = \frac{V_{cc}}{2C_{int}R}. \tag{8}$$

To determine the total jitter, the influence of a noisy switching moment on a complete period has to be examined. Fig. 5 shows the signal waveforms of the op-amp output in case there is no noise present and the influence of noise on the oscillation signal. We assume that the absolute value of the voltage step is the same

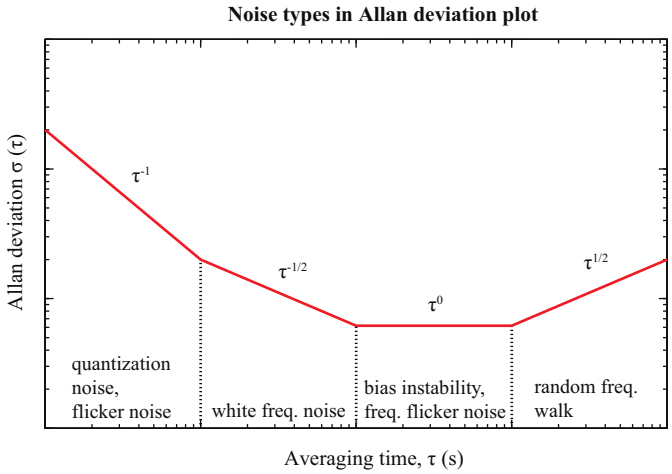

Fig. 9. Sample plot of Allan deviation and the characteristics of a noise source (image modified from [44,45]).

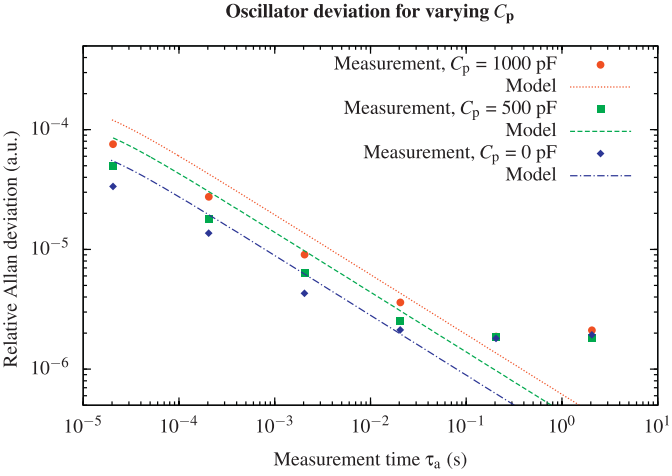

Fig. 10. Relative Allan deviation over 200 samples as a function of the measurement time for different values of C_p. The resistance R is kept at 120 kΩ and C_{int} at 500 pF.

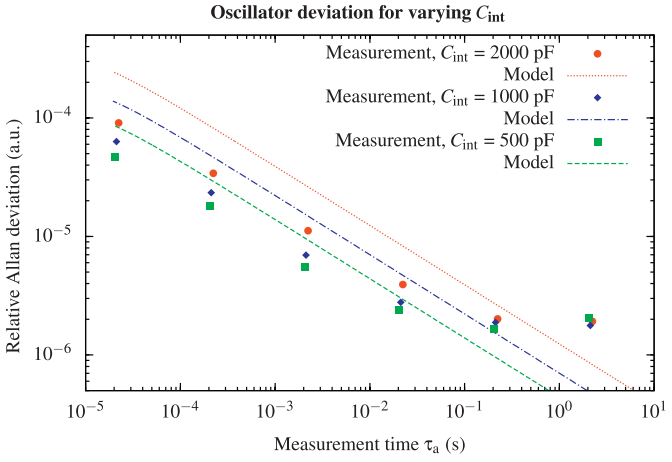

Fig. 11. Relative Allan deviation over 200 samples as a function of the measurement time for different values of C_{int}. The resistance R is kept at 120 kΩ and parasitic capacitance at 500 pF.

for each switching moment, since this step is determined by the charge going into C_{int}. Starting at switching moment t_1, noise V_n can cause the comparator to switch earlier or later and as a result the maximum level of the peak after switching is higher or lower. A lower peak decreases the length of the first half-period, since

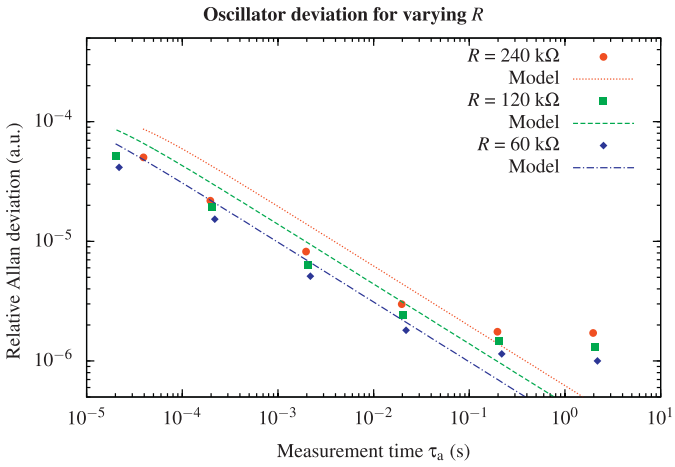

Fig. 12. Relative Allan deviation over 200 samples as a function of the measurement time for different values of R. The feedback capacitance and the parasitic capacitance are kept constant. (C_{int} = C_p = 500 pF).

the signal reaches the comparator switching level earlier as shown in the figure. Contrarily, a higher peak causes the first half-period to lengthen. Noise around switching point t_2 has influence on the length of both, the first and the second half-period. Switching earlier will cause the first half-period to shorten, and as a result the voltage after switching will be closer to $V_{cc}/2$, which also shortens the second half-period. Noise around switching point t_3 can shorten or lengthen the second half-period, and also influences the voltage level after switching for the following period. Assuming that the noise at each switching point has the same intensity and is uncorrelated, the jitter over one period is given by

$$\sigma_{jp} = \sqrt{\sigma_t(t_1)^2 + (2\cdot\sigma_t(t_2))^2 + \sigma_t(t_3)^2} = \sqrt{6}\cdot\sigma_t, \tag{9}$$

where $\sigma_t(t_1)$, $\sigma_t(t_2)$ and $\sigma_t(t_3)$ corresponds to the noise contribution of the switching moments t_1, t_2 and t_3 in Fig. 5. The equation above gives the jitter over one period. To reduce the jitter on the period measurement the average value over multiple periods can be used. To determine this, first the jitter over n switching moments is defined:

$$\sigma_{tm}(n) = \sqrt{\sigma_t(t_1)^2 + (2\cdot\sigma_t(t_2))^2 + (2\cdot\sigma_t(t_3))^2 + \cdots + \sigma_t(t_n)^2}. \tag{10}$$

This summation can also be expressed as

$$\sigma_{tm}(n) = \sqrt{(4n-6)}\cdot\sigma_t. \tag{11}$$

From this, the average jitter over the number of periods N_p can be expressed as

$$\sigma_{jp}(N_p) = \frac{\sqrt{(8N_p-2)}}{N_p}\cdot\sigma_t \quad \text{using} \quad n = 2N_p + 1. \tag{12}$$

Using (6), (7), (8) and (12) the jitter relative to the oscillation period as a function of the rms-noise voltage can be written as

$$\sigma_{jn}(N_p) = \frac{\sigma_{jp}(N_p)}{T_{osc}} = \frac{C_{int}}{2V_{cc}(C_{off}+\Delta C)}\frac{\sqrt{(8N_p-2)}}{N_p}\cdot V_n. \tag{13}$$

The number of periods N_p is related to the time over which the period is measured. This averaging time can simply be found by multiplying the number of periods by its period length:

$$\tau_a = N_p T_{osc}, \tag{14}$$

where τ_a is the averaging time. Eventually, the averaging time is important for characterizing the noise performance. Therefore, we express (13) as a function of the averaging time

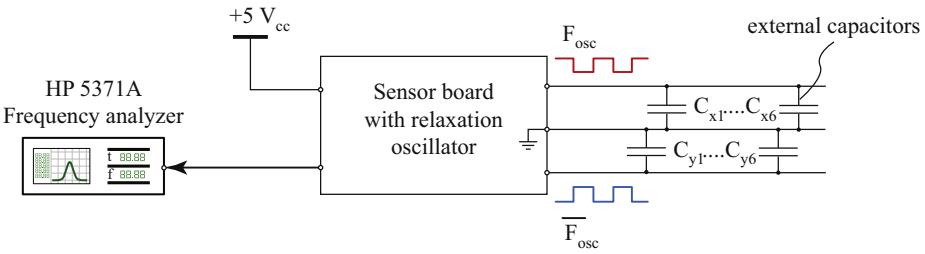

Fig. 13. Frequency measurement setup.

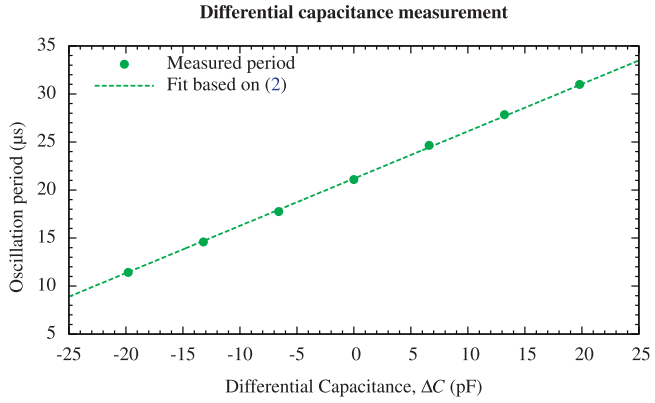

Fig. 14. Measured frequency of the relaxation oscillator when the differential capacitance is changed from −20 pF to 20 pF.

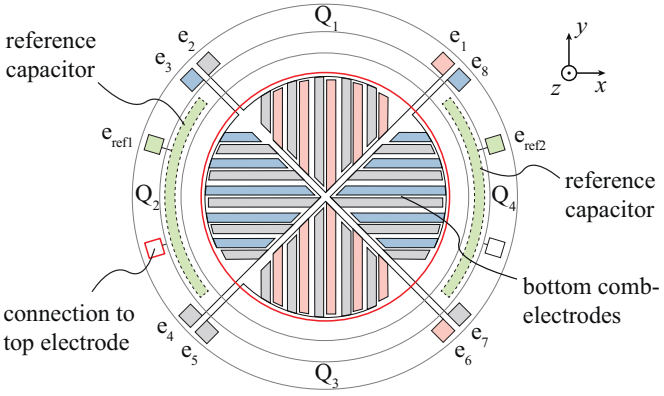

Fig. 15. Configuration of the bottom electrodes (top view). The electrodes are divided in four quadrants, each quadrant consists of a pair of comb-fingers.

$$\sigma_{jn}(\tau_a) = \frac{\sigma_{jp}(N_p)}{T_{osc}} = \frac{C_{int}}{2V_{cc}(C_{off}+\Delta C)}\frac{\sqrt{(8(\tau_a/T_{osc})-2)}}{(\tau_a/T_{osc})}\cdot V_n. \quad (15)$$

For $\tau_a \gg T_{osc}$ this can be approximated by

$$\sigma_{jn}(\tau_a) \approx \frac{C_{int}}{V_{cc}(C_{off}+\Delta C)}\sqrt{\frac{2T_{osc}}{\tau_a}}\cdot V_n. \quad (16)$$

Using (2) this can be expressed as

$$\sigma_{jn}(\tau_a) \approx \frac{2C_{int}}{V_{cc}}\sqrt{\frac{2R}{\tau_a(C_{off}+\Delta C)}}\cdot V_n. \quad (17)$$

From this equation it can be seen that when expressing (13) in terms of the averaging time τ_a, the total jitter is also dependent on the resistance R.

3.2. Noise sources

The jitter σ_{jn} is defined as a function of the rms-noise V_n in series with the comparator signal. To determine V_n, the noise sources in the circuit are analysed and their effect on the noise at the input of the comparator is determined. To this end, we consider the schematic with the relevant noise sources shown in Fig. 6, where the voltage and current noise of the op-amp are indicated by v_{n1} and i_{n2}, respectively. The voltage and current noise of the comparator are indicated by v_{n4} and i_{n5}, respectively and the noise in resistance R is shown as current noise source i_{n3} parallel to the resistance. In this analysis, the noise is considered to be white (flat-band spectrum) and noise sources are assumed to be uncorrelated. In case of the noise generated by the resistor R this is a valid approximation, for the noise contribution of the op-amp this assumption results in a slight under-estimation of the noise since for lower frequencies pink noise has a dominant contribution, where for higher frequencies white noise has a dominant contribution.

3.2.1. Op-amp noise

Voltage noise v_{n1} at the input of the op-amp will cause a proportional noise at the output of the op-amp. The proportionality is determined by the voltage divider seen from the output of the op-amp to point Q of the circuit, which is determined by the feedback capacitor C_{int} and all impedances which are connected to point Q in the circuit. For simplicity, we assume that the impedance is dominated by the capacitances and therefore we ignore the presence of R in the circuit. With this assumption, the output referred noise voltage $V_{out\text{-}n1}$ as a result of noise at the input of the op-amp v_{n1} is given by

$$v_{out\text{-}n1} = v_{n1}A, \quad (18)$$

where A is the closed-loop amplification factor of the op-amp:

$$A = \frac{C_{int}+C_{off}+C_x+C_y+C_p}{C_{int}}. \quad (19)$$

The rms-noise is then given by

$$V_{out\text{-}n1}(BW) = v_{n1}A\sqrt{BW}, \quad (20)$$

where BW is the effective noise bandwidth. The effective bandwidth of the op-amp is given by

$$BW_{amp} = \frac{BW_1}{A}, \quad (21)$$

where BW_1 is the unity gain bandwidth of the op-amp.

Current noise i_{n2} and i_{n3} at the input of the op-amp will effectively flow through C_{int} because the voltage at point Q is kept at $V_{cc}/2$. The feedback capacitor C_{int} integrates this current to a voltage, equal to [33]:

$$v_{out\text{-}ni}(t_r) = \frac{1}{C_{int}}\int_0^{t_r} i_{ni}(t)dt \quad \text{with} \quad i = 2 \vee 3, \quad (22)$$

where $i_{ni}(t)$ with $(i = 2 \vee 3)$ represents the noise current in the time domain. The time t_r in which the noise current charges C_{int} is equal

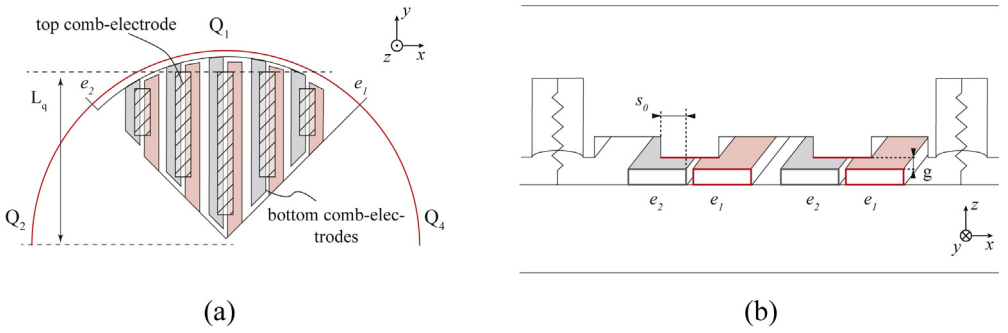

Fig. 16. (a) Schematic representation of the comb-electrode configuration in a single quadrant where the hatched part indicates the position of the top electrode. (b) Part of the cross section showing the position of the top electrode with respect to the bottom electrodes.

Table 3
CPLD capacitor connection states.

Electrodes		e_{ref1}	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_{ref2}
State	Name										
0	S_{off}	0	0	0	0	0	0	0	0	0	0
11	S_{ref1}	F_{osc}	0	0	0	0	0	0	0	0	0
21	S_{Fx}	0	0	0	F_{osc}	$\overline{F_{osc}}$	0	0	$\overline{F_{osc}}$	F_{osc}	0
22	S_{Fy}	0	F_{osc}	$\overline{F_{osc}}$	0	0	$\overline{F_{osc}}$	F_{osc}	0	0	0
23	S_{Fz}	0	F_{osc}	$\overline{F_{osc}}$	F_{osc}	F_{osc}	F_{osc}	F_{osc}	F_{osc}	F_{osc}	0
24	S_{Mx}	0	$\overline{F_{osc}}$	$\overline{F_{osc}}$	0	0	F_{osc}	F_{osc}	0	0	0
25	S_{My}	0	0	0	$\overline{F_{osc}}$	$\overline{F_{osc}}$	0	0	F_{osc}	F_{osc}	0
26	S_{Mz}	0	$\overline{F_{osc}}$	F_{osc}	$\overline{F_{osc}}$	F_{osc}	$\overline{F_{osc}}$	F_{osc}	$\overline{F_{osc}}$	F_{osc}	0
–	S_{ref2}	0	0	0	0	0	0	0	0	0	F_{osc}

to half of the oscillator period ($t_r = T_{osc}/2$). Assuming a flat spectral density and first order frequency roll off with bandwidth $BW \gg 1/t_r$, it can be shown that [33,36]

$$V_{\text{out-n}i} = \frac{1}{C_{\text{int}}} i_{ni} \sqrt{\frac{T_{\text{osc}}}{2}} \quad \text{with} \quad i = 2 \vee 3, \tag{23}$$

which can be expressed as

$$V_{\text{out-n}i} = \frac{1}{C_{\text{int}}} i_{ni} \sqrt{\frac{4R(C_{\text{off}} + \Delta C)}{2}} \quad \text{with} \quad i = 2 \vee 3. \tag{24}$$

3.2.2. Comparator noise

The current noise source i_{n5} at the input of the comparator generates a noise voltage proportional to the impedance seen at this point. Since the output impedance of the op-amp is very low, the current source is in fact short-circuited and therefore the contribution of the current noise source can be neglected. The voltage noise v_{n4} in series with the input of the comparator will add up to the noise from the output of the op-amp. The rms-voltage of the comparator voltage noise source is given by

$$V_{\text{out-n4}} = v_{n4} \sqrt{BW_{\text{comp}}}. \tag{25}$$

where BW_{comp} is the effective noise bandwidth of the comparator.

3.2.3. Comparator bandwidth

The influence of the comparator on the noise bandwidth in a relaxation oscillator has been studied extensively by Gierkink [37]. The noise at the input of the comparator is only passed on during the time that the input stage of the comparator is switching, i.e. only during the transition from one state to the other the transconductance of the input stage converts the input voltage noise into a noise current. The output current of the input stage ultimately results in charging of the comparators internal capacitances in order to switch the output from a low to high state or vice versa. The noise current will be effectively integrated in a similar way as the noise currents i_{n2} and i_{n3} are integrated by C_{int}, only the integration time

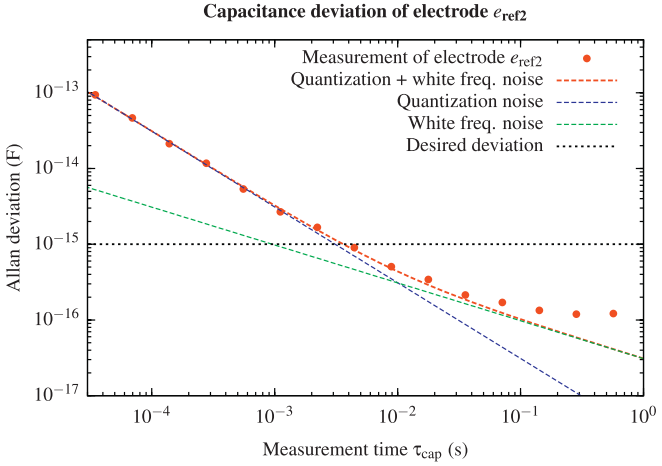

Fig. 17. Allan deviation of the measured capacitance of electrode e_{ref2} as a function of the averaging time τ_{cap}. (C_{int} = 500 pF, R = 60 kΩ, C_{ref2} = 5.460 pF).

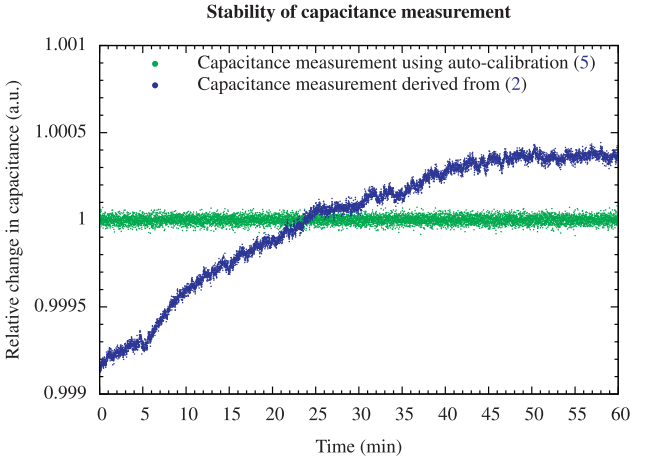

Fig. 18. Relative change of measured capacitance of electrode e_{ref2} over a measurement time of 60 min with auto-calibration (green) and without auto-calibration derived from (2) (blue). (C_{int} = 500 pF, R = 60 kΩ, C_{ref2} = 5.460 pF). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

will not be related to the oscillator period, but will be defined by the switching time of the comparator. From the specified slew-rate of the comparator (160 V μs^{-1}) we can easily estimate that the minimum switching time is in the order of 0.03 μs which would be reached if the comparator's input stage is driven instantaneously from one extreme to the other. In our case the input voltage is gradually changing in time and therefore the switching time will be

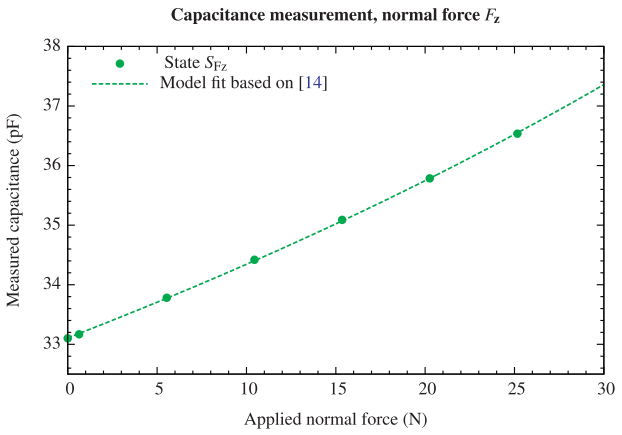

Fig. 19. Measured capacitance when a normal force F_z is applied from 0 to 25 N.

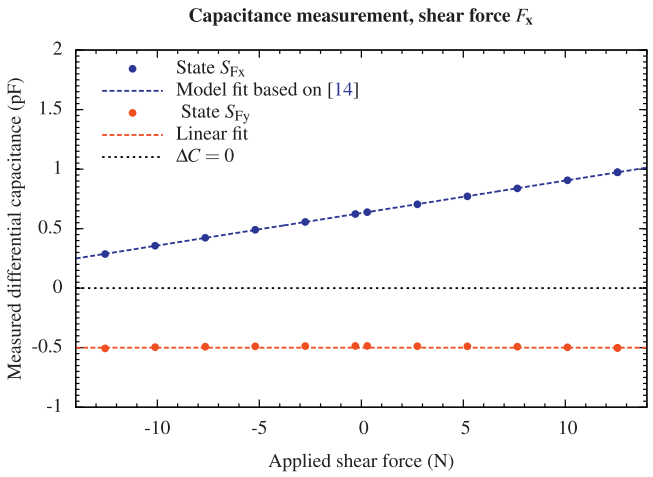

Fig. 20. Measured differential capacitance when a shear force F_x is applied from −12 to 12 N.

longer. Measurement of the slope of the output voltage shows that the switching time is in the order of 0.3 μs, therefore we assume that $BW_{comp} \approx 3$ MHz.

3.2.4. Total equivalent comparator noise

Since the bandwidth of the comparator is the lowest, the output referred rms-noise voltage can be found by using $BW = BW_{comp}$ in (20). The contribution of the current noise sources can be found using (23) and the comparator noise is given in (25). In Table 1 the contribution of the noise sources is given, where the component values given in Table 2 are used to calculate the rms-noise. As can be seen, the voltage noise of the op-amp and the comparator dominate in the contribution to the rms-noise voltage. Due to the FET input op-amp used in the circuit the noise current i_{n2} is very low and therefore its contribution to the op-amp output voltage noise negligible.

All noise sources are considered to be uncorrelated, therefore we obtain the total equivalent rms-noise V_n by calculating the root of the sum of squares:

$$V_n = \sqrt{V_{out\text{-}n1}^2 + V_{out\text{-}n2}^2 + V_{out\text{-}n3}^2 + V_{n4}^2}. \quad (26)$$

3.2.5. Quantization jitter

To measure the frequency, a high-speed counter will be used where the number of counts over one or more periods is measured. This quantization of the frequency will lead to errors in the frequency measurement. The high-speed counter will start counting at the rising-edge of the oscillator signal, the counter is stopped when the number of periods N_p over which the frequency is measured is reached. In case there is no coherence between the oscillation frequency and the counter frequency an error is introduced at the begin and end of each measurement, which is visualized in Fig. 7. The relative error on the frequency measurement is given by

$$t_q = \frac{t_a + t_b}{N_p T_{osc}}, \quad (27)$$

where t_a and t_b are the timing errors at the begin and end, respectively. The maximum error occurs when the oscillation period is slightly less than an integer multiple of the frequency counter and is worst-case two times the counter clock period (T_{clk}), the error is zero when the oscillator period is exactly an integer multiple of T_{clk}. Assuming no coherence, the quantization error has a uniform distribution [38,39] and the rms-value is given by

$$\sigma_q(\tau_a) = \frac{T_{clk}}{\tau_a \sqrt{6}}. \quad (28)$$

3.3. Noise in capacitance measurement

The period jitter as a result of circuit noise and quantization noise results in a deviation in the capacitance measurement through the transfer function from period to capacitance. Since the circuit jitter and the quantization jitter are uncorrelated, the contribution of both to the total period jitter can be found by

$$\sigma_{tot}(\tau_a) = \sqrt{\sigma_{jn}^2(\tau_a) + \sigma_q^2(\tau_a)}. \quad (29)$$

The transfer function for a relative change in period to a relative change in capacitance is given in (4). From this equation it can be seen that the total jitter directly converts into a deviation in the capacitance σ_{cap} by

$$\sigma_{cap}(\tau_a) = \sigma_{tot}(\tau_a) \cdot C_{off}. \quad (30)$$

If the capacitance is calculated using the auto-calibration method in Eq. (5), three measurements have to be performed to calculate the unknown capacitance. This will result in an increase in the deviation in capacitance, due to the jitter in each individual measurement. When the measured capacitance is approximately equal to the reference capacitance, an approximation for the deviation when using three measurements is given by

$$\sigma_{3cap}(\tau_a) \approx \sigma_{tot}(\tau_a) \cdot \sqrt{2(2C_{off}^2 + C_{ref}^2 + C_{off}C_{ref})}. \quad (31)$$

Here, it is assumed that there is no correlation between the numerator and denominator in (5), which results in an over-estimation of the deviation in the capacitance.

4. Experimental results

4.1. Implementation

Fig. 8 shows the realized capacitive read-out circuit. To keep the part where the force sensor is mounted on as compact as possible, the system consists of two parts. On one printed circuit board (PCB) the oscillator is placed together with the force sensor. The micro-controller (AVR ATMega32) and CPLD (Altera EPM7064S) are placed on a second PCB and are connected to the sensor-board using a flexible connection. There is no specific requirement on the micro-controller that can be used, but a higher clock frequency of the micro-controller will result in a lower quantization noise of the frequency measurement, as explained in Section 3.2.5. The CPLD is chosen mainly for its low pin-count, compared to its alternatives. Communication with the read-out system is done

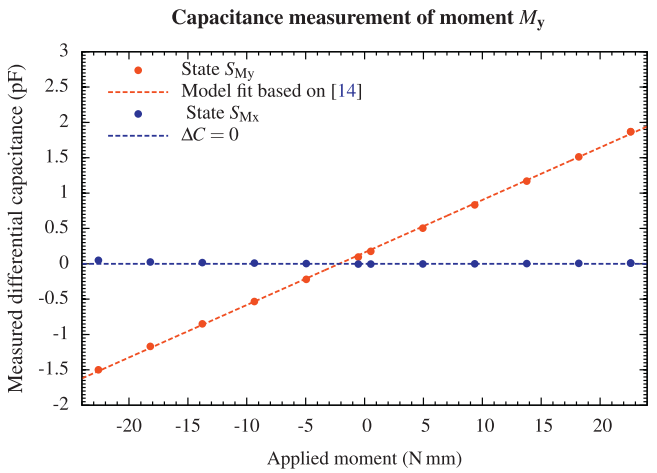

Fig. 21. Measured differential capacitance when a moment M_y is applied from −22 to 22 N mm.

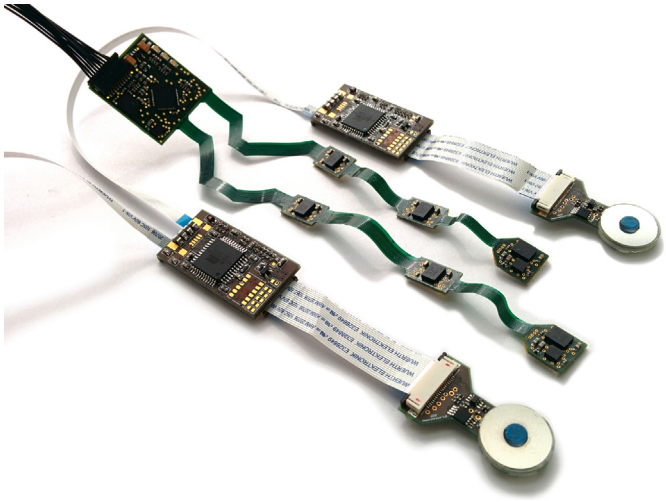

Fig. 22. Force sensors and kinematic sensors.

via an I2C interface. The op-amp and comparator in the oscillator circuit are realized using an AD8066 dual amplifier. Further, the counter sampling frequency F_{clk} is 32 MHz ($T_{clk} = 1/F_{clk}$). Using (2) and the values listed in Table 2, the calculated oscillation frequency is 53 kHz, assuming $C_x = C_y = 0$. The oscillation frequency is chosen to be significantly lower than the op-amp bandwidth to ensure a linear relation between the measured capacitance and the oscillation period [19]. The offset capacitance C_{off} is chosen at 39 pF, which implies that ΔC must be higher than −39 pF. For the force sensor presented in [14], the differential capacitance at maximum load is 5 pF which is within the lower range limit. The upper limit is determined by C_{int}, the maximum capacitance must be below $C_{int}/2$ as explained in Section 2.1.

4.2. Relaxation oscillator noise

For measuring the noise performance of the circuit, a high speed frequency counter is desired to minimize the noise introduced by quantization in the frequency measurement. Therefore, a frequency analyser with a high counter resolution of 150 ps is used (HP 5371A). The quantization noise introduced by the frequency counter is significantly lower than the expected noise from the oscillator and therefore negligible. The influence of C_{int}, C_p and R on the noise performance is examined by measuring Allan deviation [41–43] as a function of averaging time τ_a over which the oscillation frequency is measured. The Allan deviation provides a convenient measure of the noise sources in the system, where the slope of the deviation identifies the type of noise as indicated in Fig. 9. The Allan deviation in terms of the oscillation period is defined as the deviation of the differences between successive averages of the oscillation period:

$$\sigma_a = \left[\frac{1}{2(M-1)} \sum_{i=1}^{M-1} (y_{i+1} - y_i)^2 \right]^{1/2}, \tag{32}$$

where M is the number of samples over which the Allan deviation is determined and y_i are the oscillation period averages with averaging time τ_a. The relative Allan deviation is defined as

$$\sigma_{an} = \frac{\sigma_a}{\mu_{tp}}, \tag{33}$$

where μ_{tp} is the mean of the oscillation period.

For the noise performance measurement, the component values listed in Table 2 are used as initial starting point. The measurement setup shown in Fig. 13 is used, where capacitances C_x and C_y are not connected. The parasitic capacitance of the force sensor in [14] is approximately 500 pF. Therefore, in all measurements a static parasitic capacitance of 500 pF is added to simulate the presence of the sensor, unless otherwise noted. The time τ_a is varied by increasing the number of periods N_p over which the frequency is measured, starting from 1 and using increments by a factor of 10 up to 10^5.

Fig. 10 shows the influence of the parasitic capacitance on the deviation of the oscillator frequency. As predicted by the model for the op-amp voltage noise in (18), a higher value for C_p increases the jitter in the oscillator. Also, for higher values of the measurement time τ_a, the total deviation decreases up to an average time of 200 ms ($N_p = 10^4$). For higher values random walk and drift dominate in the contribution to the jitter.

The influence of the feedback capacitance C_{int} is shown in Fig. 11. A higher value for C_{int} decreases the slope of the oscillator signal and therefore increases the contribution of the voltage noise at the input of the comparator to the jitter as shown in Eq. (15).

Fig. 12 shows the influence of resistance R on the deviation of the oscillator frequency. For this measurement, the feedback capacitance C_{int} and the parasitic capacitance C_p is kept constant at 500 pF. Since R changes the frequency of the oscillator, the number of periods N_p is adjusted such that measurement time τ_a is approximately equal for all values of R. As shown in the figure, a lower value for R decreases the measured deviation, due to the increased slope of the oscillation signal.

4.3. Differential capacitive measurement

To prove that switching in and out-of-phase with the oscillator signal F_{osc} results in a period which is proportional to differential capacitance as shown in (2), a differential capacitive measurement is performed with the measurement setup shown in Fig. 13 and the component values from Table 2. The differential capacitance is varied from −20 pF to 20 pF using discrete capacitors. To this end, 6 capacitors with a capacitance value of 3.3 pF are connected parallel to the out-of-phase signal (C_y) while no capacitors are connected to the in-phase signal (C_x). The differential capacitance is varied by moving a capacitor from C_y to C_x, resulting in a difference in capacitance of 6.6 pF for every step while keeping the total capacitance ($C_y + C_x$) constant. The capacitors are first measured using an LCR-meter (HP 4284A) to ensure that the maximum deviation is within 1% of the capacitance value. The resulting frequency is measured using an HP 5371A frequency analyser. The measured oscillation period as function of the differential capacitance is shown in Fig. 14, and shows that the measured oscillation period is in good

agreement with the model in (2). The offset capacitance C_{off} was fitted to 43 pF and R was fitted to 123 kΩ.

4.4. Multi-axis force sensor

To prove the functionality of the proposed capacitive measurement system, we interface the system to the force sensor presented in [14]. This force sensor consists of two main parts: a top electrode which will displace when a force and/or torque is applied and a bottom part with electrodes. The displacement of the top electrode is determined by measuring the capacitances of the (differential) electrodes integrated in the sensor, from the measured capacitances the applied load is calculated. Fig. 15 shows the electrode configuration in the bottom part of the sensor and in Fig. 16(a) and (b) a detailed representation of the top and bottom electrodes is shown. A complete explanation of the operating principle of the sensor can be found in [14].

4.4.1. Measurement setup

The measurement setup shown in Fig. 3 is used to measure the (differential) capacitances of the electrodes in the sensor. Connection states are defined in the CPLD which determine the electrode configuration. The defined connection states are shown in Table 3, where F_{osc} and $\overline{F_{osc}}$ indicate that the selected capacitor is switched in-phase or 180° out-of-phase with the oscillator signal, respectively. The sensor capacitors in the first row of the table correspond to the electrode overview given in Fig. 15. The states in the CPLD are selected by the microcontroller and the frequency is measured over an adjustable number of periods of the oscillator signal using an internal counter running at 32 MHz. The counter values are sent to a PC for further data processing. A complete measurement cycle consists of measuring the period of each state listed in Table 3, the corresponding capacitance is calculated using (5), where e_{ref1} is used as reference capacitor.

4.4.2. Allan deviation in capacitive measurement

The deviation in the capacitive measurement is determined by measuring the capacitance of the second reference electrode. The capacitance of this electrode is determined using three consecutive measurements, as explained in Section 2.2. First, the oscillation period of the free running oscillator is measured (State S_{off} in Table 3) then the oscillation period when connecting the first reference electrode is measured (State S_{ref1} in Table 3) followed by measuring the oscillation period when connecting the second reference capacitor (State S_{ref2} in Table 3). The capacitance of the second electrode is calculated using (5). The Allan deviation as a function of the averaging time is determined, to observe the noise characteristics of the measurement. The averaging time is varied by changing the number of periods N_p over which the oscillation period is measured. Since three measurements are performed, the total measurement time for measuring the capacitance is given by

$$\tau_{cap} = N_p(T_{off} + T_{ref1} + T_{ref2}), \tag{34}$$

where T_{off}, T_{ref1} and T_{ref2} are the oscillation period of states S_{off}, S_{ref1} and S_{ref2}, respectively. The measured Allan deviation as a function of the measurement time τ_{cap} is shown in Fig. 17. In the graph, the contribution of the quantization noise obtained using the model in (28) and the contribution of the white frequency noise obtained from the measurement shown in Fig. 12 is also shown, where (31) is used to calculate the deviation. As shown, a total measurement time of more than 280 ms does not improve the Allan deviation on the measurement due to low frequency noise. The measured mean value of the capacitance e_{ref2} is 5.460 pF, the lowest measured deviation on the measurement is 0.12 fF at a total measurement time of τ_{cap} = 280 ms, which corresponds to N_p = 8192. The desired resolution is shown in the same graph from which it can be seen that a measurement time of 4.4 ms and higher results in a deviation which is better than the desired resolution.

4.4.3. Stability of capacitive measurement

The stability of the capacitance measurement is determined using the same switching scheme as used in previous section, where a total measurement time of τ_{cap} = 280 ms is used. Fig. 18 shows the relative change of the measured capacitance of e_{ref2} with a mean value of 5.460 pF over a time of 60 min. When the capacitance is calculated using the auto-calibration method in (5), any common-mode variation in oscillation frequency due to, e.g. temperature fluctuation is cancelled out, resulting in a standard deviation over the complete measurement period of 0.12 fF. When the capacitance is derived from the oscillation frequency using (2), the measured standard deviation is significantly higher (2.0 fF).

4.4.4. Force measurements

As a proof of concept, force and moment measurements are performed. To measure the internal capacitances of the force sensor, all the states in Table 3 are measured successively with a measurement time of 4.4 ms per channel. To apply forces, the measurement setup presented in [14] is used. The measured capacitance of the sensor as a function of the applied normal force, moment and shear force is shown in Figs. 19, 20 and 21, respectively. The initial offset in the differential capacitance for states S_{Fx} and S_{Fy} (Fig. 20) is caused by misalignment of the top and bottom electrode caused during the fabrication of the sensor. The measured response of the sensor to the applied forces and moment is in good agreement with the response measured in [14].

5. Discussion

5.1. Noise performance

The measured jitter in the oscillator is lower than the theoretically predicted values from the analysis in Section 3. Two main contributions to the calculated jitter are the op-amp and comparator voltage noise. For the comparator, the bandwidth is estimated by the slope measured at the output, which might result in too high estimation of the bandwidth. The effective bandwidth depends on the charging times of internal capacitances [37]. Without detailed knowledge of the internal circuitry of the op-amp used as comparator, it is difficult to estimate an accurate value for this bandwidth. Further, the specified noise density of the dual op-amp used in the circuit might be lower in practice. Qualitatively, the measurements are in agreement with the model for the noise in the circuit. From the measurements and from the model it can be seen that lower values for C_{int}, C_p and R result in lower noise.

5.2. Capacitance measurement

The Allan deviation measurement of the capacitance in Fig. 18 shows that a total averaging time of τ_{cap} = 4.4 ms results in a deviation of 0.9 fF and an acquisition rate of 225 Hz when using the auto-calibration in (5). A total acquisition consist of measuring 6 capacitor configurations, resulting in a sample rate of 38 Hz which is sufficient for the desired application of measuring interactions at the fingertip. The deviation of 0.9 fF results in an error ranging from 0.12% to 0.01% of the full scale for measuring shear force and normal force, respectively. From the same measurement it can also be seen that the deviation for short averaging times is dominated by the quantization noise of the frequency counter. Around the averaging time of τ_{cap} = 4.4 ms, an increase of the counter frequency with a factor four (F_{clk} = 128 MHz) would approximately result in a deviation which is a factor two lower. Therefore, the most attractive method for improving the deviation at low averaging times is

increasing the counter frequency. Currently this counter frequency is limited by the internal counter of the micro-controller, which is 32 MHz. The deviation can be improved further by optimizing the component values for the measurement range. Increasing the voltage V_{cc} is also a possibility, however, since the logic components are compatible to a maximum of 5 V, level converters or high voltage logic would be required. Depending on the application, the averaging time can also be increased to reduce the deviation on the measurement. The lowest measured deviation is 0.12 fF at a total averaging time of τ_{cap} = 280 ms (3.5 Hz), which could be used for quasi-static measurements.

5.3. Power consumption and resolution

The noise analysis in Section 3 and the measurements in Section 4 are performed to reveal the influence of the individual components on the noise characteristics of the oscillator. With this analysis the best combination of components can be chosen to obtain an optimal resolution for the given measurement range and shows the influence of a parasitic capacitance on the noise. For the implemented read-out interface there was no specific requirement on the power consumption of the circuit. Therefore, the components used in the circuit were selected based on their noise characteristics to obtain the desired resolution. Currently the CPLD and op-amps are dominant in the power consumption. The op-amps can be replaced by a low-power alternative with similar noise characteristics. The CPLD can be replaced by standard logic components to reduce power consumption, but the use of a CPLD gives great flexibility in defining the connection states, since any (differential) capacitor combination can be freely redefined. As an alternative, the presented system can be realized using a micro-controller with integrated asynchronous logic. This will reduce overall power consumption and requires less components.

5.4. System design

The force sensor and the sensing circuit is designed to be integrated in a system which also includes kinematic sensors [46]. Fig. 22 shows a photograph of the combined system. Currently, a maximum of three force sensors including capacitive read-out can be connected to the system using daisy chaining.

6. Conclusion

A multi-electrode differential capacitive sensing circuit is designed and realized for the read-out of a multi-axis capacitive force–torque sensor. The sensing circuit is based on a new method for measuring differential capacitance by using a relaxation oscillator. Reprogrammable asynchronous logic can be used to select and measure the capacitors connected to the system, such that any desired combination can be defined. The noise performance of the oscillator in the system is analysed and characterized using the Allan deviation to determine the oscillator stability. This revealed the influence of individual component values on the noise performance of the system and provides a design guide for obtaining a good noise performance. Auto-calibration using a three-measurement approach shows a clear improvement in the stability for long-term measurements, since it minimizes all multiplicative and additive errors in the read-out circuit. Capacitance measurements show that a deviation of 0.9 fF for a capacitance value of 5.5 pF is obtained at an acquisition rate of 225 Hz including auto-calibration. The lowest obtained deviation is 0.12 fF for the same capacitance value at an acquisition rate of 3.5 Hz. For fast acquisition rates, the read-out system is mainly limited by the quantization noise due to the frequency counter, and can be improved by using a faster counter. The read-out circuit can be further improved by optimizing the component values for the desired capacitance range, to obtain a lower noise level. The system is successfully interfaced to the multi-axis capacitive force–torque for the read-out of six capacitor configurations at an acquisition rate of 38 Hz. The measured response of the sensor to the applied forces and moment is in good agreement with the response measured in [14].

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