Regular Correspondence

A Voltage-Controlled Switched-Capacitor Relaxation Oscillator

KEN MARTIN

Abstract—**A new switched-capacitor (SC) oscillator is described. The oscillator is easily modified to be either voltage controlled or digitally programmed. Although the oscillator is practical only when its oscillating frequency is less than about 1/25 the clock frequency (because of the excess phase jitter that develops at higher ratios), it is useful in a number of low frequency applications, especially when stability is important.**

I. Introduction

The realization of monolithic analog switched-capacitor (SC) filters using MOS technology is now well understood [1]-[6]. Recently, a number of other analog signal processing functions realizable using SC techniques have been reported. Examples include a half-wave rectifier [7], a zero-crossing detector and a peak detector [8], a tracking filter, a phase-lock loop and a balanced demodulator [9], and an SC oscillator [10].

This correspondence describes a new SC building block, specifically, a relaxation oscillator that should be useful in a number of signal processing systems. As opposed to the oscillator of [10], the new structure is insensitive to parasitic capacitances. Furthermore, the oscillating frequency can be either digitally programmed or voltage controlled with very good linearity. It is practical only when the oscillating frequency is much less than the clock frequency and when a square-wave output is acceptable.

II. Circuit Realization

The circuit of the SC relaxation oscillator is shown in Fig. 1. To understand its operation, assume that the second op amp has its output saturated at $-V_{ss}^{1}$ and V' is slightly positive. The capacitor K_2C will inject a charge ΔQ into the feedback capacitor C during ϕ_2 where ΔQ is equal to K_2CV_{ss}. (ϕ_1 and ϕ_2 are two phase nonoverlapping clocks.) This will cause V' to go negative by $\Delta V'$ where $\Delta V'$ is equal to K_2V_{ss}.

If this change in voltage is enough to make V' negative, then V_{out} will saturate positive to $+V_{cc}$, and hence V' will be driven more negative by $K_1(V_{cc}+V_{ss})$. In each additional period, the capacitor K_2C will now cause V' to go positive by $\Delta V' = K_2V_{cc}$ until V' becomes larger than zero, V_{out} saturates negative, and K_1C drives V' more positive by $K_1(V_{cc}+V_{ss})$, whereupon K_2C starts charging V' back to zero. If one makes the assumption that $K_2 \ll K_1$, then the oscillating frequency is given by

$$f_0 = \frac{K_2}{K_1}\frac{f_{CLK}}{\left(2+\frac{V_{ss}}{V_{cc}}+\frac{V_{cc}}{V_{ss}}\right)}. \quad (1)$$

Manuscript received December 22, 1980; revised March 20, 1981.

The author is with the Department of Electrical Sciences and Engineering, University of California, Los Angeles, CA 90024.

[1] V_{cc} and V_{ss} are defined with respect to the virtual ground of the first op amp which is assumed to be 0 V.

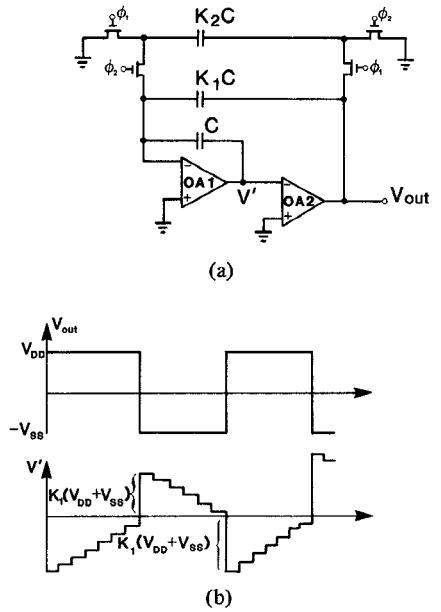

Fig. 1. (a) An SC stray insensitive relaxation oscillator. (b) Associated waveforms V_{out} and V'.

For $V_{ss} = V_{cc}$, the oscillating frequency is only dependent on the ratio of K_2 to K_1 which can be realized very accurately. Even when $V_{ss} \neq V_{cc}$, the dependence on the supply voltages is still small as long as the differences are small.

The major shortcoming of the circuit is due to that fact that V_{out} is being sampled at the end of ϕ_1 by the capacitor K_2C. This sampled charge is then integrated onto the capacitor C at the beginning of ϕ_2. Thus, the voltage V' will change only at the beginning of ϕ_2, and therefore each period can only be a multiple of the clock period. Initially it was felt that this meant that the oscillating frequency was restricted to an integer relationship with the clock frequency, although experimentally this was not found to be exactly true (see Section III).

If a 50 percent duty cycle is not important, then the circuit could be realized using inverters instead of op amps, saving some area on the IC. Replacing the second op amp only by an inverter has no effect on either the oscillating frequency or the duty cycle irrespective of its threshold voltage.

The oscillating frequency can be digitally programmed by connecting (or disconnecting) capacitors in parallel with K_2C, similarly to the technique used in [11].

In order to realize a voltage-controlled oscillator, a switched feed-in is added as shown in Fig. 2. The clock phasing on the feed in capacitor (K_0C) is such that for V_{out} positive, the input voltage (V_{in}) is integrated with a positive sign, and conversely V_{in} is integrated with a negative sign when V_{out} is negative. This causes the oscillating frequency to increase when V_{in} is larger than zero or decrease when V_{in} is less than zero according to the formula (valid for $K_0, K_2 \ll K_1$ and $V_{cc} = V_{ss}$)

$$f_0 = \left(\frac{K_2}{4K_1}\right)f_{CLK} + V_{in}\left(\frac{K_0}{4K_1V_{cc}}\right)f_{CLK}. \quad (2)$$

From (1) and (2), it can be seen that the assumption K_2, $K_0 \ll K_1$ is equivalent to $4f_0 \ll f_{CLK}$.

0018-9200/81/0800-0412$00.75

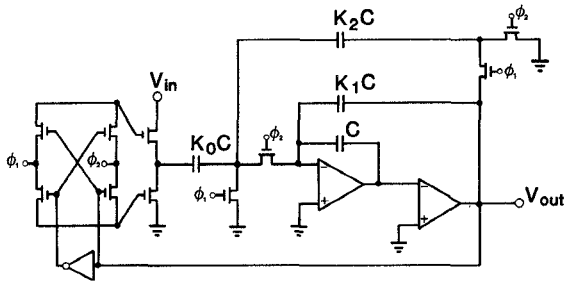

Fig. 2. A modified version of the oscillator of Fig. 1 to allow voltage-controlled operation.

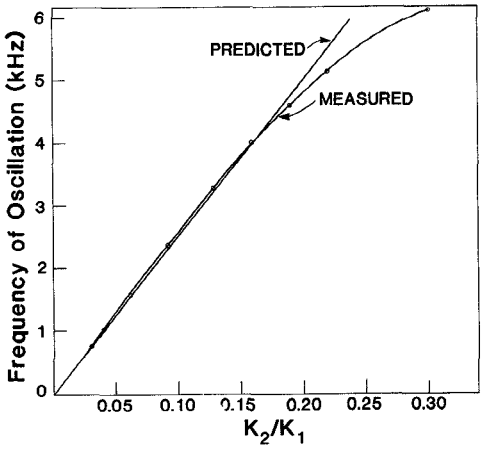

Fig. 3. Measured and predicted oscillating frequencies of the circuit of Fig. 1 for various ratios of K_2/K_1 when $K_1 = 0.359$ and $f_{CLK} = 100$ kHz.

Replacing the second op amp only by an inverter results in a VCO composed of one op amp, two inverters, four capacitors, and ten switches, which is easily integrated on a moderate-sized chip area.

III. Experimental Verification

The circuit of Fig. 1 was built using discrete components. An LF347 op amp was used for the first op amp, while the second op amp was replaced by a CMOS inverter. The switches used were CMOS 4016 transmission gates and ±5 V was used for the power supplies.

In Fig. 3 the oscillating frequency is plotted for various ratios of K_0/K_2. Also included in Fig. 3 is the predicted curve using (1). The clock frequency was 100 kHz, and K_1 was taken to be 0.359.

The agreement between the predicted curve and the measured curve is quite good for $K_2/K_1 < 0.16$. This corresponds to a clock frequency to oscillating frequency ratio of 25:1. The deviations between the curves for larger values of K_2/K_1 are probably due to the simplified analysis of the circuit based on the assumption of $K_2/K_1 \ll 1$ which is no longer true.

Next, the circuit was modified to realize the VCO of Fig. 2. The capacitor ratios used were $K_0 = K_2 = 0.0109$ and $K_1 = 0.359$. The measured oscillating frequency for various values of V_{in} is plotted in Fig. 4, along with the predicted values using (2).

The agreement between the predicted oscillating frequency and the measured frequency of the VCO is again quite good. (The clock frequency to center frequency ratio was 128:1.) The slight discrepancy between the two curves of Fig. 4 is possibly due to the inaccuracies of K_0 and K_2, estimated at 3–5 percent due to the stray capacitances of the discrete

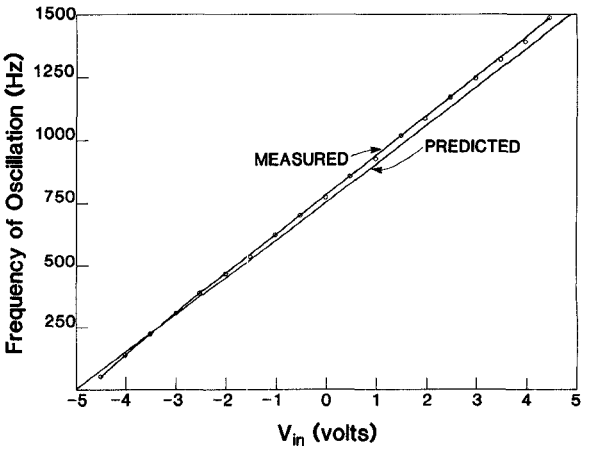

Fig. 4. Measured and predicted oscillating frequencies of the circuit of Fig. 2 as a function of V_{in} for $K_0 = K_2 = 0.0109$, $K_1 = 0.359$, and $f_{CLK} = 100$ kHz.

circuitry. This would correspond to a 3–5 pF inaccurary in the 100 pF capacitors K_0C and K_2C.

Even though individual periods of the oscillator were always observed to be composed of multiple clock periods, it was possible to get clock frequency to oscillating frequency ratios that were noninteger multiples when the oscillating frequency was averaged over a number of periods. (The frequency counter used a 1 s gate for all measurements.) Indeed, for the VCO of Fig. 2 with $K_0/K_1 = K_2/K_1 = 0.0304$, it was possible to control the oscillating frequency to a resolution better than 1 Hz by adjusting V_{in}.

Finally, it should be mentioned that the duty cycle was 47 percent for small values of K_2K_1 (i.e., less than 0.15). For larger values, the phase jitter caused the duty cycle to vary noticeably from one cycle to the next (although it was always less than one clock period). The reason for the 3 percent error has not been determined at the present time.

IV. Conclusions

A switched-capacitor oscillator has been described that is easily modified to be either voltage controlled or digitally programmed. Although the oscillator is probably practical only when its oscillating frequency is less than 1/25 the clock frequency (because of excess phase jitter at higher ratios), it is felt that it will be useful in a number of low frequency applications such as phase-lock loops, digitally programmed high-order filters, tracking filters, and low frequency modem transmitters.

References

[1] B. J. Hosticka, R. W. Brodersen, and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600–608, Dec. 1977.

[2][2] K. Martin, "Improved circuits for the realization of switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 237–244, Apr. 1980.

[3] G. M. Jacobs, D. J. Allstot, R. W. Brodersen, and P. R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 1014–1021, Dec. 1978.

[4] P. Fleischer and K. Laker, "A family of active switched-capacitor biquad building blocks," *Bell Syst. Tech. J.*, vol. 98, pp. 2235–2269, Dec. 1979.

[5] K. Martin and A. Sedra, "Exact design of switched-capacitor bandpass filters using coupled-biquad structures," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 469–475, June 1980.

[2]Reference [2] is a revised version of a Bell-Northern Research Internal Tech. Rep. TR1E81-78-06, "Switched-capacitor filters," Mar. 1978.

[6] M. S. Lee, "Parasitics-insensitive switched-capacitor ladder filters," *Electron Lett.*, vol. 16, pp. 472–473, June 1980.
[7] C. Hewes, W. Eversole, D. Mayer, T. Hui, R. Hester, and R. Pettengill, "A CCD/NMOS VOCODER," in *Proc. Int. Conf. Appl. CCD's*, San Diego, CA, Oct. 1978, pp. 3A.17–3A.24.
[8] B. White, G. Jacobs and G. Landburg, "A monolithic dual tone multifrequency receiver," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 991–997, Dec. 1979.
[9] K. Martin and A. Sedra, "Switched-capacitor building blocks for adaptive systems," *IEEE Trans. Circuits Syst.*, vol. CAS-28, June 1981.
[10] E. A. Vittoz, "Micropower switched-capacitor oscillator," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 622–624, June 1979.
[11] D. Allstot, R. Brodersen, and P. Gray, "An electrically-programmable switched capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 1034–1041, Dec. 1979.

Resistive-Gate-Induced Thermal Noise in IGFET's

K. K. THORNBER

Abstract—**The contribution to the noise in the drain current of an IGFET caused by thermal fluctuations in a resistive gate is calculated. It is found that such induced noise becomes important when the gate conductance becomes comparable to the device transconductance.**

I. Introduction

As is well known, the source-to-drain current in an IGFET is controlled by the gate voltage. If, rather than being constant, this voltage is a function of position, then the drain current is governed by this spatial dependence. Hence, thermally induced spatial voltage fluctuations in a resistive gate will induce fluctuations in the drain current, thereby enhancing the device noise.

Two illustrative examples are treated here. If the inducing fluctuations are longitudinal to the drain current, then for devices operated in saturation, the additional noise induced from the resistive gate becomes comparable to the intrinsic thermal noise of the device when the gate inductance drops to $g_m/18$, g_m being the device transconductance. If the inducing fluctuations are transverse to the drain current, the usual case, the induced noise becomes comparable to the intrinsic noise when the gate conductance reaches $g_m/6$. Thus, to avoid enhancing the noise of an IGFET device when using a resistive gate, care must be taken to keep the gate conductance higher than the device transconductance.

II. Longitudinal Fluctuations in Gate Voltage

In Fig. 1 we show an ordinary IGFET structure in which the resistive gate is held at voltage V_g^0 at both its source and drain ends. Thermal fluctuations in local voltages at position x in the gate δv_x induce fluctuations in gate voltage along the entire gate $\delta V_g(x) = V_g(x) - V_g^0$, which in turn induce fluctuations in the drain current $\delta I_d = I_d - I_d^0$. (As usual, the superscript zero designates noiseless values of the variables.) In what follows, we shall first determine δI_d as a function of $\delta V_g(x)$, then $\delta V_g(x)$ as a function of δv_x. The thermal statistics of δv_x will then determine those of δI_d [1]–[3].

In order to relate δI_d and $\delta V_g(x)$, we start with the relation between drain current and gate voltage for IGFET's in the gradual-channel approximation.

Manuscript received March 2, 1981; revised April 13, 1981.
The author is with Bell Laboratories, Murray Hill, NJ 07974.

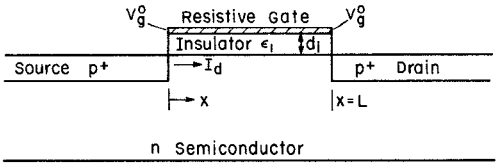

Fig. 1. A resistive-gate IGFET subject to longitudinal fluctuations in gate voltage. (Lateral view.)

$$I_d = \frac{\mu\epsilon_i w}{d_i}\left(V_g(x) - V_t - V(x)\right)\frac{dV(x)}{dx}. \tag{1}$$

Here μ is the carrier mobility, w is the channel width, ϵ_i is the insulator dielectric constant, d_i is the insulator thickness, and V_t is the threshold voltage. Defining fluctuations in the channel voltage as $\delta V(x) = V(x) - V^0(x)$, the (linear) noise can be written

$$\delta I_d = A(x)\frac{d\delta V(x)}{dx} + \frac{\mu\epsilon_i w}{d_i}\left(\delta V_g(x) - \delta V(x)\right)\frac{dV^0(x)}{dx} \tag{2}$$

where we define

$$A(x) = I_d^0/dV^0/dx = \frac{\mu\epsilon_i w}{d_i}\left(V_g^0(x) - V_t - V^0(x)\right) \tag{3}$$

and note that $\delta V_g(0) = \delta V_g(L) = 0$ owing to the short-circuit constraint on the gate voltage fluctuations. Solving (2) for $\delta V(x)$ and noting that since the source and drain voltage are fixed, $\delta V(0) = \delta V(L) = 0$, it follows that

$$\delta I_d = \frac{\mu\epsilon_i w}{d_i}\frac{1}{L}\int_0^L dx'\,\frac{dV^0(x')}{dx}\,\delta V_g(x'). \tag{4}$$

(Or one can simply integrate (2) on x; however, this latter trick is not always possible as, for example, when V_g^0 is a function of x.) Solving (1) for the noiseless $V^0(x)$ and inserting into (4), we obtain

$$\delta I_d = \frac{I_d^0}{V_g^0 - V_t}\int_0^L dx\,\delta V_g(x)(1 - x/\lambda)^{-1/2} \tag{5}$$

where $\lambda = \mu\epsilon_i w(V_g^0 - V_t)^2/2d_i I_d^0$. This expression is the desired relation between δI_d and $\delta V_g(x)$. (Note $\lambda \to L$, with $\lambda = L$ in saturation.)

It is straightforward to express the gate-voltage fluctuation $\delta V_g(x')$ at x' induced by a local spontaneous thermal fluctuation δv_x at x:

$$\delta V_g(x') = -\delta v_x(x'/L), \qquad 0 < x' < x \tag{6a}$$

$$\delta V_g(x') = +\delta v_x(L - x')/L, \qquad x < x' < L. \tag{6b}$$

Hence, inserting (6a), (6b) into (5), we find that

$$\delta I_d = I_d\frac{\delta v_x}{V_g - V_t}\left(\frac{\lambda}{L}\right)^2\left(2\frac{L}{\lambda}\left(1 - \frac{x}{\lambda}\right)^{1/2} - \frac{4}{3}\left(1 - \left(1 - \frac{L}{\lambda}\right)^{3/2}\right)\right) \tag{7}$$

for a fluctuation at x. Since the spontaneous thermal fluctuation δv_x is independent of x, it follows from integrating over the resistive gate that

$$\overline{\delta I_d^2} = \left(\frac{I_d}{V_g - V_t}\right)^2 F\left(\frac{\lambda}{L}\right)(4kTR_g\Delta f) \tag{8a}$$

$$F(z) = z^4\left(\frac{4}{z^2}\left(1 - \frac{1}{2z}\right) - \left(\frac{4}{3}\right)^2\left(1 - \left(1 - \frac{1}{z}\right)^{3/2}\right)^2\right) \tag{8b}$$

0018-9200/81/0800-0414$00.75