A Voltage-Controlled Capacitance Offset Calibration Technique for High Resolution Dynamic Comparator

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Abstract—**This paper presents a high resolution and wide range offset calibration technique for high resolution comparators. The proposed calibration technique significant reduces the calibration capacitance from conventional 2^n binary-scaled capacitors array to a small voltage-controlled capacitor. Furthermore, it utilizes inherent system clock to perform calibration and does not require extra clock phase. After proposed calibration, simulation result shows an offset of conventional dynamic comparators being reduced from 35mV to 350µV (one sigma) operating at 1GHz in 65nm CMOS technology with only 20µW power in calibration.**

Keywords-offset calibration, dynamic comparator

I. INTRODUCTION

Comparators are commonly used as building blocks of memory circuits and analog-to-digital converters (ADC). These systems usually require the comparators being low-offset, high-speed and low-power consumption. While high speed and low power operation are benefited from technology scaling, the reduction of feature size leads to a larger mismatch of transistors. For instance, the offset of Lewis-Gray dynamic comparator [1] in 65nm CMOS technology can be up to 35mV at 1 sigma. One common solution for suppressing the offset of the comparators is adding a pre-amplifier [2] but the pre-amplifier is suffered from static power dissipation and offset from itself which limit the performance of the comparator. Some analog technique [3] can cancel the offset of the pre-amplifier but the design complexity and die area will increase.

Instead of using pre-amplifier, a digital calibration technique was proposed in [4] which calibrates comparator offset through unbalancing the output loading of the comparator. When calibrating offset of n-bit resolution comparators, since the output capacitor array requires up to 2^n of MOS capacitor at each output the diffusion and parasitic capacitance of the 2^n binary-scaled MOS will affect the speed of the comparator and calibration accuracy as the resolution increases. Another offset calibration technique was purposed in [5] which calibrates offset through applying a reference voltage to an extra input pair of transistors in the comparator. Even though this can achieve large calibration range, the reference voltage has to be in the necessitated accuracy of calibrating resolution. Nevertheless, it does not relax the design complexity of analog circuits in high resolution.

In this paper, a new high resolution offset calibration technique is proposed which does not require an accurate reference voltage and it can calibrate a comparator offset to 350µV at 1 sigma. Furthermore, a voltage-controlled variable capacitor is employed in place of 2^n MOS capacitors array at the proposed calibration technique which significant reduces the total capacitance at high resolution calibration. Moreover, the concept of this offset calibration is to balance the regenerative current with capacitor load and achieve high resolution by small capacitance variation step which is defined from a coarse reference voltage step and the reference voltage is the only power consumption of the proposed calibration which is very low.

II. CALIBRATION SCHEME

The block diagram of the proposed offset calibration is illustrated in Fig. 1, which consists of a dynamic comparator, two voltage-controlled capacitors, an offset detector, an output flip sensor, two multiplexers (MUX) and a reference ladder. The basic concept of the proposed technique is to cancel the comparator offset through varying the capacitance at the outputs of the comparator. During calibration, common mode voltage V_{cm} is employed to both inputs of the calibrating comparator. As the outputs of the comparator preset to V_{dd}, one

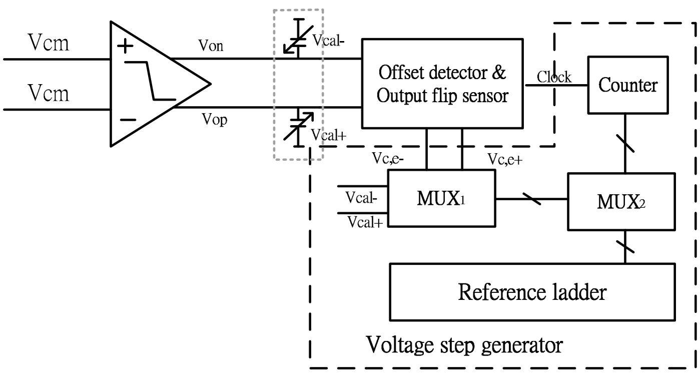

Figure 1. Simplified block diagram of calibration architecture.

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of the outputs will pull to ground when offset is presented. After the offset detection logic decides the offset polarity through the states of the comparator outputs, it starts the binary counter and determines which loading capacitor should be varied through the MUX1. Then, the counter controls MUX2 to choose a reference voltage from reference ladder for varying one of the loading capacitors of the comparator. While the loading capacitance keeps increasing, the offset is reduced. Once the comparator outputs exchange the flipped states, the flip sensor produces a signal to stop the calibration.

III. CIRCUIT IMPLEMENTATION

Fig. 2 shows a differential pair dynamic comparator [6] which is usually used in flash [7] and binary-search ADC [8] . This comparator has the advantage of high-speed, low-power and high-sensitivity. However, its offset usually is large due to small transistor sizing for small die area and low power dissipation. The operation of the comparator can be described as follows. When STROBE is at 0V, the current source transistor M11 is switched off, which means no current path from supply to ground. At the same time, M7-M8 and M9-M10 reset the internal nodes and the outputs of the comparator to V_{dd} in order to cancel the memory effect. When STROBE goes high, M11 is switched on and input transistors M1-M2 force currents through the back-to-back inverters M3-M5 and M4-M6. As the magnitudes of current I_{d1} and I_{d2} depending on the input signal, when STROBE is at 1V, the output of regenerative inverter in series with the stronger input transistor will pull from V_{dd} to ground.

The offset of this comparator is mainly generated from the mismatch between M1 and M2 [9] because they control the current to the regenerative inverters. The following equation [4] indicates how M1 and M2 affect the offset of the comparator.

$$\Delta V_{offset} = \frac{I_{M1}}{gm_{M1}} \cdot \frac{\Delta W}{W} \tag{1}$$

where ΔV_{offset} denotes the change of the offset voltage, gm_{M1} is the trans-conductance of the input transistor M1 and I_{M1} is the average drain current of transistor M1. ΔW is the difference of width of M1 and M2, and W is the summation of width of M1 and M2. According to Eq. (1), it is clear that the offset is proportional to the transistor mismatch of M1 and M2 in the comparator.

While the inputs of the comparator are applied V_{cm} during calibration, I_{d1} and I_{d2} should be equal and differential output of the comparator should appear to be meta-stable. However an unbalance always emerges even if a little mismatch between the differential branches and one of the output branches will be pulled to ground while other kept in V_{dd} consequently. This unbalance can be diminished with adjusted capacitor loading at the output of the comparator according to the following equation [4] .

$$\Delta V_{od} = \frac{I_{M1}}{gm_{M1}} \cdot \frac{\Delta C}{C} \tag{2}$$

where ΔV_{od} represent the change of the offset voltage, gm_{M1} is the trans-conductance of the input transistor M1 and I_{M1} is the average drain current of transistor M1. ΔC is C1-C2 at the comparator load and C is $C1+C2$. As ΔV_{od} is change proportionally with ΔC, the minimum offset step and the maximum offset range which can be calibrated is relied on the value ΔC.

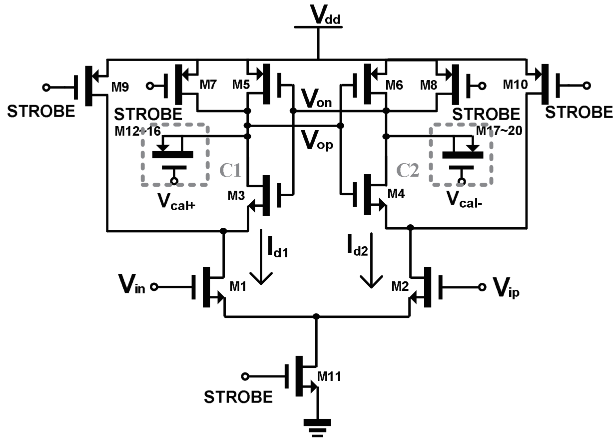

Figure 2. Circuit schematic of differential pair comparator.

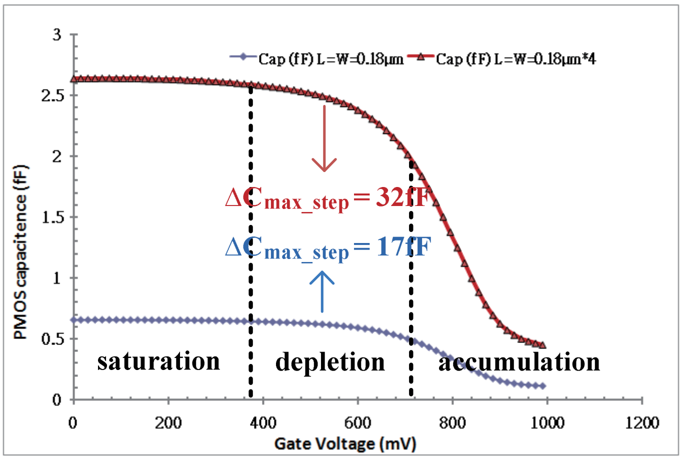

Figure 3. Characteristic curve of PMOS capacitance versus gate voltage, while W=L=0.18μm and W=L=0.18*4μm

The voltage-controlled capacitor is implemented with PMOS transistor which is transistors M12-M20 as shown in Fig. 2. The characteristic curve of PMOS capacitance versus the gate voltage is depicted in Fig. 3. The PMOS capacitor can be separated in three regions of operation regard of the gate voltage of the transistor. When gate voltage is V_{dd}, the PMOS capacitor is in accumulation region which means the transistor is totally turned off. As gate voltage is less than V_{dd} but still larger than the threshold voltage of the transistor, it is in depletion region. Finally, when the gate voltage is low enough to turn on the transistor, it operates in saturation region. As demonstrated in Fig. 3, the variation of the capacitance against gate voltage is not a constant in each region. Since the proposed calibration used all of three regions in order to maximize the calibration range, the smallest variable step of capacitance has to be designed being able to calibrate the required smallest step of offset.

The characteristic curve of the loading PMOS device that is four times larger than default design is also illustrated in Fig. 3. The curve shows that while the loading capacitance increase, the capacitance variation also becomes larger in same controlled voltage step. Therefore, the voltage step generator has to produce a smaller voltage step in order to keep the calibrated offset resolution. A comparison of variation capacitance with difference transistor size loading in fixed gate-source voltage step is demonstrated in Fig. 3. The maximum variation of capacitance is 0.017fF with 15mV gate voltage per step, where the width and length of the PMOS is equal to 0.18μm. And the maximum variation of capacitance is 0.032fF while the PMOS is four times larger.

As mention before, the reference voltage for the voltage-controlled capacitors are generated from a coarse reference ladder. As long as the reference voltage is monotonic, the accuracy of the reference ladder is not important. Hence, a reference ladder in thermometer style is chosen which generates sequence step voltage through a series of resistance voltage divider from supply to ground. These reference voltages will sequentially be selected from an n-to-one multiplexer which controlled by a binary D flip-flop counter, where n is the number of reference voltage. The circuit implementation of 2-bit example is illustrated in Fig. 4. The multiplexers in front of the voltage-controlled capacitor and the CLK signal for the counter are controlled by the $V_{c,e\pm}$ signals which are determined by the offset polarity from the offset detector.

Signal behavior of the differential pair comparator with calibration is plotted in Fig. 5, which shows a calibration operation when a positive offset existing at the comparator. As the calibration start, V_{in} and V_{ip} are connected to V_{cm} and V_{cal+} and V_{cal-} are employed to V_{dd} initially. Since the voltage variable capacitor is PMOS device, when the gate voltage is V_{dd}, the transistor is switched off, which indicates there is no capacitance at the output of the comparator except the extra diffusion capacitance of the PMOS and parasitic. Because of the positive offset could seem as a positive DC voltage adding to V_{cm} at the positive input V_{ip} of the comparator, the negative output V_{on} of the comparator is pull to ground. Through increasing the capacitance at this output node by decreasing the reference voltage V_{cal-}, the voltage level of V_{on} changes from ground to supply which implies the offset is calibrated within the resolution of the comparator.

Since the calibration scheme requires an active comparator output to trigger the counter, meta-stability may lead the calibration stop functioning. Nevertheless, if the comparator reaches meta-stable condition which means the offset already being calibrated to less than the resolution of the comparator and the calibration is done.

IV. SIMULATION RESULTS

The performance of the proposed offset calibration was verified with simulation using a standard 65nm CMOS process. Except the differential pair comparator, another widely used Lewis-Gray comparator also being introduced for verification which is shown in Fig. 6. The sizing of both comparators is listed in table I. The proposed offset calibration is performed in 1GHz with 15mV per variation step from reference ladder and 1V supply. Twenty times Monte-Carlo

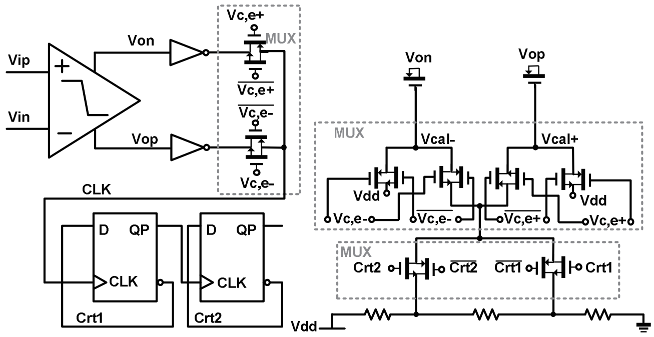

Figure 4. Circuit implementation of 2-bit reference ladder with counter.

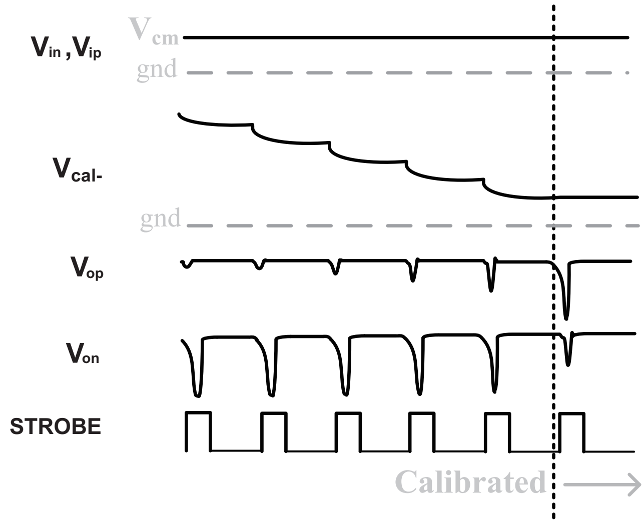

Figure 5. Signal behavior of diff pair comparator under calibration.

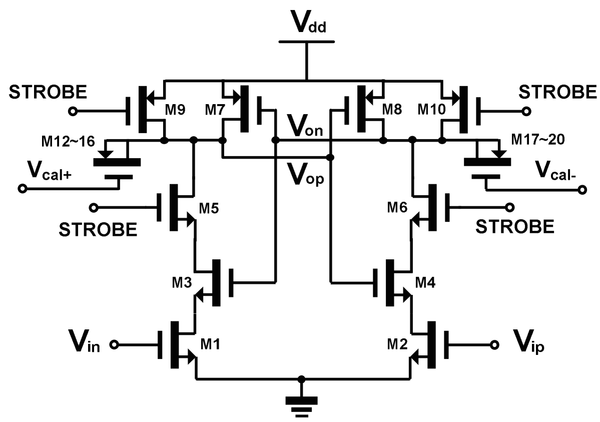

Figure 6. Schematic of Lewis-Gray comparator.

with random process and mismatch simulation has been done with both comparators.

The offset of Lewis-Gray comparator before calibration and after calibration is demonstrated in Fig 7. While the maximum offset before calibration is 35mV, 300μV is obtained after calibration. It can be noticed that the calibrated offset will have opposite polarity of the original offset which is because the calibration stops when the comparator output flipped to inverse state. The maximum offset of differential pair comparator before calibration is up to -25mV and after calibration it compressed to 350μV which is illustrated in Fig. 8. Since all the digital logic circuits of calibration do not have switching in the ADC conversion, the total calibration power is 20μW which is only come from the coarse reference ladder.

TABLE I. TRANSISTOR DIMENSION

	Lewis-Gary		Diff pair	
Transistor	**W (μm)**	**L (μm)**	**W (μm)**	**L (μm)**
M1	**1.0**	**0.06**	**3.0**	**0.06**
M2	**1.0**	**0.06**	**3.0**	**0.06**
M3	**1.0**	**0.06**	**3.0**	**0.06**
M4	**1.0**	**0.06**	**3.0**	**0.06**
M5	**1.0**	**0.06**	**0.5**	**0.06**
M6	**1.0**	**0.06**	**0.5**	**0.06**
M7	**0.5**	**0.06**	**0.135**	**0.06**
M8	**0.5**	**0.06**	**0.135**	**0.06**
M9	**0.135**	**0.06**	**0.135**	**0.06**
M10	**0.135**	**0.06**	**0.135**	**0.06**
M11	**N/A**	**0.06**	**3.0**	**0.06**
M12~M16	**0.18**	**0.18**	**0.18**	**0.18**
M17~M20	**0.18**	**0.18**	**0.18**	**0.18**

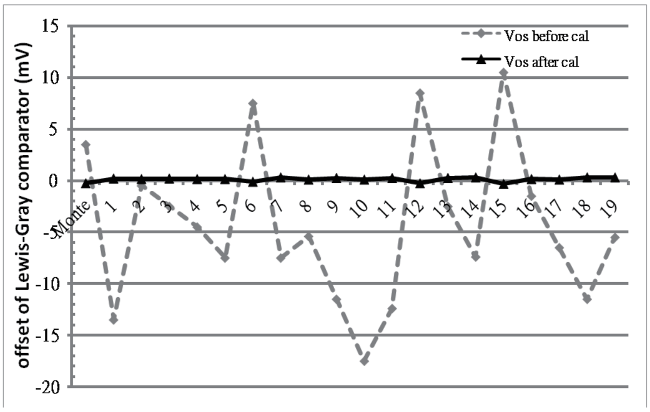

Figure 7. Offset of Lewis-Gray comparator before and after calibration.

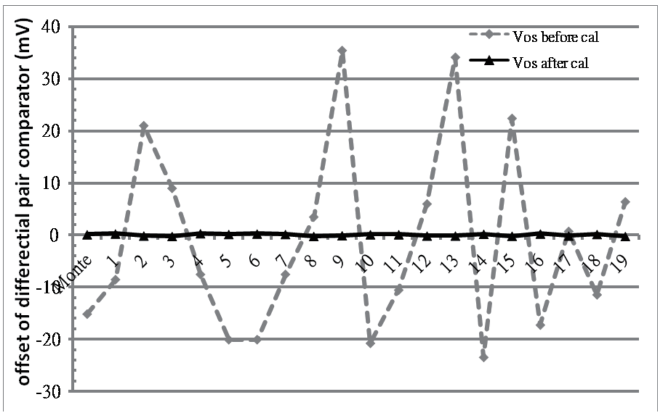

Figure 8. Offset of diff pair comparator before and after calibration.

V. CONCULSION

A new offset calibration technique is proposed, and it can apply to popular types of dynamic comparators. Simulation result shows the offsets of Lewis-Gray comparator and differential pair comparator after calibration decrease almost 99% with low power consumption. As the technology scaling down, the power consumption of the one stage dynamic comparator will decrease and the speed will increase but the transistor mismatch will become large. The proposed calibration technique can calibrate offset in high resolution against the process variation.

ACKNOWLEDGMENT

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