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Low-cost, high-precision measurement system for capacitive sensors

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Abstract. This paper describes a low-cost realization of a precision capacitance measurement instrument. The method is based on synchronous modulation and demodulation operating at a frequency of 100 kHz. A two-channel multiplying digital-to-analogue converter is used to generate a sinusoidal drive voltage and to perform multiplication with the demodulation signal. The modulation and demodulation signals are generated using a direct digital synthesizer, which is implemented using a field programmable gate array. Experimental results show a reproducibility of better than $\pm 0.005\%$ in the range from 50 pF to 600 pF.

1. Introduction

In electronic measurement systems, capacitive polymer thin film humidity sensors are often the most suitable devices for the measurement of the relative humidity (RH) of ambient air and such humidity sensors are thus gaining significance in several applications. The specified capacitance of commercially available humidity sensors ranges from 50 pF to 600 pF. Consequently, the sensitivity of these sensors varies from 0.3 up to 2 pF per % RH.

The main sensory effect is the variation in permittivity caused by sorption of water in the humidity-sensitive polymer film. This results in a variation of the capacitance of the sensor as a function of the relative humidity of the surroundings. An inherent undesirable effect is, however, the change of the resistance of the sensor. Thus, the dielectric loss increases with increasing humidity which results in a high dissipation factor. For precise measurements the sensor must be considered as a lossy capacitor with an impedance instead of a pure capacitance, whereby only the imaginary part of this impedance corresponds to the relative humidity. The requirements for the read-out circuit are fulfilled using a real measurement of the sensor impedance, carried out at a constant frequency of 100 kHz and with no DC voltage over the sensor.

Various types of capacitance measurements have been reported in the literature to fulfil the requirements of different applications. The method which uses a capacitor as a frequency-dependent element in a multivibrator circuit [1–3] is problematic in humidity sensors due to the non constant measurement frequency and neglect of the fact that the sensor is not a pure capacitor but an impedance.

Switched capacitor techniques [4, 5] are more suitable for integrated circuit design because of their complex structure. Problems arising with the need for reference capacitors are also evident in the charge amplifier technique proposed in [6]. In contrast to the former methods, bridge-based techniques are able to yield a real impedance determination. The accuracy of these methods depends on the reliability of the reference components and the accuracy of the operator's handling. Automatic balancing of the bridge [7–9] ultimately results in a more complicated circuit structure.

The synchronous modulation and demodulation method is another promising technique which accomplishes the demands for the identification of a complex vector (impedance). A constant excitation voltage source and phase stability of the reference and sensor signals must be ensured. Some approaches to this end have been undertaken [10, 11], also with stray capacitance elimination [12, 13]. However, synchronous demodulation is most commonly done using simplified multiplication with a square wave signal, which is sensitive to all Fourier components of the reference signal.

This paper describes a low-cost system based on this synchronous demodulation technique with both sinusoidal drive and reference signals operating at a constant frequency of 100 kHz. The required multiplication is implemented using a multiplying digital-to-analogue converter (MDAC). This mixed analogue/digital realization

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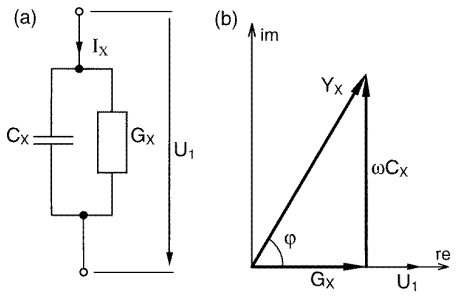

Figure 1. (a) Equivalent circuit of a real capacitive sensor with (b) complex representation of the sensor admittance.

eliminates essential error sources due to processing with analogue multipliers and avoids the costs of fast analogue-to-digital converters (ADCs). The latter are necessary for digital demodulation methods. We equipped our system with an additional autocalibration feature which eliminates phase and gain errors and additionally puts down the absolute accuracy to the precision of one reference resistor and the frequency stability of the quartz oscillator. Moreover, an offset compensation technique suppresses all DC offset errors in the system.

2. Theory of operation

A capacitive sensor can easily be modelled (figure 1(a)) as an admittance with an electric equivalent of an ideal capacitance in parallel with a resistance (loss conductance). The dissipation factor D describes the relationship between the capacitance and the parallel resistance in a real capacitor:

$$D = \frac{1}{\omega C_X R_X}. \tag{1}$$

The principle of measurement is based on the fact that the current through an unknown capacitance (impedance), which is fed by a sinusoidal voltage, shows characteristic magnitude and phase shifts. The phase shift between the excitation voltage and the measured current depends on the in-phase (conductance) and quadrature (susceptance) component of this sensor admittance (figure 1(b)). Knowing the frequency, the capacitance can be calculated from the susceptance. The method used for verification of the unknown sensor admittance is based on a synchronous demodulation technique [14].

Figure 2 shows a block diagram of the capacitance measurement system. The measurement system consists of a digital and an analogue signal domain. The basic element of the circuit is a two-channel MDAC (DAC7801, Burr Brown). This integrated circuit is used on the one hand to convert the digitally generated sinusoidal signal to an analogue excitation voltage (MDAC A) and serves on the other hand as real multiplication for the demodulation (MDAC B). The significant advantage to a solely analogue realization is the fact that no analogue reference signal is needed. The problems concerning the amplitude and phase shift stability of this reference signal are shifted into the digital domain and thus become easy to stabilize.

The digital frequency generator is a key element in the digital domain. The requirements for this circuit comprise the generation of a sinusoidal signal for driving the sensor and the availability of a phase shifted sinusoidal reference signal of the same frequency to perform the demodulation. This function is best achieved by means of a direct digital synthesizer DDS [15]. The frequency-stabilized and amplitude-controlled output signal of the MDAC A of the form

$$\boldsymbol{U}_1 = U_{REF} \cdot \sin \omega t \tag{2}$$

is applied to the unknown sensor admittance which can be expressed as

$$\boldsymbol{Y}_X = G_X + \mathrm{j}\omega C_X. \tag{3}$$

The current through it is sensed by a current to voltage converter with a transimpedance R_T, the corresponding output voltage U_X is used as a reference voltage for the second MDAC which performs the demodulation. To obtain the imaginary part of Y_X the signal must be multiplied by the quadrature reference signal $\cos \omega t$. After low-pass filtering the voltage $\boldsymbol{U}_{QUAD}$ is found to be

$$\boldsymbol{U}_{QUAD} = \tfrac{1}{2} U_{REF} R_T \omega C_X. \tag{4}$$

This output DC voltage is directly proportional to the unknown capacitance C_X.

In the same manner the real part of the admittance $\boldsymbol{Y}_X$ can be obtained by multiplying the voltage U_X by the inphase reference signal $\sin \omega t$

$$\boldsymbol{U}_{INPHASE} = \tfrac{1}{2} U_{REF} R_T \frac{1}{R_X}. \tag{5}$$

In this particular case the output DC voltage is directly proportional to the unknown loss conductance.

The practical realization of this synchronous demodulation comprises a multiplier (MDAC B) with the opportunity to feed in either an in-phase or a quadrature reference signal (i.e. a sine or cosine component).

With certain assumptions of ideal circuit behaviour, the unknown capacitance can be calculated using equation (4), knowing the frequency, the reference voltage, the feedback resistance and the transfer characteristic of the transimpedance amplifier.

3. Error analysis and circuit details

Considering the proposed configuration, the main error sources can be classified as follows:

- offset errors and any change of DC levels in the system;
- gain errors and errors due to any change of the transfer characteristic of the system (proportionality errors);
- errors due to finite phase resolution of the digitally generated reference signal;
- errors due to demodulation of superharmonics.

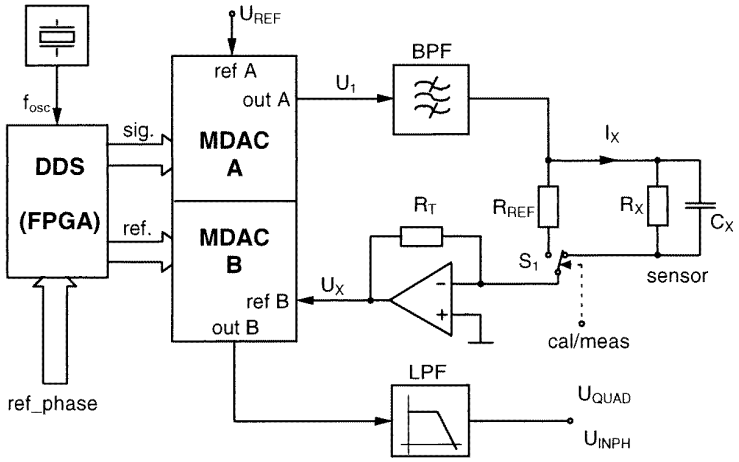

Figure 2. Schematic diagram of the synchronous demodulation technique for capacitance measurements.

To avoid and limit the influence of these errors a number of features were introduced to improve the entire performance of the system. To separate the different error sources equations (4) and (5) can be generally rewritten as:

$$\boldsymbol{U}_{QUAD} = \tfrac{1}{2}U_{REF}(t,\vartheta)R_T(t,\vartheta)G(t,\vartheta)\omega(t,\vartheta)C_X + U_{OFF}(t,\vartheta) = K(t,\vartheta)\omega(t,\vartheta)C_X + U_{OFF}(t,\vartheta) \quad (6)$$

$$\boldsymbol{U}_{INPHASE} = \tfrac{1}{2}U_{REF}(t,\vartheta)R_T(t,\vartheta)G(t,\vartheta)\frac{1}{R_X} + U_{OFF}(t,\vartheta) = K(t,\vartheta)\frac{1}{R_X} + U_{OFF}(t,\vartheta). \quad (7)$$

In these equations G represents the transfer characteristic of the transimpedance amplifier circuit and the used bandpass filter. The possible parameter changes are indicated by their dependence on t(= time, ageing of components) and temperature ϑ.

3.1. Offset errors and compensation

Let us first of all identify the sources of offset errors which cause these unwanted effects. In our application generation of the sinusoidal signal is inherently associated with a DC offset. We use an optimized sine ROM with a 10-bit data range. However, the applied DAC7801 covers an output range of 12-bit. To maximize the output voltage we set the two least significant bits (LSBs) to zero, thus the limits of the output voltage are defined as

$$U_{MAX} = +U_{REF}\frac{2044}{2048} \qquad U_{MIN} = -U_{REF}\frac{2048}{2048}.$$

Hence, the output has a constant DC offset. In fact, considering the drive voltage of the sensor this DC offset is eliminated by the inserted bandpass filter (BPF). However, each DC offset, which is added to the detected current signal (e.g. op-amp offset voltage) is directly fed to the multiplier input. In this case the DC offset of the generated reference signal is relevant, because the multiplication of two DC components results again in a DC signal which cannot be distinguished from the original sensor signal. Another source of error is the DC offset added by the final low-pass filter (LPF). To overcome these undesirable effects, an additional signal processing procedure is employed. Considering the measurements of the capacitance and the use of a quadrature reference signal, demodulation is not only carried out with the components $\sin(\omega t)$ and $\cos(\omega t)$, but also with the components $-\sin(\omega t)$ and $-\cos(\omega t)$. If the sensor signal is additionally multiplied by a reference signal which is inverted, that is to say phase shifted by 180°, only the sign of the output signal in equation (4) changes, whereby the DC offset remains constant. This may be expressed as:

$$\boldsymbol{U}_{QUAD1} = K(t,\vartheta)\omega(t,\vartheta)C_X + U_{OFF}(t,\vartheta) \quad (8)$$

$$\boldsymbol{U}_{QUAD2} = -K(t,\vartheta)\omega(t,\vartheta)C_X + U_{OFF}(t,\vartheta). \quad (9)$$

With the assumptions that the available offsets and the sensor signal change very slowly, the two measurements can be carried out consecutively. The offset can be cancelled by subtraction of the obtained data from equations (8) and (9) and division by two

$$\boldsymbol{U}_{QUAD} = \left|\frac{\boldsymbol{U}_{QUAD1} - \boldsymbol{U}_{QUAD2}}{2}\right| = K(t,\vartheta)\cdot\omega(t,\vartheta)\cdot C_X. \quad (10)$$

The proposed procedure can easily be implemented in the design of the DDS.

The DC offset and its variations due to temperature behaviour and ageing of components can be eliminated by incorporating the described procedure in an automatic measurement control.

3.2. Gain errors and autocalibration arrangement

Unfortunately, in practice the absolute accuracy and drift of the reference voltage source causes errors. Furthermore, the operational amplifiers' finite gain and frequency dependence at 100 kHz contributes to the non ideal behaviour of the circuit. As a consequence of these errors the measured phase shift given with an ideal capacitance would not be 90° and the resulting amplitude is falsified by gain errors in the signal path. Therefore, calculation of capacitance using equation (4) is not accurate.

To overcome these problems, an option to calibrate the system was introduced. As part of the system a high-stability reference resistor R_{REF} (see figure 2) was added. This resistor can be switched in automatically via a relay S1 (or a FET switch), to replace the capacitor which is being measured. The insertion of this reference resistor and the simultaneous multiplication with the in-phase component fulfils two essential requirements. Under the assumption of an ideal resistance the phase shift of the reference signal can be set by maximizing the amplitude of the output voltage $\boldsymbol{U}_{INPHASE}$. The obtained phase shift represents the unknown phase shift of the signal path and can be used afterwards to correct the reference signal phase shift during capacitance measurements. Furthermore the proportionally factor $K(t, \vartheta)$ in equation (6) can be determined. With autocalibration $R_X = R_{REF}$ we can calculate

$$K(t, \vartheta) = \boldsymbol{U}_{INPHASE} \cdot R_{REF}(t, \vartheta). \tag{11}$$

Inserting this proportionally factor $K(t, \vartheta)$ in equation (6), the unknown capacitance is found to be

$$C_X = \frac{\boldsymbol{U}_{QUAD}}{\boldsymbol{U}_{INPHASE} R_{REF}(t, \vartheta)\omega(t, \vartheta)}. \tag{12}$$

By regular repetition of these steps in combination with the offset compensation any drifts of the transfer characteristics and the reference voltage of the system can be cancelled. Thus, the absolute accuracy of the system depends on the accuracy and stability of the reference resistor and the frequency of the modulation signal, which is derived from a quartz oscillator.

3.3. Sinusoidal signal generation and error estimation

A DDS is used to generate the signals required for excitation and demodulation. A field programmable gate array (FPGA) was employed to implement the digital portions of this circuit [16]. This DDS comprises a phase accumulator and a sine ROM. This sine ROM is an optimized gate implementation with minimized hardware requirements. In this application a ROM with 5-bit address and 10-bit data bus width was employed. With an oscillator frequency of 16 MHz and a duration of 15 clock cycles for updating the MDAC, the accumulator frequency and also the resulting sampling frequency is 1.066 MHz.

A further requirement on the signal generator is the possibility of changing the phase shift of the reference signals. To achieve a phase shift of 90° (e.g. for autocalibration purposes) the address bit (MSB-1) must be inverted. This feature is easy to implement and ensures an exact and stable phase shift of 90°. The phase is represented by a 5-bit word, consequently the phase can be altered in steps of $360°/2^5 = 11.25°$. This increment is too large for a satisfactory compensation of the phase shift due to the analogue electronics. For this reason an additional accumulator was used, which adds a deterministic jitter to the phase. The time average of the resulting phase corresponds to the desired phase. This results in a phase resolution $\Delta\phi = 360°/2^{11} = 0.1797°$. The digital portion of the frequency synthesizer is shown in figure 3.

Due to this finite phase adjustment of the reference signal, we can derive equation (13) to determine the error ε_{QUAD} by calculation of the difference between the multiplication with an ideal reference signal and multiplication with a reference signal which has a deviation of $\Delta\phi/2$:

$$\varepsilon_{QUAD} = \sin\phi\left(1 - \cos\frac{\Delta\phi}{2}\right) + \cos\phi \sin\frac{\Delta\phi}{2}. \tag{13}$$

For an ideal capacitor this error is 0.000 12%. For a capacitor with a dissipation factor of $D = 0.07$ (worst case for humidity sensors) the maximum error is 0.01%.

A further error source which is evident using the proposed measurement technique is the influence of superharmonics in both the excitation and reference signal. In this case the problem occurs because demodulation of these spurious spectral lines again results in a DC signal which is added to the actual sensor signal. Thorough theoretical analyses of these superharmonic effects in DDSs are given in the literature [15, 17] where it was shown that careful selection of clock frequencies and signal frequencies are of utmost importance for minimizing these superharmonic effects.

Instead of this error estimation with a numerical analysis, we have made a more practical approach. Figure 4 shows the measured magnitude voltage spectrum of the generated sinusoidal signal at the output of MDAC A. From this spectral performance it can be observed that the spectral line of the third superharmonic is attenuated at 36 dB. A further spectral line at 966 kHz is attenuated at 20 dB. This signal is fed directly to a bandpass filter which performs a further reduction of these superharmonics. The attenuation of the third harmonic is increased to 42 dB. The discrete line at 966 kHz gives an attenuation of more than 60 dB. With the assumption of the same spectral performance of the reference signal we can expect a maximum error signal with an attenuation of approximately 42 dB (sig.) + 36 dB (ref.) = 78 dB (at 300 kHz). Therefore the maximum error of the DC output signal can be determined with an error of 0.0126%. Furthermore it should be noted that the generation of a phase resolution for the 11-bit reference signal introduces additional phase noise. This realization acts like a noise shaper [15], which again results in a reduction of the discrete spectral lines. Thus the influence of discrete spectral line demodulation is further reduced.

4. Experimental results

The instrument was tested under laboratory conditions using the following configuration. A Macintosh II serves as a central unit to control the circuit and to perform data monitoring and recording. A digital input/output card is used to set the phase shift (ref./phase) of the reference signal and gives the signal (cal./meas.) for carrying out the switching of the relay (S1) for autocalibration purposes. The DC voltage is measured using a HP3458A Multimeter connected via a GPIB to the host computer. In addition, a second HP3458A Multimeter is used to measure the ambient temperature via a thermistor probe.

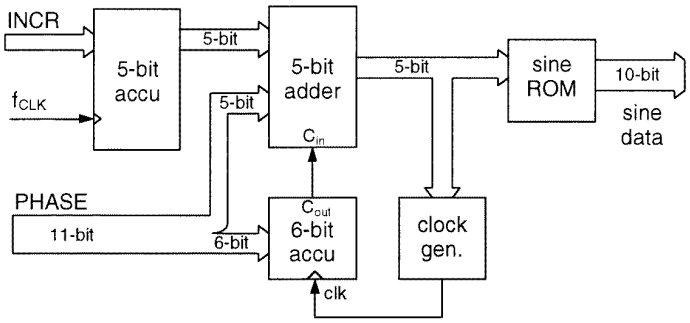

Figure 3. DDS architecture of the signal generator implemented in a FPGA.

Table 1. Capacitance data obtained with the new instrument at 100 kHz, C_{100}, are compared with nominal values, C_N, of the test capacitors and with a reference measurement performed with an LCR meter at 1 kHz, C_1.

Nominal value C_N (pF)	$C_1 \pm$ accuracy (pF)	C_{100} (pF)	Difference $C_{100} - C_N$ (pF)	Difference $C_{100} - C_1$ (pF)
47 ± 1.2	50.1 ± 0.4	49.79	+ 2.79	− 0.31
69 ± 1.7	71.8 ± 0.44	71.49	+ 2.49	− 0.31
150 ± 3.8	153.8 ± 0.6	153.62	+ 3.62	− 0.18
270 ± 6.8	278.7 ± 1.75	278.00	+ 8.00	+ 0.7
330 ± 8.25	335.7 ± 1.87	336.05	+ 6.05	+ 0.35
383 ± 9.6	386.7 ± 1.97	387.17	+ 7.17	+ 0.47
470 ± 11.8	470.7 ± 2.14	471.66	+ 1.66	+ 0.66
470 ± 11.8	470.7 ± 2.14	471.43	+ 1.43	+ 0.43
470 ± 11.8	478.7 ± 2.15	479.32	+ 9.32	+ 0.62
620 ± 15.5	632.7 ± 2.46	634.18	+ 14.18	+ 1.48

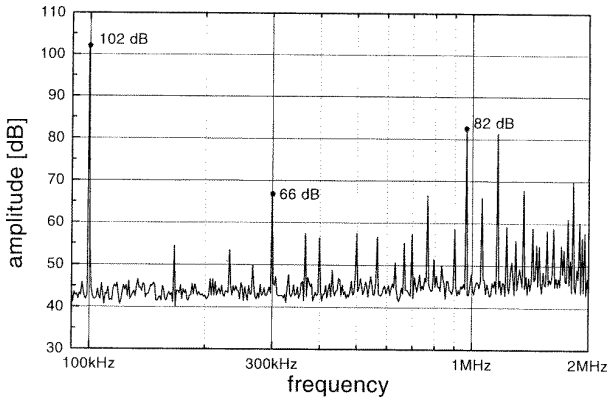

Figure 4. Measured voltage magnitude output spectrum of the direct digital synthesizer (DDS).

4.1. Linearity tests

Reference capacitors (Siemens, Styroflex KS, ±2.5%) were used to evaluate the linearity of the set-up in the required measurement range of 50 pF up to about 600 pF. The exact values of the capacitors were determined using an LCR meter HP4261A operating at a measurement frequency of 1 kHz. The results are summarized in table 1.

The commercial LCR meter is specified for an absolute accuracy which is not constant. It essentially depends on the measurement range being used. The maximum errors can also be deduced from table 1. Furthermore the stray capacitance of the measurement set-up for both the LCR meter and our circuit is already corrected in the results shown in table 1. The results obtained with our instrument are, in the whole range, within the accuracy of the LCR meter. Consequently we can specify that our system accuracy and linearity are better than 0.8%. These were not very promising results. We thus made further efforts to improve the method and found that, for our system linearity, it was irrelevant whether we measure the capacitance or the resistance. The only difference between them is the multiplication with a reference signal which is phase shifted by 90°. We know that our phase shift generated in the digital domain is precise and constant. Consequently, we carried out reference resistor measurements to characterize our system. With the known constant frequency it is easy to calculate the capacitance from the magnitude of the equivalent conductance. For this particular purpose we used precision resistors (VISHAY, ±0.1%). From the results summarized in table 2 it can be seen that the errors of our instrument are, over the whole measurement range, within the guaranteed resistance accuracy of 0.1%.

4.2. Stability tests and resolution

We took measurements over a period of several hours in order to evaluate the stability and reproducibility. Our test capacitor (Siemens, Styroflex KS, ±1%) was specified with a temperature coefficient of −(60–180) ppm $^{\circ}C^{-1}$. We carried out the measurements over 16 h at time steps of 5 min. The results can be seen from figure 5. The bold curve is the capacitance obtained with our instrument. The

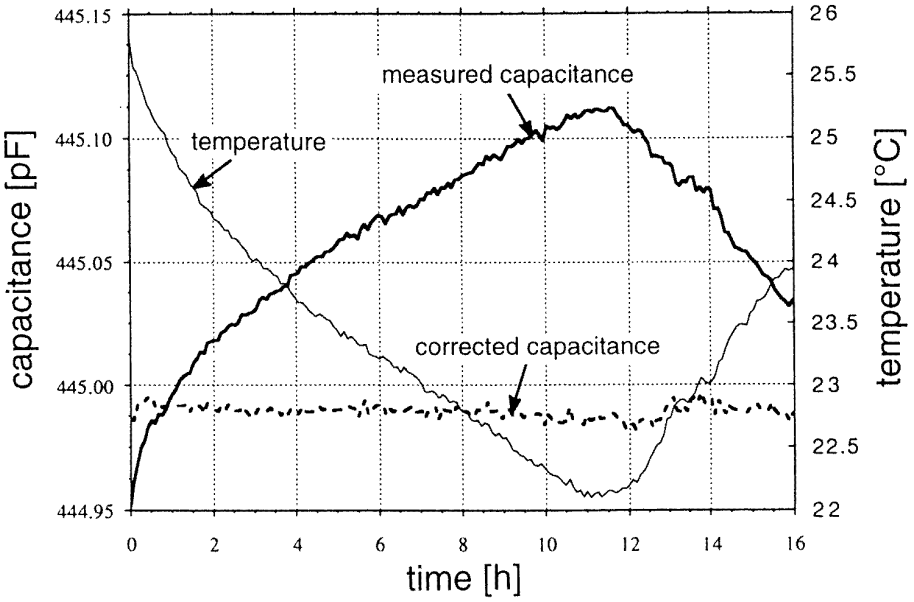

Figure 5. Capacitance of a standard capacitor (Siemens, Styroflex KS, ±1%) as function of time in comparison to the ambient temperature.

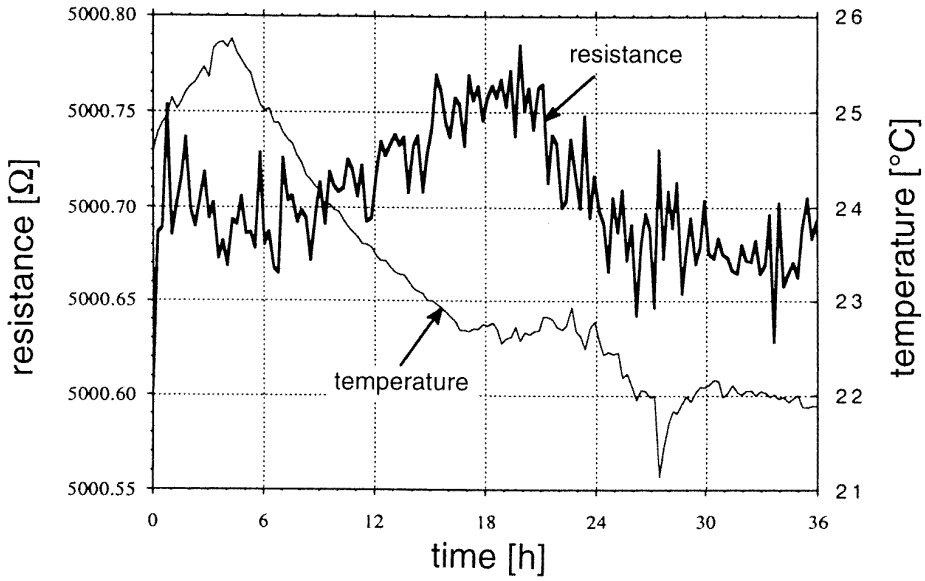

Figure 6. Results of measurements with a precision reference resistor (VISHAY, ±0.1%) as a function of time in comparison to the ambient temperature.

measured capacitance has a distinct correlation with the measured ambient temperature over the measurement time. Assuming that the measured deviation is only due to the temperature characteristic of the sample capacitor we can calculate a corrected capacitance which is represented by the broken curve. Considering these aspects, the calculated temperature coefficient amounts to -0.0432 pF $^{\circ}C^{-1}$ or -97 ppm $^{\circ}C^{-1}$, which is within the specified range. The fluctuation of the corrected capacitance over 16 h is within 0.02 pF (= 0.0045%). The mean value at 25 °C is found to be 499.99 pF with a standard deviation of 2.5 fF. It could be possible that the temperature behaviour is not solely due to the capacitor. Therefore we made the same measurement whereby the capacitor was replaced by a precision reference resistor (VISHAY, ±0.1%; temperature coefficient, <2.5 ppm $^{\circ}C^{-1}$). The deviation of the measured resistance changes over 16 h is presented in figure 6. The results indicate a maximum fluctuation within this time of 0.2 Ω(= 0.004%). The mean value is 5000.7 Ω. The measured maximum change of 40 ppm over 16 h agrees well with the corrected results of the sample capacitor.

To characterize the instrument for practical applications with capacitive humidity sensors, we cannot assume ideal

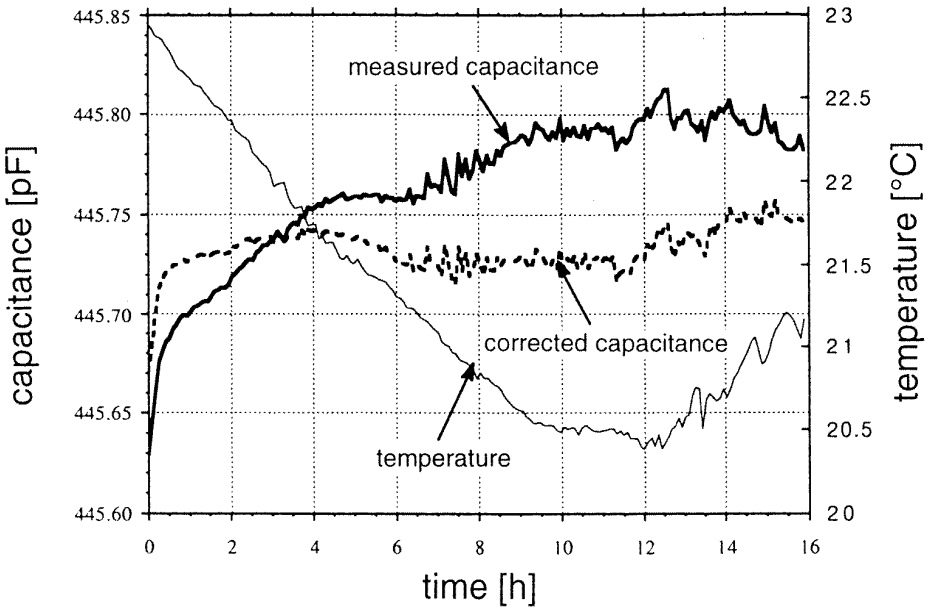

Figure 7. Capacitance of a simulated humidity sensor with dissipation factor of 0.07 as a function of time.

Table 2. Nominal value of reference resistors R_N in comparison with the data obtained with the new instrument R_{100} and the equivalent capacitance C_{EQ} at 100 kHz.

Nominal resistance R_N (Ω)	Measured resistance R_{100} (Ω)	Difference $R_N - R_{100}$ (%)	Equivalent capacitance C_{EQ} (pF)
1666.66	1666.61	−0.003	954.93
2000	1999.78	−0.011	795.77
2500	2499.7	−0.012	636.62
3333.33	3333.15	−0.005	477.46
5000	5000.9	0.018	318.31
10 000	10 002.4	0.024	159.15
14 700	14 695	−0.034	108.26
20 000	19 986	−0.07	79.57

capacitors as these sensors are specified to ensure a dissipation factor of smaller than 0.07. The real sensor parameters were simulated by means of a 442 pF capacitor (Siemens, Styroflex KS, ±1%) in parallel with a resistor of 50 kΩ (VISHAY, ±0.1%). The calculated dissipation factor is equivalent to 0.072. The measured capacitance and temperature curves can be seen in figure 7.

During the first 30 min of the measurement time we observe a warm-up effect. Neglecting this, the maximum fluctuation is 0.05 pF (= 0.011%). The mean value is found to be 445.73 pF, with a standard deviation of 8.7 fF. Including the warm-up phase the maximum deviation is 0.1 pF (= 0.022%). One reason for this deterioration in behaviour is the fact that the phase shift of the electronics is definitely not sufficiently compensated. With an increasing dissipation factor, the error due to the phase shift resolution error of max. 0.1797° increases.

The obtained resolution of the instrument strongly depends highly on the properties of the DC voltage meter. With an integration time of 500 ms of the HP3458A Multimeter we could still observe a stable display at 10 fF.

5. Conclusions and outlook

We have demonstrated a novel measurement instrument suitable for capacitance sensors ranging from 50 pF to 600 pF, in particular for humidity sensor applications. Using an autocalibration feature and an offset compensation option, we minimized the errors due to component drifts and uncertainty in electronic components. We investigated the performance and achieved a resolution of better than 10 fF with a guaranteed linearity of 0.1%. The results indicate a reproducibility of ±0.005% for capacitance sensors with a dissipation factor smaller than 0.07, neglecting the warm-up phase of 30 min. For nearly ideal capacitors with very small dissipation factors the reproducibility is better than 0.002%.

The complexity of the circuitry is in apparent contradiction to our claim of low cost and may seem disproportionate with respect to the achieved performance. However, the complete circuit consists essentially of only three active components: a field programmable gate array (XILINX XC3042 at a cost of less than US $10), a dual-channel multiplying DAC and a number of operational amplifiers housed in one DIL package.

The prototype could be easily modified for universal use as a capacitance and/or impedance meter. Another interesting field of application is the use of the technique for a general lock-in amplifier for amplitude and phase measurements at high frequencies. This mixed analogue/digital synchronous demodulation technique could provide a low cost and viable alternative to solely analogue or solely digital signal processing which is difficult to implement.

The advantage of this implementation is that due to the digital nature of the solution there are no components

which need to be adjusted. This simplifies duplication and production costs. It is to be expected that in the future more complex circuit solutions will be used, bringing reductions in production and service costs since with the advance in field programmable devices more complex circuit topologies can be implemented without necessarily increasing the cost of the system.

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