NXP's Nonlinear Device Model Verification for ADS 2022

Adam Mahan
EDA and Metrology Team
Radio Power Solutions
NXP Semiconductor

Contents

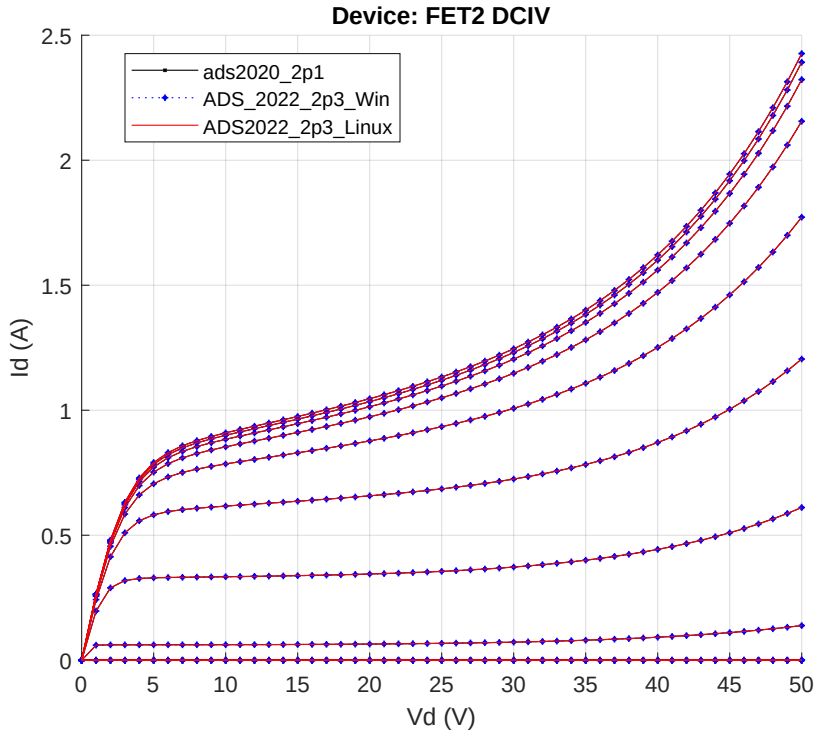
1.1 Introduction

This benchmark compares the FET^2 model implementation in the RF Power Design Kit version 2.3, and a previous release for historical comparison. The kit was recompiled for ADS 2022. All results are shown for MS Windows 10 64bit and Red Hat 7 Linux. All ADS releases use the same test benches for DC-IV, 1-Tone Harmonic Balance, Large-Signal S-parameters, Small-Signal S-parameters and Transient simulations.

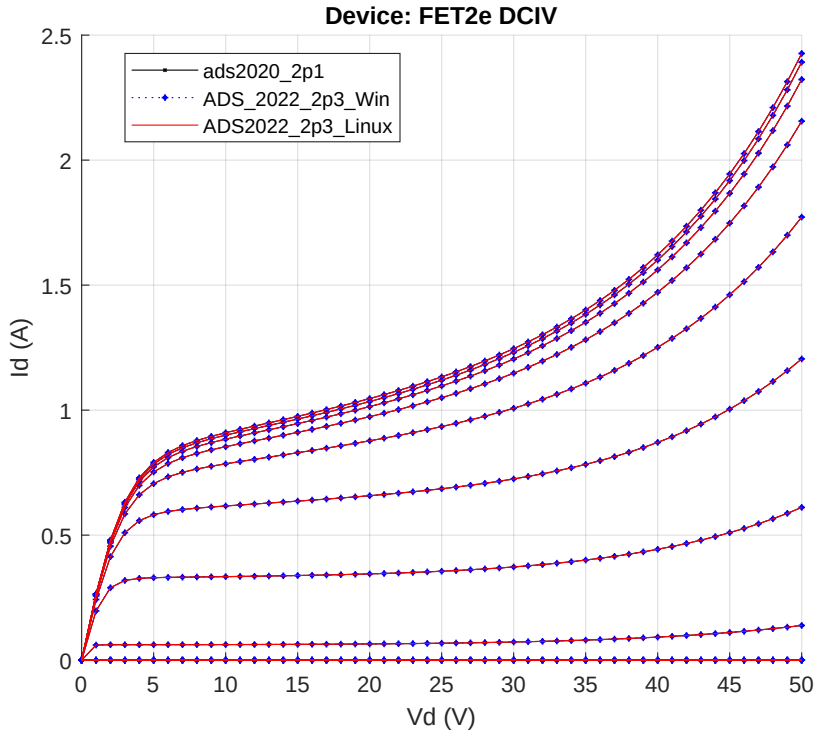
All of these FET^2 models are identical except for method of input of model parameters. The FET^2 model has the model parameters hard-coded into the simulation netlist. The Encoded FET^2 model reads the encrypted model parameters from a file. The filename is hard-coded into the simulation netlist. The new FET^2 model for waveform engineering supports access to the internal drain to source and capacitive currents. The Waveform Engineering FET^2model differs from the FET^2 by the model name and number of terminals. This waveform engineering FET^2 model made its first appearance in ADS2016.01.

1.2 DCIV Simulation Tests

DC-IV curves were generated with Vg = -2 to 10 Volts with 1 Volt steps and Vd = 0 to 50 Volts with 1 Volt Steps.

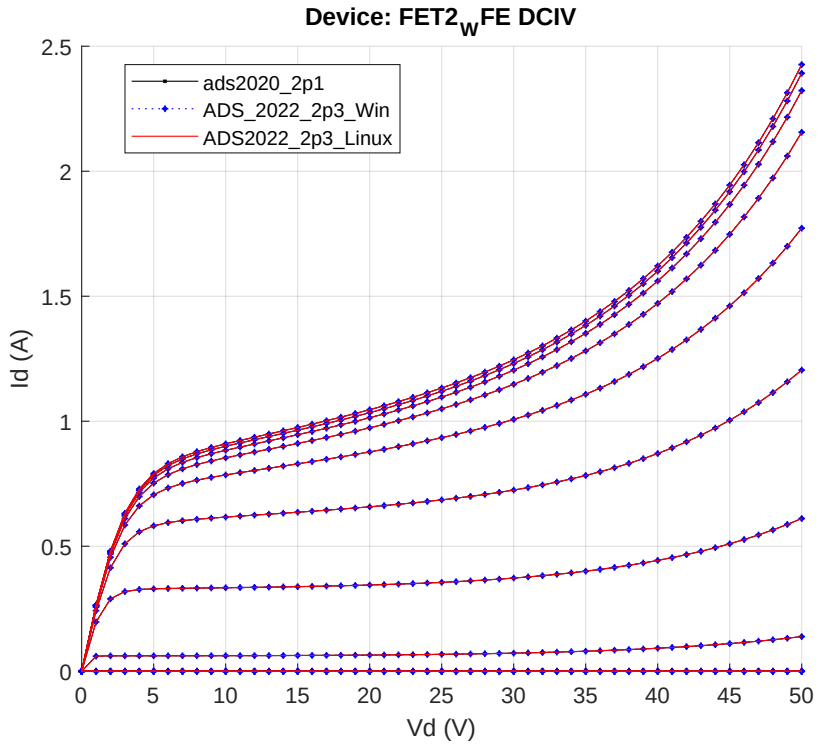


(a) Model Card FET2 DC-IV

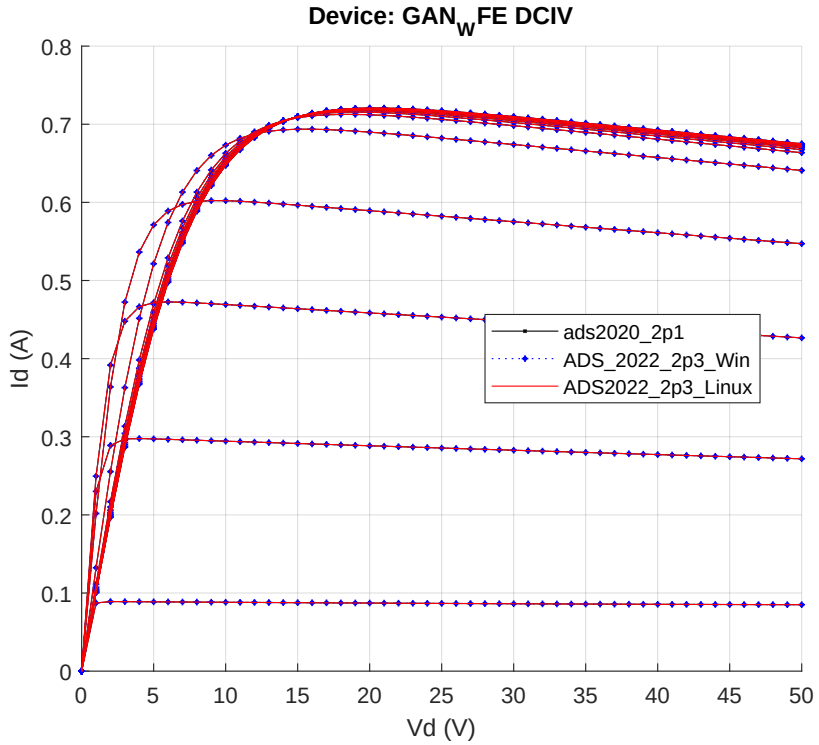


(b) Encoded FET2 DC-IV

Fig. 1.1. FET2 DC-IV Tests



(a) Waveform Engineering FET2 DC-IV

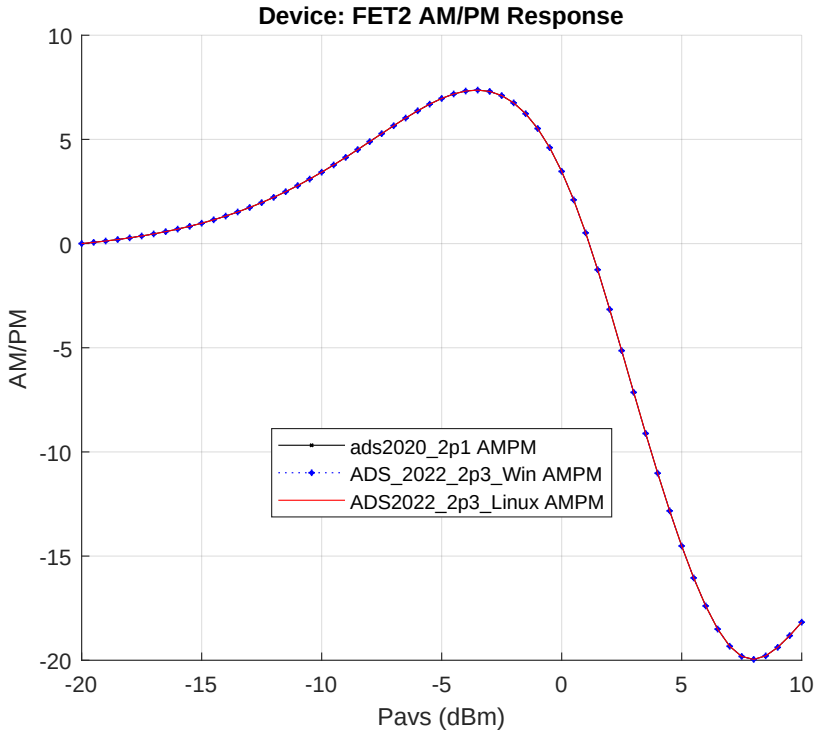


(b) GAN WFE DC-IV

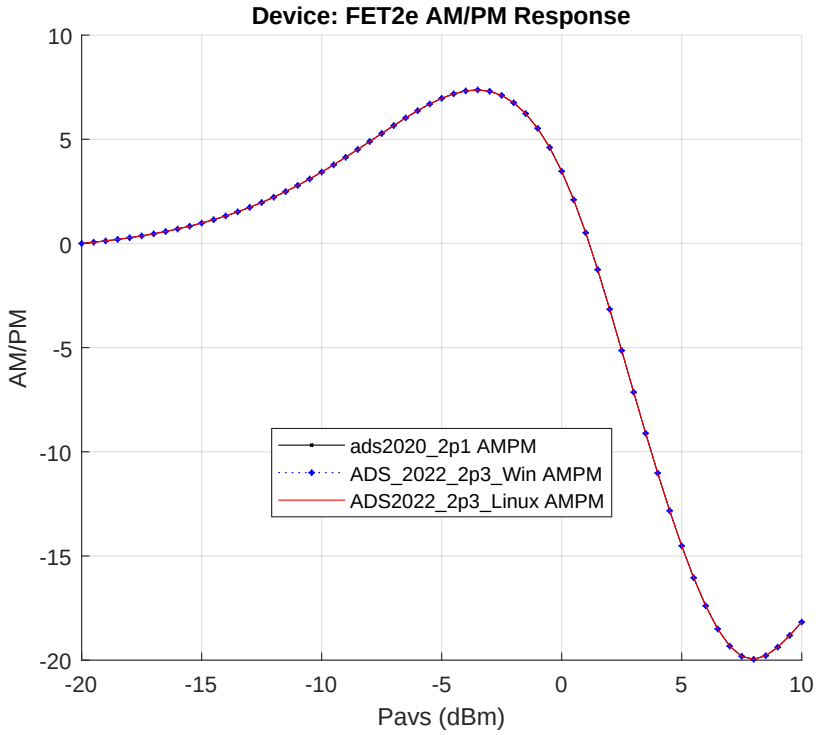
Fig. 1.2. FET2 DC-IV Tests

1.3 HB 1Tone Simulation Tests

The 1 tone harmonic balance test bench was set up to do a simple input power sweep with Pin = -20 to 10 dBm every 0.5 dBm. Simple L-C matching circuits were used on the Gate and Drain side to match the device impedance to 50 Ohms at the simulation ports. The gate bias voltage was set to 2.76 Volts and drain bias voltage was set to 28.0 Volts. The frequency of operation is 2.14 GHz. The fundamental order was set to 5 using the Krylov engine and a fundamental oversample of 2 for convergence. The following graphs show AM/PM, Transducer Gain, IRL, Re(Zin), Im(Zin) and Pout.

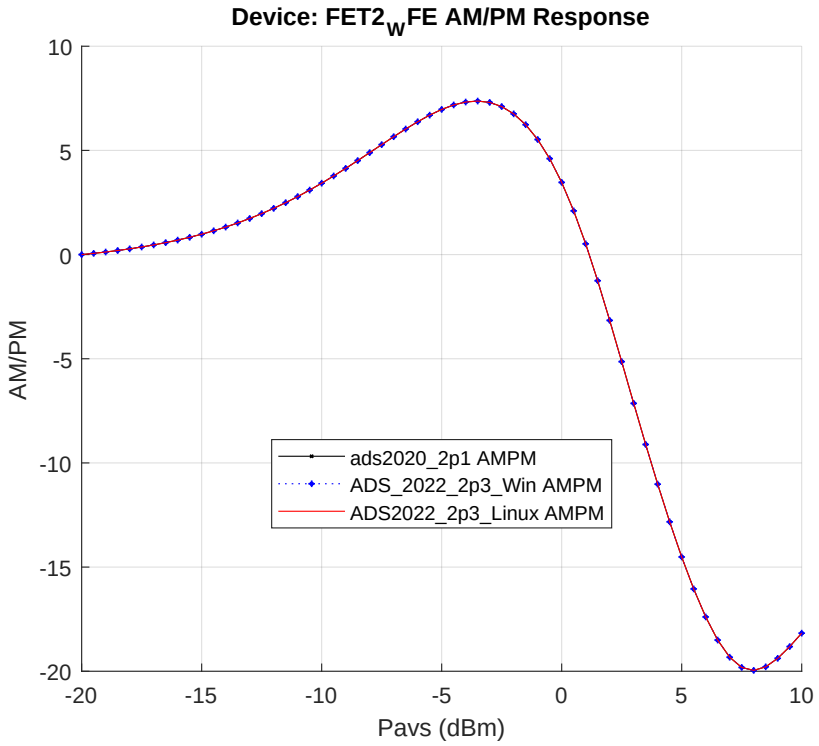


(a) Model Card FET2 HB-1Tone AM/PM

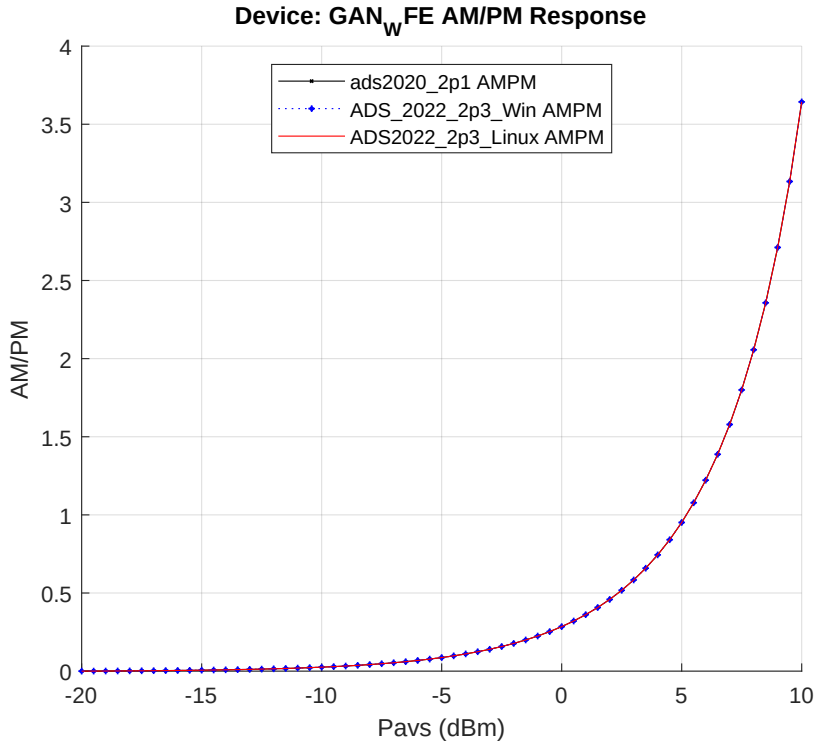


(b) Encoded FET2 HB-1Tone AM/PM

Fig. 1.3. FET2 HB-1Tone Results for **??** AM/PM versus Input Power

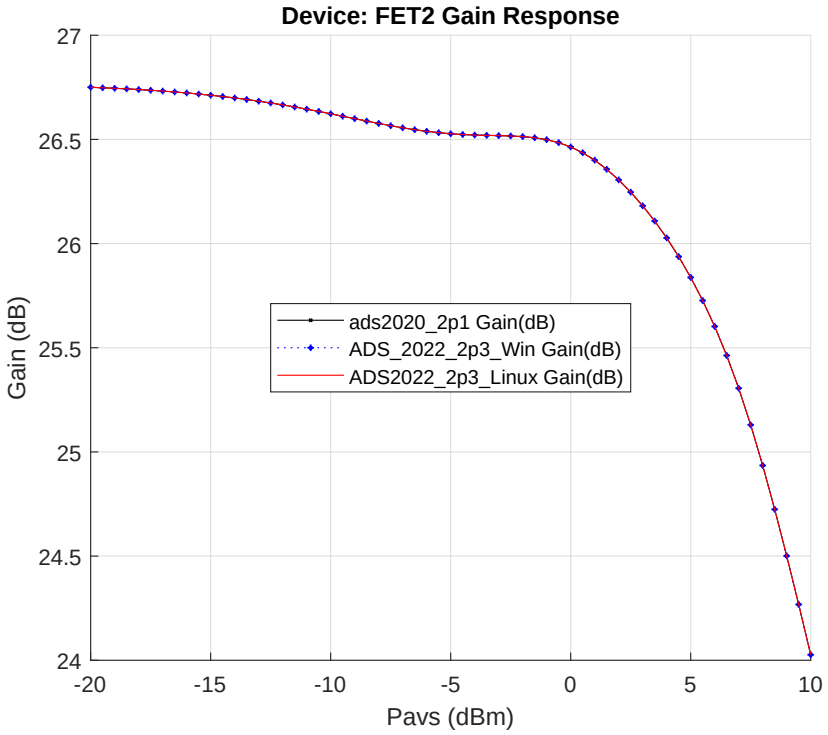


(a) Waveform Engineering FET2 HB-1Tone AM/PM

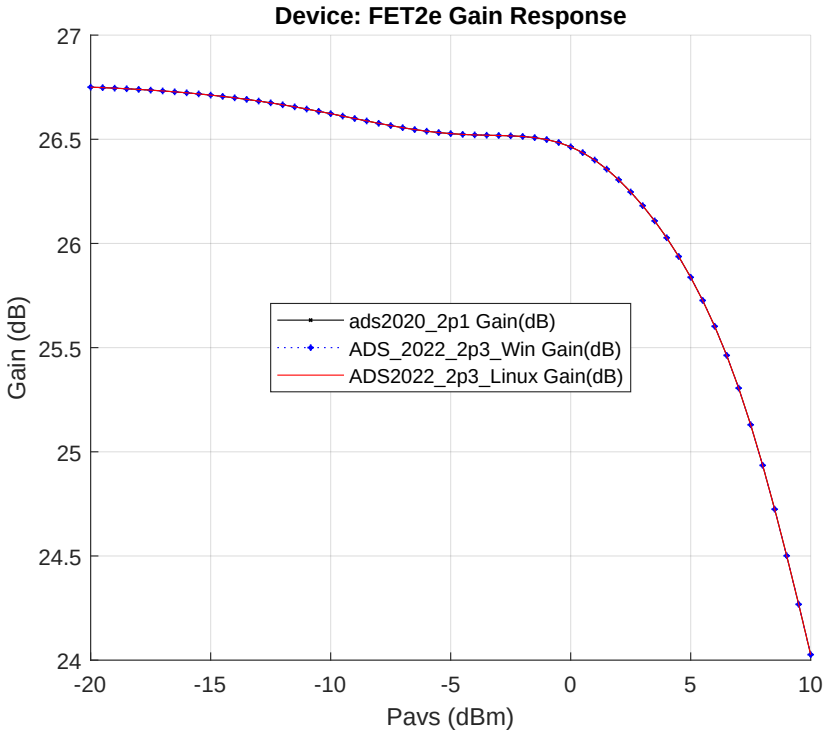


(b) GAN WFE HB-1Tone AM/PM

Fig. 1.4. FET2 HB-1Tone Results for **??** AM/PM versus Input Power

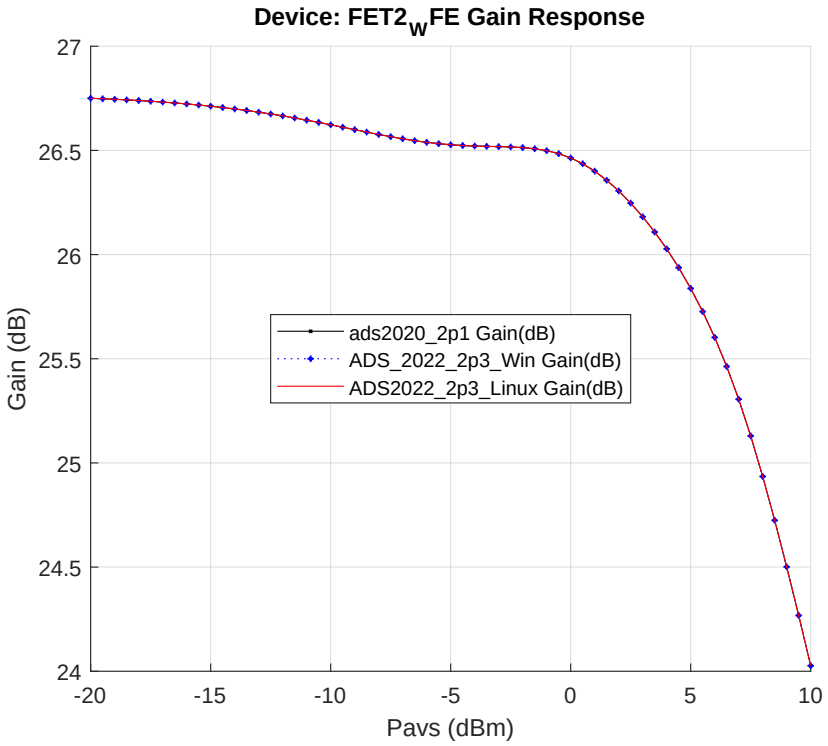


(a) Model Card FET2 HB-1Tone Transducer Gain

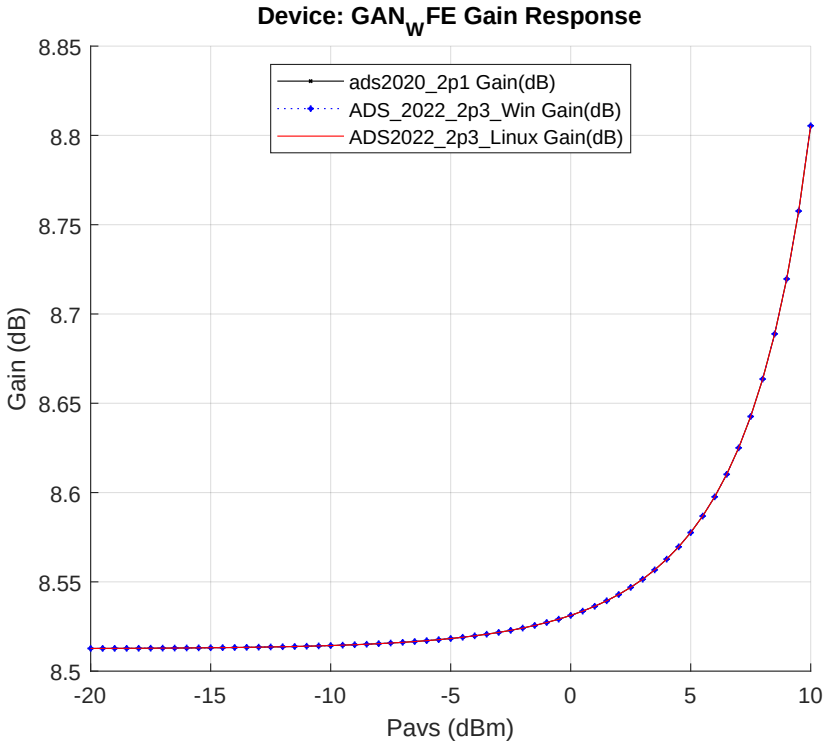


(b) Encoded FET2 HB-1Tone Transducer Gain

Fig. 1.5. FET2 HB-1Tone Results for **??** Gain versus Input Power

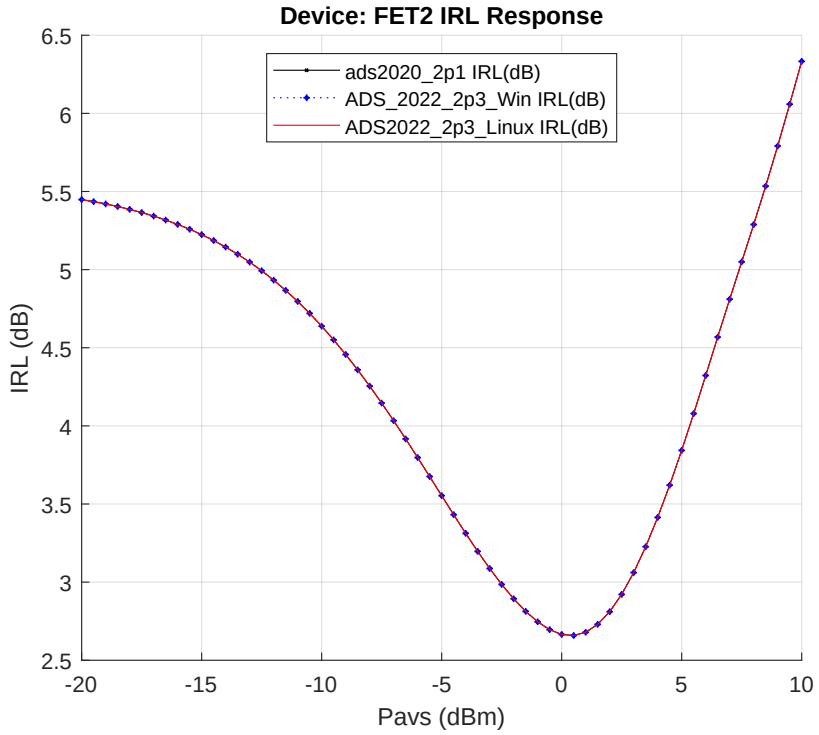


(a) Waveform Engineering FET2 HB-1Tone Transducer Gain

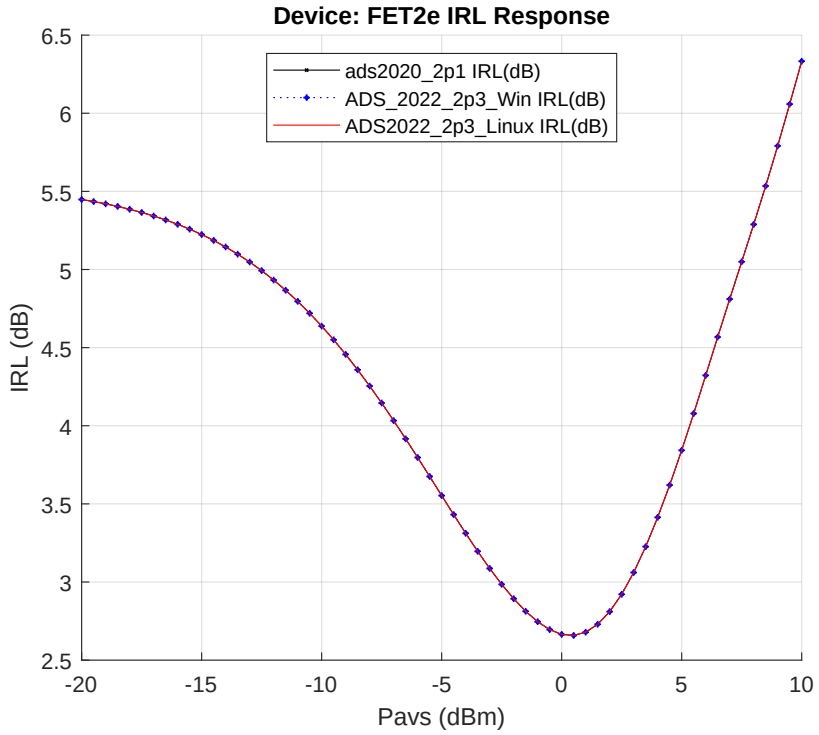


(b) GAN WFE HB-1Tone Transducer Gain

Fig. 1.6. FET2 HB-1Tone Results for **??** Gain versus Input Power

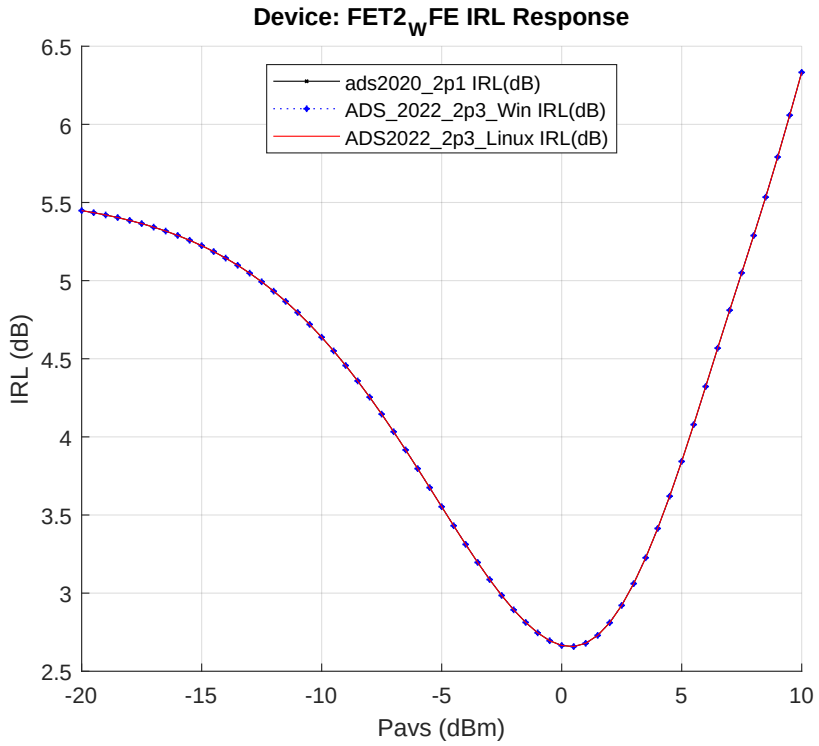


(a) Model Card FET2 HB-1Tone IRL

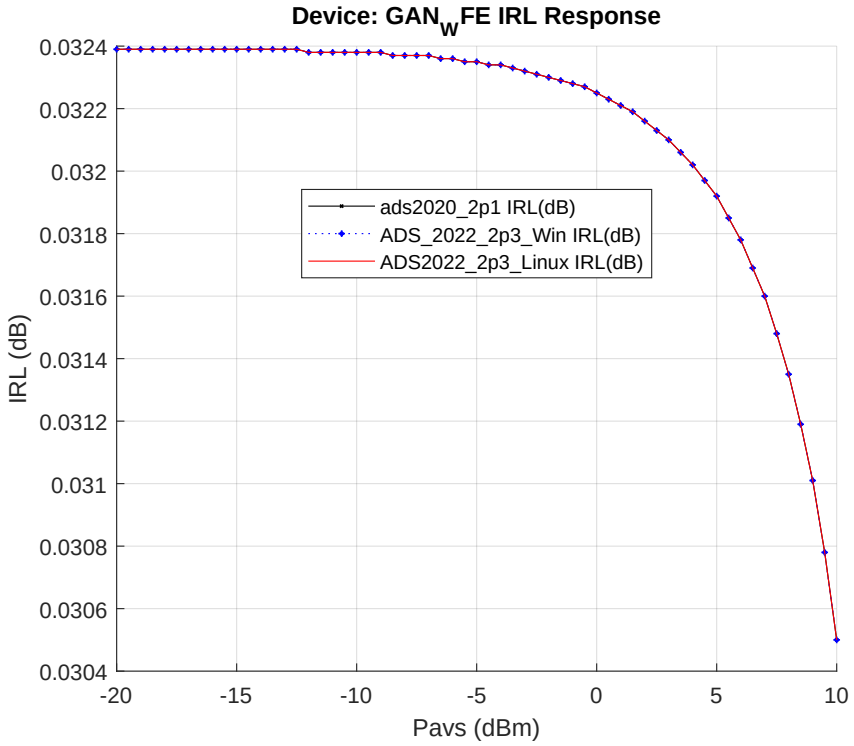


(b) Encoded FET2 HB-1Tone IRL

Fig. 1.7. FET2 HB-1Tone Results for **??** IRL versus Input Power

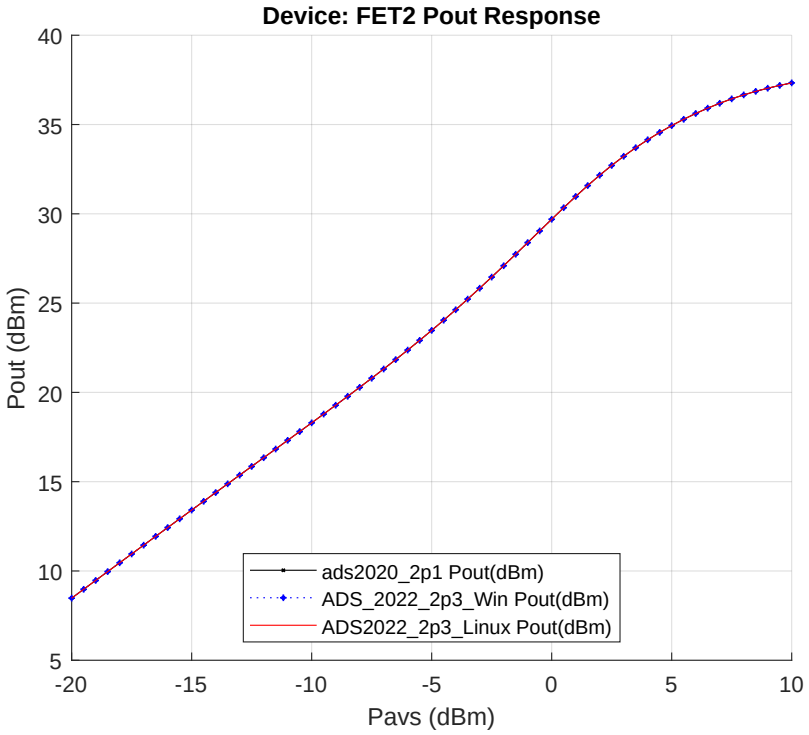


(a) Waveform Engineering FET2 HB-1Tone IRL

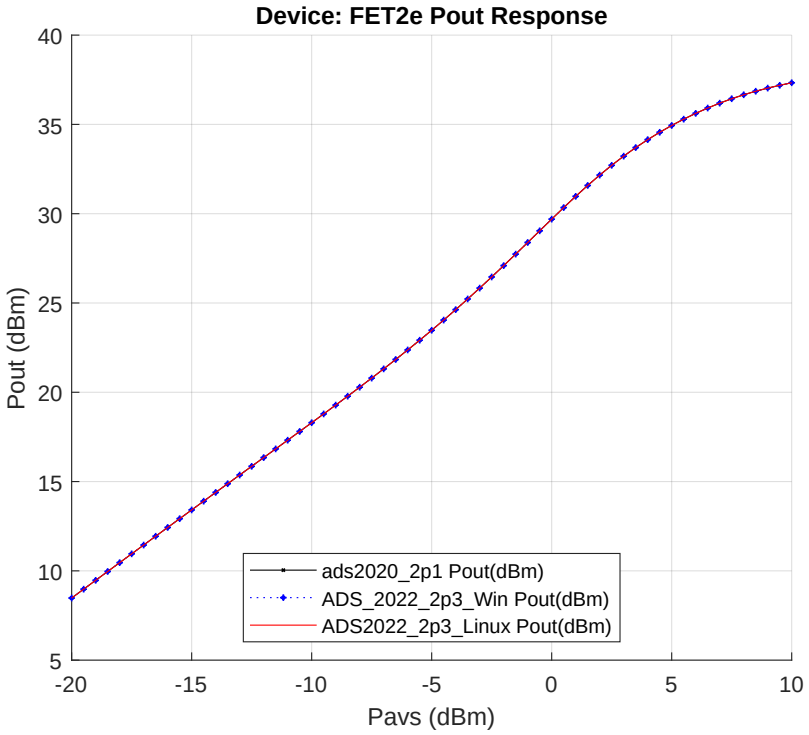


(b) GAN WFE HB-1Tone IRL

Fig. 1.8. FET2 HB-1Tone Results for **??** IRL versus Input Power

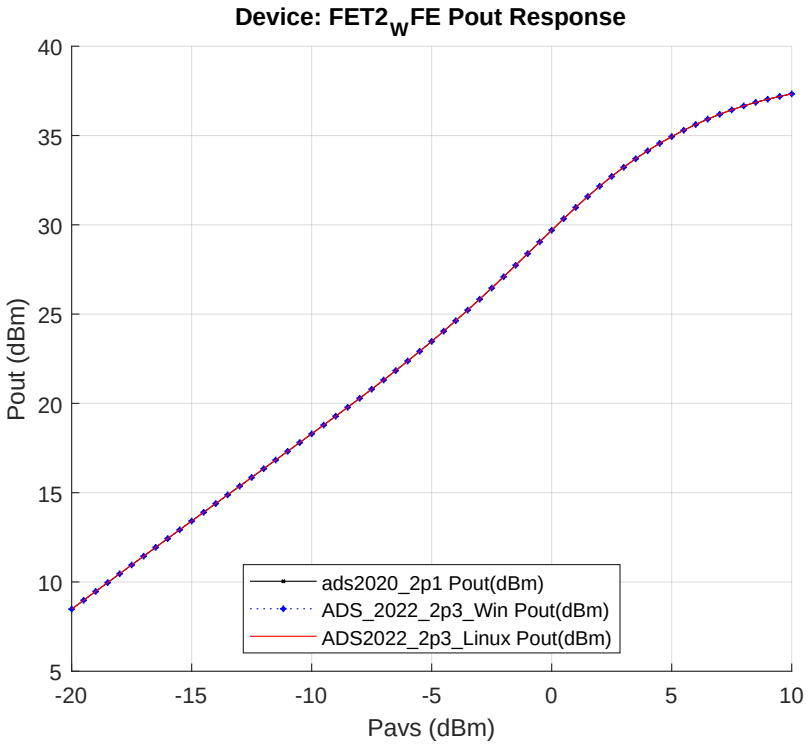


(a) Model Card FET2 HB-1Tone Pout

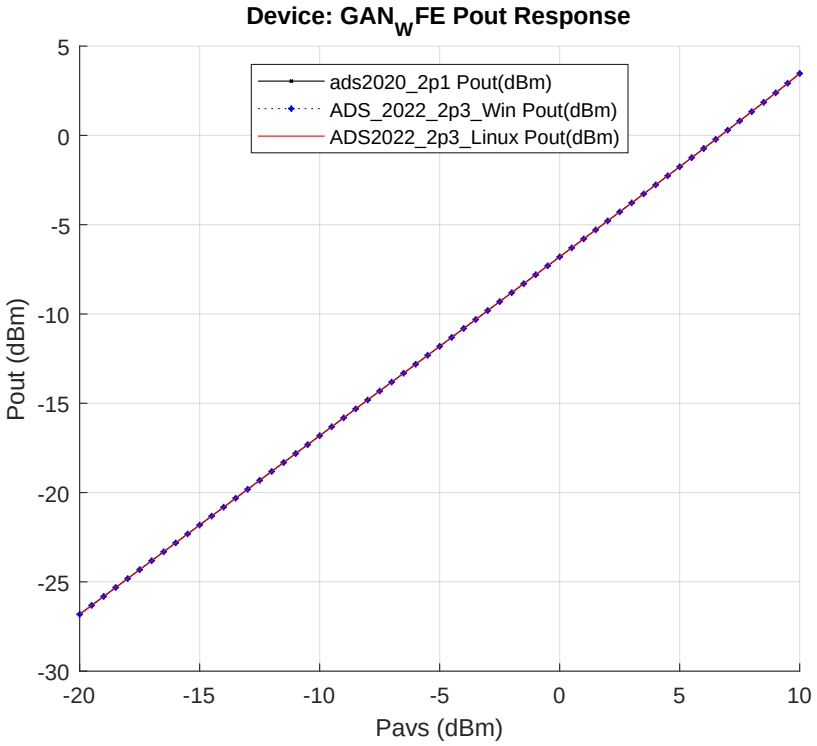


(b) Encoded FET2 HB-1Tone Pout

Fig. 1.9. FET2 HB-1Tone Pout(dBm).

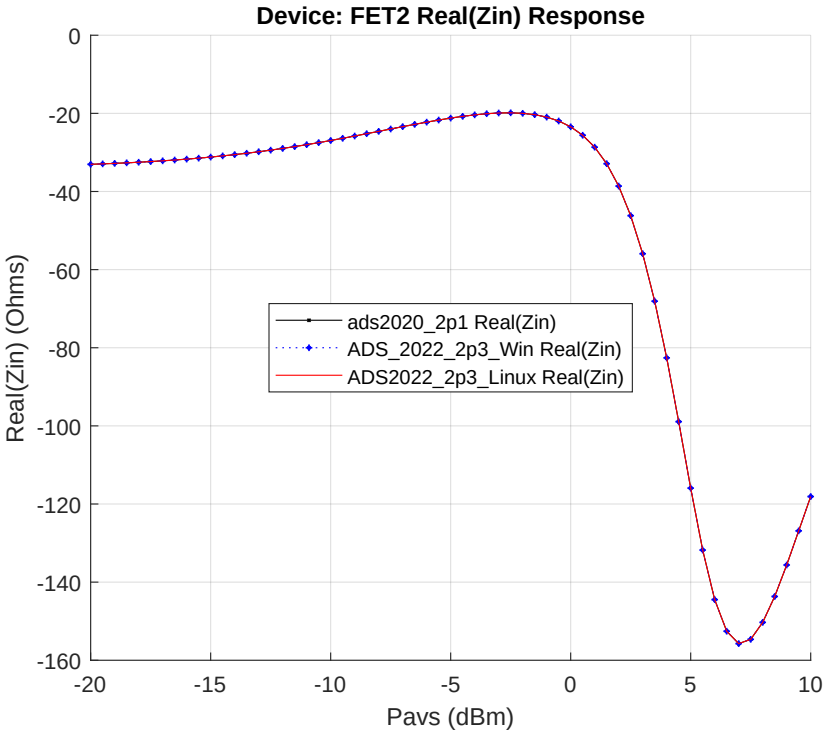


(a) Waveform Engineering FET2 HB-1Tone Pout

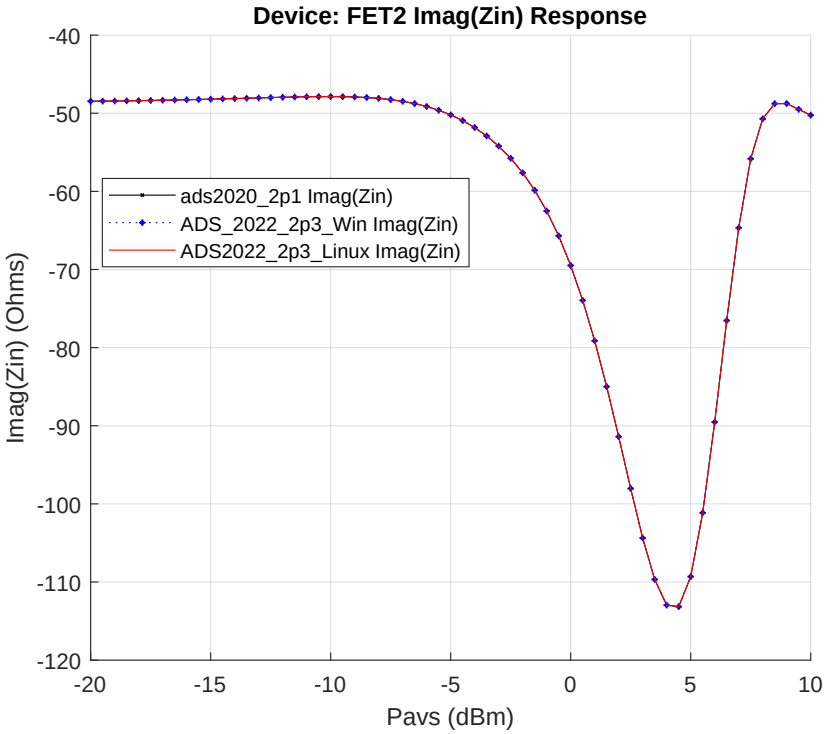


(b) GAN WFE HB-1Tone Pout

Fig. 1.10. FET2 HB-1Tone Pout(dBm).

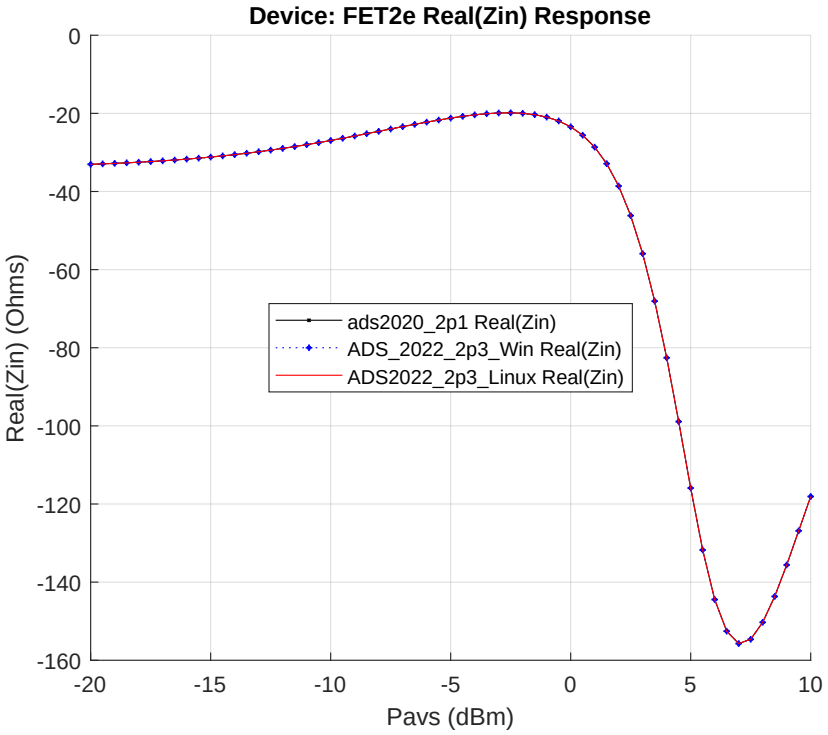


(a) Model Card FET2 HB-1Tone Zin

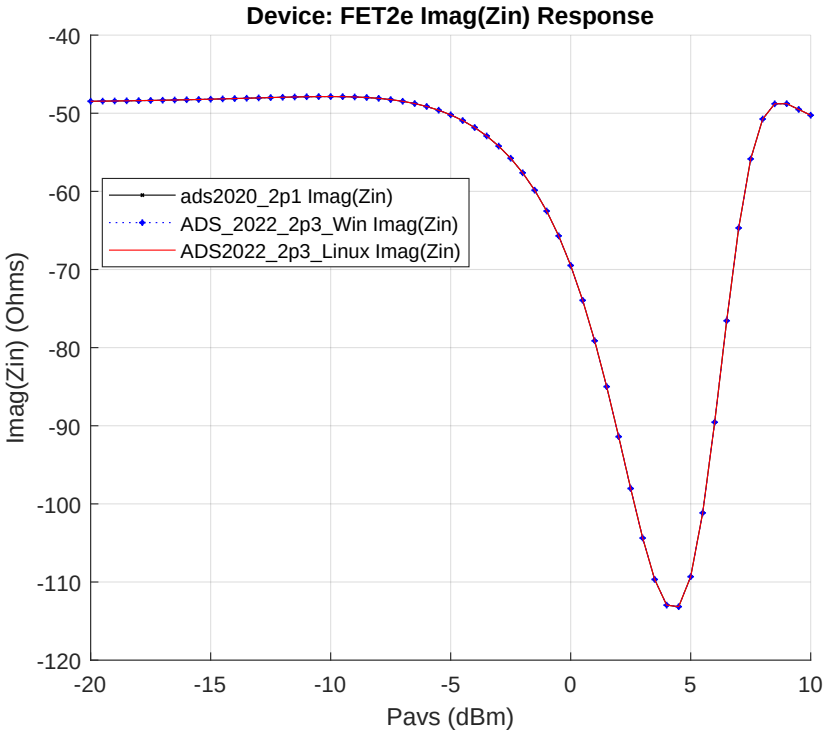


(b) Model Card FET2 HB-1Tone Zin

Fig. 1.11. HB-1Tone Results for Input Impedance versus Input Power

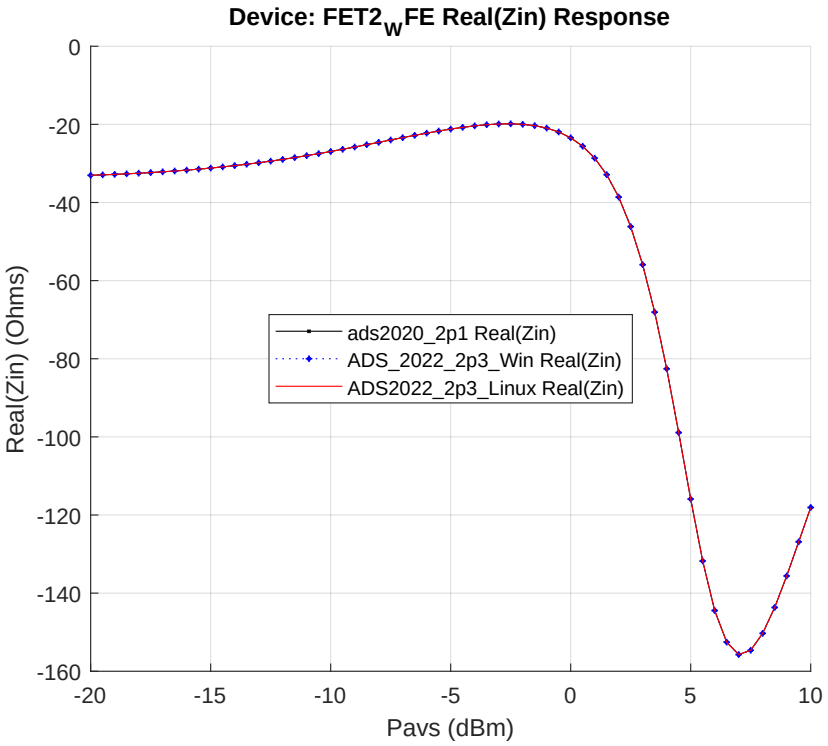


(a) Encoded FET2 HB-1Tone Zin

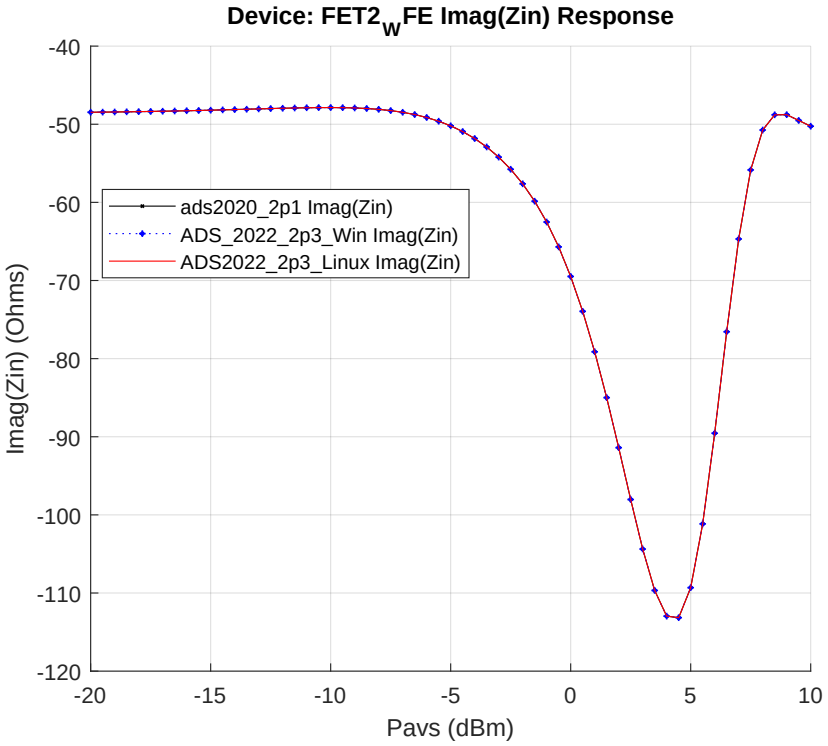


(b) Encoded FET2 HB-1Tone Zin

Fig. 1.12. HB-1Tone Results for Input Impedance versus Input Power



(a) Waveform Engineering FET2 HB-1Tone Zin

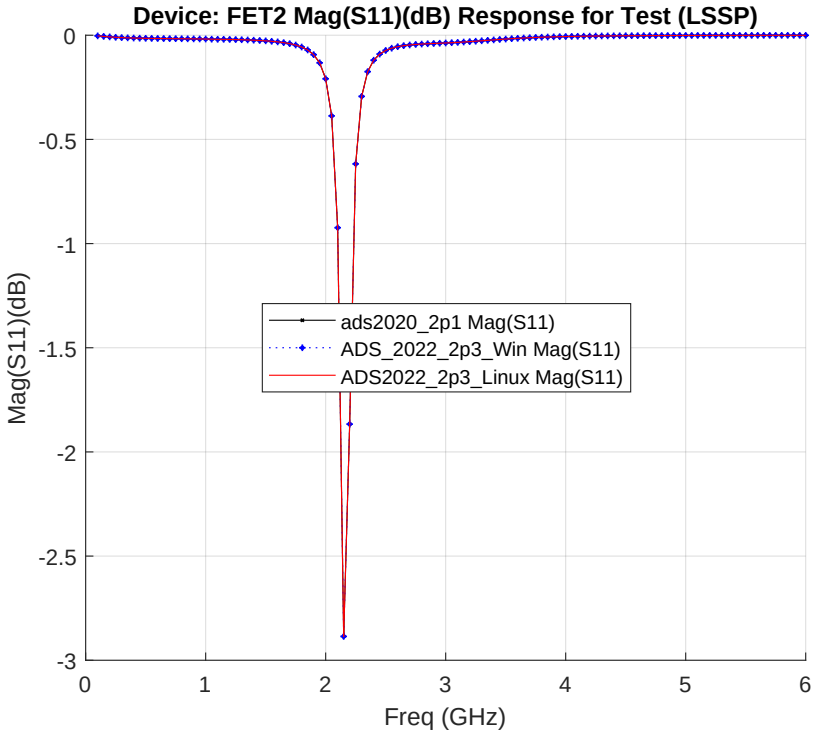


(b) Waveform Engineering FET2 HB-1Tone Zin

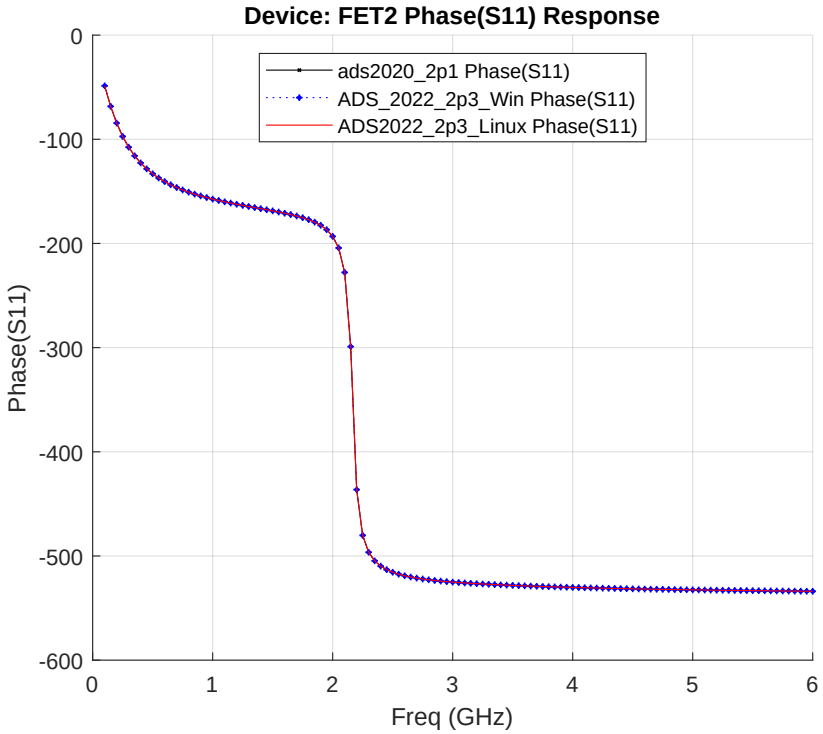
Fig. 1.13. HB-1Tone Results for Input Impedance versus Input Power

1.4 LSSP Simulation Tests

The following curves show the results of the Large Signal S-parameter simulation. This test bench also uses the simple L-C matching circuits on the gate and drain that were used in the 1 Tone harmonic balance test bench. Input Power was set to -10 dBm, Vg = 2.76 Volts, Vd= 28 Volts. Zo = 50 Ohms and frequency was swept from 0.1 to 6 GHz every 50 MHz. The fundamental order was set to 3 using the Krylov engine and fundamental oversample of 1 for convergence. The following plots are magnitude and phase of all four Large Signal S-Parameters.

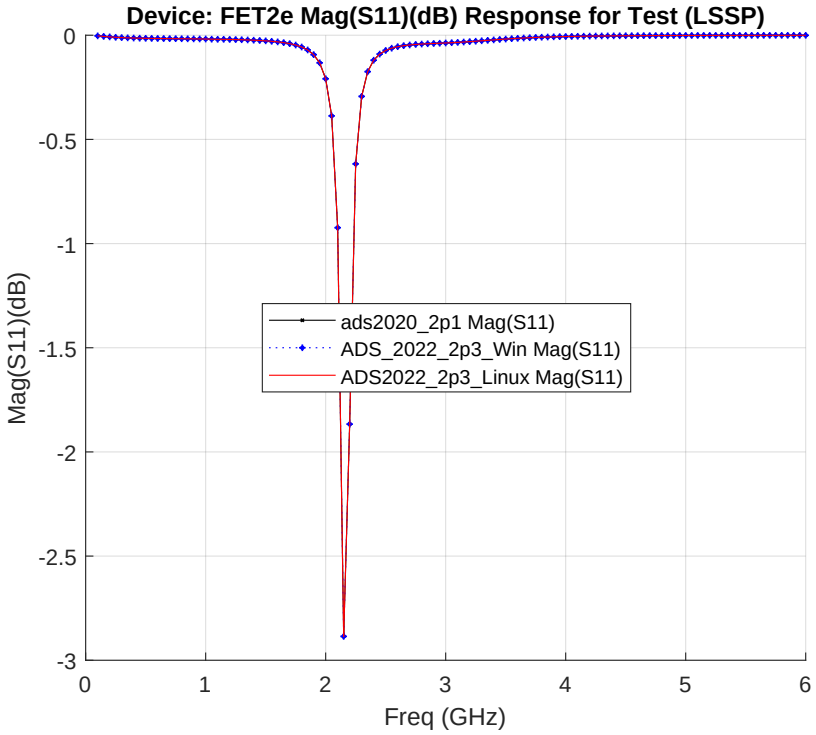


(a) Model Card FET2 LSSP S11

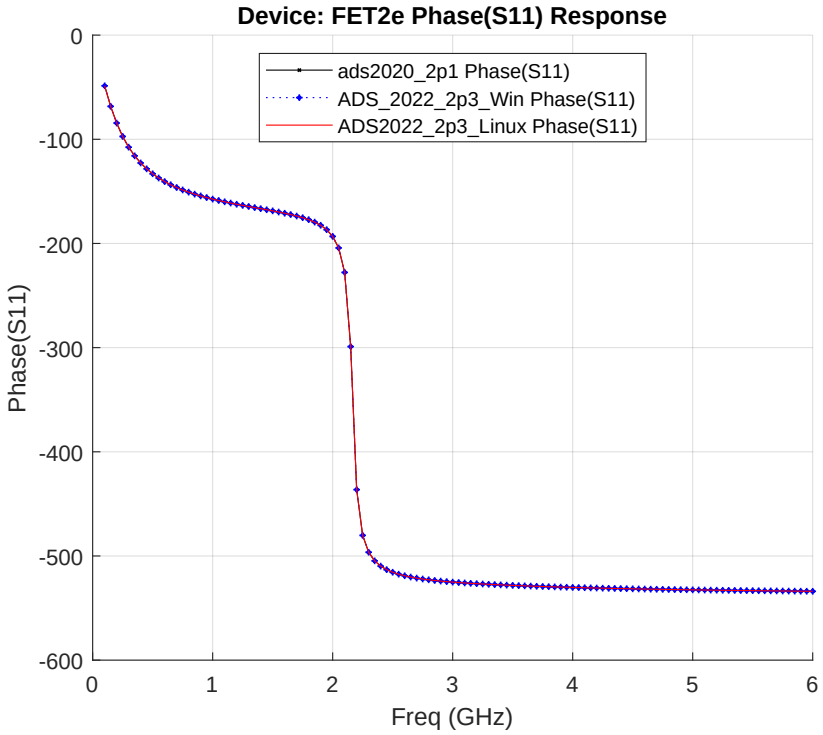


(b) Model Card FET2 LSSP S11

Fig. 1.14. FET2 LSSP Results for Mag(S11) and Phase(S11) versus Frequency

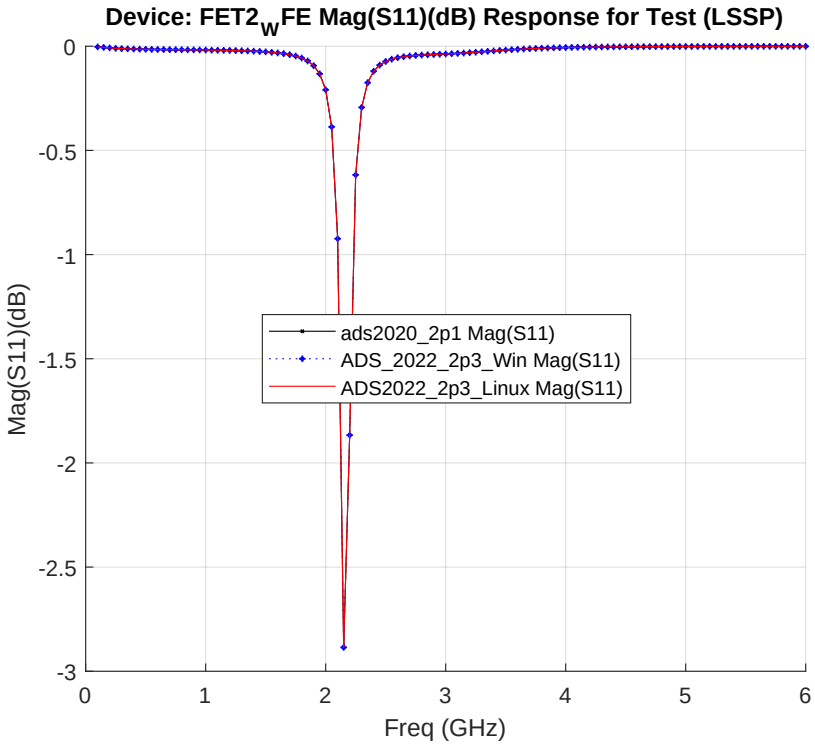


(a) Encoded FET2 LSSP S11

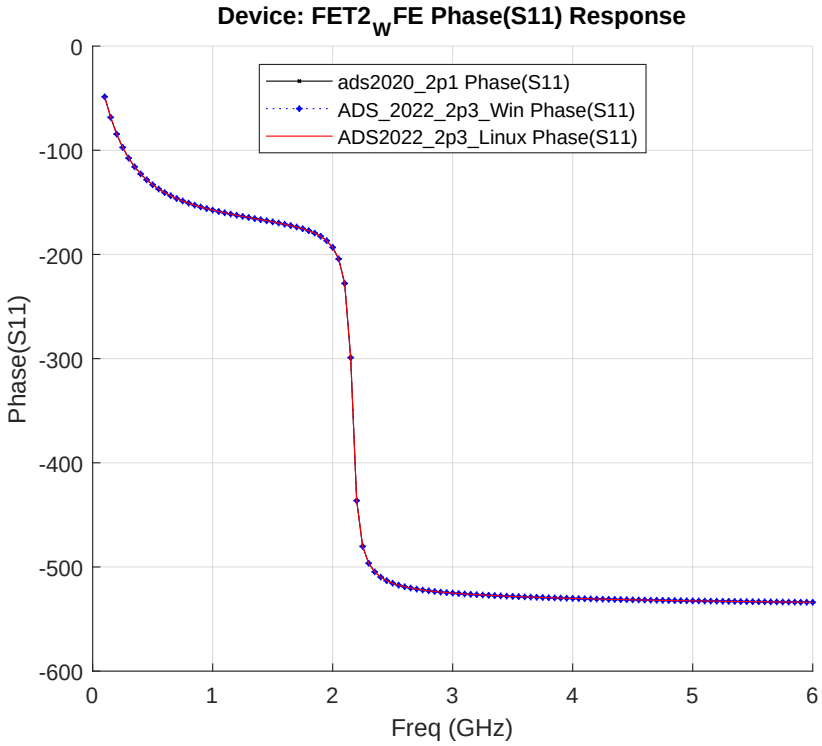


(b) Encoded FET2 LSSP S11

Fig. 1.15. FET2 LSSP Results for Mag(S11) and Phase(S11) versus Frequency

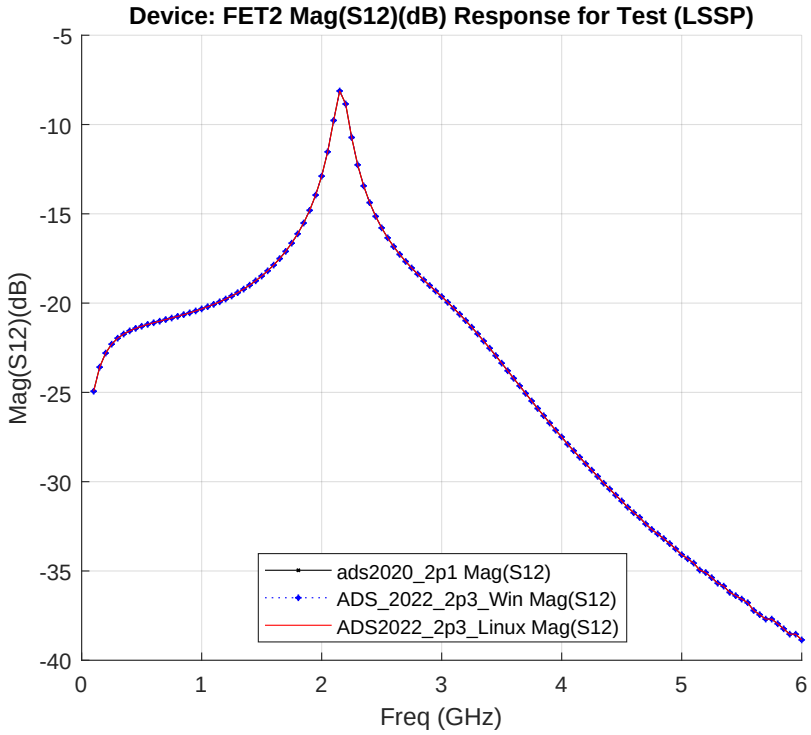


(a) Waveform Engineering FET2 LSSP S11

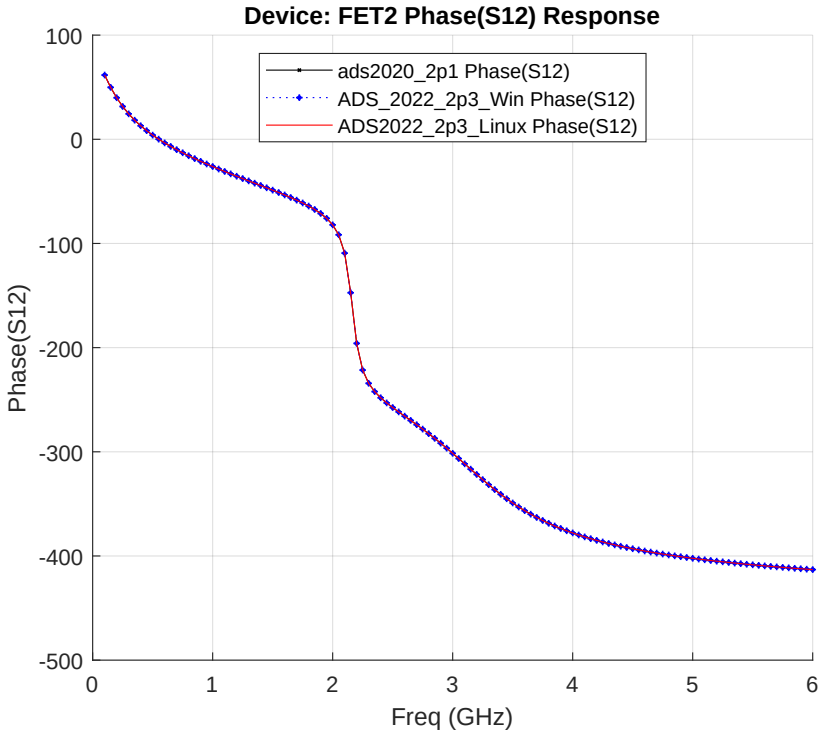


(b) Waveform Engineering FET2 LSSP S11

Fig. 1.16. FET2 LSSP Results for Mag(S11) and Phase(S11) versus Frequency

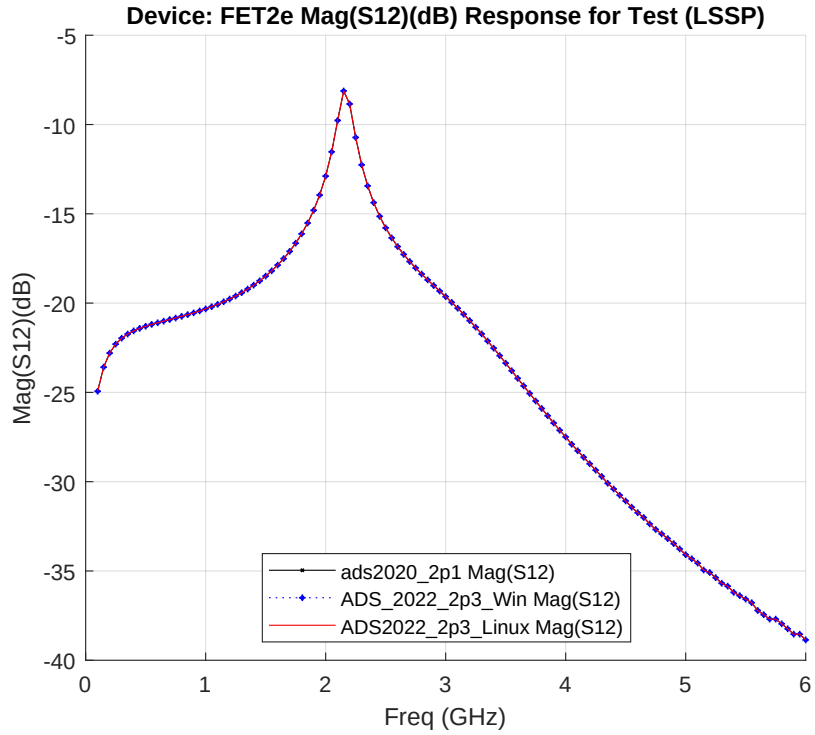


(a) Model Card FET2 LSSP S12

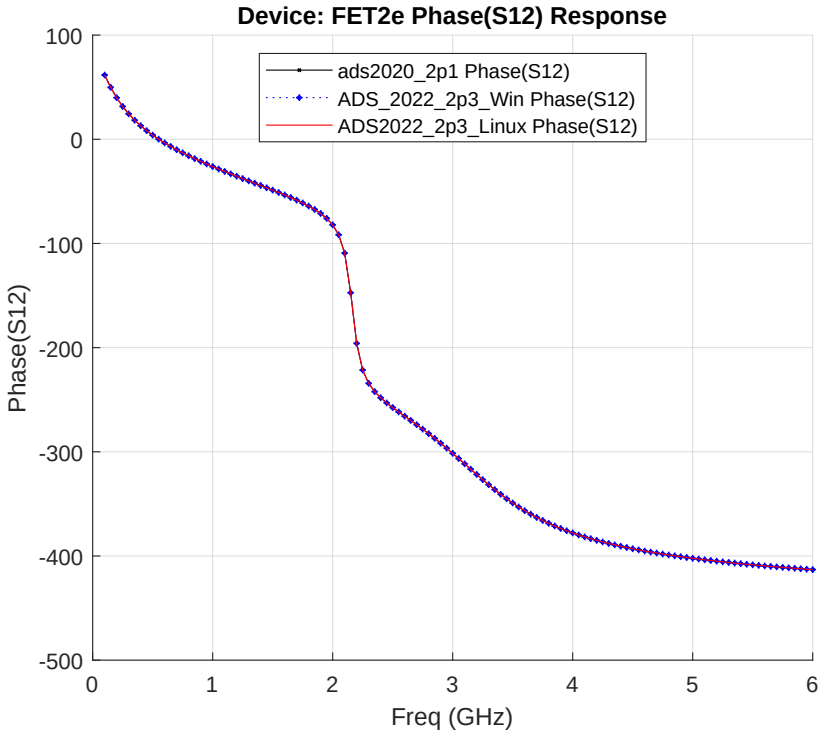


(b) Model Card FET2 LSSP S12

Fig. 1.17. FET2 LSSP Results for Mag(S12) and Phase(S12) versus Frequency

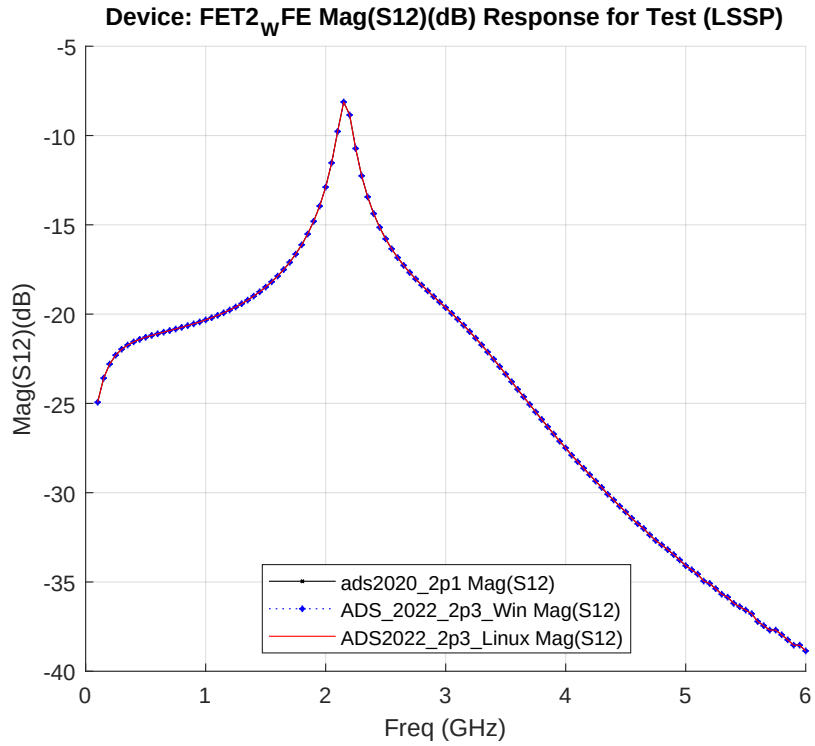


(a) Encoded FET2 LSSP S12

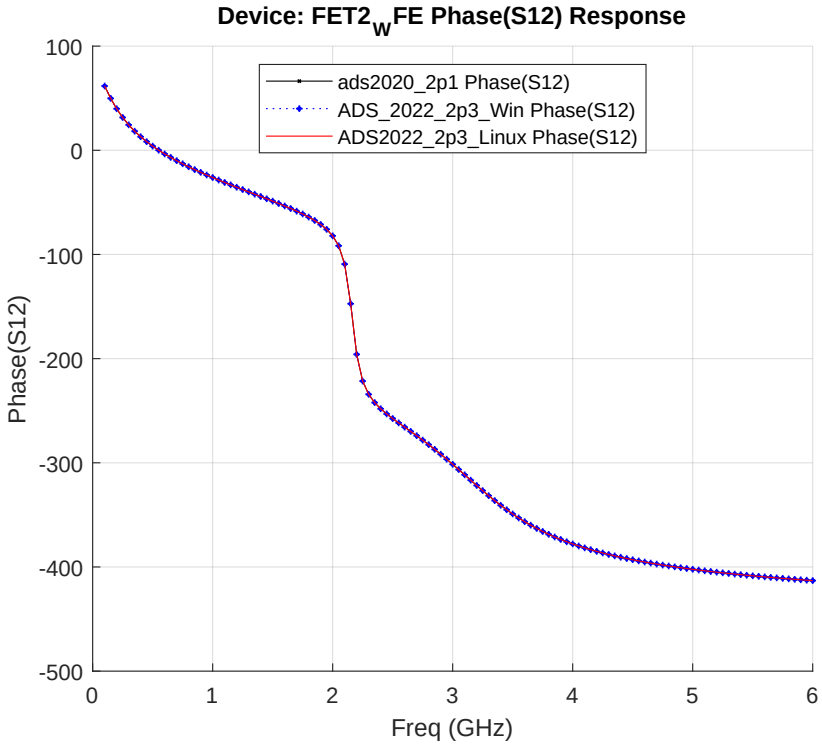


(b) Encoded FET2 LSSP S12

Fig. 1.18. FET2 LSSP Results for Mag(S12) and Phase(S12) versus Frequency

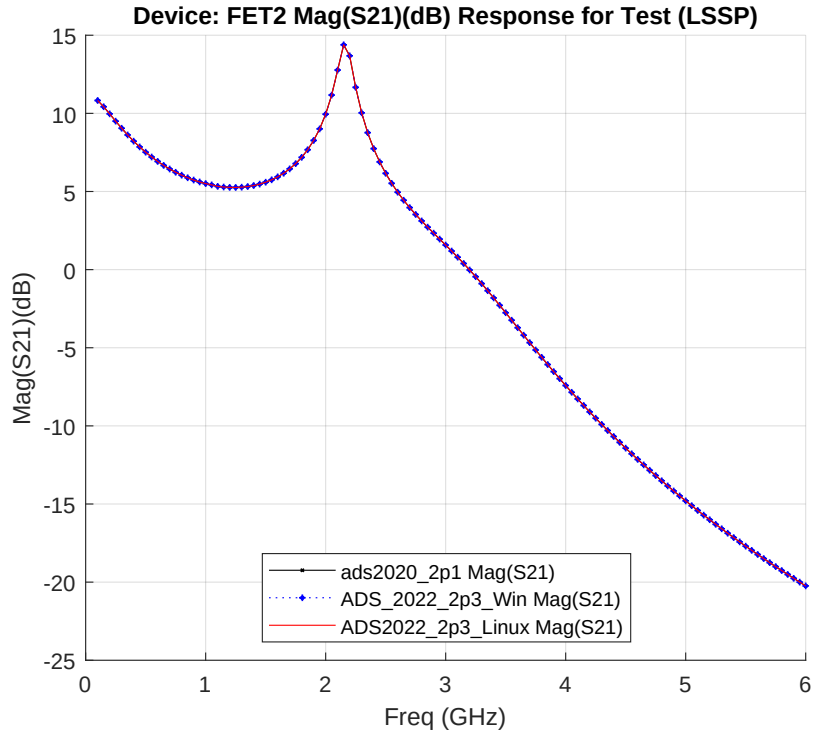


(a) Waveform Engineering FET2 LSSP S12

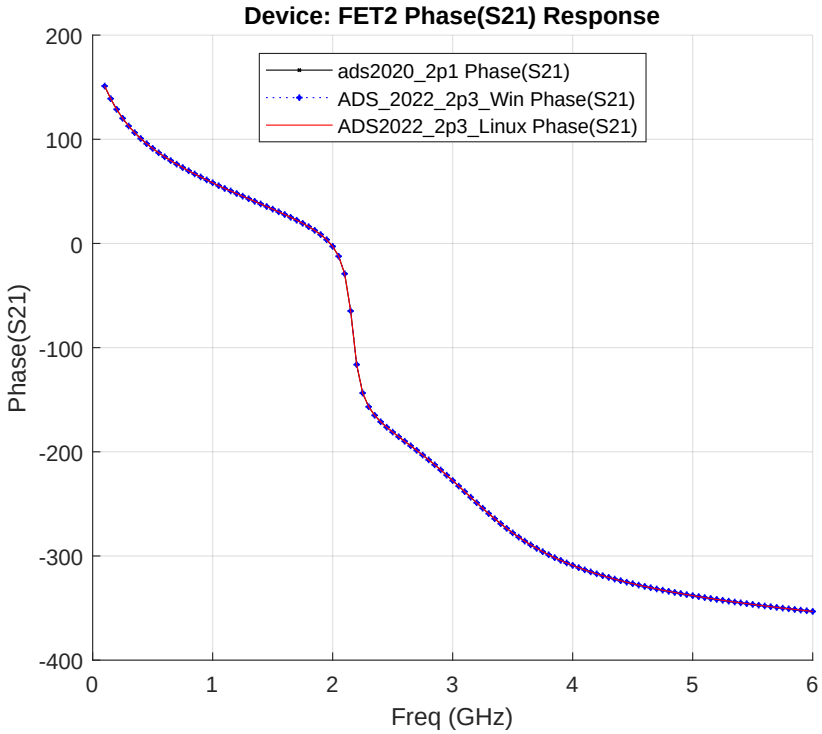


(b) Waveform Engineering FET2 LSSP S12

Fig. 1.19. FET2 LSSP Results for Mag(S12) and Phase(S12) versus Frequency

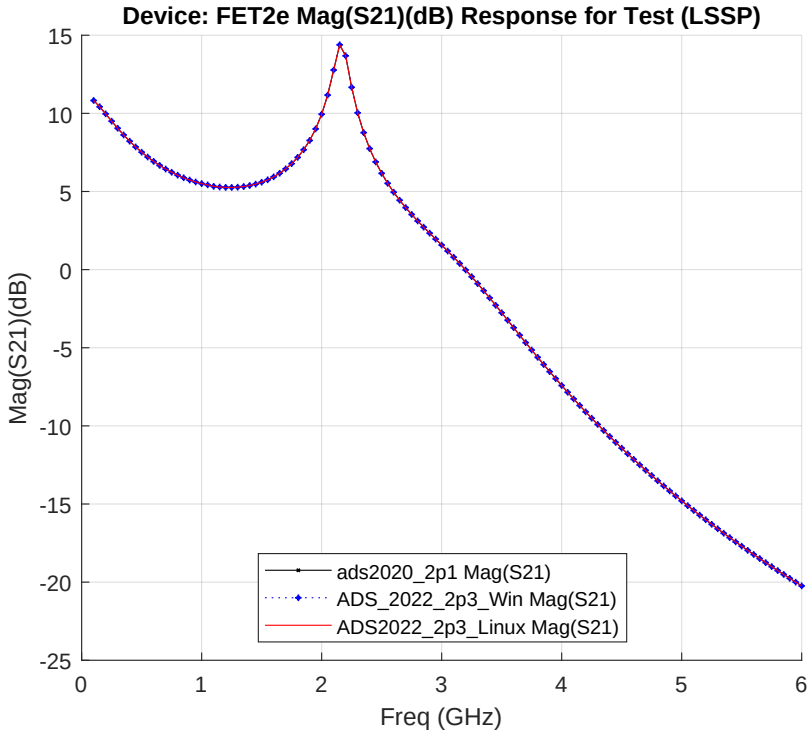


(a) Model Card FET2 LSSP S21

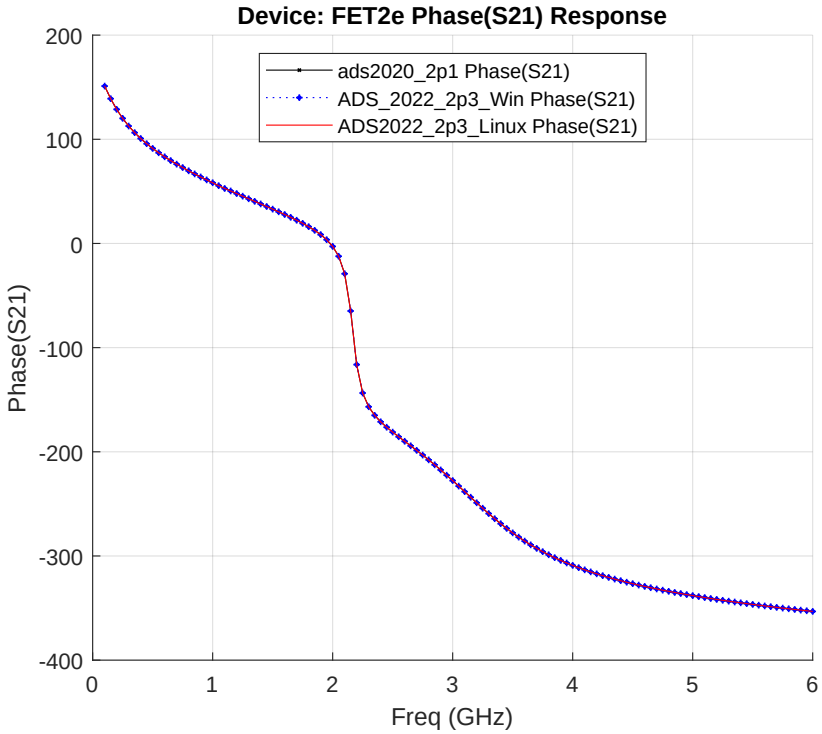


(b) Model Card FET2 LSSP S21

Fig. 1.20. FET2 LSSP Results for Mag(S21) and Phase(S21) versus Frequency

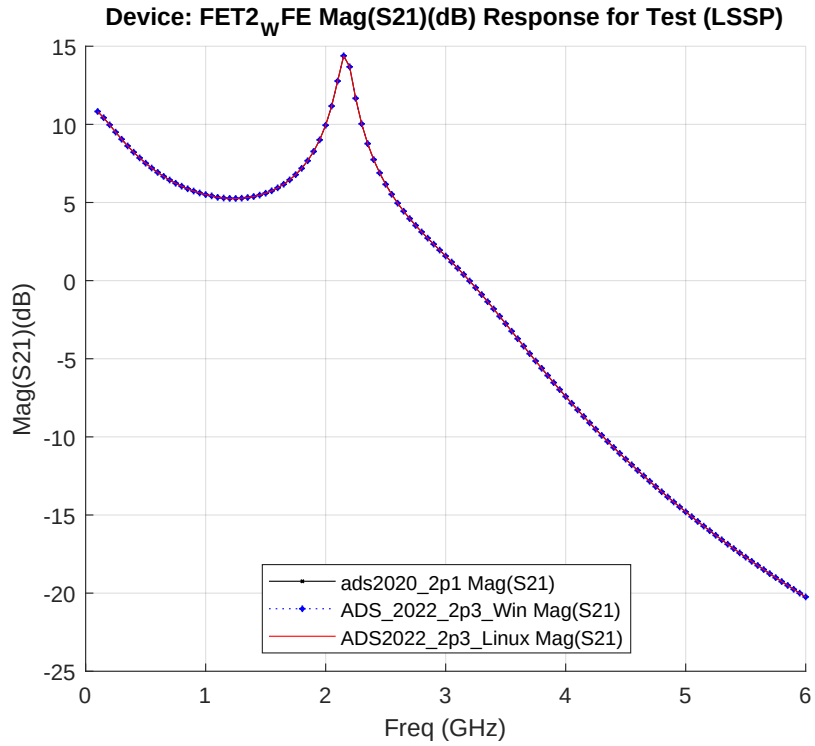


(a) Encoded FET2 LSSP S21

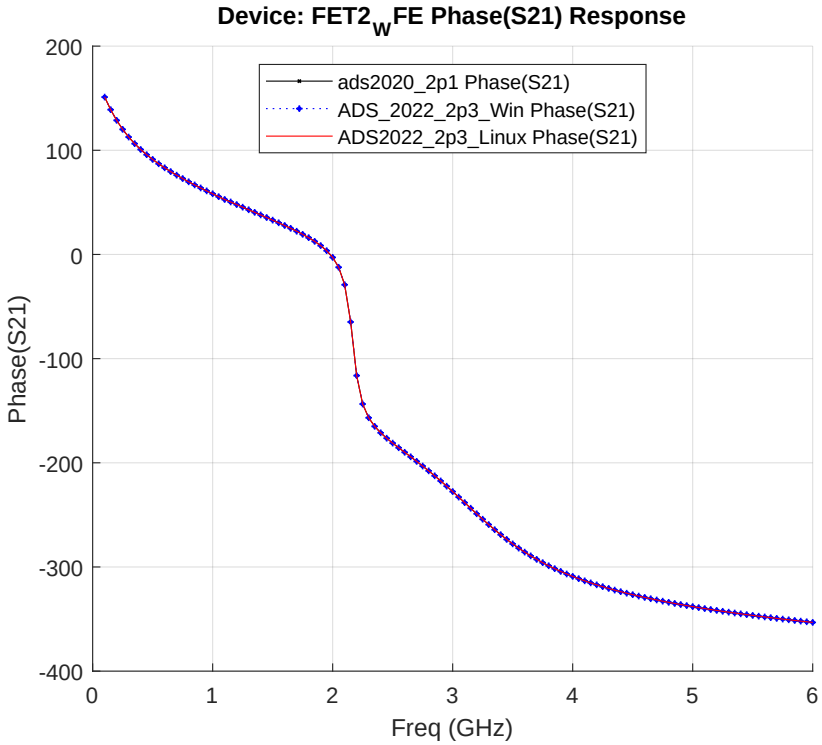


(b) Encoded FET2 LSSP S21

Fig. 1.21. FET2 LSSP Results for Mag(S21) and Phase(S21) versus Frequency

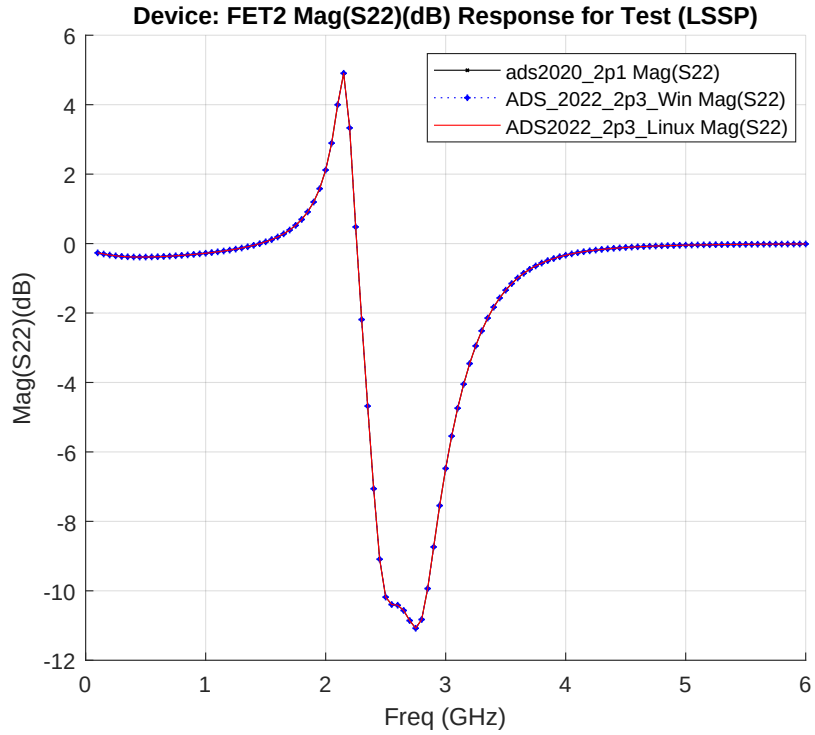


(a) Waveform Engineering FET2 LSSP S21

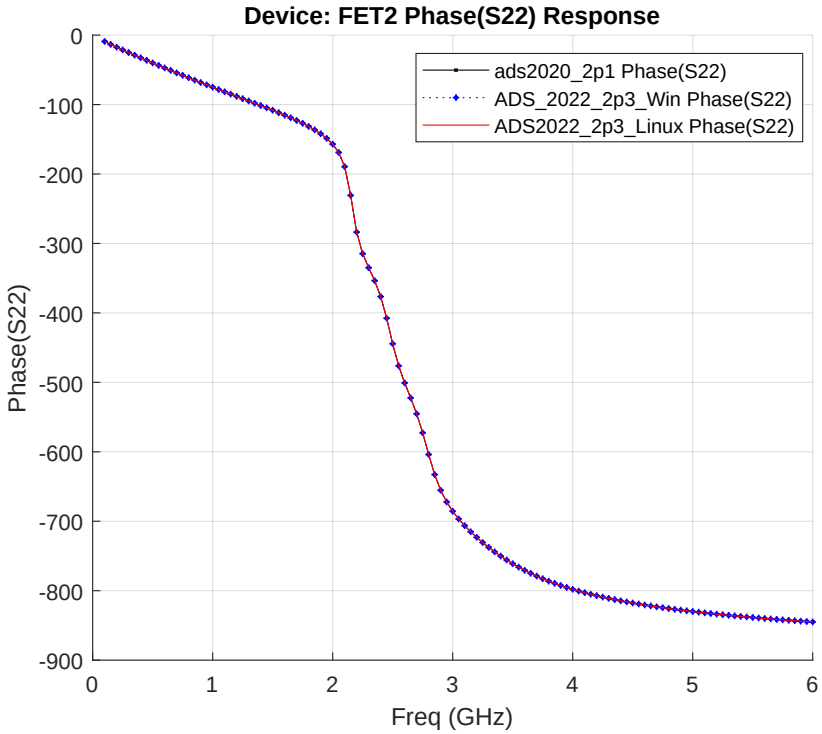


(b) Waveform Engineering FET2 LSSP S21

Fig. 1.22. FET2 LSSP Results for Mag(S21) and Phase(S21) versus Frequency

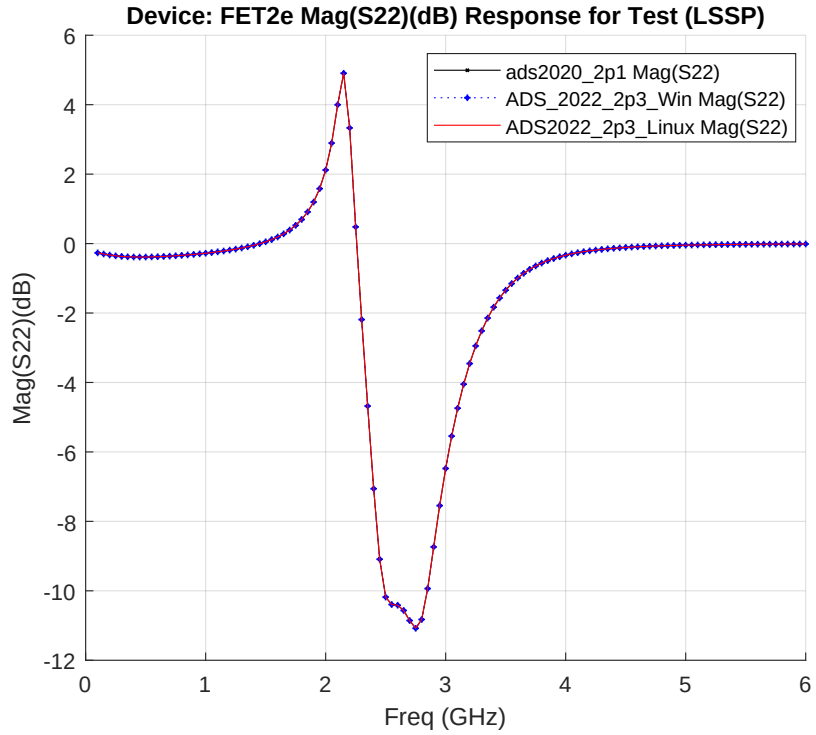


(a) Model Card FET2 LSSP S22

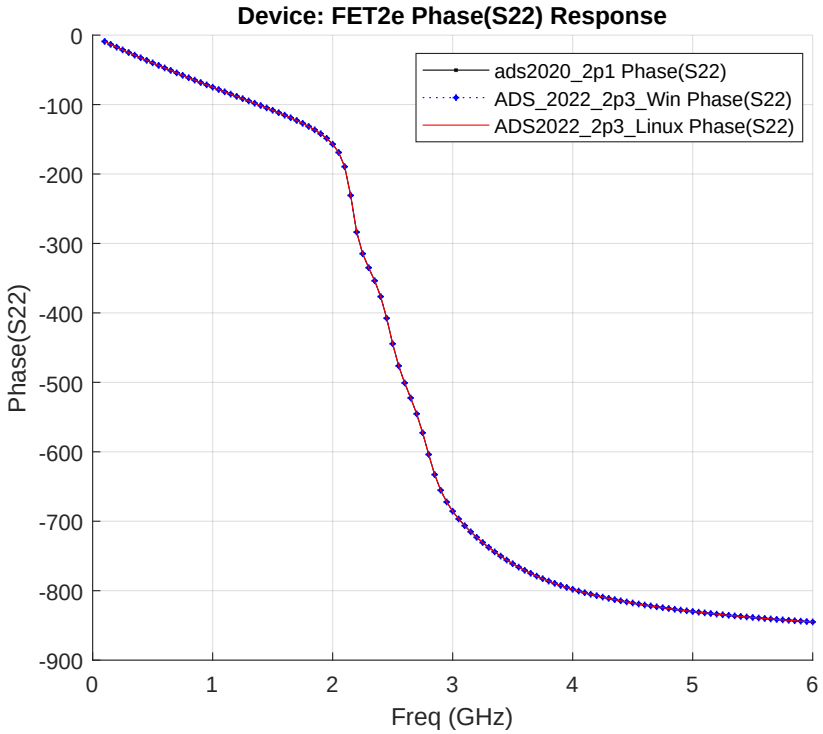


(b) Model Card FET2 LSSP S22

Fig. 1.23. FET2 LSSP Results for Mag(S22) and Phase(S22) versus Frequency

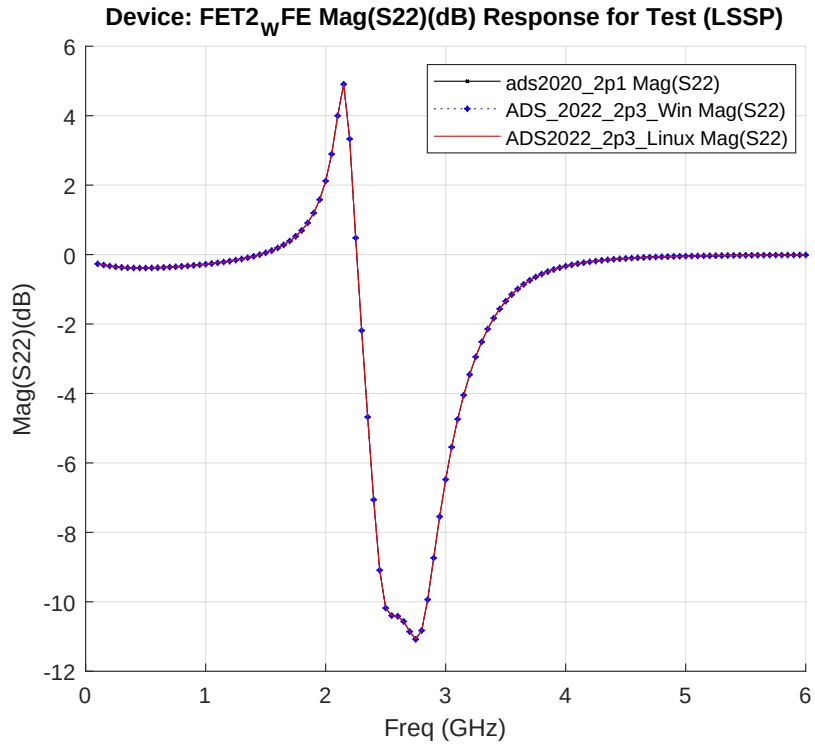


(a) Encoded FET2 LSSP S22

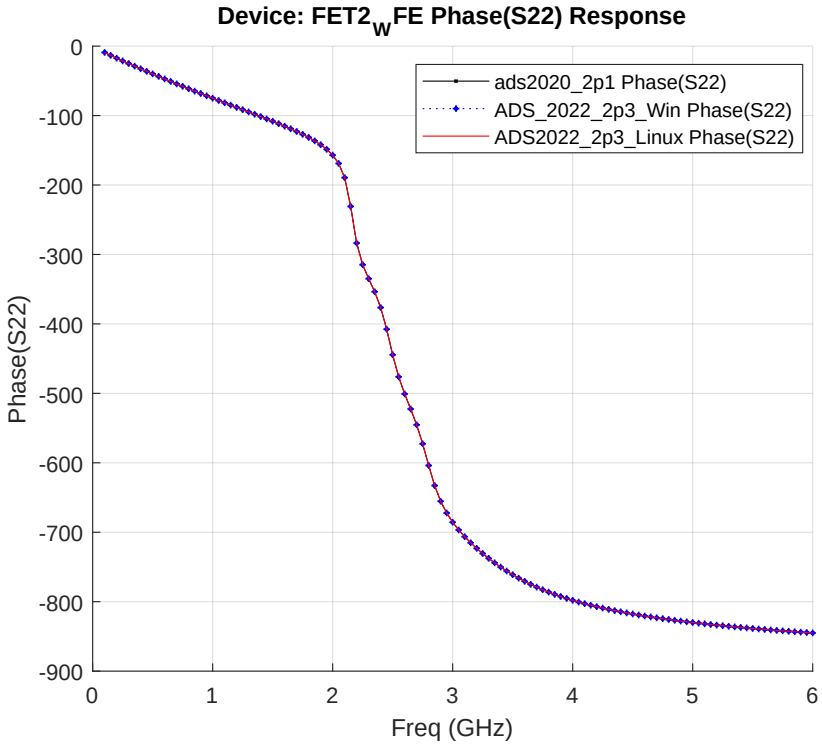


(b) Encoded FET2 LSSP S22

Fig. 1.24. FET2 LSSP Results for Mag(S22) and Phase(S22) versus Frequency



(a) Waveform Engineering FET2 LSSP S22

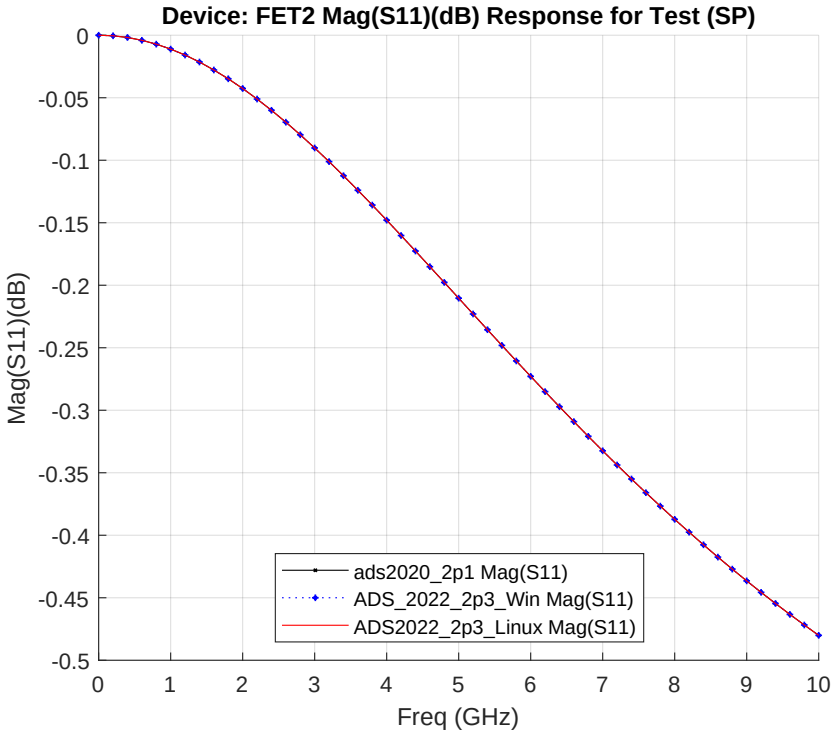


(b) Waveform Engineering FET2 LSSP S22

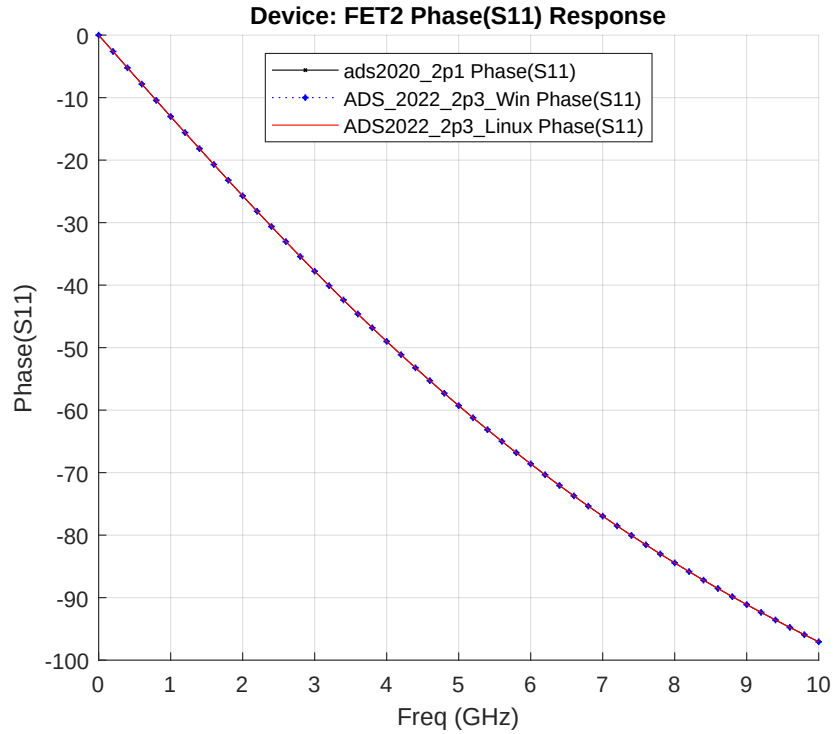
Fig. 1.25. FET2 LSSP Results for Mag(S22) and Phase(S22) versus Frequency

1.5 S-Parameters Simulation Tests

The S-parameter comparisons in the following curves were for the basic intrinsic FET2 model without matching circuitry. The characteristic impedance was modified to 5 Ohms with Vg=2.76 Volts and Vd= 28 Volts. The frequency was swept from 0 to 10 GHz every 200 MHz. The following plots are magnitude and phase of all four S-Parameters. ADS2017 and previously ADS2016 enforces passivity on the simulated 2-port S-Parameter by adjusting the S21 and S22 values at DC, 0 Hz, only. A S21 value of mag(0.0) at a phase(0.0) and the S22 value of mag(1.0) at a phase(0.0) are forced on the DC frequency.

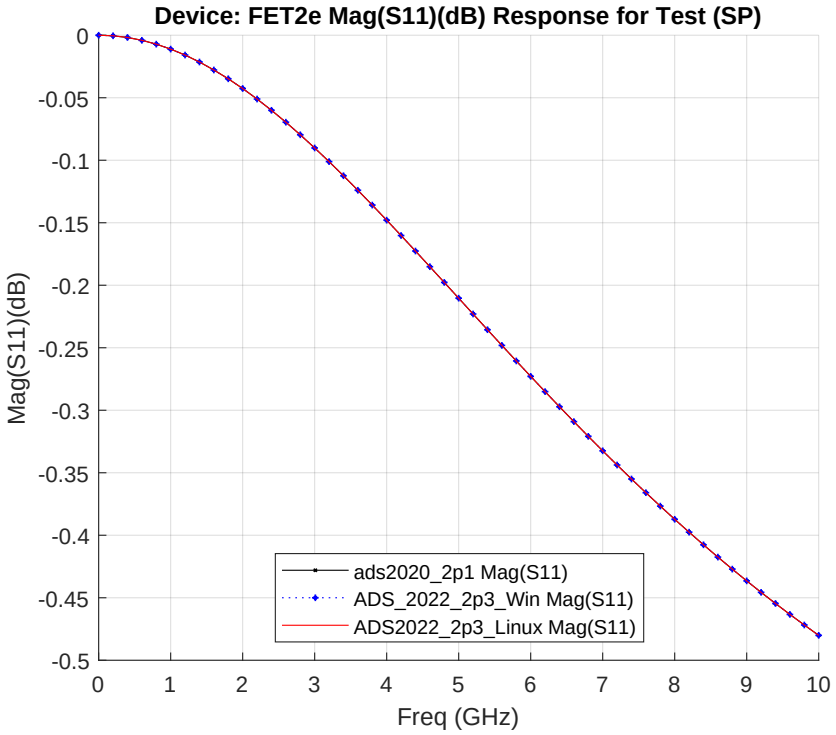


(a) Model Card FET2 SP S11

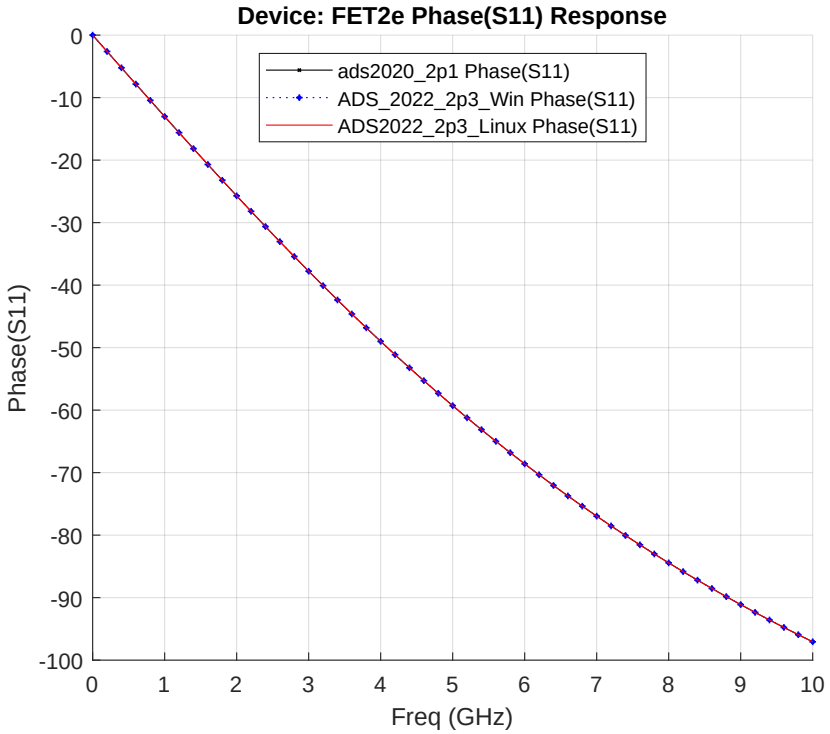


(b) Model Card FET2 SP S11

Fig. 1.26. FET2 SP Results for Mag(S11) and Phase(S11) versus Frequency

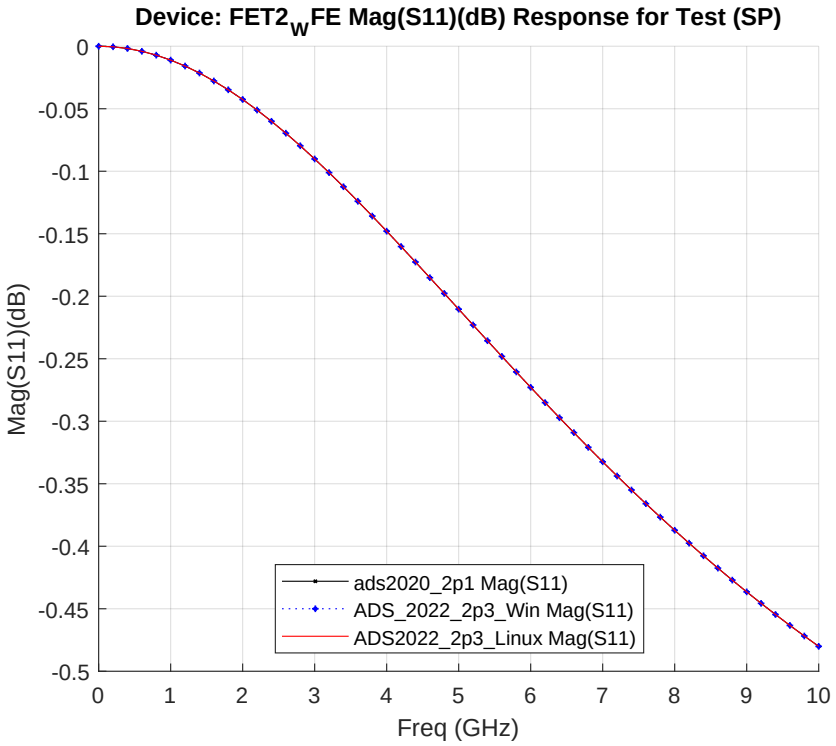


(a) Encoded FET2 SP S11

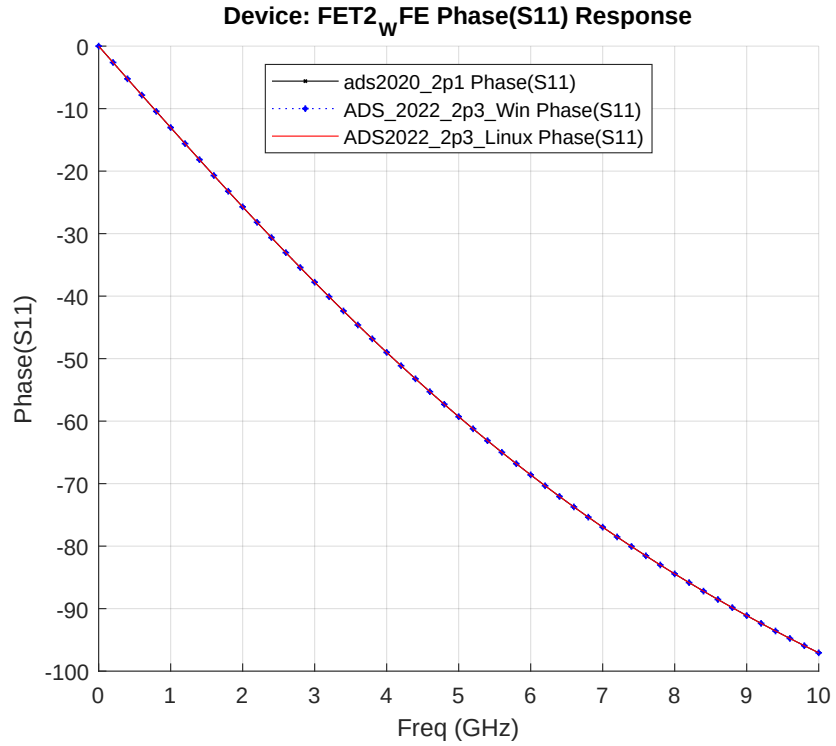


(b) Encoded FET2 SP S11

Fig. 1.27. FET2 SP Results for Mag(S11) and Phase(S11) versus Frequency

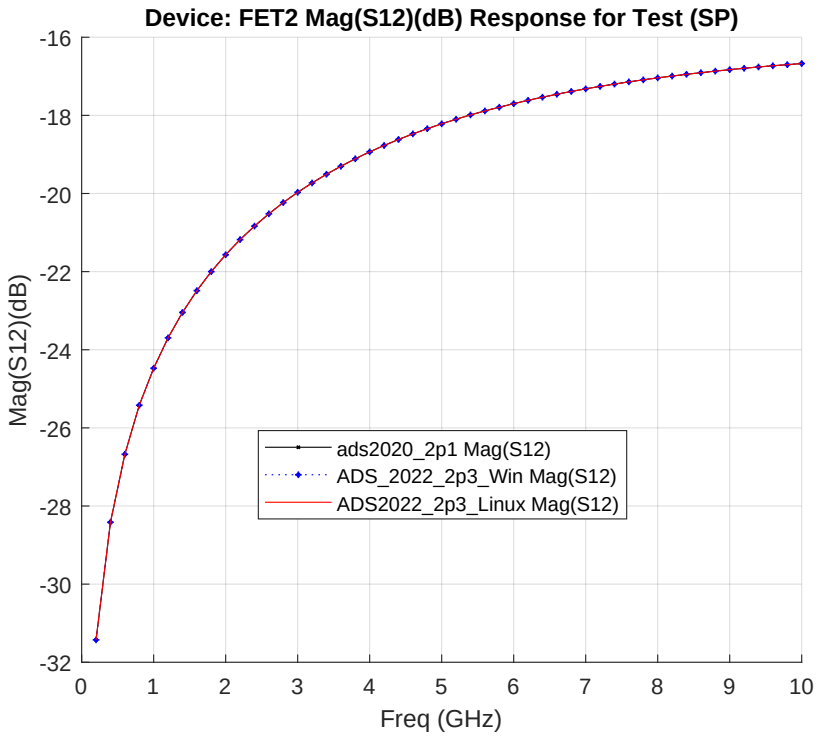


(a) Waveform Engineering FET2 SP S11

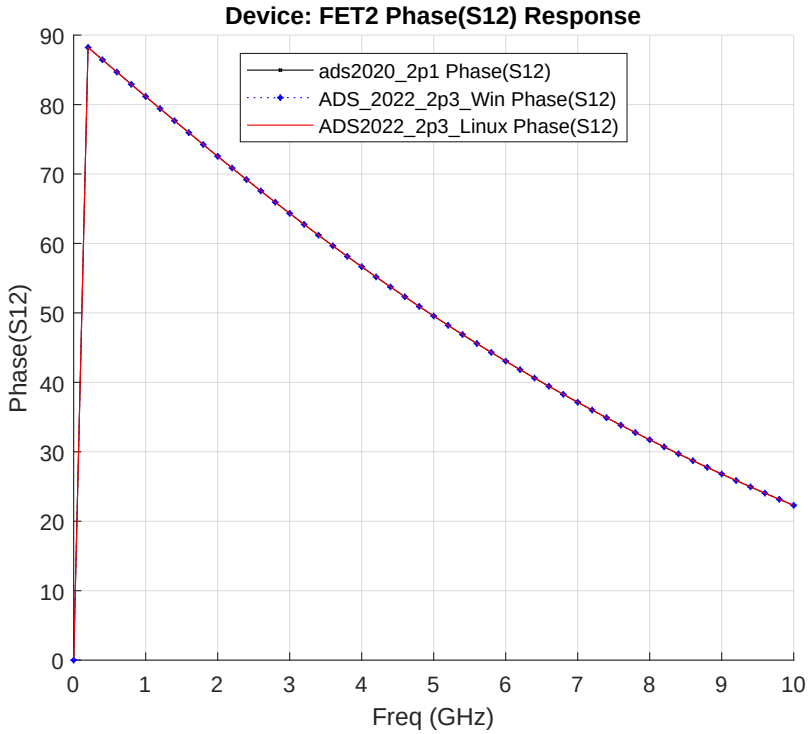


(b) Waveform Engineering FET2 SP S11

Fig. 1.28. FET2 SP Results for Mag(S11) and Phase(S11) versus Frequency

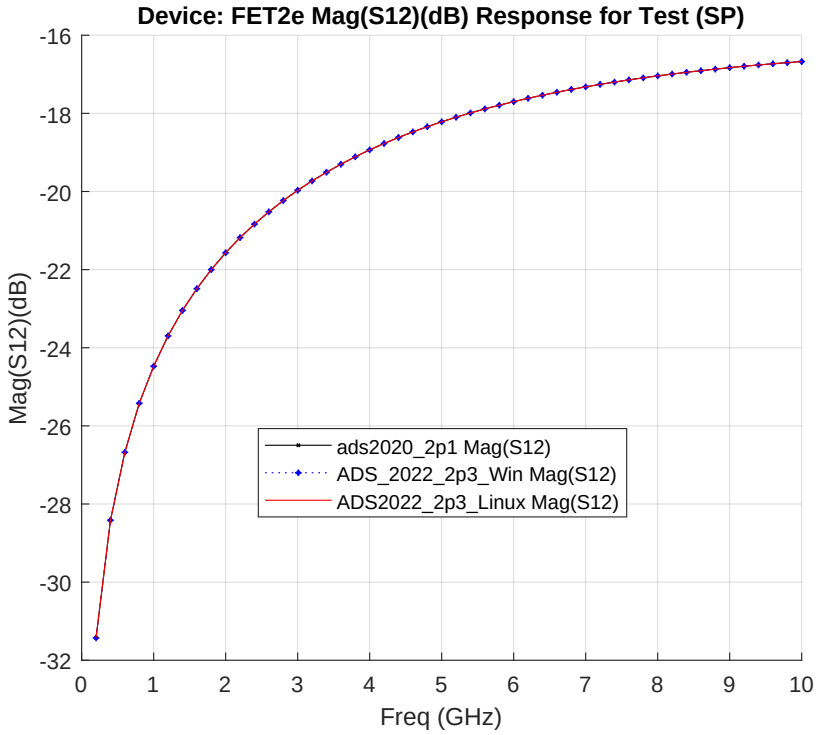


(a) Model Card FET2 SP S12

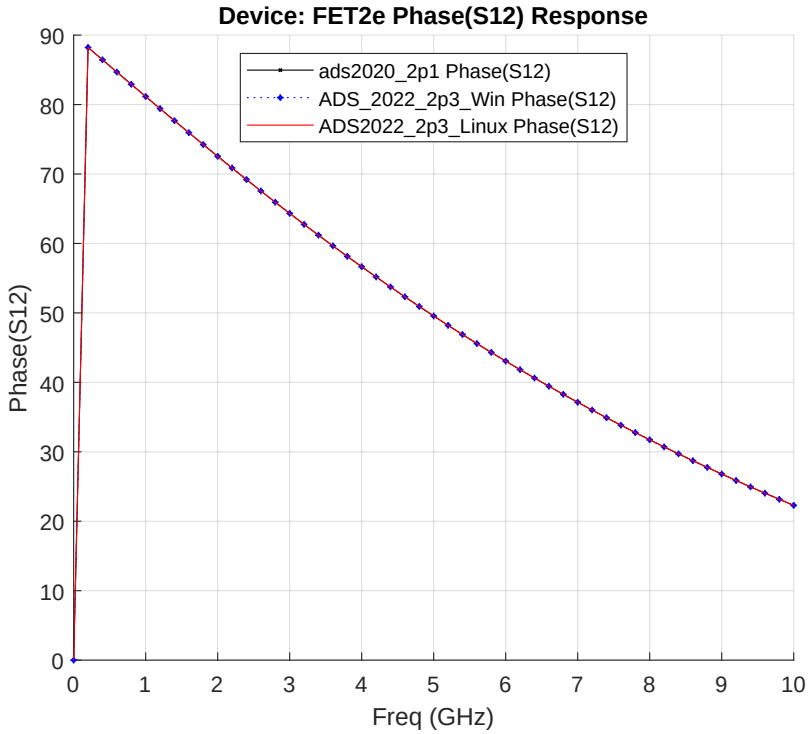


(b) Model Card FET2 SP S12

Fig. 1.29. FET2 SP Results for Mag(S12) and Phase(S12) versus Frequency

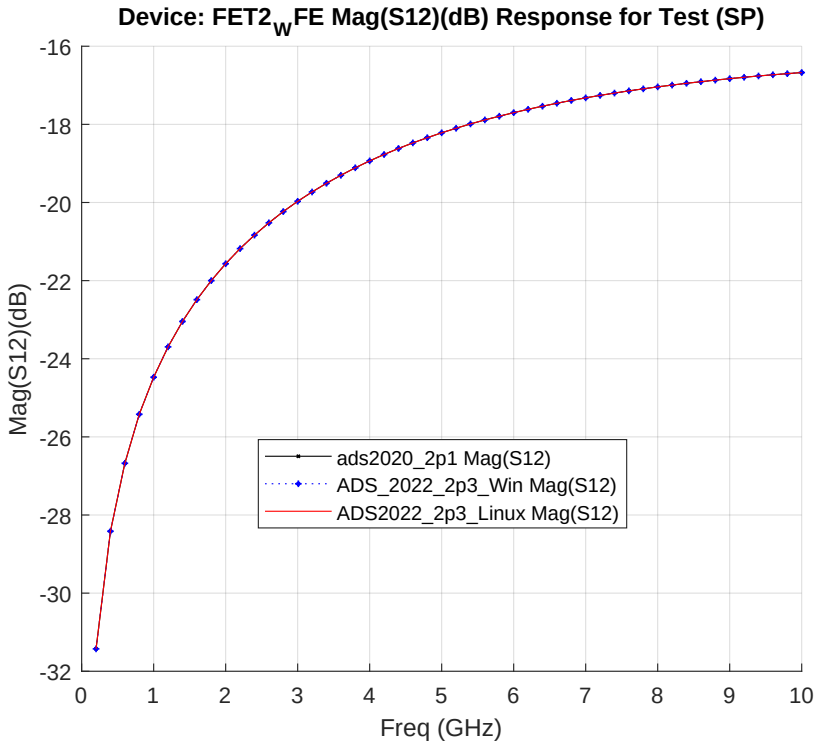


(a) Encoded FET2 SP S12

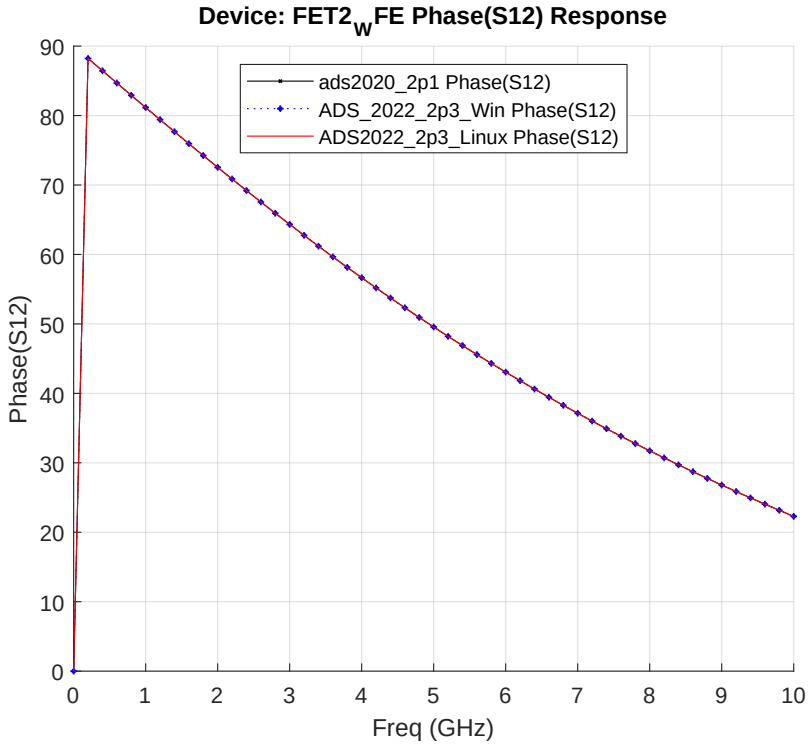


(b) Encoded FET2 SP S12

Fig. 1.30. FET2 SP Results for Mag(S12) and Phase(S12) versus Frequency

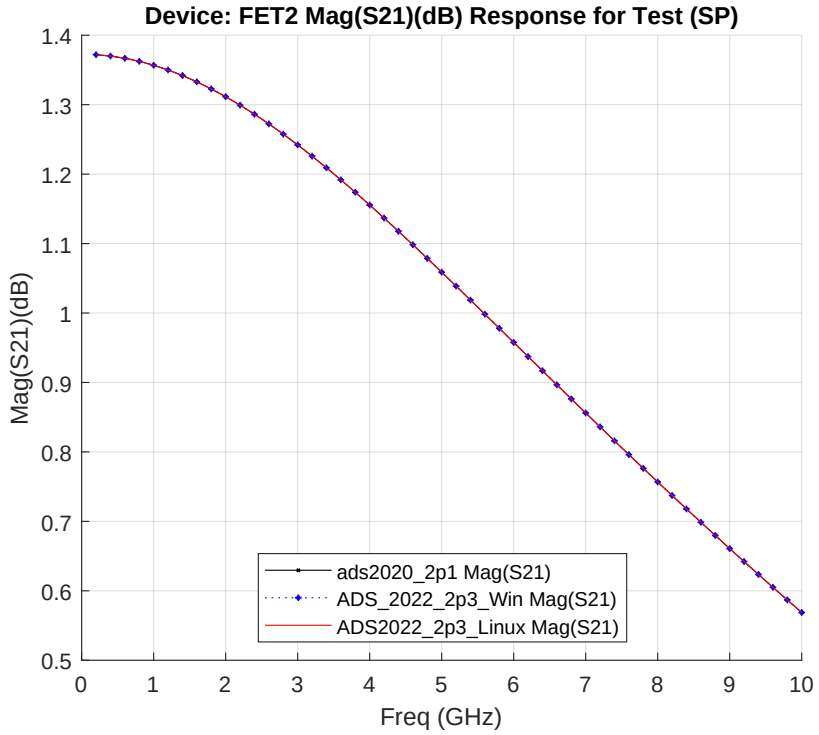


(a) Waveform Engineering FET2 SP S12

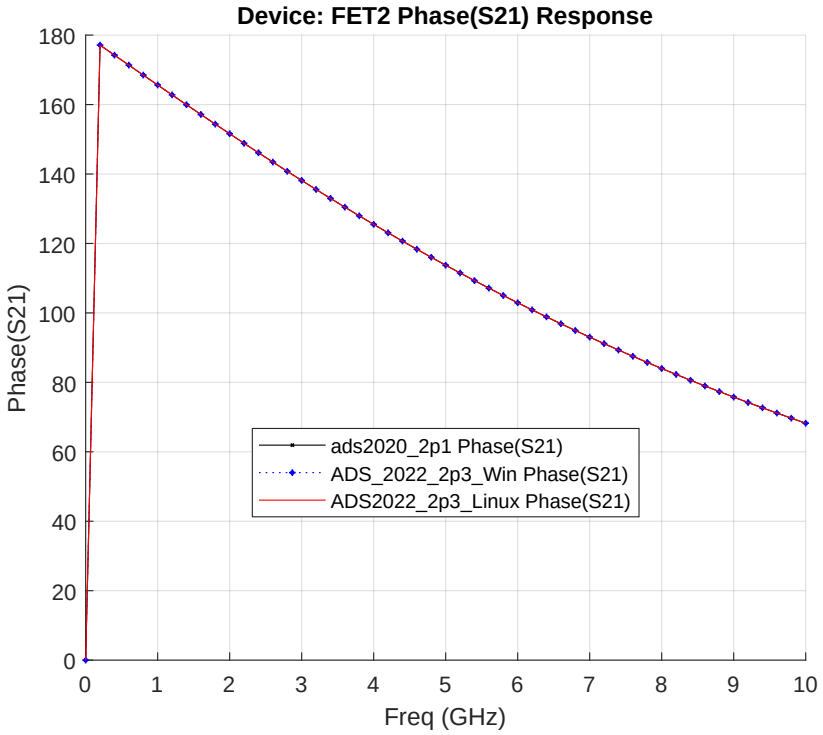


(b) Waveform Engineering FET2 SP S12

Fig. 1.31. FET2 SP Results for Mag(S12) and Phase(S12) versus Frequency

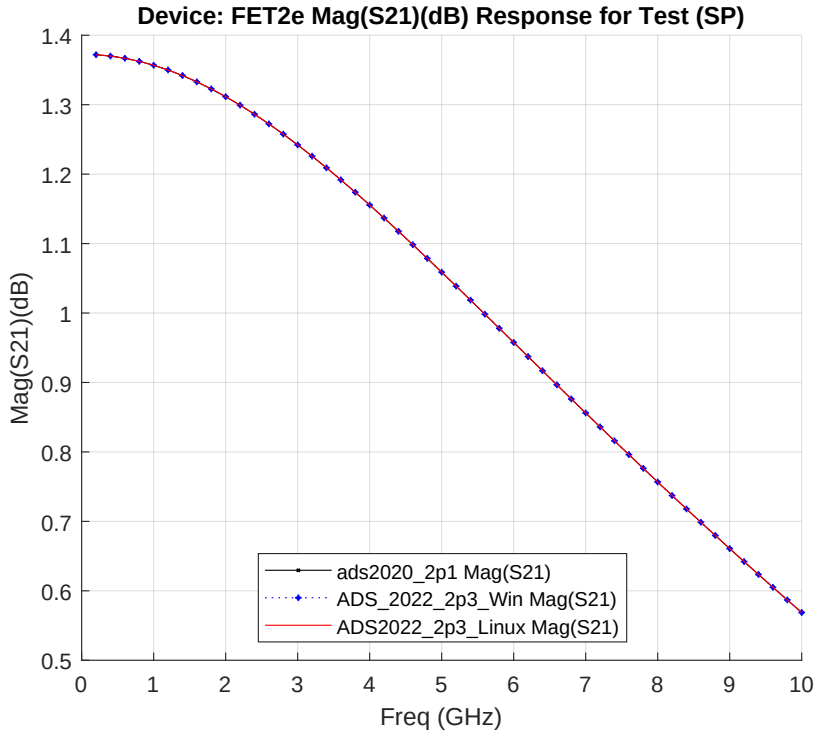


(a) Model Card FET2 SP S21

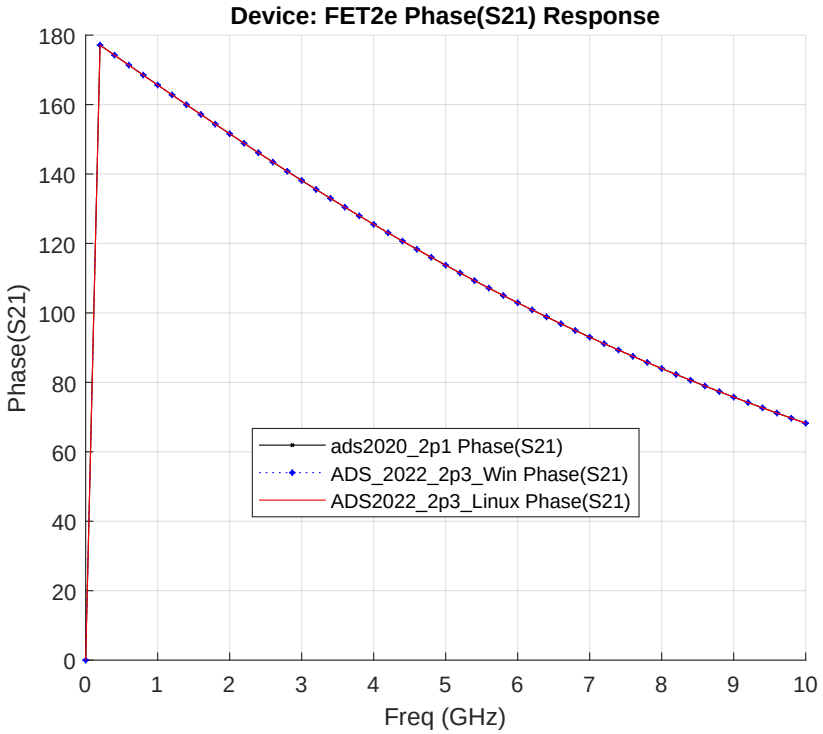


(b) Model Card FET2 SP S21

Fig. 1.32. FET2 SP Results for Mag(S21) and Phase(S21) versus Frequency

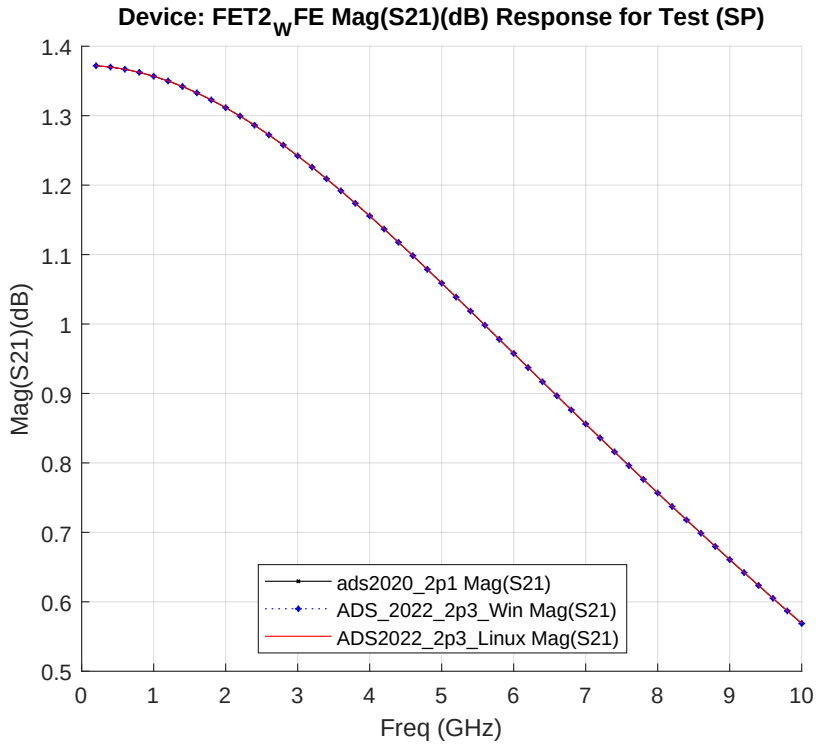


(a) Encoded FET2 SP S21

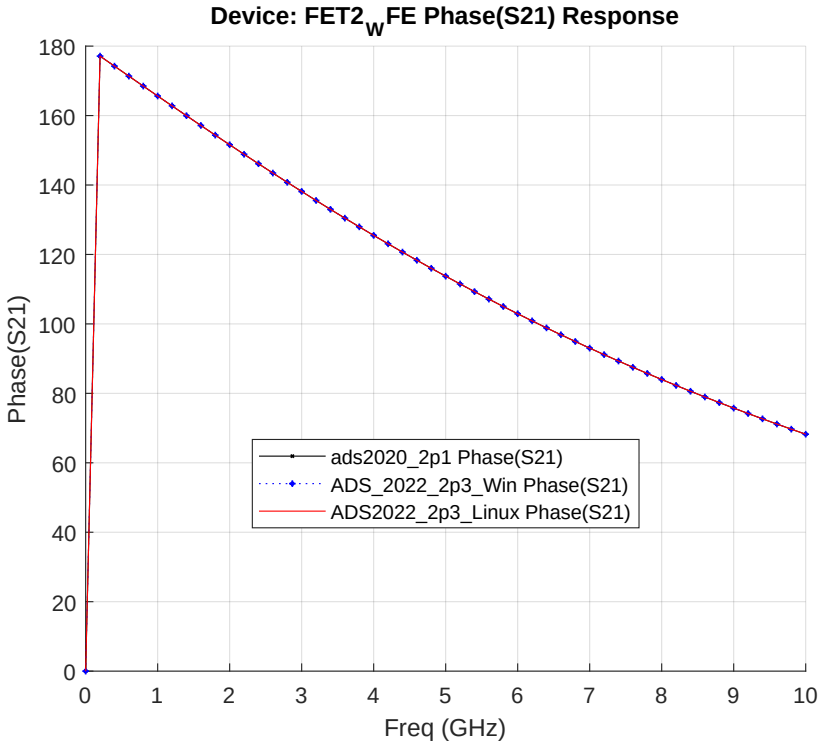


(b) Encoded FET2 SP S21

Fig. 1.33. FET2 SP Results for Mag(S21) and Phase(S21) versus Frequency

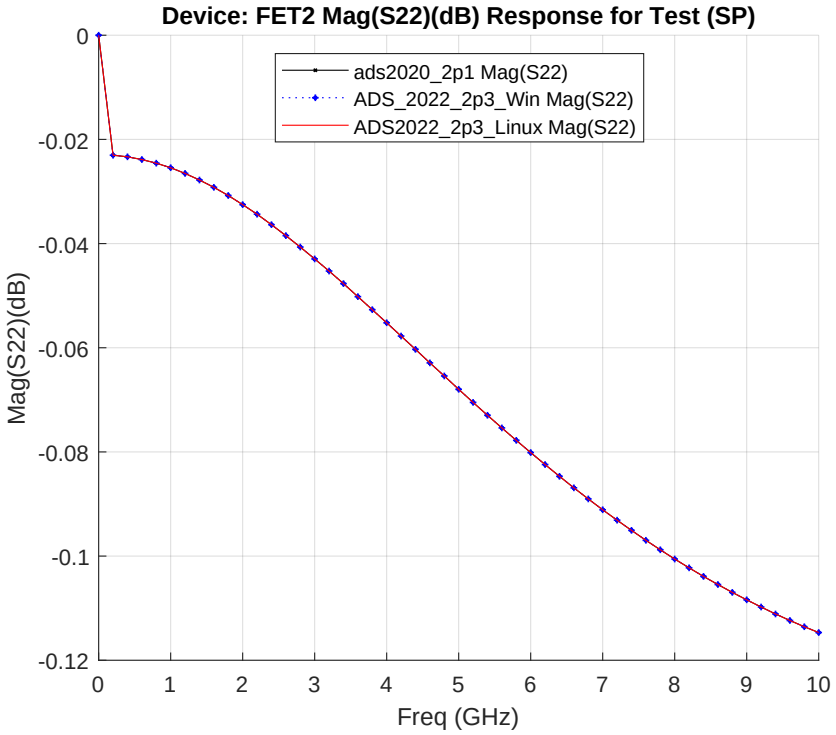


(a) Waveform Engineering FET2 SP S21

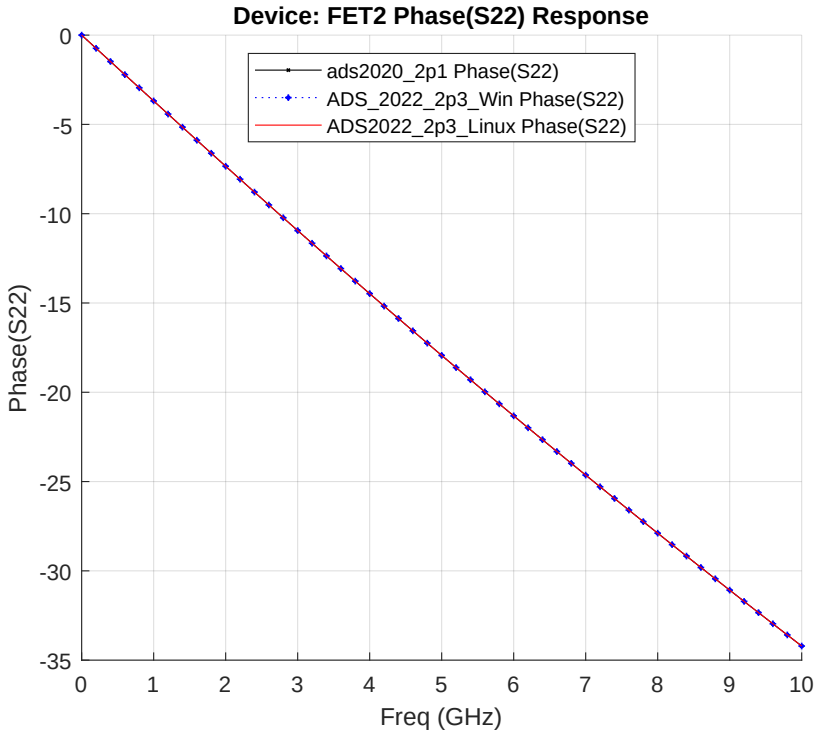


(b) Waveform Engineering FET2 SP S21

Fig. 1.34. FET2 SP Results for Mag(S21) and Phase(S21) versus Frequency

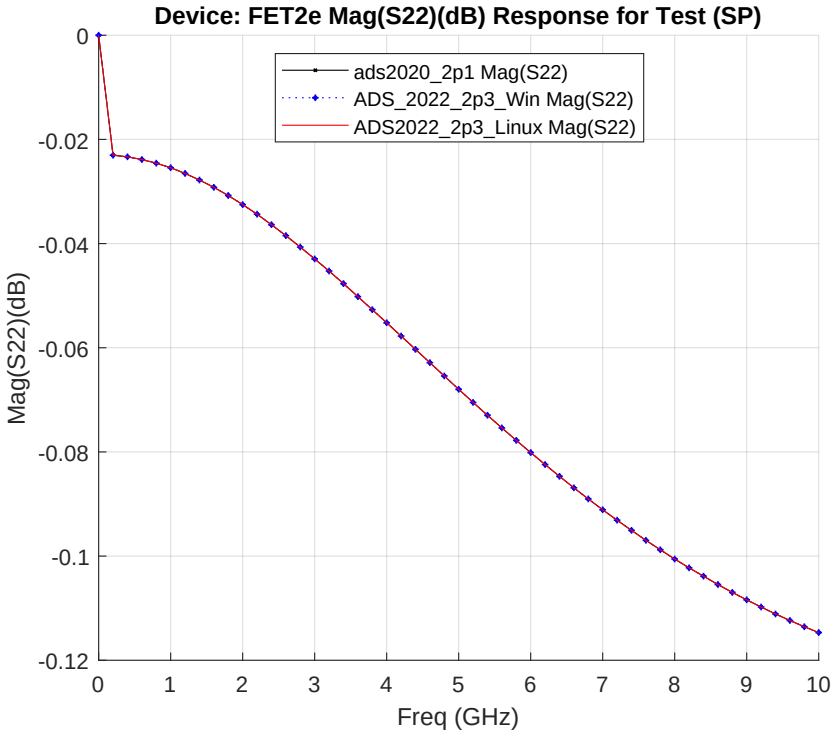


(a) Model Card FET2 SP S22

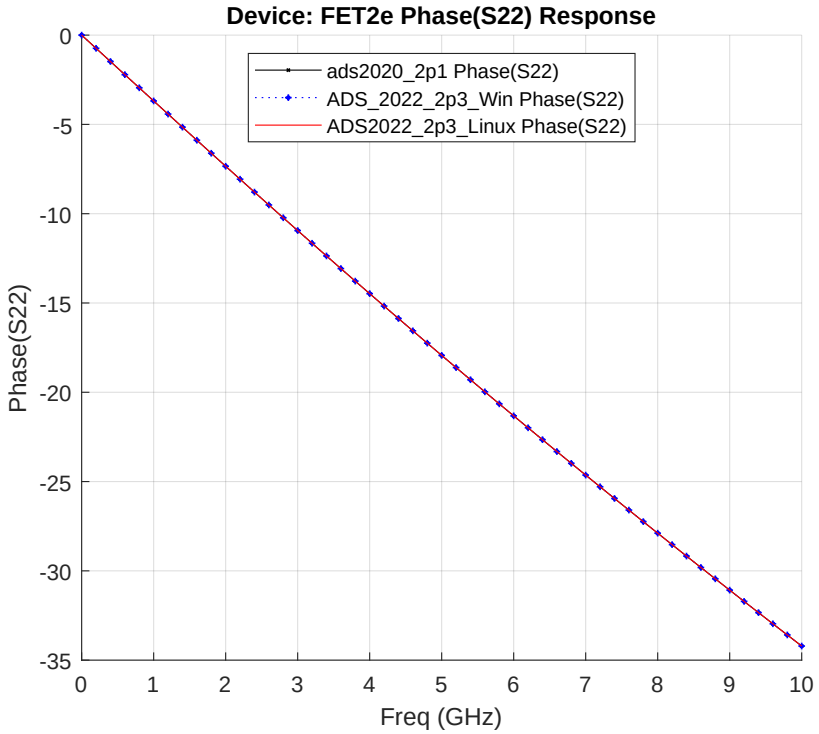


(b) Model Card FET2 SP S22

Fig. 1.35. FET2 SP Results for Mag(S22) and Phase(S22) versus Frequency

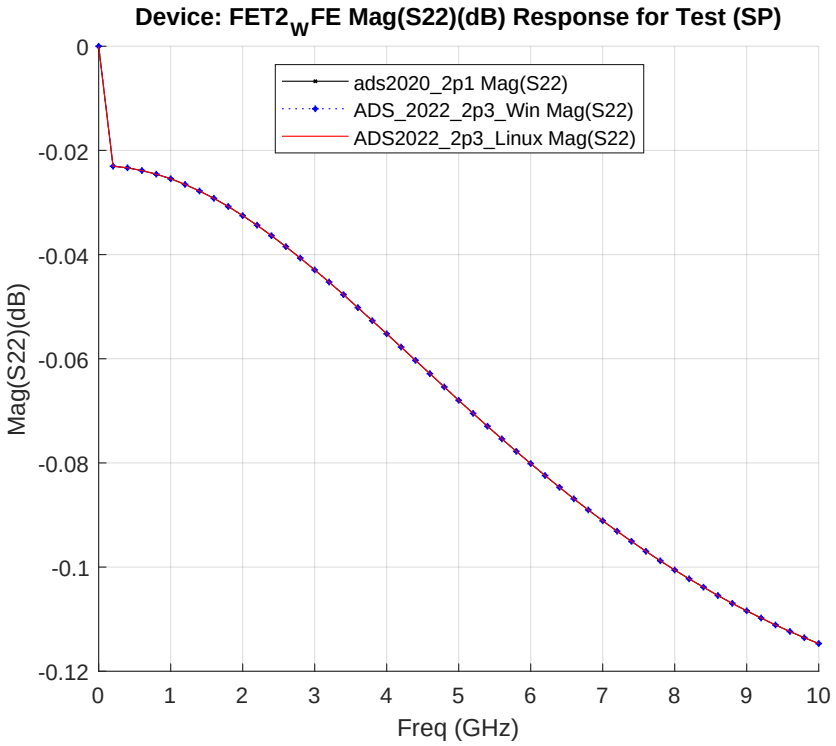


(a) Encoded FET2 SP S22

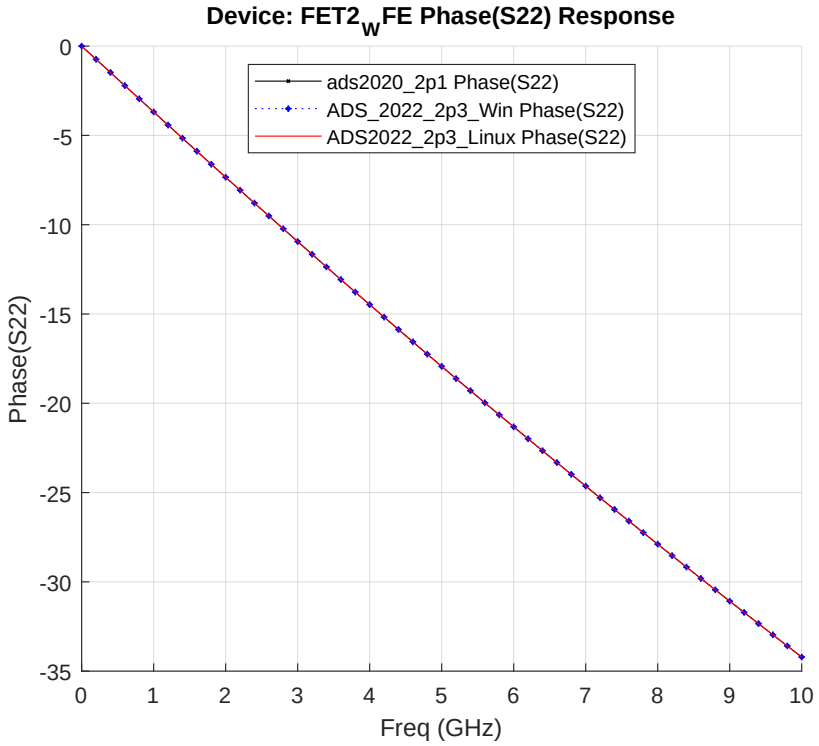


(b) Encoded FET2 SP S22

Fig. 1.36. FET2 SP Results for Mag(S22) and Phase(S22) versus Frequency



(a) Waveform Engineering FET2 SP S22

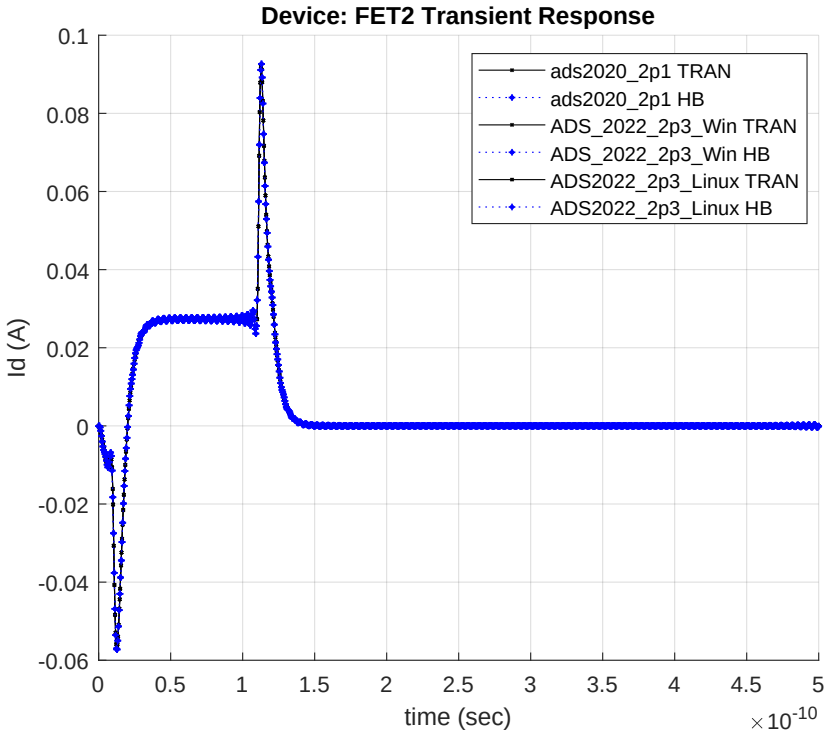


(b) Waveform Engineering FET2 SP S22

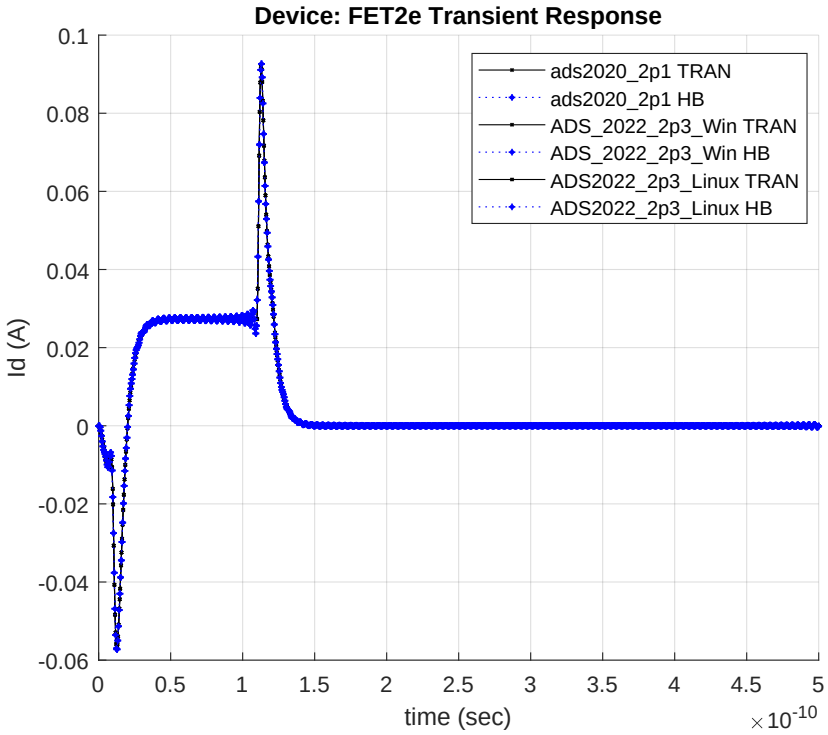
Fig. 1.37. Waveform Engineering FET2 SP Results for Mag(S22) and Phase(S22) versus Frequency

1.6 Transient Simulation Tests

The Transient test bench actually has two simulations within it, a transient simulation and a harmonic balance simulation. The gate bias voltage Vg= 2.76 Volts, drain voltage Vd=28 Volts with a characteristic impedance of 5 Ohms. For the transient simulation, a voltage pulse signal is applied to the input at the fundamental frequency of 2 GHz with a width of 100 picoseconds, a rise time of 10 picoseconds and a fall time of 10 picoseconds. The time is swept from 0 to 0.5 nanoseconds with a maximum time step of 0.5 picoseconds and a fundamental order of 32. The harmonic balance simulation uses the same test setup as the transient simulation except the fundamental order which is 128. Both curves shown are of the drain current versus time going into the device. The curve from the harmonic balance simulation is generated by using the time series function to get the drain current versus time.

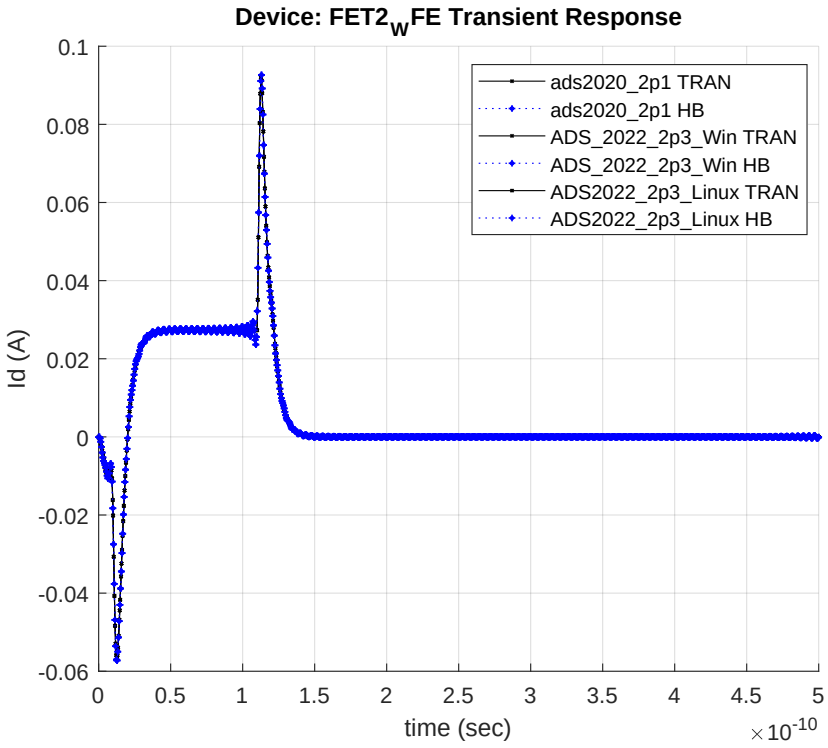


(a) Model Card FET2 Transient



(b) Encoded FET2 Transient

Fig. 1.38. Transient Results of pulsed Drain Current versus Time



(a) Waveform Engineering FET2 Transient

Fig. 1.39. Transient Results of pulsed Drain Current versus Time

1.7 Conclusion

The models are new for ADS 2022 and show excellent agreement with the previous models. The LDMOS and GaN model implementations within the ADS2022 RF Power Kit 2.3 are ready for use.