MAJOR PROJECT REPORT

On

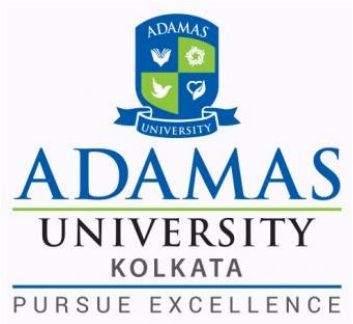
"Development of high resolution Brain generated Event Related potential recorder (B-Cap)"

Submitted in partial fulfilment of the requirements for the award of

Bachelor of Technology (B.Tech)

In the department of

Computer Science & Engineering



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School of Engineering & Technology

ADAMAS University, Kolkata, West Bengal

Jan 2024 – June 2024

CERTIFICATE

This is to certify that the project report entitled ***"Development of high resolution Brain generated Event Related potential recorder (B-Cap)"*** submitted to the School of Engineering & Technology (SOET), **ADAMAS UNIVERSITY, KOLKATA** in partial fulfilment for the completion of **Semester – 8th** of the degree of **Bachelor of Technology** in the department of **Computer Science & Engineering**, is a record of bonafide work carried out by **Dron Guin**, **UG/02/BTCSEAIML/2020/005** under our guidance.

All help received by us from various sources have been duly acknowledged.

No part of this report has been submitted elsewhere for award of any other degree.

_____

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ACKNOWLEDGEMENT

The satisfaction and euphoria that accompany the successful completion of any task would be incomplete without the mentioning of the people whose constant guidance and encouragement made it possible. I take pleasure in presenting before you, my project, which is the result of a studied blend of both research and knowledge.

I express my earnest gratitude to **Prof. (Dr.) Sajal Saha, Professor, Dept. of CSE, Adamas University, Kolkata, as Principal Investigator and Dr. Nisarga Chand, Assistant Professor, ECE, Adamas University, Mr. Uttam Basak, Technical Assistant, ECE, Adamas University, Mr. Sauren Sarkar, Technical Assistant, ECE, Adamas University** for their constant support, and also I am grateful to **, Uttio Das Sharma (ECE Student, Semester-6), Amit Mourya (CSE Student, Semester-4) and Riyaz Alam (ECE Student, Semester-4)** for their companionship and valuable efforts.

Finally, I express my gratitude to all other members who are involved either directly or indirectly for the completion of this project.

_____

Dron Guin

(UG/02/BTCSEAIML/2020/005)

DECLARATION

I, the undersigned, declare that the project entitled ‘Development of high resolution Brain generated Event Related potential recorder (B-Cap)’, being submitted in partial fulfillment for the award of Bachelor of Engineering Degree in Computer Science & Engineering, affiliated to ADAMAS University, is the work carried out by me.

_____

Dron Guin

(UG/02/BTCSEAIML/2020/005)

ABSTRACT

In recent years the Brain Computer Interface (BCI) is one of the emerging technologies in the whole world. To adapt with new BCI technology, we have to understand the development of miniaturized sensors and efficient signal processing schemes in the world of Nano-technology. To fulfill this, there is a requirement to develop High Resolution Brain generated Event Related Potential Recorder. The uniqueness of our concept is to miniaturize the brain electrodes (ERP sensors) and develop the efficient hardware architecture (Universal Multiplexer or U-MUX) for recording very high-resolution data. The major areas of applications of this project are in health care sectors, defense areas, human computer interaction (HCI) etc.

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Chapter 1: INTRODUCTION

1.1 Background and Motivation:

In recent years, the convergence of neuroscience and technology has propelled the field of Brain-Computer Interface (BCI) research into uncharted territories, offering unprecedented possibilities for human-computer interaction and healthcare applications. The fundamental premise of BCI technology lies in its ability to decode and interpret intricate neural signals, enabling seamless communication between the human brain and computing systems. As we delve into this dynamic realm, a critical challenge emerges – the acquisition of high-resolution electroencephalography (EEG) data, a cornerstone for decoding the complexities of neural activity with precision.

Traditional EEG systems, while revolutionary in their own right, grapple with inherent limitations, particularly concerning the number of channels and spatial resolution. Electrode placement constraints, coupled with cost considerations, have prompted the exploration of novel solutions to enhance the capabilities of BCI systems. Against this backdrop, our research embarks on a transformative journey, with a distinct focus on the design and implementation of a Universal Multiplexer (U-MUX).

The U-MUX serves as the linchpin in our quest to acquire significantly large amounts of analog brain wave data through a singular channel. This strategic approach not only addresses cost concerns but also unlocks the potential for ultra-high-resolution EEG data acquisition. The impetus for this research is grounded in the imperative to surmount the limitations of existing EEG systems, particularly in terms of channel count and spatial resolution.

Recent strides in BCI technology, exemplified by Fiedler et al.'s work [1], showcase innovations in high-density EEG caps with dry multi-pin electrodes. This pioneering effort underscores the urgency of pushing the boundaries of conventional EEG technology. In parallel, patents such as the one by Dvorak and Fenton [2], introducing a high-density EEG system tailored for precision psychiatry, accentuate the diversity of applications and potentials inherent in cutting-edge BCI technologies.

Despite these advancements, fundamental questions persist in the field. The optimal configuration of electrodes, the impact of electrode density, and the achievable resolution under

diverse conditions of measurement noise demand meticulous exploration. Ryynanen et al.'s foundational study [3] offers critical insights into the effect of electrode density and measurement noise on the spatial resolution of cortical potential distribution. This study, while dating back to 2004, remains pertinent in shaping our understanding of these crucial parameters.

Our research, therefore, stands at the intersection of these critical considerations. By focusing on the development and optimization of the U-MUX, our objective is to pioneer a scalable, cost-effective solution that not only advances the spatial resolution and channel capacity of BCI systems but also addresses long-standing questions regarding electrode configuration and measurement noise impact.

This interdisciplinary endeavor aligns with the evolving trajectory of neuro-technology research and positions our work at the forefront of transformative advancements in understanding and harnessing human neural activity. As we navigate the uncharted territories of BCI technology, our research endeavors to contribute not only to the theoretical underpinnings of neuro-technology but also to the practical development of systems that hold promise for real-world applications, ultimately shaping the future landscape of human-computer interaction.

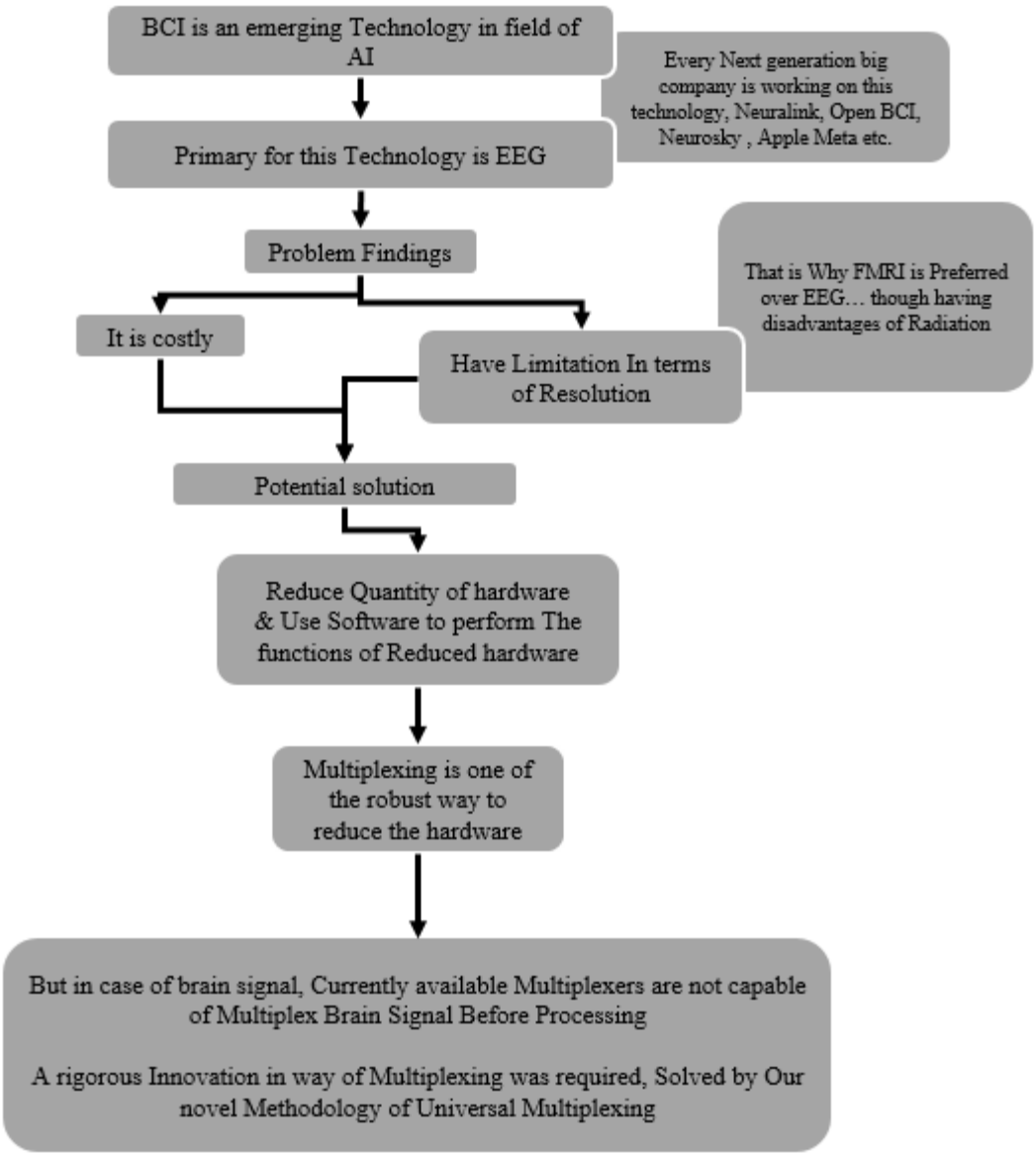


Fig 1.1: Motivation of the project

1.2 Purpose of the Project:

The primary objective of the Project Week application is to augment the data acquisition capabilities of existing PCI (Peripheral Component Interconnect) technology. This enhancement aims to provide the artificial intelligence embedded within Brain-Computer Interface (BCI) technology with a more diverse dataset. The ultimate goal is to improve the accuracy of predicting thought processes. As of the present moment, the resolution of EEG (Electroencephalography) technology employed in BCI is constrained by the limited number of sensors in use.

To overcome this limitation and acquire higher-resolution data, the project necessitates the development of a novel hardware configuration, encompassing both design and operation aspects. Our principal model comprises two innovative technologies: Universal Multiplexer (U-MUX) and Mesh Sensor Technology (MST). Together, these advancements establish the micro-level infrastructure necessary for the implementation of advanced EEG techniques. While employing a substantial number of sensors introduces various challenges, our ongoing research endeavors to address and overcome these obstacles.

This research is inherently challenging, given the complexities associated with utilizing a large number of sensors. Our commitment is unwavering as we strive to achieve the desired outcome of enhancing machine understanding of human thoughts with increased precision.

1.3 Problem Statement:

The overarching challenge is to advance the capabilities of Brain-Computer Interface (BCI) technology by addressing issues related to limited Electroencephalography (EEG) resolution, intricacies in designing and operating a hardware configuration with an increased sensor count, seamless integration of Universal Multiplexer (U-MUX) and Mesh Sensor Technology (MST), effective management of high sensor count challenges, and the enhancement of predictive accuracy in understanding human thoughts. This multifaceted problem necessitates innovative solutions to optimize data acquisition, signal processing, and overall system reliability in the pursuit of achieving a more sophisticated and accurate BCI system.

1.4 Objective:

- **EEG Resolution Enhancement:** Elevate BCI technology by overcoming EEG resolution limitations, addressing constraints for diverse and accurate data crucial for AI processing in the BCI framework.
- **Advanced Hardware for Increased Sensors:** Design a novel hardware configuration supporting a higher sensor count, integrating key technologies – the Universal Multiplexer (U-MUX) and Mesh Sensor Technology (MST) – essential for sophisticated EEG techniques in the BCI framework.
- **Practical Sensor Management:** Tackle challenges in managing a high sensor count, addressing issues in data management, signal processing, and system reliability inherent in extensive sensor use.
- **BCI System Optimization:** Optimize the BCI system for enhanced predictive accuracy in deciphering human thoughts, striking a balance between sensor abundance and prediction precision through innovative solutions.

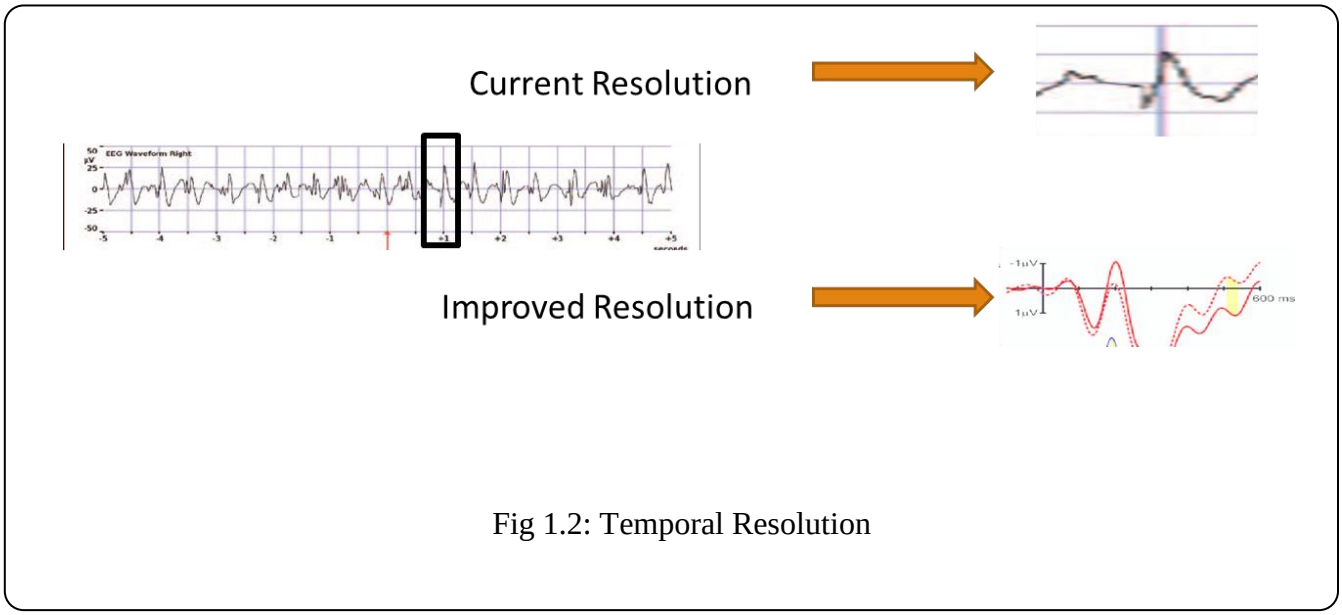


Fig 1.2: Temporal Resolution

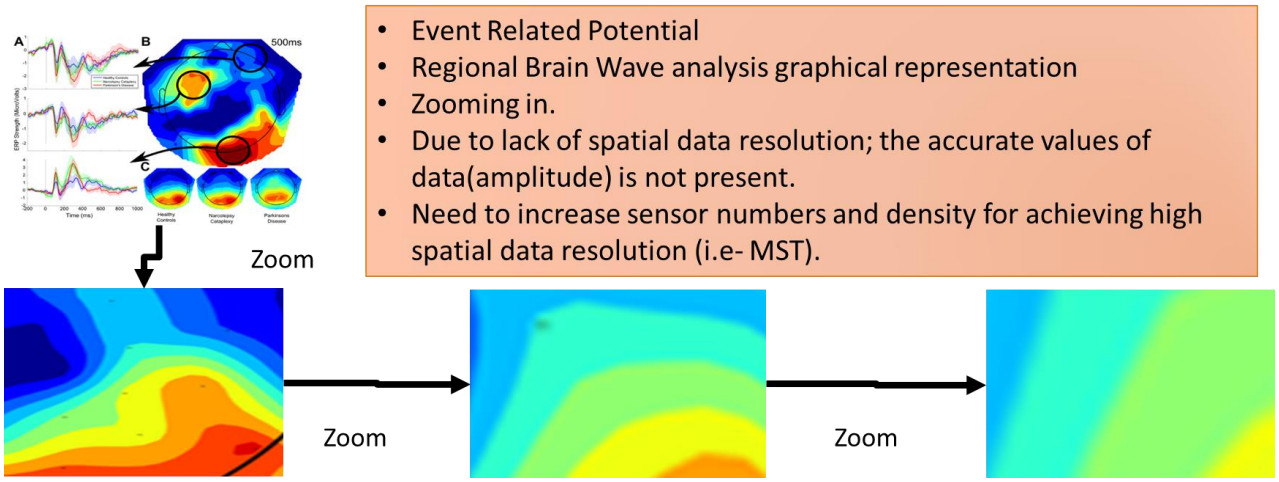


Fig 1.3: Spatial Resolution

1.5 Structure of the project

Phase	Task	Duration
Preparation and Research	Define Project Scope and Objectives	July 2022 - September 2022
	Literature Review	August 2022 - October 2023
Hardware Development	Universal Multiplexer Construction	October 2022 - August 2023
System Integration	BCI System Integration	January 2024 - March 2024
Optimization and Testing	Incremental Probe Addition	May 2024 - July 2024
	Ergonomic Hardware Design	May 2024 - July 2024
	Efficient Brain Data Processing	January 2024 - August 2024
	Noise Reduction Strategies Implementation	April 2024 - June 2024
	Signal Extraction Techniques Implementation	April 2024 - June 2024
Algorithm and Model Development	AIML Model Development	January 2024 - October 2024

Intellectual Property and Strategy	Copyrighting and Patenting	March 2024 - June 2024
Establishment of Start-up	Start-up Establishment	October 2023 - May 2024

Table 1.1: Structure of the project

Chapter 2: LITERATURE REVIEW

The landscape of Brain-Computer Interface (BCI) technology has witnessed significant advancements, particularly in the realm of high-density electroencephalography (HD-EEG). This literature review provides an extensive examination of recent studies, each contributing unique insights into the development and challenges associated with HD-EEG technology. The selected papers not only showcase innovative approaches but also shed light on critical considerations for enhancing the resolution, precision, and practicality of BCI systems.

Fiedler et al. (2022) [1] present a pioneering study introducing a novel 256-channel cap equipped with dry multi-pin electrodes designed explicitly for HD-EEG applications. The primary objective of the research is to evaluate the performance of this dry EEG cap concerning traditional gel-based caps. The study methodically compares electrode-skin impedances, resting-state EEG, and visual evoked potentials (VEP) in a cohort of 30 volunteers.

The findings of this study are particularly relevant to our research objective, as they directly address the challenges associated with limited EEG resolution. The dry EEG cap demonstrated average impedances below 900 kΩ for 252 out of 256 dry electrodes, a crucial feature enabling compatibility with state-of-the-art EEG amplifiers. Furthermore, the study reports an impressive 84% channel reliability and a substantial 69% reduction in preparation time with the dry EEG cap. These results underscore the potential for significantly enhancing the efficiency and practicality of BCI systems by leveraging advancements in electrode technology.

This study's implications for our research lie in its exploration of wearable, high-density EEG systems, aligning with our objective to develop an advanced BCI system. Additionally, the evaluation of impedance, resting-state EEG, and VEP provides a holistic understanding of the dry EEG cap's performance, informing our approach to data acquisition and signal processing.

Dvorak and Fenton (2023) [2]: Dvorak and Fenton introduce a novel EEG system designed explicitly for precision psychiatry, incorporating a wearable cap with EEG electrodes and a sophisticated mechanism for dynamic adjustment. The study delves into the system's design, functionalities, and potential applications in psychiatry. A key feature of this system is the integration of linear actuators within the cap, allowing for size adjustments and movement of EEG electrodes.

This patent holds significant relevance to our research, particularly in the context of exploring innovative approaches to EEG system design. The incorporation of linear actuators addresses challenges related to electrode placement and adaptability, aligning with our objective of enhancing the BCI system's precision and adaptability. The neurofeedback mechanism presented in the study is also noteworthy, as it introduces a potential avenue for real-time interaction with the user based on detected abnormal brain activity.

The innovative aspects of this EEG system align with our goal of advancing BCI technology, specifically in the context of precision psychiatry. Understanding the capabilities and functionalities of such systems is crucial for informing the design and integration of advanced features into our proposed BCI system.

Ryynanen et al. (2004) [3] delve into the intricacies of electroencephalography (EEG) spatial resolution by employing an inverse cortical EEG solution. The study utilizes a three-layer spherical head model to explore the source-field relationship of cortical potentials and scalp EEG fields. The primary focus is on evaluating spatial resolution under varying conditions of measurement noise.

While this study predates the previously mentioned papers, its relevance remains paramount. The investigation into electrode density and its impact on spatial resolution provides fundamental insights that are critical for our research. The study reveals that as measurement noise increases, the advantage of dense electrode systems diminishes. This underscores the importance of carefully considering electrode density in our proposed BCI system design.

The findings of Ryynanen et al. hold implications for optimizing the spatial resolution of our BCI system, aligning with our objective of achieving higher accuracy in understanding human thoughts. Understanding the impact of measurement noise and electrode spacing on spatial resolution is essential for informing decisions regarding the configuration and placement of electrodes in our system.

The study by Fiedler et al. [4] provides crucial insights into the development of a high-density EEG cap with dry multi-pin electrodes. The comparison with traditional gel-based caps and the reported improvements in channel reliability and preparation time reduction make this paper a cornerstone in our exploration of advanced EEG technologies.

Dvorak and Fenton's [5] patent introduces a unique EEG system designed for precision psychiatry, incorporating a wearable cap with dynamic adjustments through linear actuators. The innovative design and neurofeedback mechanism contribute valuable perspectives to our research, guiding the exploration of advanced features for real-time interaction and adaptability in our proposed BCI system.

Ryynanen et al.'s [6] study, though dating back to 2004, remains foundational in understanding the impact of electrode density and measurement noise on spatial resolution. The insights gained from this investigation are crucial for informing decisions regarding the optimal configuration and placement of electrodes in our BCI system, aligning with our objective of achieving higher spatial resolution.

The synthesis of these three key studies offers a comprehensive understanding of recent advancements in high-density electroencephalography (HD-EEG) technology. The integration of innovative designs, such as the 256-channel cap with dry multi-pin electrodes and the precision psychiatry EEG system, coupled with fundamental insights into spatial resolution considerations, sets the stage for our proposed research.

These selected papers collectively contribute valuable perspectives on addressing challenges related to limited EEG resolution, system design, and spatial resolution optimization. As we embark on the development of an advanced BCI system, the lessons drawn from these studies will inform crucial decisions in electrode technology, system architecture, and the overall enhancement of BCI capabilities. The interdisciplinary nature of these findings underscores the dynamic landscape of BCI research and the potential for transformative advancements in neuro-technology.

Comparative study of the Literature:

Study	Authors	Focus on key findings	Relevance to our research
Fiedler et al. (2022)	Fiedler et al.	Introducing a 256-channel cap with dry multi-pin electrodes for HD-EEG. Comparison with traditional gel-based caps, demonstrating compatibility with state-of-the-art EEG amplifiers. Average	Relevance lies in addressing limited EEG resolution challenges, potential for significantly enhancing BCI system efficiency.

		impedances below 900 kΩ for 252 out of 256 dry electrodes. 84% channel reliability and 69% reduction in preparation time.	
Dvorak and Fenton (2023)	Dvorak and Fenton	Introducing a novel EEG system for precision psychiatry. Wearable cap with EEG electrodes and dynamic adjustments through linear actuators. Neurofeedback mechanism for real-time interaction based on detected abnormal brain activity.	Relevant for exploring innovative EEG system design, addressing challenges related to precision and adaptability in BCI systems.
Ryynanen et al. (2004)	Ryynanen et al.	In-depth exploration of EEG spatial resolution. Using an inverse cortical EEG solution with a three-layer spherical head model. Evaluation of spatial resolution under varying conditions of measurement noise.	Paramount relevance in understanding electrode density impact on spatial resolution, crucial for optimizing spatial resolution in our BCI system design.

Table 2.1: Comparative study of the Literature

Chapter 3: TECHNOLOGY USED

The foundation of our research lies in the exploration and integration of cutting-edge technologies to advance Brain-Computer Interface (BCI) systems. Throughout the developmental phases, a diverse array of technologies is strategically employed to address specific challenges and enhance the overall functionality of the proposed system. From the foundational use of Electroencephalography (EEG) to measure brain waves to the integration of advanced artificial intelligence techniques and interactive platforms, each phase contributes to the realization of a sophisticated BCI system. This comprehensive overview delves into the technologies utilized at each phase, shedding light on their significance and the rationale behind their selection.

Phases of the project:

Phase	Technology Used	Why it is Used
Phase 1: Conceptualization	Electroencephalography (EEG)	EEG serves as the foundational technology to measure brain waves, providing essential data for understanding neural activity and facilitating the development of Brain-Computer Interface (BCI) systems.
Phase 2: Knowledge Integration	Neuroelectrophysiology, Biosensors, Bio-signaling, Signal Transmission in Wired Medium, Analog Multiplexer	Required knowledge areas for developing the idea include neuroelectrophysiology, understanding biosensors, bio-signaling, signal transmission in wired mediums, and the creation of a unique analog multiplexer for multiplexing brain waves.
Phase 3: System Design	Hybrid Electronics System Design, Data Acquisition System	Hybrid electronics system design is essential for integrating diverse components. The data acquisition system is crucial for collecting high-quality EEG data, forming the basis for subsequent analysis and interpretation.

Phase 4: Simulation Environment	Electronic Simulation Environment	The electronic simulation environment allows for the virtual testing and refinement of the proposed system before physical implementation, reducing development time and potential errors.
Phase 5: Communication Technology	Inter-process Communication	Utilizing inter-process communication and LAN technology facilitates seamless communication between system components, enhancing overall system efficiency and responsiveness.

Table 3.1: Phases of the project

Chapter 4: Methodology

Development of the Universal Multiplexer for High-Resolution Brain Wave Data Acquisition

The methodology for the development of the Universal Multiplexer (U-MUX) encompasses a series of meticulous steps aimed at achieving the acquisition of significantly large amounts of analog brain wave data in a singular channel. This approach is integral to reducing costs and increasing the feasibility of acquiring ultra-high-resolution data from electroencephalography (EEG) sensors. The accomplishment of this milestone is the result of a thorough and systematic process involving the following key steps:

1. **Development of Two Cross One Simulation of U-MUX:**

In this initial phase, a detailed simulation model of the Two Cross One U-MUX is crafted. The simulation involves the creation of a virtual environment that emulates the functionality of the U-MUX, allowing for testing and validation of the theoretical design. This step is crucial for refining the U-MUX concept before moving to the hardware implementation.

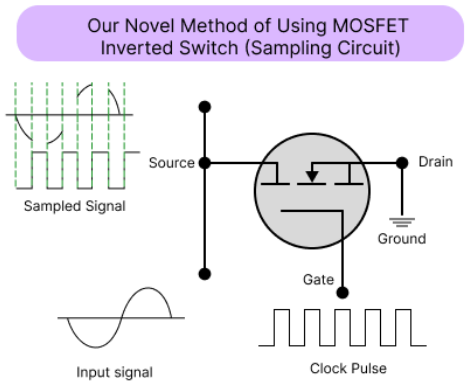


Fig 4.1: Novel methodology of MOSFET switching

2. **Development of Two Cross One Hardware Multiplexer:**

Building upon the insights gained from the simulation, the next step involves the physical development of the Two Cross One U-MUX. This hardware implementation mirrors the simulated model, and meticulous attention is given to component selection, circuit design, and prototype

construction. Rigorous testing is conducted to ensure the hardware multiplexer aligns with the expected performance parameters.

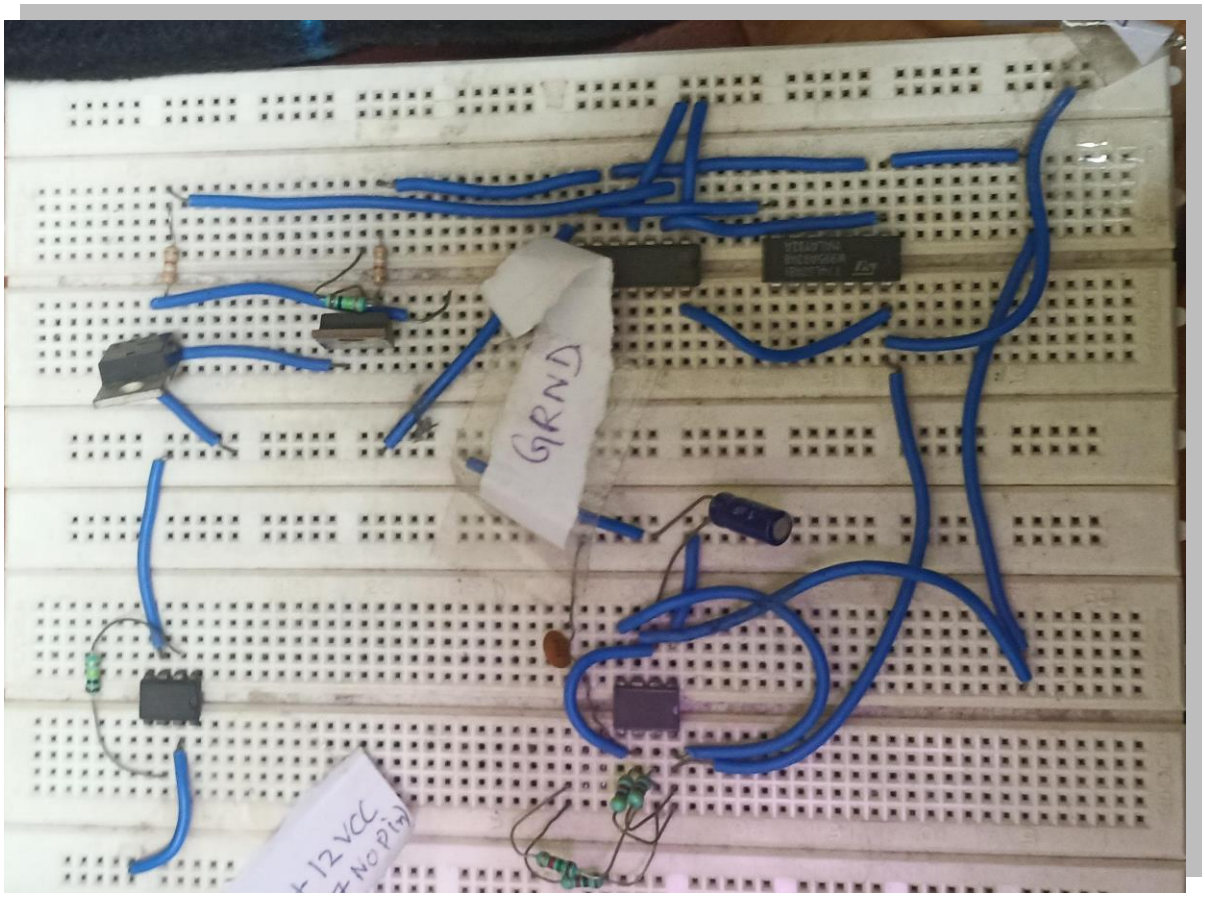


Fig 4.2: Hardware Realization of 2:1 U-MUX prototype

3. **Simulation of 4 Cross One Multiplexer:**

With the successful development of the Two Cross One U-MUX, the methodology advances to the simulation of a more complex 4 Cross One Multiplexer. This simulation extends the capabilities of the U-MUX to accommodate a larger number of input channels, providing insights into scalability and potential challenges that may arise as the multiplexer configuration becomes more intricate.

4. **Simulation of Eight Cross 1 Multiplexer:**

Building upon the insights gained from the 4 Cross One simulation, the methodology progresses to the simulation of an Eight Cross One Multiplexer. This phase aims to push the boundaries of the U-MUX design, testing its robustness and efficiency in handling a more extensive array of input signals. The simulation results inform further refinements and optimizations.

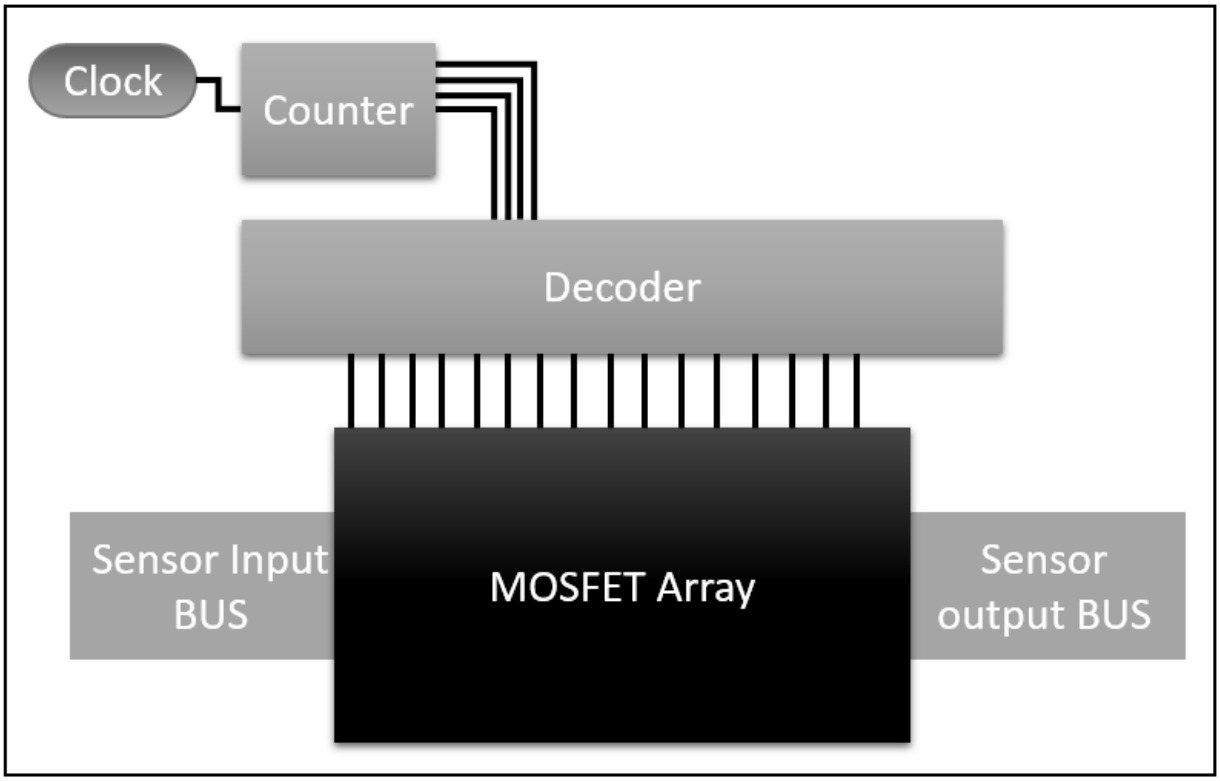


Fig 4.3: U-MUX Block Diagram

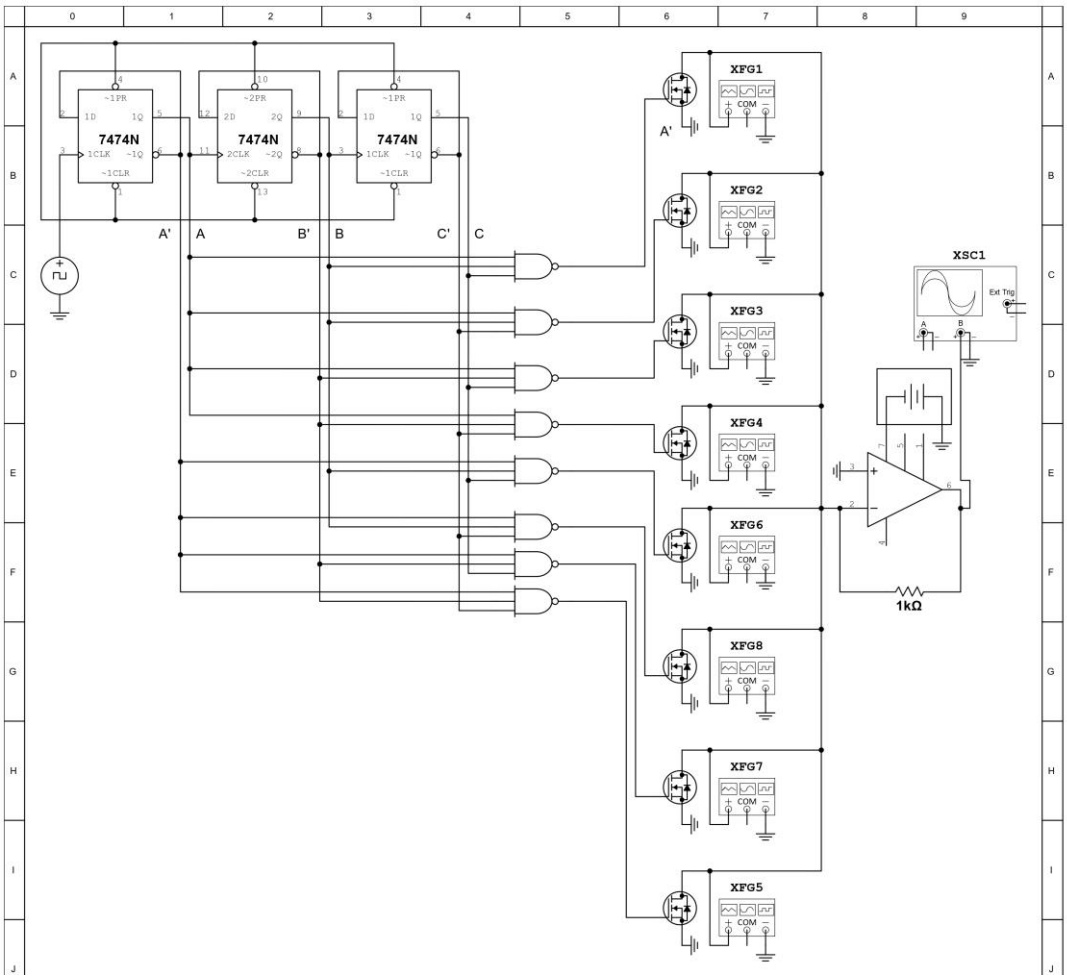


Fig 4.4: 8x1 U-MUX Simulation

5. Hardware Development of 8 Cross One Universal Multiplexer:

The final and critical step involves the physical realization of the Eight Cross One U-MUX. This hardware development phase requires precision in translating the simulated models into a functional multiplexer. Component integration, signal routing, and calibration are paramount in ensuring that the hardware U-MUX operates seamlessly, demonstrating its capability to acquire high-resolution brain wave data.

Throughout each phase of the methodology, thorough documentation is maintained, encompassing design specifications, simulation results, hardware configurations, and testing procedures. This meticulous approach ensures transparency, reproducibility, and the foundation for

future iterations or expansions of the Universal Multiplexer in the pursuit of advancing Brain-Computer Interface technology.

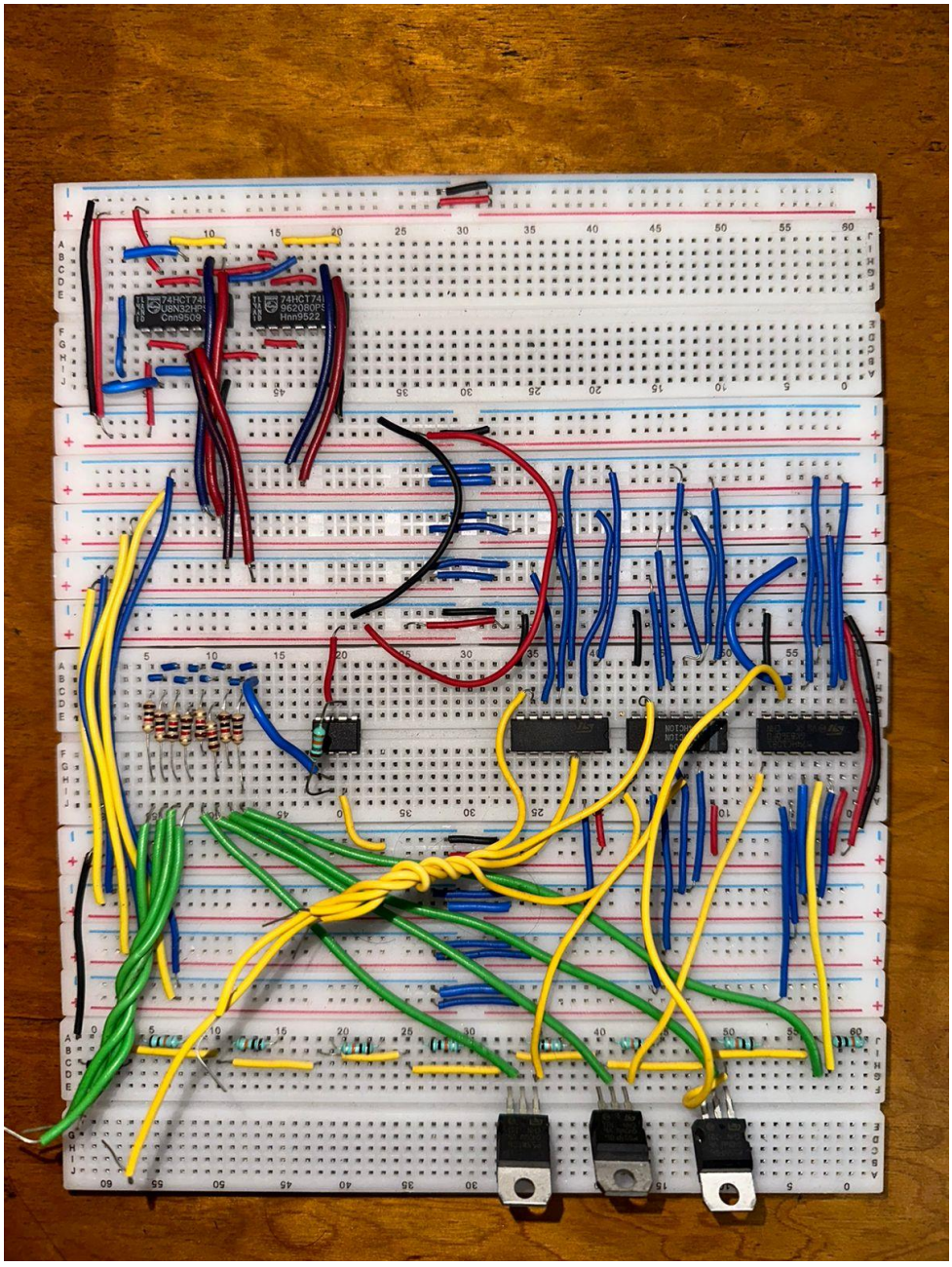


Fig 4.5: Hardware Development of 8 Cross One Universal Multiplexer

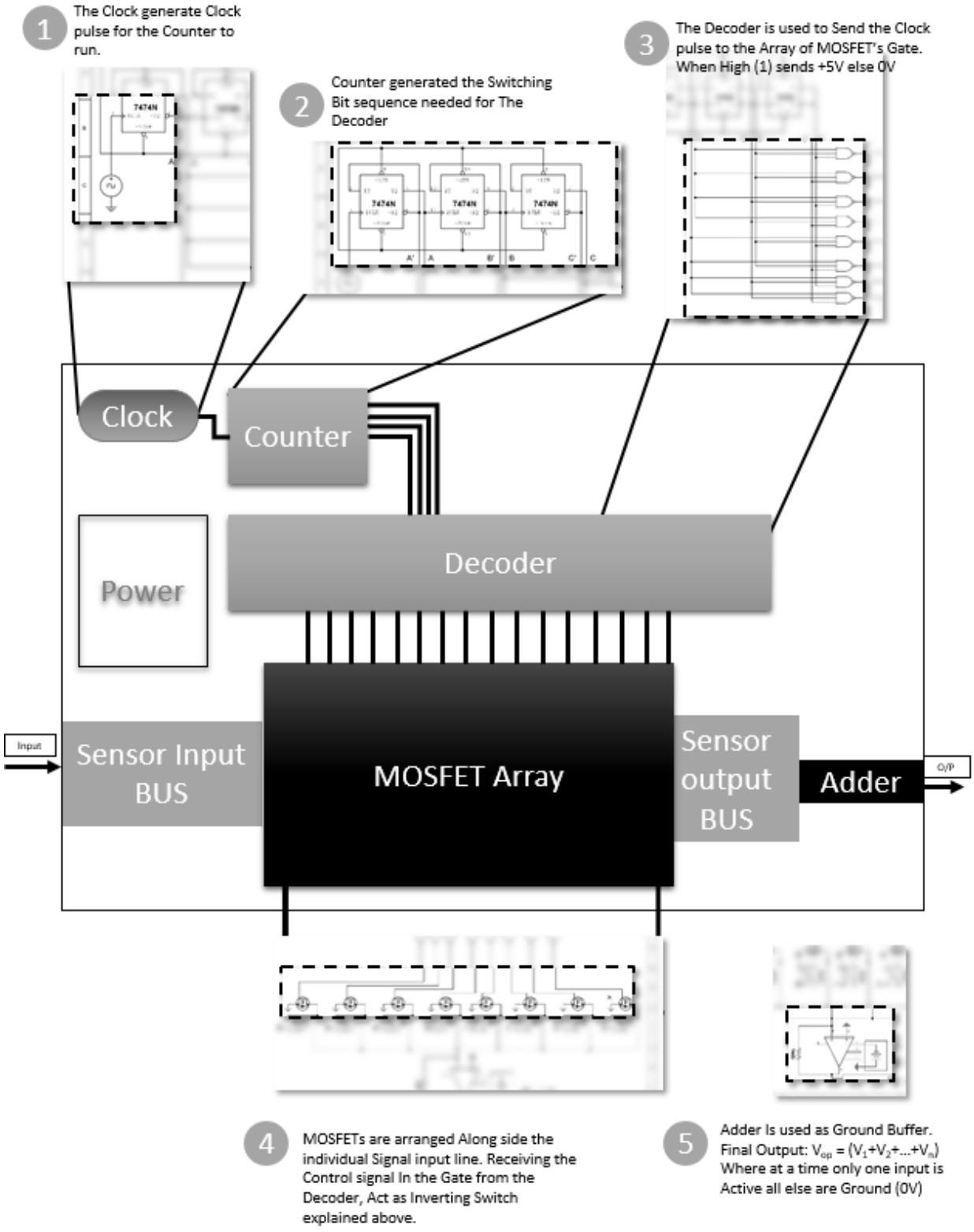
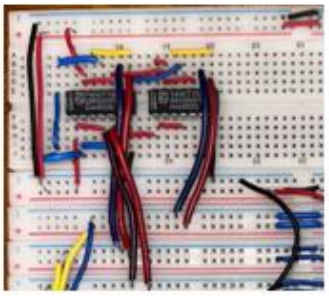
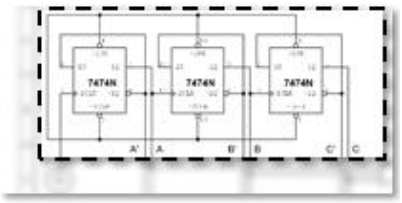


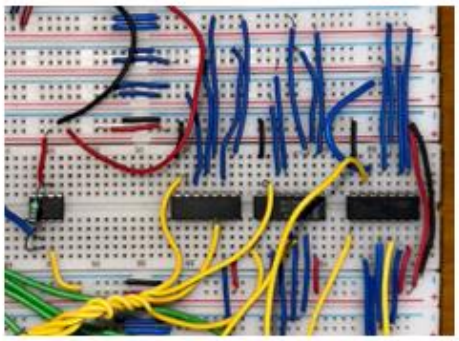
Fig 4.6: U-MUX Working Principle



1

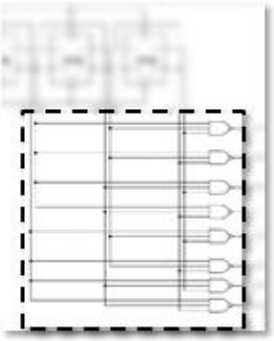
Counter generated the Switching Bit sequence needed for The Decoder

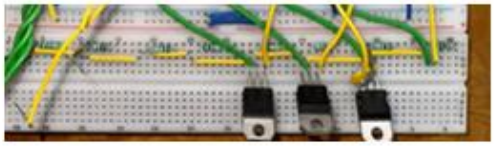


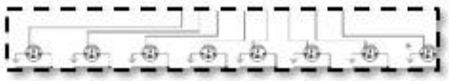


2

The Decoder is used to Send the Clock pulse to the Array of MOSFET's Gate. When High (1) sends +5V else 0V

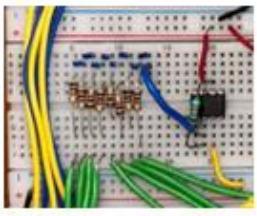






3

MOSFETs are arranged Along side the individual Signal input line. Receiving the Control signal In the Gate from the Decoder, Act as Inverting Switch explained above.



4

Adder Is used as Ground Buffer.
Final Output: $V_{op} = (V_1+V_2+...+V_n)$
Where at a time only one input is Active all else are Ground (0V)

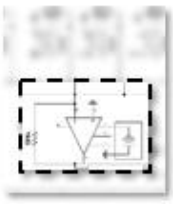


Fig 4.7: 8:1 U-MUX Tested Prototype 1 part By Part

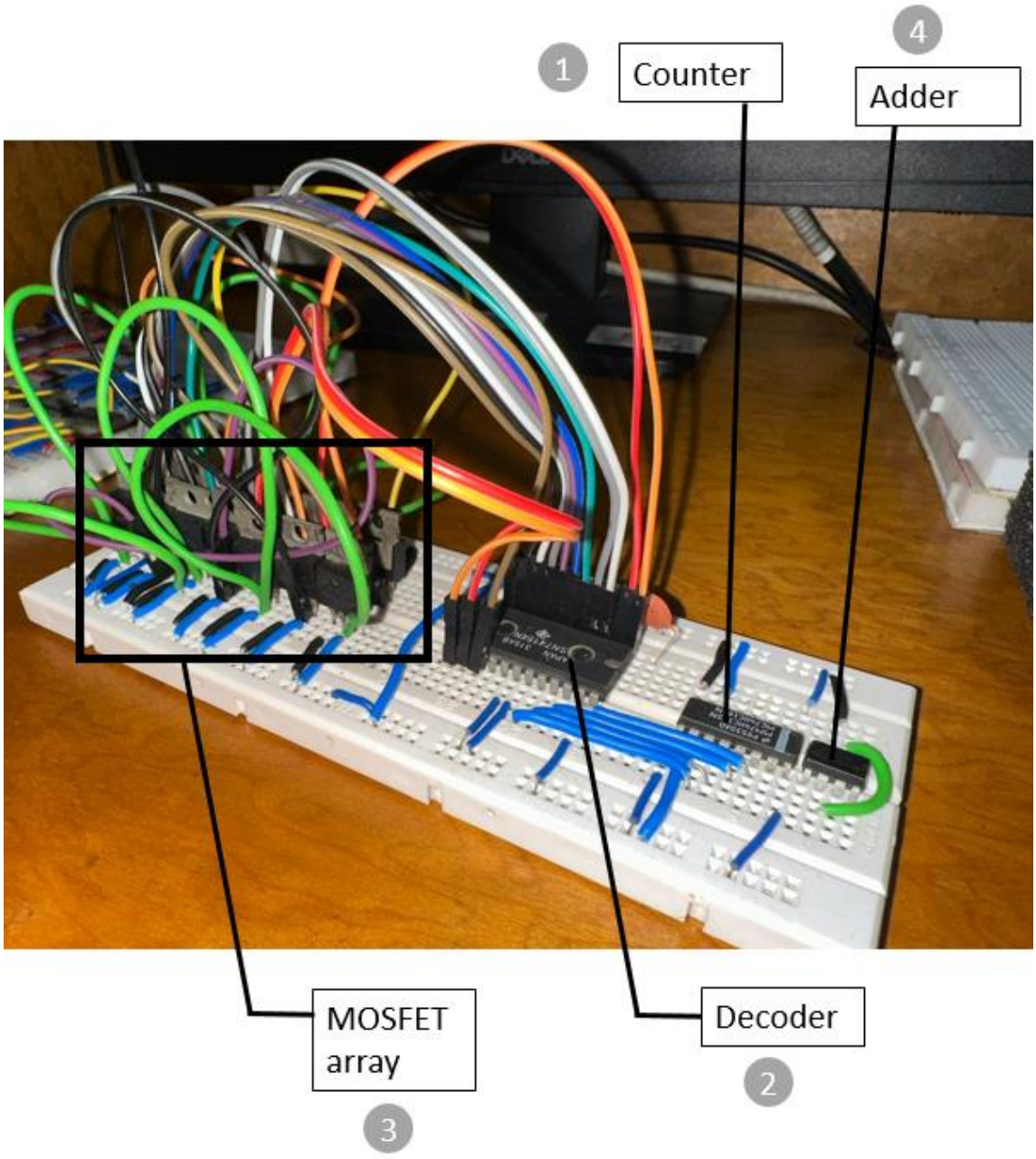


Fig 4.8: 16:1 U-MUX Tested Prototype 1

Chapter 5: Output

Explanation of the multiplexed signals displayed on the Digital Storage Oscilloscope (DSO):

The captured image on the Digital Storage Oscilloscope (DSO) serves as a visual representation of the successful multiplexing of eight signals within a single cycle of the Universal Multiplexer (U-MUX). The DSO, a critical tool in signal analysis, allows for the visualization of the temporal behavior and amplitude characteristics of the multiplexed signals, providing invaluable insights into the efficiency and functionality of the multiplexing process.

a. **Signal Amplitudes:** Each distinct waveform within the captured image corresponds to an individual signal that has undergone the multiplexing process. The amplitude of each waveform represents the strength or intensity of the respective signal during the observed cycle. Variations in amplitude across the multiplexed signals can be indicative of differences in signal strength or intensity.

b. **Temporal Alignment:** The horizontal axis of the DSO display represents time, with each division indicating a specific time interval. The multiplexed signals are temporally aligned within a single cycle, showcasing the synchronization achieved by the U-MUX. This alignment is crucial for ensuring accurate reconstruction of the individual signals during the subsequent demultiplexing process.

c. **Distinctive Signal Patterns:** Each waveform exhibits a unique pattern, allowing for the identification of individual signals within the multiplexed stream. The distinctive patterns enable a clear distinction between the signals, facilitating their separation during the demultiplexing phase.

d. **Cycle Completeness:** The entire display encompasses a single cycle of the multiplexing process. This cycle reflects the duration required for the U-MUX to sequentially combine and transmit all eight signals. The completeness of the cycle is indicative of the efficiency and reliability of the multiplexing operation.

e. **Signal Integrity**: Observations related to signal integrity can be made by examining the overall shape and consistency of each waveform. Anomalies such as distortions, spikes, or irregularities could signify potential issues in the multiplexing process or provide insights into the need for signal conditioning.

f. **Multiplexer Performance Metrics:** The DSO image serves as a basis for assessing various performance metrics of the U-MUX, including but not limited to channel reliability, crosstalk, and overall signal fidelity. Analyzing the captured signals allows for the quantitative evaluation of these metrics, ensuring the robustness of the multiplexing system.

In summary, the DSO image encapsulates the successful multiplexing of eight signals in a single cycle, offering a visual testament to the functionality and efficiency of the Universal Multiplexer. The interpretation of this image contributes valuable insights into the temporal and amplitude characteristics of the multiplexed signals, essential for validating the performance of the U-MUX in the broader context of the proposed Brain-Computer Interface (BCI) system.

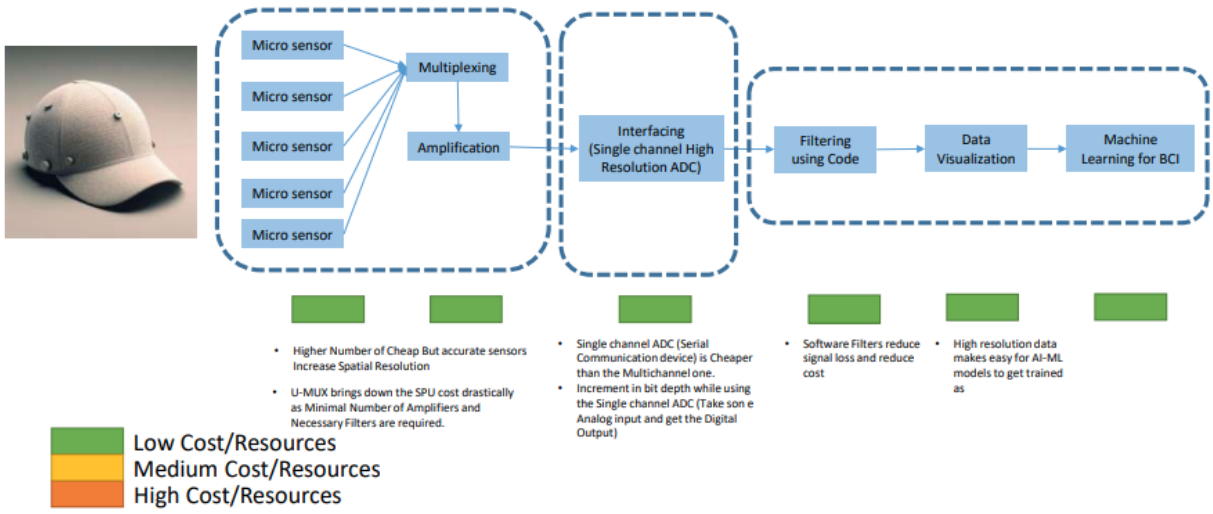


Fig 5.1: Proposed System Architecture

Explanation of the Proposed BCI System Architecture Comparison:

The presented image illustrates a comprehensive comparison between the existing and proposed architectures of the Brain-Computer Interface (BCI) system. This juxtaposition is particularly focused on the crucial stage of signal processing and amplification within the semiconductor level design. The narrative accompanying the image highlights key distinctions that significantly impact the efficiency, cost, and feasibility of the BCI system.

a. **Existing System Architecture:** In the existing BCI system architecture, the conventional approach involves routing brain signals directly to signal amplification without prior multiplexing. This design choice poses inherent challenges, especially considering that brain signals are inherently low in amplitude at the semiconductor level. Amplifying such weak signals directly incurs difficulties in signal integrity and reliability.

Furthermore, as the number of channels increases in the existing system, the demand for additional hardware units grows exponentially. This not only escalates the overall system cost but also introduces practical limitations in terms of probe size and deployment due to the complexity associated with accommodating numerous hardware units.

b. **Proposed System Architecture:** In contrast, the proposed BCI system architecture introduces a novel approach at the semiconductor level, strategically integrating multiplexing before signal amplification. This innovative design choice carries substantial advantages, primarily addressing the challenges posed by the inherently low amplitude of brain signals.

By incorporating multiplexing at an early stage, the proposed architecture optimizes signal processing efficiency, enabling the simultaneous handling of multiple signals with enhanced robustness. This, in turn, contributes to improved signal-to-noise ratios and heightened overall system performance.

A key highlight of the proposed architecture is its impact on cost and feasibility. The early integration of multiplexing allows for a reduction in the number of required hardware units, effectively minimizing costs. This cost-effectiveness, coupled with the feasibility of miniaturizing probe sizes, becomes a transformative factor, opening avenues for deploying a higher number of probes within the constraints of limited hardware resources.

The proposed architecture aligns with the concept of advancing BCI technology by making it more accessible, cost-effective, and adaptable to various applications. The juxtaposition of existing and proposed architectures emphasizes the paradigm shift introduced by the novel semiconductor-level design, offering a promising direction for the future development of BCI systems.

In summary, the image and its corresponding explanation encapsulate the transformative potential of the proposed BCI system architecture. By reimagining the signal processing workflow at the semiconductor level, the proposed design not only addresses existing limitations but also sets

the stage for a more scalable, cost-effective, and feasible implementation of Brain-Computer Interface technology.

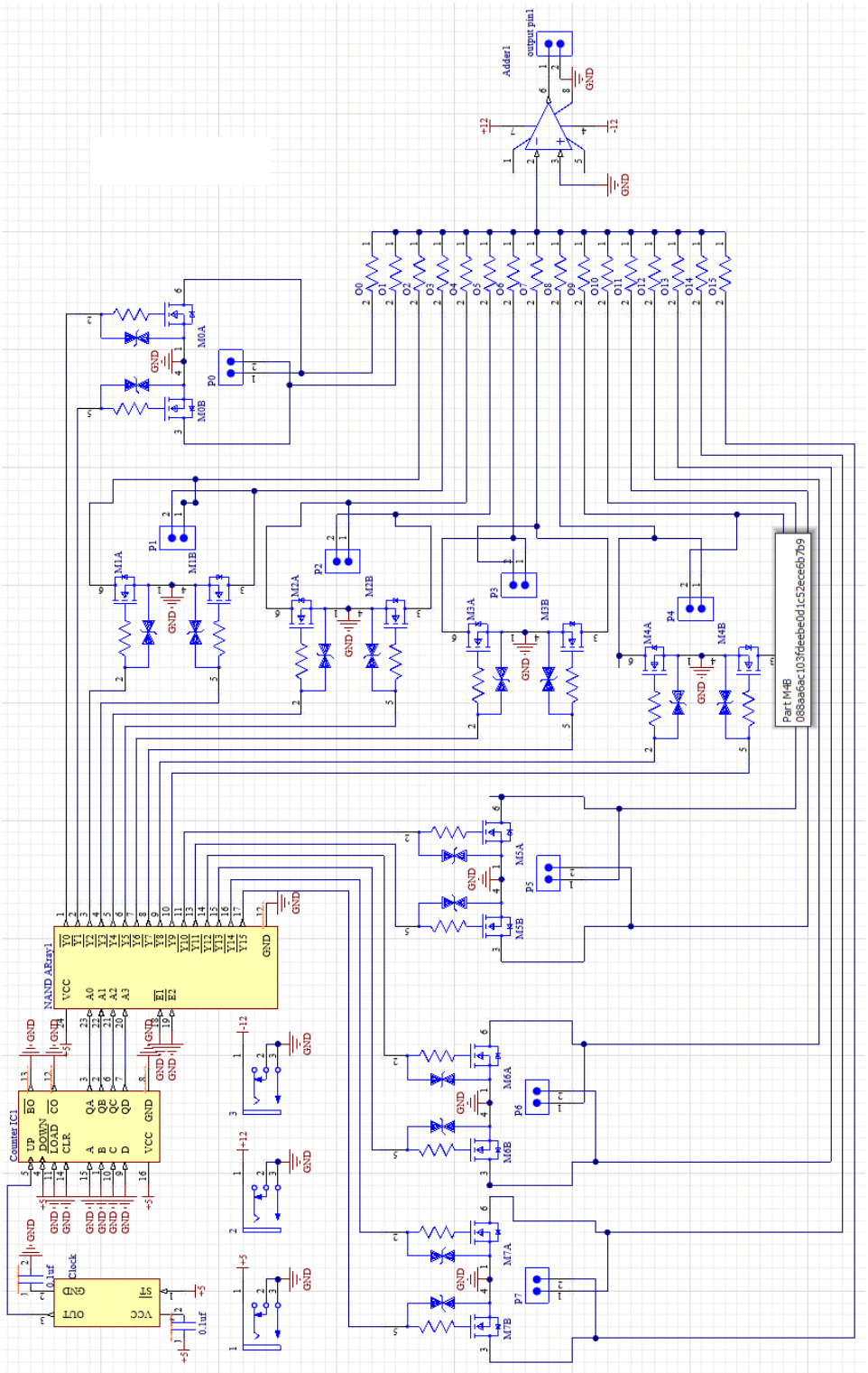


Fig 5.2: Printed Circuit Board Development of U-MUX

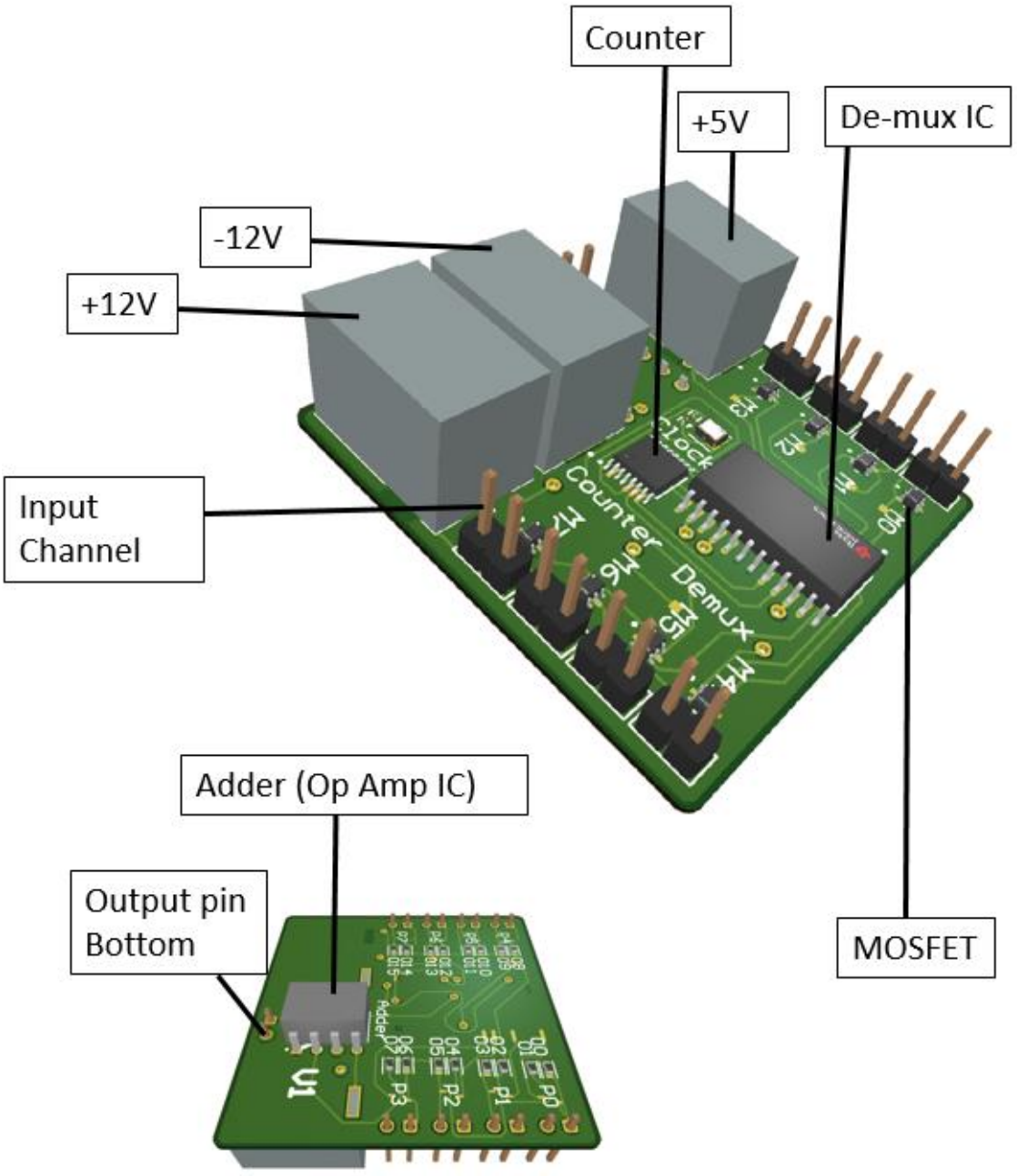


Fig 5.3: PCB 3D view

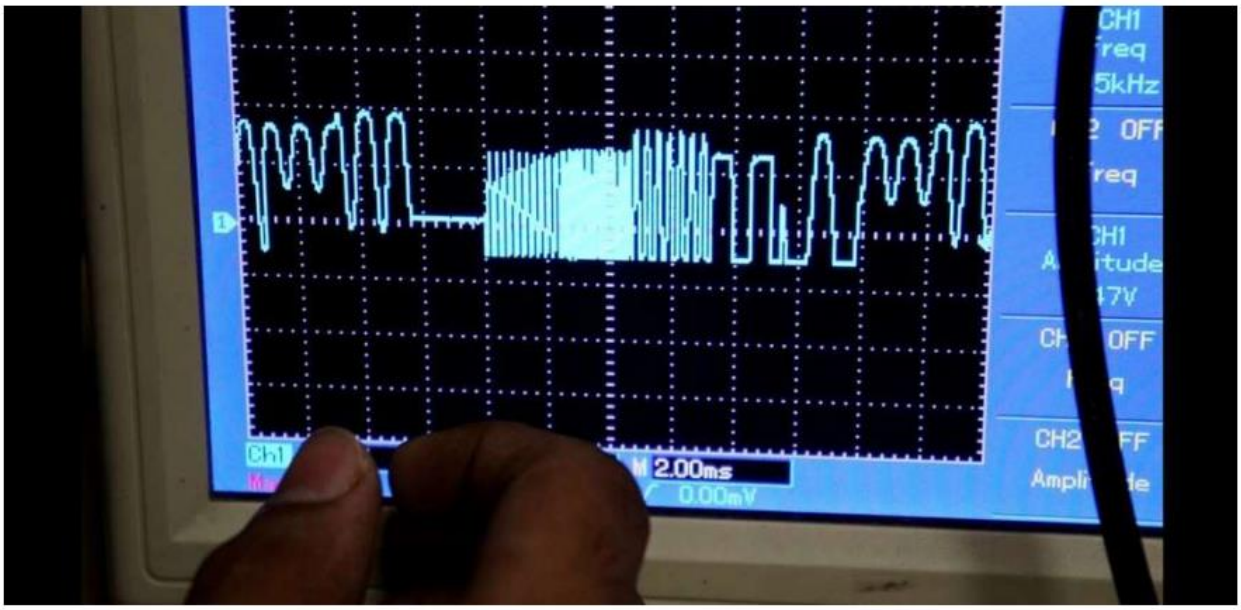


Fig 5.4: The experimental output

Chapter 6: CONCLUSION

Advancements in Brain-Computer Interface (BCI) System Architecture

The culmination of this research marks a pivotal moment in the evolution of Brain-Computer Interface (BCI) technology, introducing a novel architecture that redefines the traditional signal processing paradigm at the semiconductor level. The juxtaposition of existing and proposed architectures underscores the transformative potential of our innovative approach, offering solutions to key challenges and ushering in a new era of efficiency, cost-effectiveness, and feasibility.

Key Findings:

Signal Processing Paradigm Shift: The proposed architecture challenges the conventional signal processing flow by incorporating multiplexing before signal amplification at the semiconductor level. This strategic shift addresses the inherent challenges associated with low-amplitude brain signals, ensuring optimal signal integrity and robustness.

Cost-Effective Multiplexing: The early integration of multiplexing introduces a cost-effective solution by reducing the number of required hardware units. This not only lowers the overall system cost but also facilitates the feasibility of miniaturizing probe sizes, a crucial factor in expanding the scope and applicability of BCI technology.

Enhanced Scalability: The proposed architecture's scalability is a defining feature, allowing for the deployment of a higher number of probes within the constraints of limited hardware resources. This scalability opens avenues for diverse use cases, ranging from medical applications to human-computer interaction.

Use Cases:

Medical Applications: The novel architecture finds immediate applicability in medical scenarios, offering enhanced brain signal acquisition for diagnostic purposes. The cost-effectiveness and feasibility of deploying multiple probes pave the way for widespread adoption in neurology, psychiatry, and rehabilitation.

Human-Computer Interaction (HCI): In the realm of HCI, the proposed architecture revolutionizes the potential for seamless communication between humans and computers. The

enhanced signal processing efficiency enables more nuanced and accurate interpretations of user intent, opening avenues for natural and intuitive interaction.

Research and Exploration: Beyond practical applications, the proposed architecture serves as a boon for researchers and explorers in the field of neuroscience. The scalability and efficiency of the system empower researchers to delve deeper into understanding brain function and behavior, unlocking new realms of knowledge.

Architectural Visualization: The proposed BCI system architecture envisions a streamlined flow where brain signals are initially subjected to multiplexing at the semiconductor level before undergoing signal amplification. This visual representation portrays a modular and adaptable system, allowing for the integration of multiple probes without compromising efficiency or increasing hardware complexity.

Time Frame for Implementation: While the exact time frame for full-scale implementation depends on factors such as technological integration, regulatory approvals, and widespread adoption, preliminary assessments suggest a realistic timeline within the next five to seven years. This projection considers iterative development, testing, and refinement phases necessary for ensuring the robustness, reliability, and safety of the proposed architecture.

Chapter 7: FUTURE WORK

Future Research Directions for the Advancement of BCI System Development:

a. **Completion of Artificial Intelligence and Machine Learning (AIML) Model:** The forthcoming phase of research entails the meticulous refinement and completion of the AIML model. This iterative process involves continuous training and validation with diverse datasets, ensuring a robust foundation for accurate interpretation of intricate brain signals.

b. **Construction of the BCI System:** Subsequent steps involve the physical realization of the Brain-Computer Interface (BCI) system, incorporating the optimized semiconductor-level architecture and pioneering multiplexing techniques. This phase necessitates intricate hardware integration, circuit design, and rigorous compatibility testing.

c. **Efficient Processing of Brain Data:** Advanced algorithms and software solutions are under development to efficiently handle the substantial volume of real-time brain data. Emphasis is placed on optimizing data compression, feature extraction, and storage techniques to ensure seamless processing.

d. **Exploration of Signal Extraction Techniques**: Rigorous exploration and implementation of signal extraction techniques are underway to precisely capture and interpret specific brain signals. This includes a nuanced investigation into spectral analysis, time-domain analysis, and pattern recognition methods tailored to BCI applications.

e. **Formulation of a Robust Commercialization Strategy:** The development of a comprehensive commercialization strategy is underway, encompassing market analysis, user profiling, and potential collaborative ventures. The strategy articulates a compelling value proposition, emphasizing distinctive features, cost-effectiveness, and diverse applications of the BCI system.

f. **Establishment of a Startup Venture:** A pivotal transition from research to practical implementation involves the establishment of a startup dedicated to BCI technology. This phase encompasses securing funding, assembling a multidisciplinary team, and formulating a roadmap for systematic product development, testing, and eventual market launch.

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1. P. Fiedler, C. Fonseca, Eko Supriyanto, F. Zanow, and J. Haueisen, “A high-density 256-channel cap for dry electroencephalography,” ***Human Brain Mapping***, vol. 43, no. 4, pp. 1295–1308, Nov. 2021. [Online]. Available: https://doi.org/10.1002/hbm.25721.

2. D. Dvorak and A. A. Fenton, “High density EEG system for precision psychiatry,” [Online]. Available: https://patents.google.com/patent/WO2021248014A1/en (accessed Dec. 01, 2023).

3. O. R. M. Ryynanen, J. A. K. Hyttinen, P. H. Laarne, and J. A. Malmivuo, “Effect of electrode density and measurement noise on the spatial resolution of cortical potential distribution,” ***IEEE Transactions on Biomedical Engineering***, vol. 51, no. 9, pp. 1547-1554, Sept. 2004. [Online]. Available: https://doi.org/10.1109/TBME.2004.828036.

4. P. Fiedler, C. Fonseca, Eko Supriyanto, F. Zanow, and J. Haueisen, “A high-density 256-channel cap for dry electroencephalography,” ***Human Brain Mapping***, vol. 43, no. 4, pp. 1295-1308, Mar. 2022. [Online]. Available: https://doi.org/10.1002/hbm.25721.

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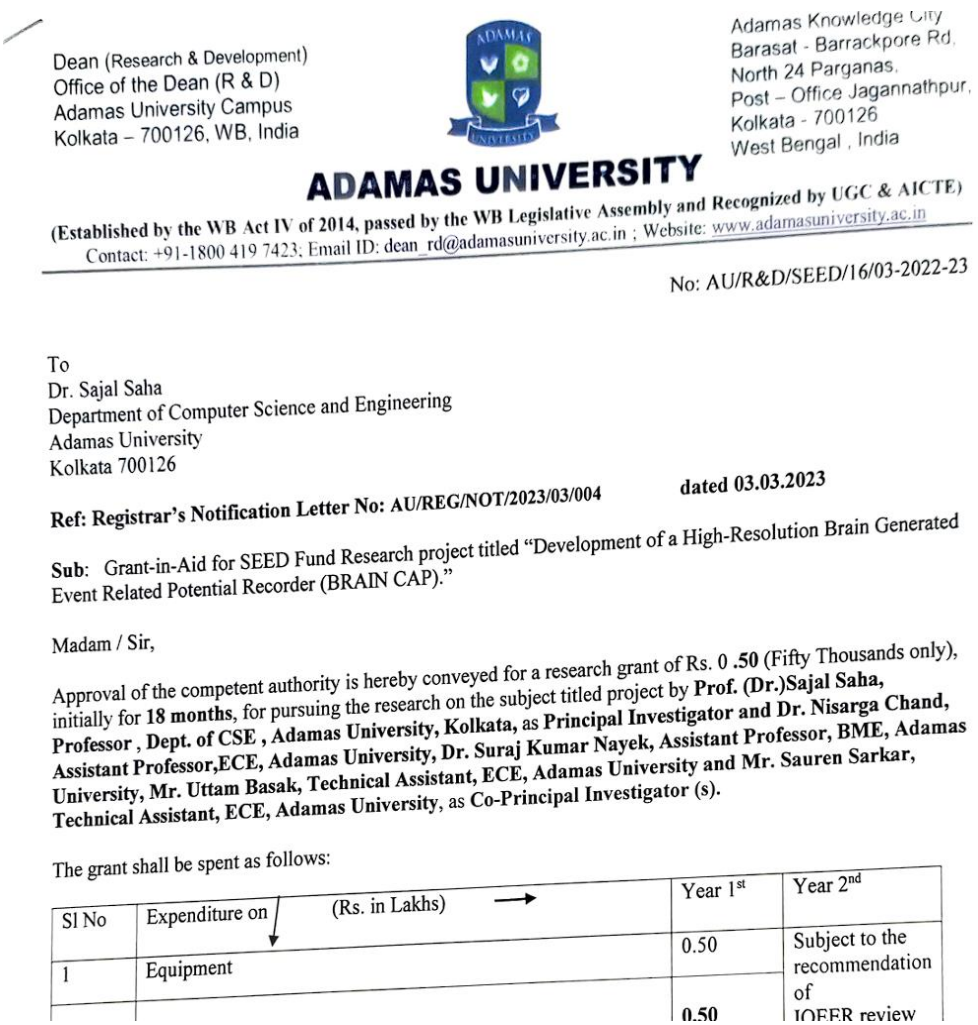
6. O. R. M. Ryynanen, J. A. K. Hyttinen, P. H. Laarne, and J. A. Malmivuo, "Effect of electrode density and measurement noise on the spatial resolution of cortical potential distribution," ***IEEE Transactions on Biomedical Engineering***, vol. 51, no. 9, pp. 1547-1554, Sept. 2004. [Online]. Available: https://doi.org/10.1109/TBME.2004.828036.

Annexure 1

Acknowledgment of the Seed grant Support received

I extend my sincere gratitude to Adamas University for their unwavering support and provision of a seed grant of Rs. 50,000. This generous financial assistance, facilitated by the competent authority's approval, serves as a cornerstone for the initiation and progression of our research project. The encouragement from Adamas University has not only provided essential resources but also exemplifies their commitment to fostering a conducive environment for academic exploration and innovation. With this seed grant, our research team, led by Prof. (Dr.) Sajal Saha, Professor, Dept. of CSE, Adamas University, Kolkata, as the Principal Investigator, and in collaboration with Dr. Nisarga Chand, Assistant Professor, ECE, Adamas University, Mr. Uttam Basak and Mr. Mr. Sauren Sarkar is well-equipped to embark on this journey of scholarly inquiry and contribute to the advancement of knowledge.



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ADAMAS UNIVERSITY

(Established by the WB Act IV of 2014, passed by the WB Legislative Assembly and Recognized by UGC & AICTE)
Contact: +91-1800 419 7423; Email ID: dean_rd@adamasuniversity.ac.in ; Website: www.adamasuniversity.ac.in

No: AU/R&D/SEED/16/03-2022-23

To
Dr. Sajal Saha
Department of Computer Science and Engineering
Adamas University
Kolkata 700126

Ref: Registrar's Notification Letter No: AU/REG/NOT/2023/03/004 **dated 03.03.2023**

Sub: Grant-in-Aid for SEED Fund Research project titled "Development of a High-Resolution Brain Generated Event Related Potential Recorder (BRAIN CAP)."

Madam / Sir,

Approval of the competent authority is hereby conveyed for a research grant of Rs. 0 **.50** (Fifty Thousands only), initially for **18 months**, for pursuing the research on the subject titled project by **Prof. (Dr.)Sajal Saha, Professor , Dept. of CSE , Adamas University, Kolkata,** as **Principal Investigator and Dr. Nisarga Chand, Assistant Professor,ECE, Adamas University, Dr. Suraj Kumar Nayek, Assistant Professor, BME, Adamas University, Mr. Uttam Basak, Technical Assistant, ECE, Adamas University and Mr. Sauren Sarkar, Technical Assistant, ECE, Adamas University**, as **Co-Principal Investigator (s).**

The grant shall be spent as follows:

Sl No	Expenditure on ↓ (Rs. in Lakhs) →	Year 1st	Year 2nd
1	Equipment	0.50	Subject to the recommendation of
		0.50	IOEER review

Attach Plagiarism Report