Universidad de Puerto Rico
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Departamento de Ingeniería Eléctrica y de Computadoras
ICOM 4215 -001D

Course Project: Design and Simulation of a RISC Microprocessor

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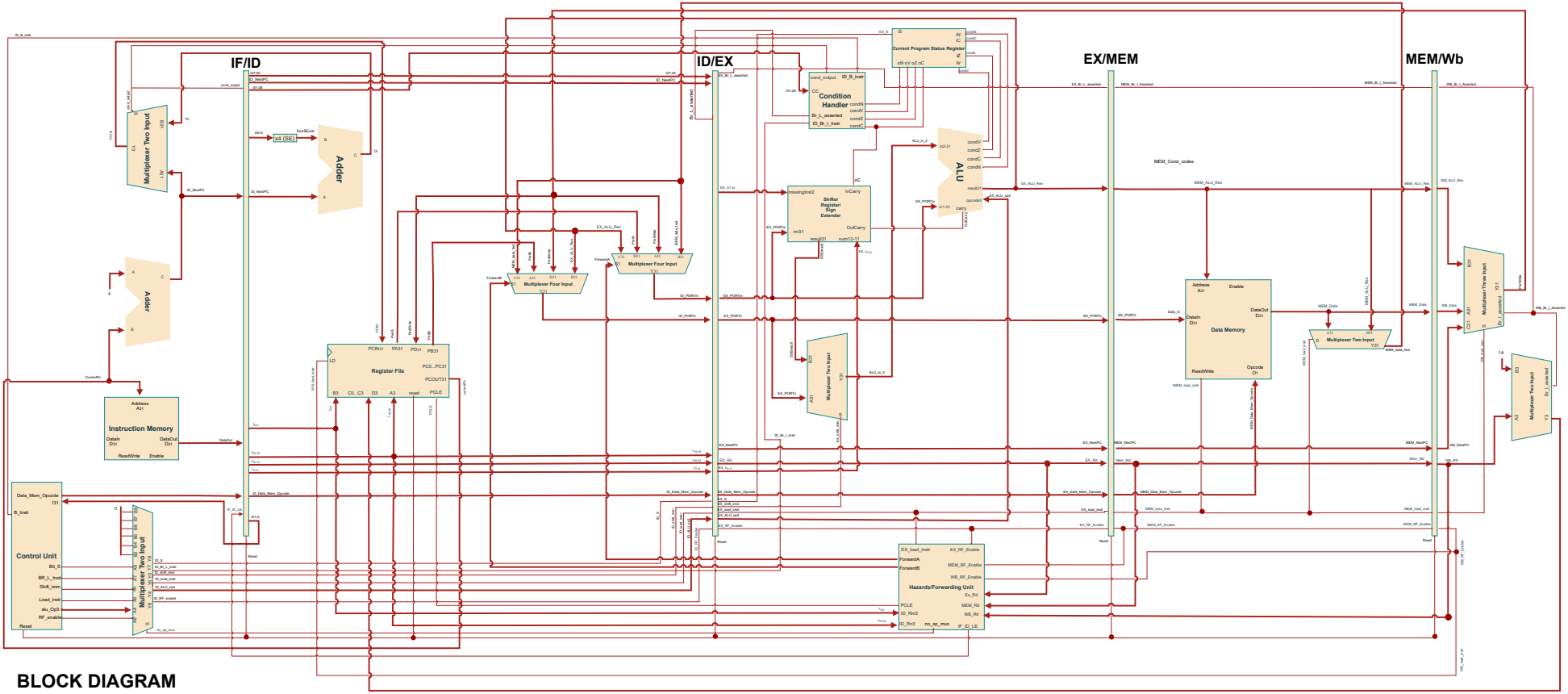
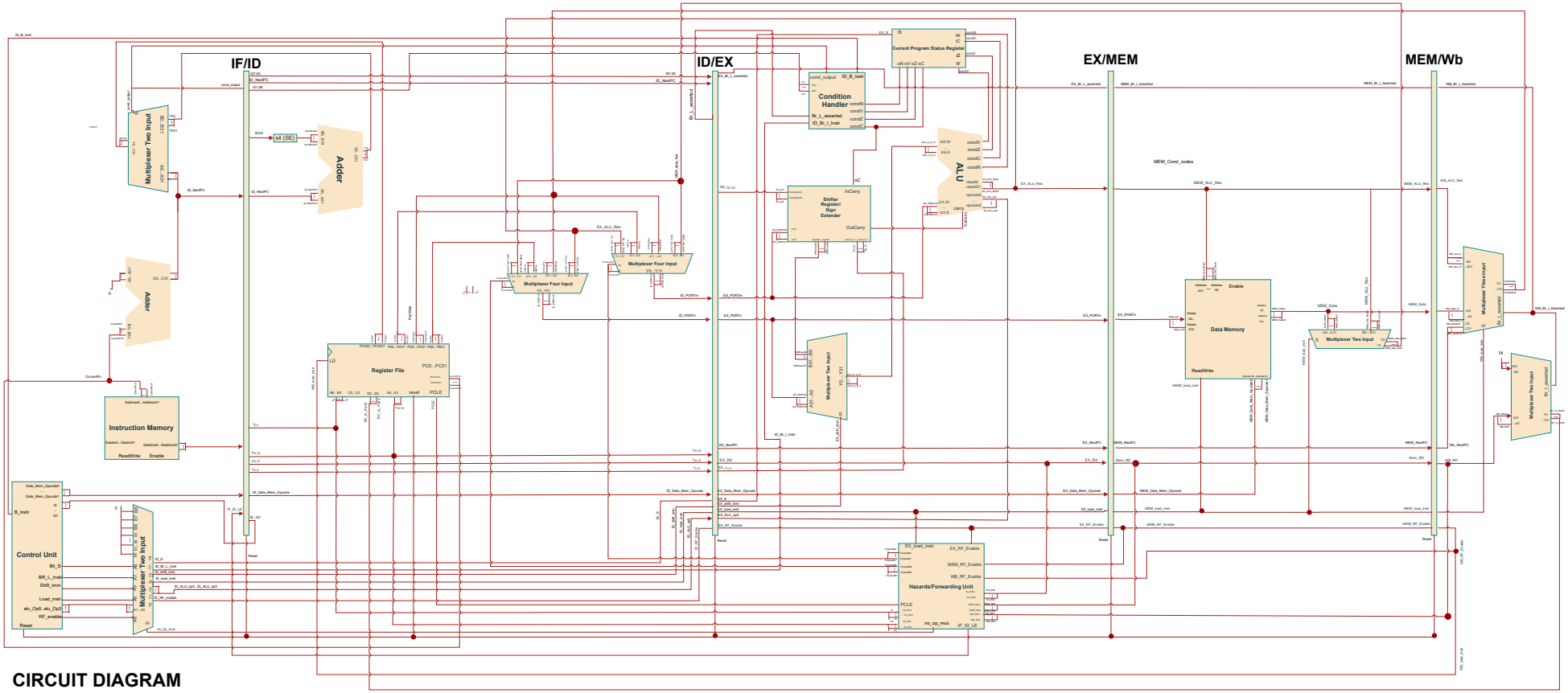


BLOCK DIAGRAM



CIRCUIT DIAGRAM

`	I_{27-25}	I_{24-21}	I_{20}	Bit_S	ID_B_instr	Br_L_Instr	Shift_imm	Load_instr	ALU_{OP}	RF_enable	Data_Mem_Opcode
Data Processing Register Shift	000	0000	0	0	0	0	0	1	0000	1	10
	000	0001	0	0	0	0	0	1	0001	1	10
	000	0010	0	0	0	0	0	1	0010	1	10
	000	0011	0	0	0	0	0	1	0011	1	10
	000	0100	0	0	0	0	0	1	0100	1	10
	000	0101	0	0	0	0	0	1	0101	1	10
	000	0110	0	0	0	0	0	1	0110	1	10
	000	0111	0	0	0	0	0	1	0111	1	10
	000	1000	0	0	0	0	0	1	1000	1	10
	000	1001	0	0	0	0	0	1	1001	1	10
	000	1010	0	0	0	0	0	1	1010	1	10
	000	1011	0	0	0	0	0	1	1011	1	10
	000	1100	0	0	0	0	0	1	1100	1	10
	000	1101	0	0	0	0	0	1	1101	1	10
	000	1110	0	0	0	0	0	1	1110	1	10
	000	1111	0	0	0	0	0	1	1111	1	10
	000	0000	1	1	0	0	0	1	0000	1	10
	000	0001	1	1	0	0	0	1	0001	1	10
	000	0010	1	1	0	0	0	1	0010	1	10
	000	0011	1	1	0	0	0	1	0011	1	10
	000	0100	1	1	0	0	0	1	0100	1	10
	000	0101	1	1	0	0	0	1	0101	1	10
	000	0110	1	1	0	0	0	1	0110	1	10
	000	0111	1	1	0	0	0	1	0111	1	10
	000	1000	1	1	0	0	0	1	1000	1	10
	000	1001	1	1	0	0	0	1	1001	1	10
	000	1010	1	1	0	0	0	1	1010	1	10
	000	1011	1	1	0	0	0	1	1011	1	10
	000	1100	1	1	0	0	0	1	1100	1	10

	000	1101	1	1	0	0	0	1	1101	1	10
	000	1110	1	1	0	0	0	1	1110	1	10
	000	1111	1	1	0	0	0	1	1111	1	10

`	I_{27-25}	I_{24-21}	I_{20}	Bit_S	ID_B_instr	Br_L_Instr	Shift_imm	Load_instr	ALU_{OP}	RF_enable	Data_Mem_Opcode
Data Processing Immediate	001	0000	0	0	0	0	1	1	0000	1	10
	001	0001	0	0	0	0	1	1	0001	1	10
	001	0010	0	0	0	0	1	1	0010	1	10
	001	0011	0	0	0	0	1	1	0011	1	10
	001	0100	0	0	0	0	1	1	0100	1	10
	001	0101	0	0	0	0	1	1	0101	1	10
	001	0110	0	0	0	0	1	1	0110	1	10
	001	0111	0	0	0	0	1	1	0111	1	10
	001	1000	0	0	0	0	1	1	1000	1	10
	001	1001	0	0	0	0	1	1	1001	1	10
	001	1010	0	0	0	0	1	1	1010	1	10
	001	1011	0	0	0	0	1	1	1011	1	10
	001	1100	0	0	0	0	1	1	1100	1	10
	001	1101	0	0	0	0	1	1	1101	1	10
	001	1110	0	0	0	0	1	1	1110	1	10
	001	1111	0	0	0	0	1	1	1111	1	10
	001	0001	1	1	0	0	1	1	0001	1	10
	001	0010	1	1	0	0	1	1	0010	1	10
	001	0011	1	1	0	0	1	1	0011	1	10
	001	0100	1	1	0	0	1	1	0100	1	10
	001	0101	1	1	0	0	1	1	0101	1	10
	001	0110	1	1	0	0	1	1	0110	1	10
	001	0111	1	1	0	0	1	1	0111	1	10
	001	1000	1	1	0	0	1	1	1000	1	10
	001	1001	1	1	0	0	1	1	1001	1	10
	001	1010	1	1	0	0	1	1	1010	1	10

	001	1011	1	1	0	0	1	1	1011	1	10
	001	1100	1	1	0	0	1	1	1100	1	10
	001	1101	1	1	0	0	1	1	1101	1	10
	001	1110	1	1	0	0	1	1	1110	1	10
	001	1111	1	1	0	0	1	1	1111	1	10

	I_{27-25}	I_{22} - B	I_{23} - U	I_{20}	Bit_S	ID_B_instr	Br_L_Instr	Shift_imm	Load_instr	ALU_{OP}	RF_enable	Data_Mem_Opcode
Load/Store Immediate Offset	010	0	0	0	0	0	0	1	0	0100	0	10
	010	0	1	0	0	0	0	1	0	0100	0	10
	010	1	0	0	0	0	0	1	0	0100	0	00
	010	1	1	0	0	0	0	1	0	0100	0	00
	010	0	0	0	0	0	0	1	1	0100	1	10
	010	0	1	0	0	0	0	1	1	0100	1	10
	010	1	0	0	0	0	0	1	1	0100	1	00
	010	1	1	0	0	0	0	1	1	0100	1	00
Load/Store Register Offset	011	0	0	0	0	0	0	0	0	0100	0	10
	011	0	1	0	0	0	0	0	0	0100	0	10
	011	1	0	0	0	0	0	0	0	0100	0	00
	011	1	1	0	0	0	0	0	0	0100	0	00
	011	0	0	0	0	0	0	0	1	0100	1	10
	011	0	1	0	0	0	0	0	1	0100	1	10
	011	1	0	0	0	0	0	0	1	0100	1	00
	011	1	1	0	0	0	0	0	1	0100	1	00

	I_{27-25}	I_{24} - L	I_{20}	Bit_S	ID_B_instr	Br_L_Instr	Shift_imm	Load_instr	ALU_{OP}	B_instr	RF_enable	Data_Mem_Opcode
Branch	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
	101	0	0	0	1	0	0	1	*	1	0	10
Branch and Link	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10
	101	1	0	0	1	1	0	1	*	1	1	10

Condcode	Description	Flag tested
0000	Equal	Z = 1
0001	Not equal	Z = 0
0010	Unsigned higher or same	C = 1
0011	Unsigned lower	C = 0
0100	Minus	N = 1
0101	Positive or zero	N = 0
0110	Overflow	V = 1
0111	No Overflow	V = 0
1000	Unsigned higher	C = 1 & Z = 0
1001	Unsigned lower or same	C = 0 or Z = 1
1010	Greater or equal	N = V
1011	Less than	N != V
1100	Greater than	Z = 0 & N = V
1101	Less than or equal	Z = 1 || N != V
1110	Always	