# A ARTIFACT DESCRIPTION APPENDIX

**Computational Artifacts**: Yes

## A.1 Artifact Description Details

All numerical simulation tests are performed on the SunRising-1 computing platform at the Computer Network Information Centre (CNIC), Chinese Academy of Sciences (CAS). Each node has 128 GB DDR4 memory, a Hygon Dhyana C86 7185 32-core CPU, and four Hygon DCU accelerators. The nodes adopt fat-tree topology and are connected through a 200 Gbps Infiniband HDR network. Logs of all tests can be obtained from https://github.com/ICPP2022/pap240-tests.

Experiment Workflow: Enter the corresponding test directory, and execute the command: sbatch misaslscd.sh. Or run the following command:

```
$ cd MISA-SLSCD/src/
$ make
$ cd ../tests/testFile/
$ mpirun -n $nproces ../../src/misaslscd configure.in
```

Experimental Details:

For the accuracy tests in Fig. 6, Fig. 7, and Fig. 8, we compare our parallel SRSCD method on a node (32 CPU cores) of SunRising-1 with other methods in published references, including OKMC, serial SRSCD, classical CD, and experiments. For each simulation case, a fixed simulation box of $32,000$ VEs with 10 nm length per VE and periodic boundary conditions are used. Each simulation case is performed three times independently, and the average results is taken. For Fig. 6, the simulation is carried out at 100°C, 20 KeV cascades are implanted into a $\alpha$-Fe system with a dose rate of $10^{-4}$ dpa/s, and a total dose of $10^{-2}$ dpa is reached. For Fig. 7, the simulation is carried out at 290°C, Frenkel pairs are implanted into a Fe-1.34at.%Cu alloy system with a dose rate of $2\times10^{-9}$ dpa/s, and a total dose of $4\times10^{-3}$ dpa is reached. For Fig. 8, the simulation is carried out at 300°C with a dose rate of $1.4\times10^{-7}$ dpa/s, 20 KeV cascades are implanted into a Fe-0.3at.%Cu alloy system, and a total dose of 0.2 dpa is reached. These and other simulation parameters are set in respective configure.in files.

For the memory usage test in Fig. 9, we compare our parallel method with the SP-SRSCD on 8 CPU cores. The case of Cu precipitation in Fe-1.34at.%Cu under electron irradiation is used. A $8,000$-VEs box with 10 nm length per VE is employed in both our parallel SRSCD code and SP-SRSCD code. Other simulation parameters and configurations are the same with accuracy tests. We track the number of defect types and different reaction types over time, and get the average memory usage per core and per defect type and its associated reactions based on the storage structures in the two codes.

For the computational performance tests in Fig. 10, the case of Cu precipitation in Fe-1.34at.%Cu under electron irradiation is used again. We perform our parallel SRSCD method and SP-SRSCD on 32, 64, 128, 256, and 512 CPU cores, respectively. For each test, a simulation box of 48×48×48 VEs (10 nm length per VE) is employed, and we track the computation time of our parallel SRSCD code and SP-SRSCD to simulate evolution for 100 seconds. Other simulation parameters and configurations are the same with accuracy tests.

For the parallel performance tests in Fig. 11, the case of vacancy accumulation in $\alpha$-Fe is used. We compare our parallel SRSCD with SP-SRSCD through weak scaling and in two cases: (1) an idealized case in which clustering reaction is not allowed and only Frenkel pair implantation, recombination, and diffusion are allowed; (2) a realistic case in which defect clustering reaction is also allowed. We track the runtime of our parallel SRSCD on 1, 2, 4, 8, 16, 32, and 64 CPU cores with a dose rate of $10^{-4}$ dpa/s, $10^{-3}$ dpa/s, $10^{-2}$ dpa/s, $10^{-1}$ dpa/s, and 1 dpa/s, respectively. All simulations are performed with 1000 VEs per cores and 20 nm length per VE. Simulations with and without clustering reactions are all started from $10^{-4}$ dpa to $10^{-3}$ dpa, the same as that of SP-SRSCD[10].

For the scalability tests in Fig. 12, a case of Cu precipitation in Fe-0.3at.%Cu under neutron irradiation with a 100 s simulation time is used. For the strong scalability, we take a fixed box with 25.6 million VEs (10 nm length per VE) and run tests on $1,600$, $3,200$, $6,400$, $12,800$, and $25,600$ CPU cores. For the weak scalability, we keep 1000 VEs (10 nm length per VE) per CPU core and run tests on $1,600$, $3,200$, $6,400$, $12,800$, $25,600$, and $32,000$ CPU cores. The test on $1,600$ cores is used as the baseline to calculate the parallel efficiency.

*Software Artifact Availability:* Some author-created software artifacts are NOT maintained in a public repository or are NOT available under an OSI-approved license.

*Hardware Artifact Availability:* There are no author-created hardware artifacts.

*Data Artifact Availability:* There are no author-created data artifacts.

*Proprietary Artifacts:* No author-created artifacts are proprietary.

## A.2 Artifact 1

*Persistent ID (GitHub URL):* https://github.com/ICPP2022/pap240-program

*Artifact name:* MISA-SLSCD

*Relevant hardware details:* The SunRising-1 computing platform is used for numerical simulations and performance evaluation in this work. Each node of the platform has 128 GB DDR4 memory, a Hygon Dhyana C86 7185 32-core CPU, and four Hygon DCU accelerators. The nodes adopt fat-tree topology and are connected through a 200 Gbps Infiniband HDR network.

*Operating systems and versions:* CentOS Linux release 7.6.1810

*Compilers and versions:* gcc-7.3.1

*Applications and versions:* MISA-SLSCD v1.0

*Key algorithms:* Adaptive synchronous algorithm