PIPELINING

Course Name

ICT 411: Computer Architecture and Organization

Course Teacher

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Referred Book

“Computer Architecture and Organization” by John P. Hayes

“Microprocessor Hardware Interfacing and Application” by Barry B. Brey

Pipelining

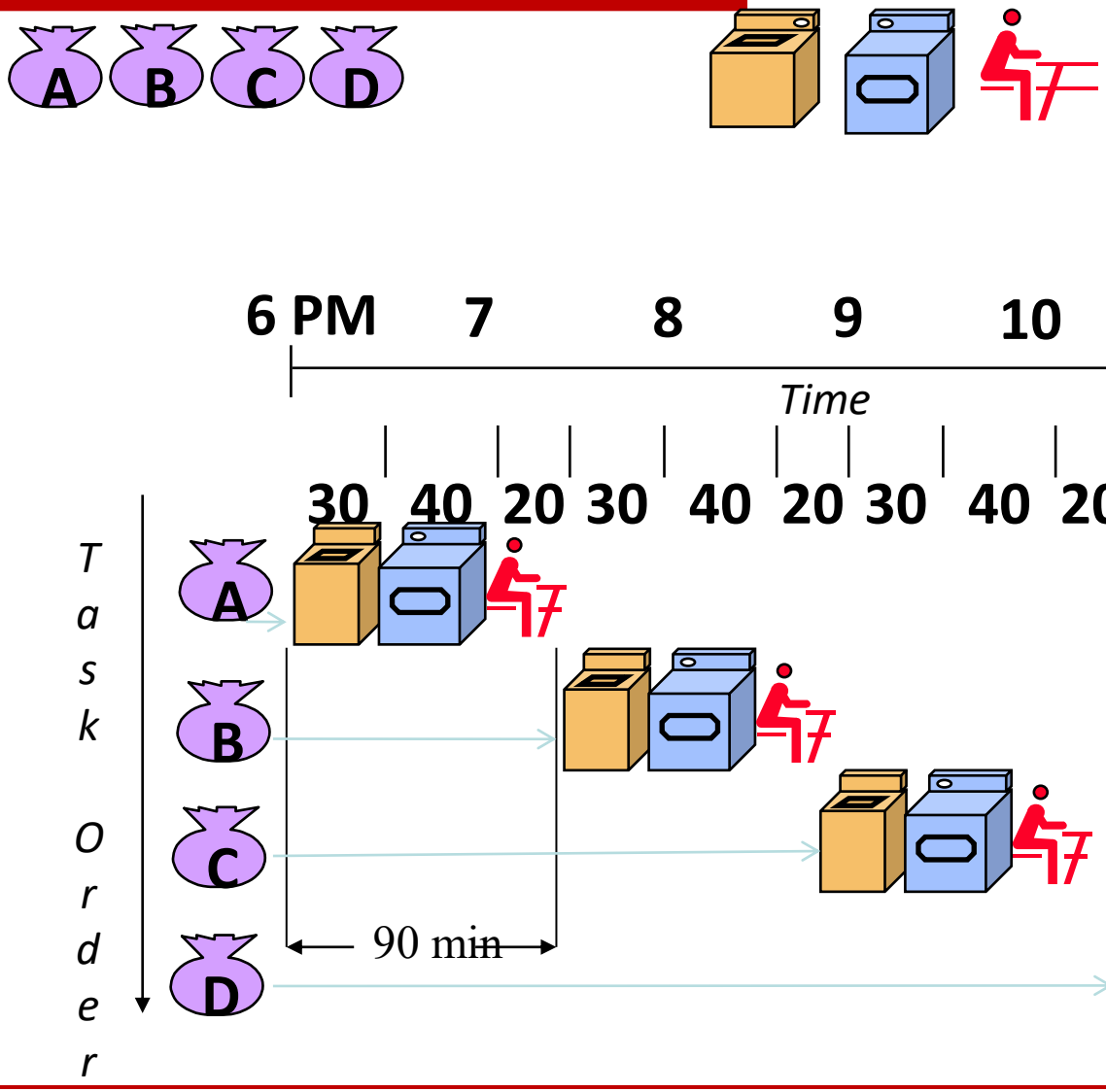
- It is a technique of decomposing a sequential process into segments
- A Pipeline is a series of stages, where some work is done at each stage. The work is not finished until it has passed through all stages.
- key to pipelining: division of a larger task into smaller overlapping tasks.

Pipelining (Contd.)

Example:

- There are **four loads** of dirty laundry that need to be washed, dried, and folded.
- We could put the first load in the **washer for 30** minutes, **dry it for 40** minutes, and then take **20 minutes to fold** the clothes.
- Then pick up the second load and wash, dry, and fold, and repeat for the third and fourth loads.
- Supposing we started at 6 PM and worked as efficiently as possible, we would still be doing laundry until midnight.

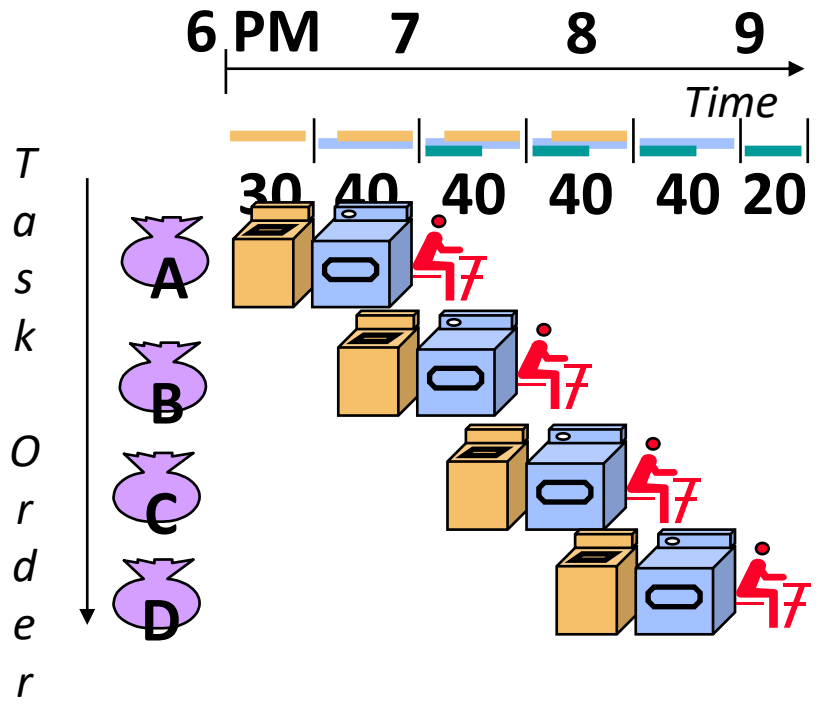
Pipelining (Contd.)



Pipelining (Contd.)

Example:

- A smarter approach to the problem would be to put the second load of dirty laundry into the washer after the first was already clean
- Then, while the first load was being folded, the second load would dry, and a third load could be added to the pipeline of laundry. Using this method, the laundry would be finished by 9:30.



Pipelining (Contd.)

Pipeline hazards:

- There are phenomena called pipeline hazards which **disrupt the smooth execution** of the pipeline. The resulting delays in the pipeline flow are called **bubbles**.
- A hazard is a potential problem that can happen in a pipelined processor. It refers to the possibility of erroneous computation when **a CPU tries to simultaneously execute multiple instructions which exhibit data dependence**.

Pipelining (Contd.)

Types of hazards:

- There are typically three types of hazards: data hazards, structural hazards, control hazard

- **structural** hazards from hardware conflicts (accessing two instruction to ALU at the same time)

- **data** hazards arising from data dependencies

- **control** hazards that come about from branch, jump, and other control flow changes

A **data dependency** occurs when an instruction depends on the results of a previous instruction.

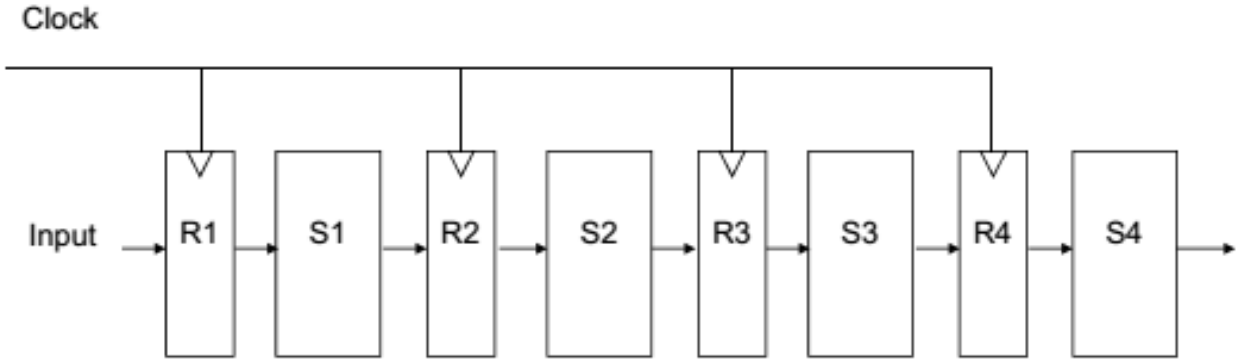
Pipelining (Contd.)

Four-segment pipeline

The simplest way of viewing the pipeline structure is to imagine that each segment consists of an **input register** followed by a **combinational circuit**

• The **register holds the data** and the combinational **circuit performs the suboperation** in the particular segment

• A clock is applied to all registers after enough time has elapsed to perform all segment activity. In this way the information flows through the pipeline one step at a time



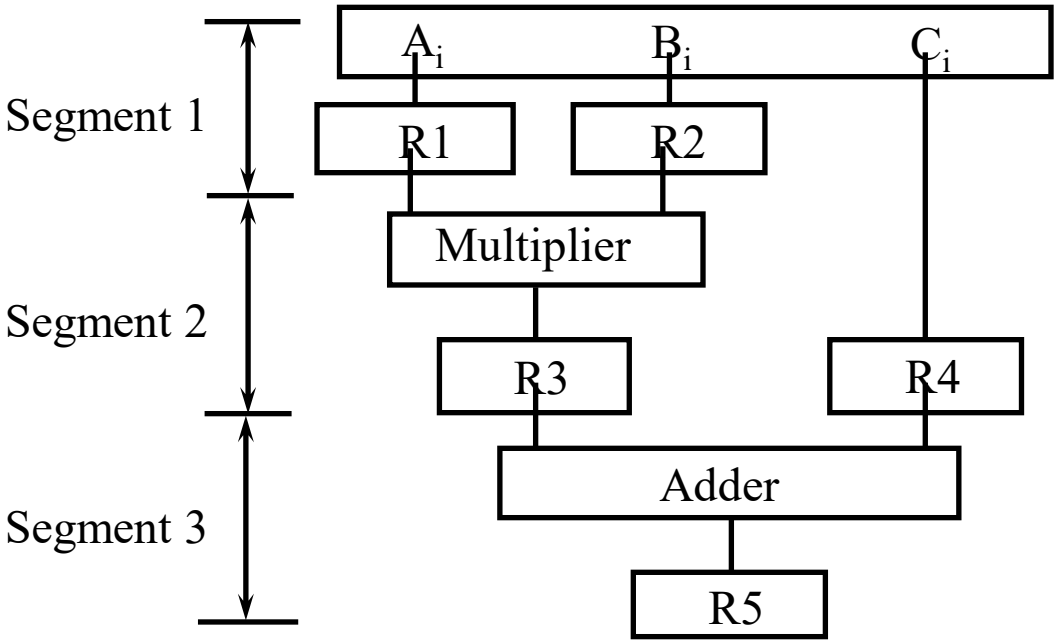
Pipelining (Contd.)

Example:

$A_i * B_i + C_i$ for i = 1, 2, 3, ... , 7

The suboperations performed in each segment are:

$R1 \leftarrow A_i$, $R2 \leftarrow B_i$	Load A_i and B_i
$R3 \leftarrow R1 * R2$, $R4 \leftarrow C_i$	Multiply and load C_i
$R5 \leftarrow R3 + R4$	Add



Pipelining (Contd.)

Example:

TABLE 9-1 Content of Registers in Pipeline Example

Clock Pulse Number	Segment 1		Segment 2		Segment 3
	$R1$	$R2$	$R3$	$R4$	$R5$
1	A_1	B_1	—	—	—
2	A_2	B_2	$A_1 * B_1$	C_1	—
3	A_3	B_3	$A_2 * B_2$	C_2	$A_1 * B_1 + C_1$
4	A_4	B_4	$A_3 * B_3$	C_3	$A_2 * B_2 + C_2$
5	A_5	B_5	$A_4 * B_4$	C_4	$A_3 * B_3 + C_3$
6	A_6	B_6	$A_5 * B_5$	C_5	$A_4 * B_4 + C_4$
7	A_7	B_7	$A_6 * B_6$	C_6	$A_5 * B_5 + C_5$
8	—	—	$A_7 * B_7$	C_7	$A_6 * B_6 + C_6$
9	—	—	—	—	$A_7 * B_7 + C_7$

Pipelining (Contd.)

Types of pipeline:

(i) Arithmetic pipeline

different stages of an arithmetic operation are handled along the stages of a pipeline

(ii) Instructional pipeline

different stages of an instruction fetch and execution are handled in a pipeline

Assignments

Assignment 1

Consider the following equation:

$$A_i + B_i * C_i$$

Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i =0 to 6

Assignment 2

Consider the following equation:

$$(A_i + B_i) * (C_i + D_i)$$

Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i =0 to 6

Questions

Thanks a lot!