VECTOR AND ARRAY PROCESSING

Course Name

ICT409: Computer Organization and Architecture

Course Teacher

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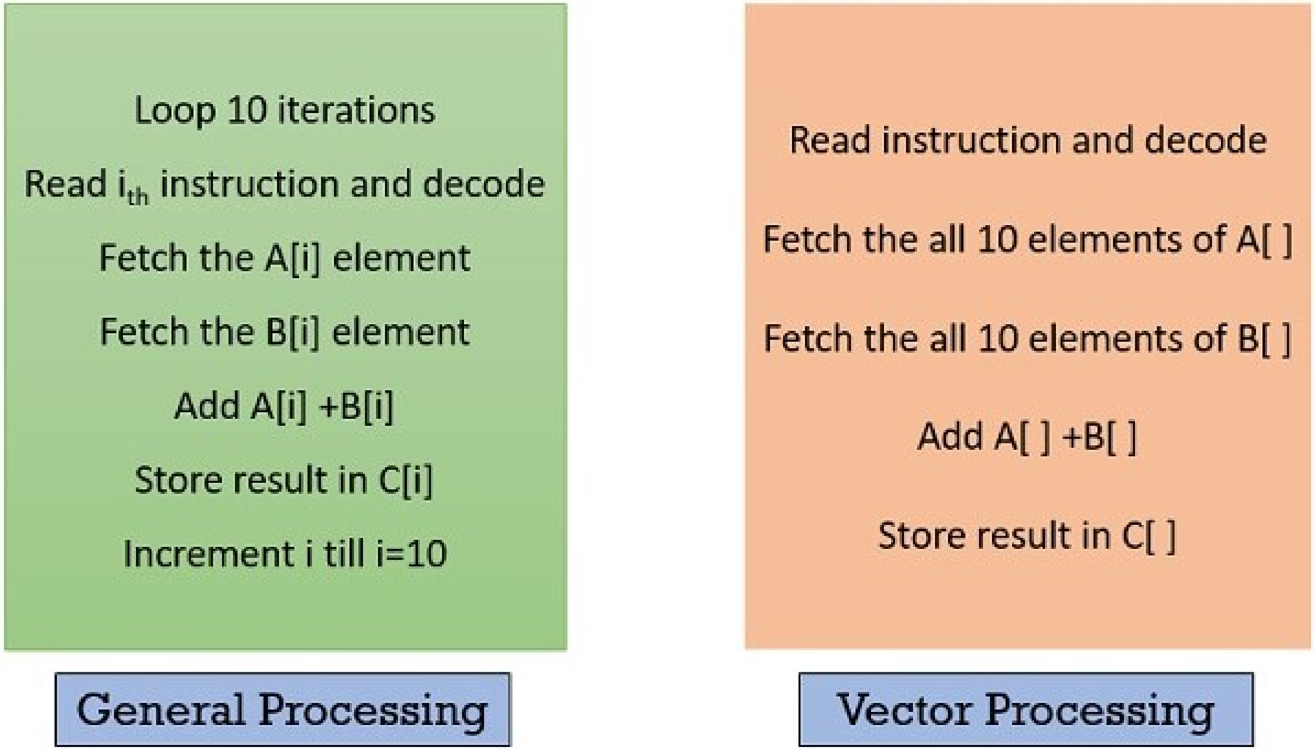
Vector Processing

- Ability to process vectors and related data structures such as matrices and multi-dimensional arrays, much faster than conventional computers
- Vector processing performs the arithmetic operation on the large array of integers or floating-point numbers. It operates on all the elements of the array in parallel providing each pass is independent of the other.

Vector Processing

Instructions in both the blocks are set to add two arrays and store the result in the third array. **Vector** processing adds both the array in parallel by avoiding the use of the loop.



Loop 10 iterations

Read i_{th} instruction and decode

Fetch the A[i] element

Fetch the B[i] element

Add A[i] +B[i]

Store result in C[i]

Increment i till i=10

General Processing

Read instruction and decode

Fetch the all 10 elements of A[ ]

Fetch the all 10 elements of B[ ]

Add A[ ] +B[ ]

Store result in C[ ]

Vector Processing

Vector Processing

- **Applications:**

1. Long range weather forecasting
2. Petroleum Exploration
3. Medical Diagnosis
4. Image Processing
5. Artificial Intelligence
6. Data analysis

Vector Processing

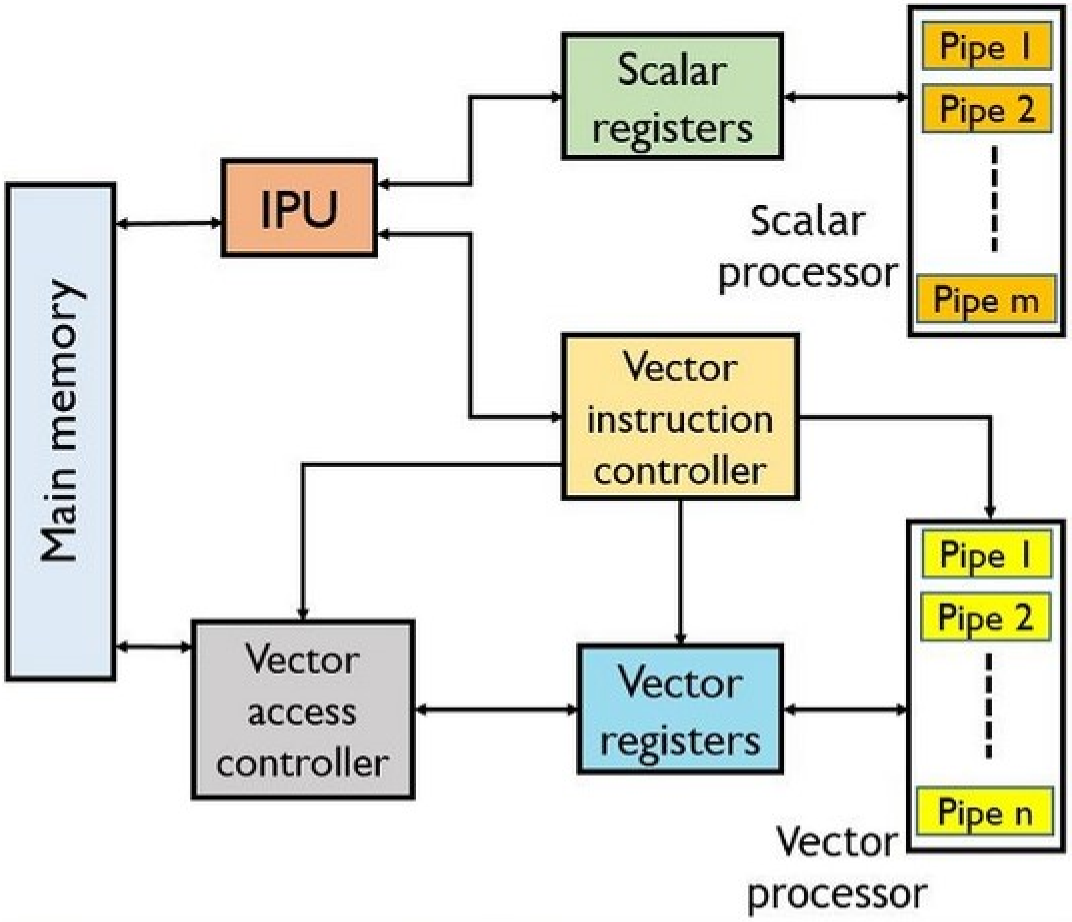
Comparison

- A **scalar processor** works on one or two data items, while the **vector processor** works with multiple data items. A **superscalar processor** is a combination of both.

Vector Processing

Architecture and Working

The figure below represents the typical diagram showing vector processing by a vector computer:



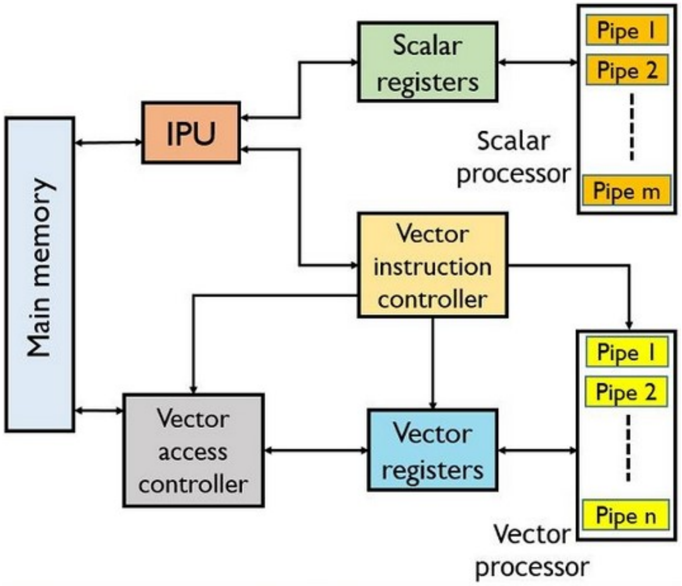
Functional Diagram of Vector Computer

Vector Processing

Architecture and Working

The functional units of a vector computer are as follows:

- IPU or instruction processing unit
- Scalar register
- Scalar processor
- Vector register
- Vector processor
- Vector instruction controller
- Vector access controller

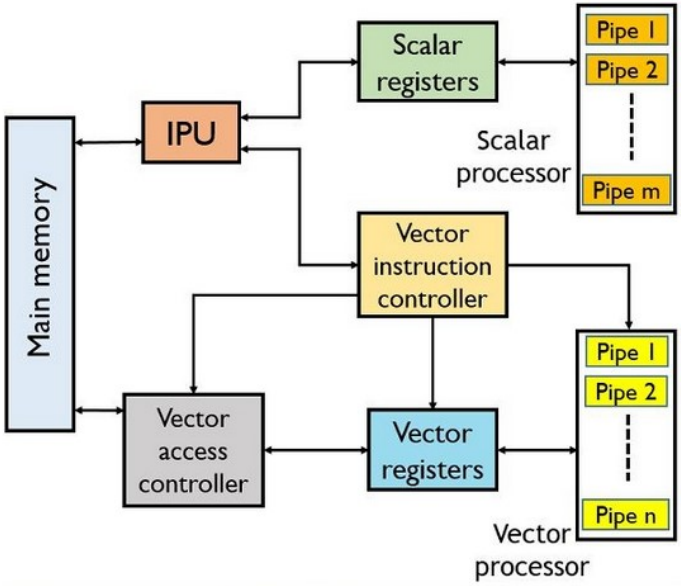


Functional Diagram of Vector Computer

Vector Processing

Architecture and Working

- Both data and instructions are present in the memory at the desired memory location. The instruction processing unit i.e., **IPU** fetches the instruction from the **memory**.
- Once the instruction is fetched then IPU determines either the fetched instruction is scalar or vector in nature. If it is **scalar** in nature, then the instruction is transferred to the **scalar register** and then further **scalar processing** is performed.
- While, when the instruction is a **vector** in nature then it is fed to the **vector instruction controller**, which first decodes the vector instruction then accordingly determines the address of the vector operand present in the memory.

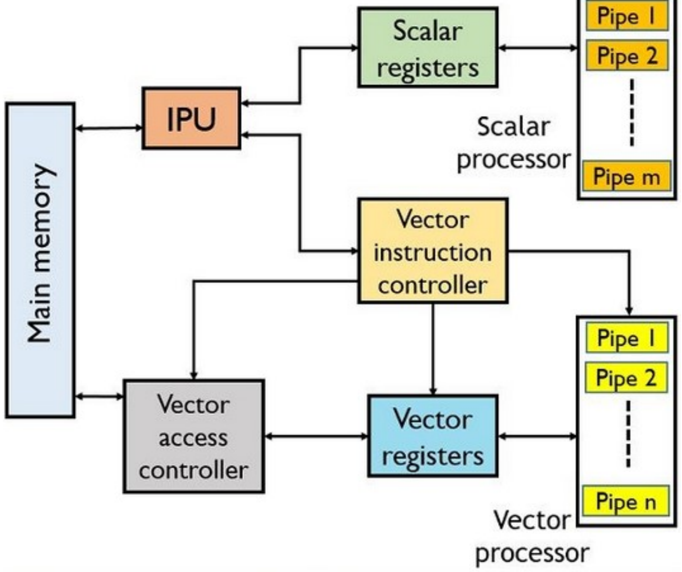


Functional Diagram of Vector Computer

Vector Processing

Architecture and Working

- Then it gives a signal to the **vector access controller** about the demand of the respective operand. This controller then fetches the desired operand from the memory. Once the operand is fetched then it is provided to the **instruction register** so that it can be processed at the vector processor.
- At times when multiple vector instructions are present, then the **vector instruction controller** provides the multiple vector instructions to the task system. And in case the task system shows that the vector task is very long then the processor divides the task into subvectors.
- These **subvectors** are fed to the vector processor that makes use of several pipelines in order to execute the instruction over the operand fetched from the memory at the same time. The various vector instructions are scheduled by the **vector instruction controller**.

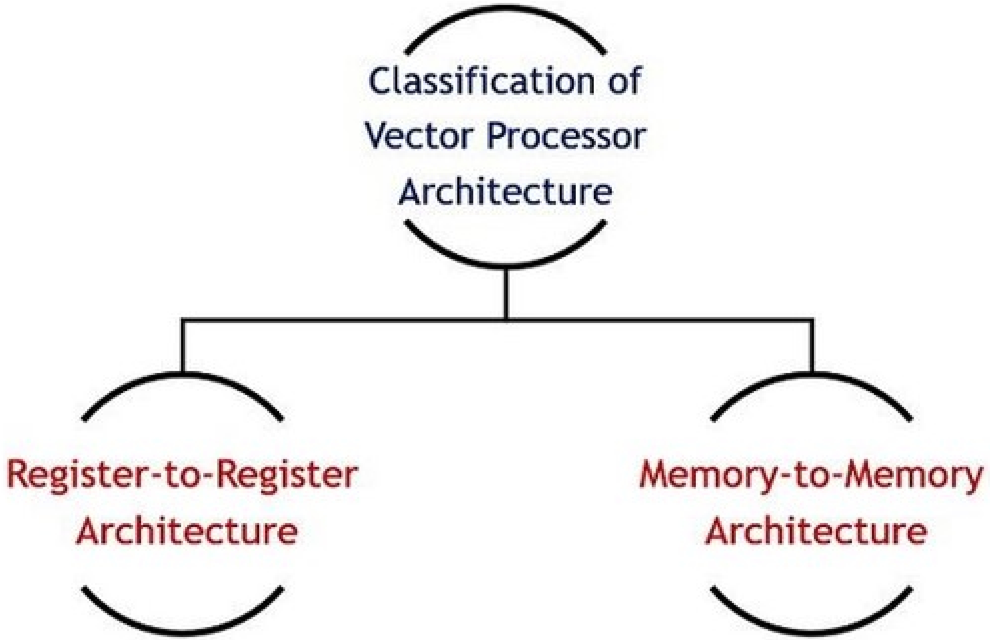


Functional Diagram of Vector Computer

Vector Processing

Classification

The classification of vector processor relies on the ability of vector formation as well as the presence of vector instruction for processing. So, depending on these criteria, vector processing is classified as follows:


Classification of Vector Processor Architecture
Register-to-Register Architecture
Memory-to-Memory Architecture

Vector Processing

Classification

Register to Register Architecture

- This architecture is highly used in vector computers. As in this architecture, the fetching of the operand or previous results indirectly takes place through the main memory by the use of registers.

Memory to Memory Architecture

- Here, the operands or the results are directly fetched from the memory despite using registers.

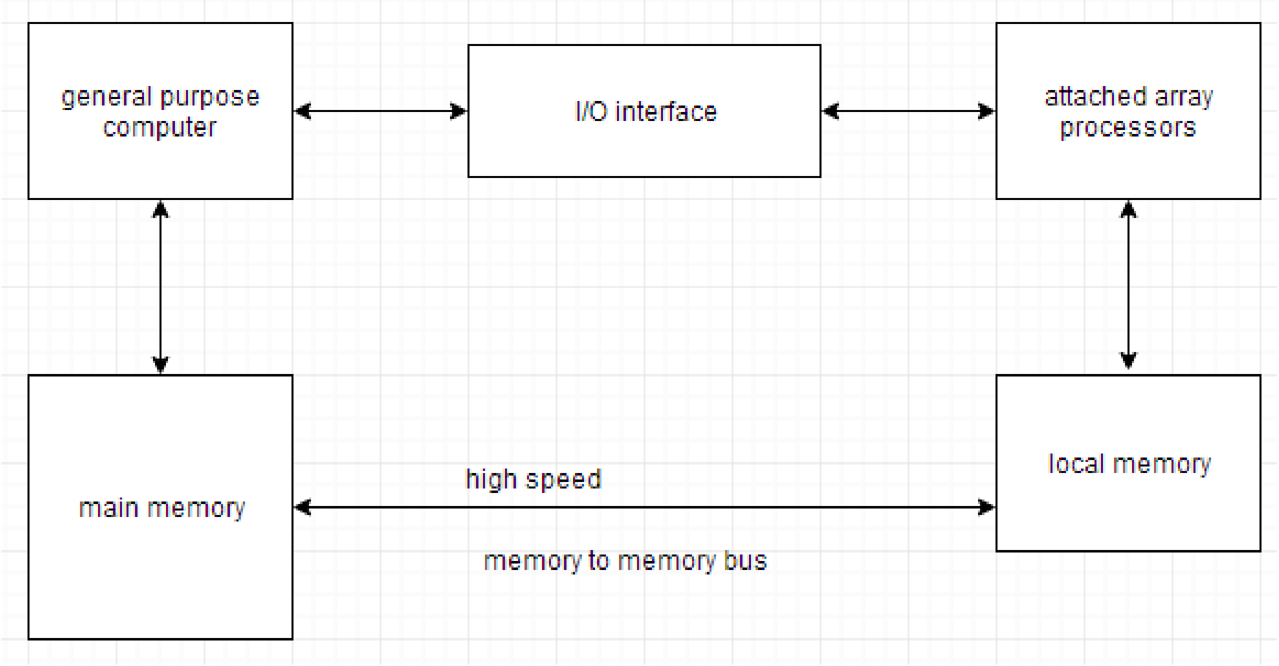
Array Processor

- Array processor performs computation on large arrays of data. They are used to improve the performance of the computer.
- Two different types of processor
  - Attached array processors
  - SIMD array processors

Array Processor

Attached array processors

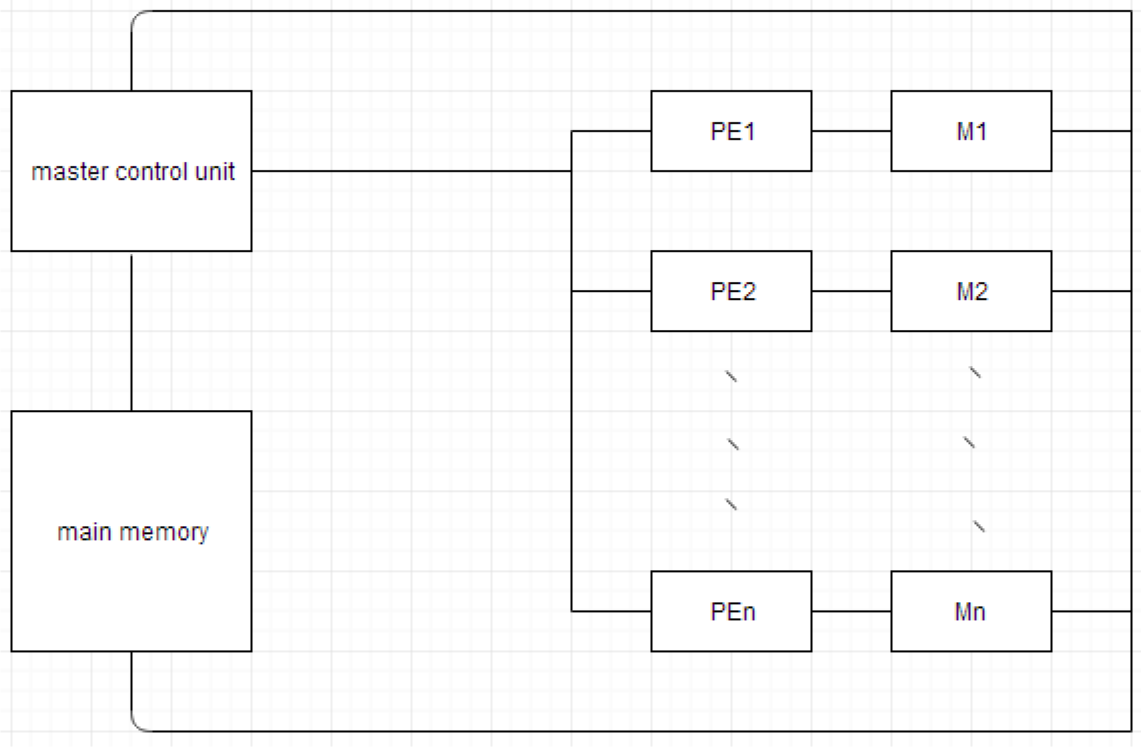
An attached array processor is a processor which is attached to a general purpose computer and its purpose is to enhance and improve the performance of that computer in numerical computational tasks. It achieves high performance by means of parallel processing with multiple functional units.



Array Processor

SIMD array processors

SIMD is the organization of a single computer containing multiple processors operating in parallel. The processing units are made to operate under the control of a common control unit, thus providing a single instruction stream and multiple data streams. A general block diagram of an array processor is shown below.



Array Processor

SIMD array processors

It contains a set of *identical* processing elements (PE's), each of which is having a local memory M. Each processor element includes an ALU and registers. The master control unit controls all the operations of the processor elements. It also decodes the instructions and determines how the instruction is to be executed.

The main memory is used for storing the program. The control unit is responsible for fetching the instructions. Vector instructions are sent to all PE's simultaneously and results are returned to the memory.

The best known SIMD array processor is the ILLIAC IV computer developed by the Burroughs corps. SIMD processors are highly specialized computers. They are only suitable for numerical problems that can be expressed in vector or matrix form and they are not suitable for other types of computations.

Array Processor

- Why use the Array Processor?
  - Array processors increases the overall instruction processing speed.
  - As most of the Array processors operates asynchronously from the host CPU, hence it improves the overall capacity of the system.
  - Array Processors has its own local memory, hence providing extra memory for systems with low memory.

Questions

Thanks a lot!