ICT 409

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Interconnection Structures

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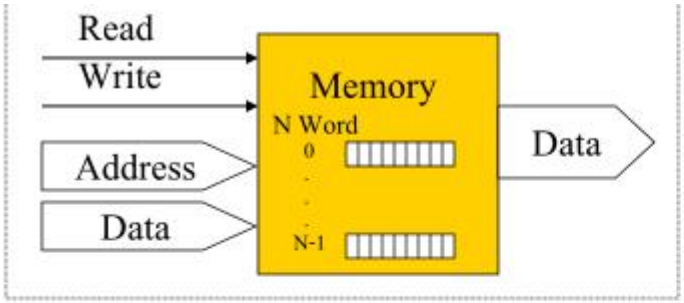
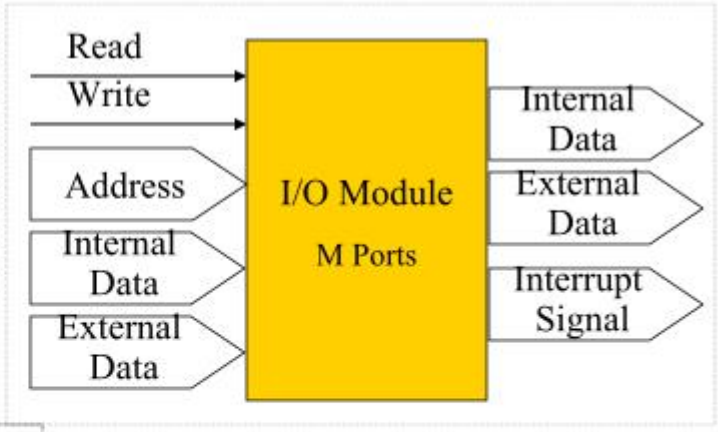
Outline

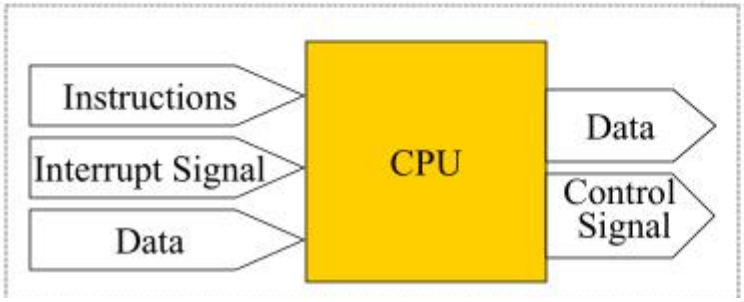
- Interconnection structure
- Types of transfer
- Intra and Inter system communication
- Bus control
  - Synchronous
  - Asynchronous
- Master and slave unit
- Arbitration
  - Daisy chaining
  - Polling
  - Independent requesting

Interconnection Structure

A **computer** *consists of* a set of components (CPU, memory, I/O) that communicate with each other. The collection of paths connecting the various modules is called the interconnection structure. The design of this structure will depend on the exchange that must be made between modules.







Types of transfer

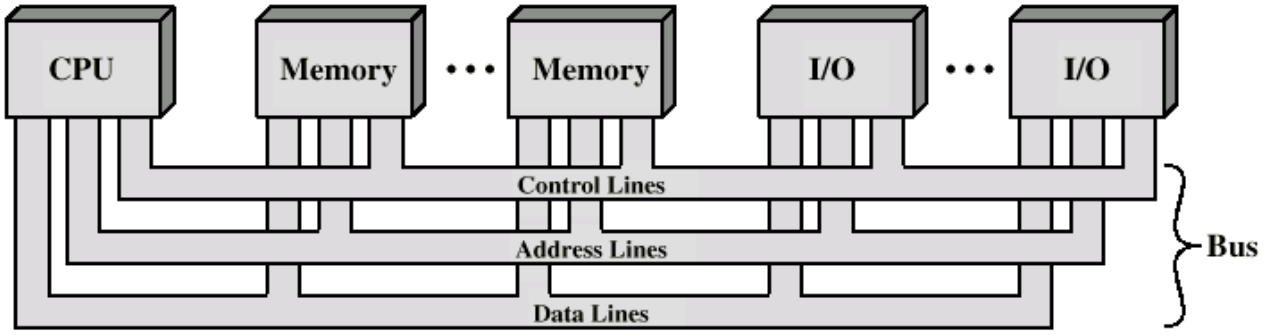
- Memory to CPU
- CPU to Memory
- I/O to CPU
- CPU to I/O
- I/O to or from Memory (DMA)

Intra and Inter system communication

- The difficulty in transferring information among the units of a computer depend on the physical distances
- *Intrasystem communication*
  - Which occurs within a **single computer system** and involves information transfer over distances of less than a meter
  - It is primarily implemented by groups of **electrical wires** called *buses*
- *Intersystem communication*
  - Which can involve communication over much **longer distances**
  - It is realized by a **variety of physical media**, including electrical cable, optical fiber, wireless link etc.

Bus

- A bus is a **set of physical connections** (cables, printed circuits, etc.) which can be shared by multiple hardware components in order to communicate with one another. A system bus consists of 50-100 lines.
- The various processor level components of a computer system are interconnected by buses
- It not only the physical links among the component but also the mechanism for controlling the exchange of signal



Communication within a computer via a single shared bus

Bus (contd.)

- The system bus consist of three main groups of lines
  - Address
    - It **transmits the addresses** of data item stored in the system's main memory or IO address space
  - Data
    - It **transmits data** over the bus
  - Control
    - It **manages the information flow** between components indicating whether the operation is a read or a write and ensuring that the operation happens at the right time

Bus Control

- Data transfers over the system bus may be
  - Synchronous
  - Asynchronous

Synchronous Bus

- Synchronous buses are the ones in which each item is transferred during a **time slot** (clock cycle) known to both the source and destination units
- Therefore, the bus interface circuits of both units are synchronized
- **Synchronization** is achieved by connecting both units to a common clock source

Asynchronous Bus

- Asynchronous buses are the ones in which each item being transferred is accompanied by a **control signal** that indicated its presence to the destination unit
- The destination can respond with another control signal to acknowledge receipt of the item

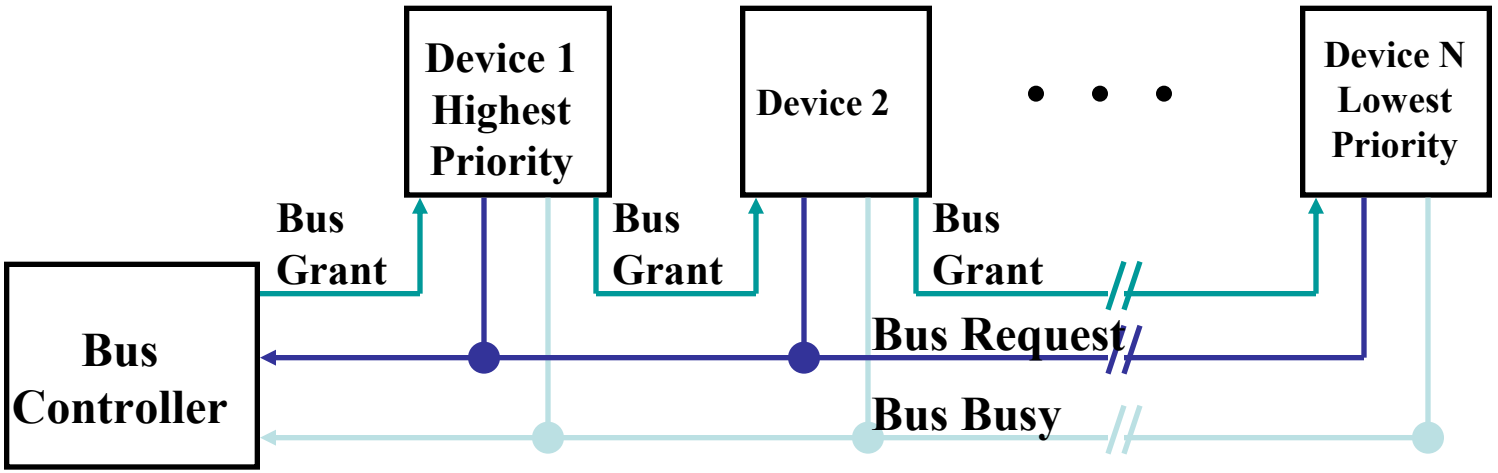
Master and slave unit

- The device currently in **control of the bus** is often termed the **bus master**
- Only a bus master may initiate a normal data transfer on the bus
- A device not currently bus master must **request control of the bus** before attempting to initiate a data transfer via the bus.
- The normal protocol is that only **one device may be bus master** at any time and that all other devices act as **slaves** to this master

Arbitration

- The possibility exists of several master/slave unit connected to a shared bus requesting **access at the same time.**
- A selection mechanism called bus arbitration
- In a single bus architecture when more than one device requests the bus, **a controller called bus arbiter decides who gets the bus**, this is called the bus arbitration.
- There are three main arbitration schemes
  - Daisy chaining
  - Polling
  - Independent requesting

Daisy Channing Arbitration

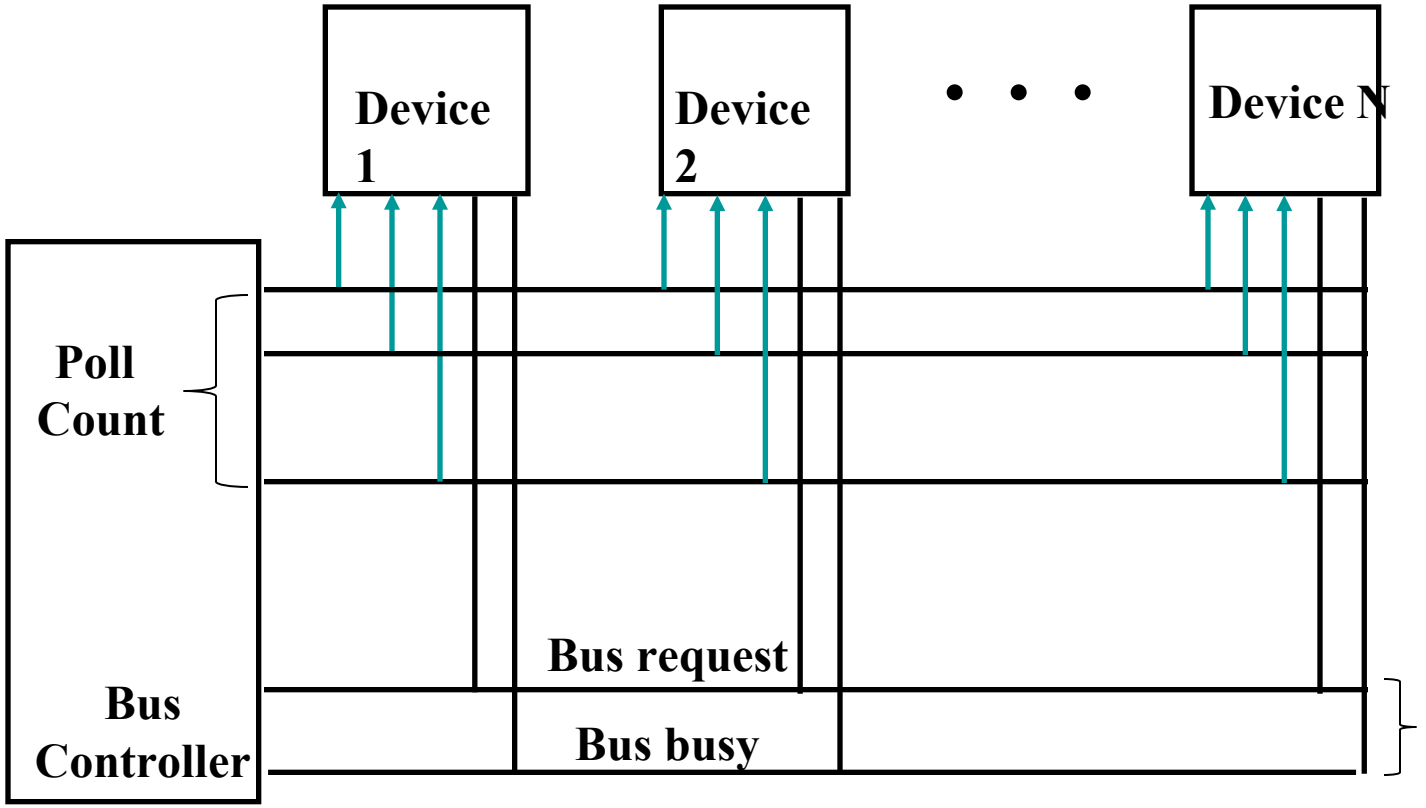


- This method involve three control signal
  - Bus request
  - Bus grant
  - Bus busy

Daisy Channing Arbitration (Contd.)

- All the bus units are connected to the **bus request** line
- When activated, it merely, serves to indicate that one or more units are requesting use of the bus
- The bus controller **responds to a bus request signal** only if **bus busy is inactive**
- This response takes the **form of a signal placed on the bus grant line**
- On the receiving the bus grant signal, a requesting unit enables its physical bus connection and activates bus busy for the duration of its new bus actively

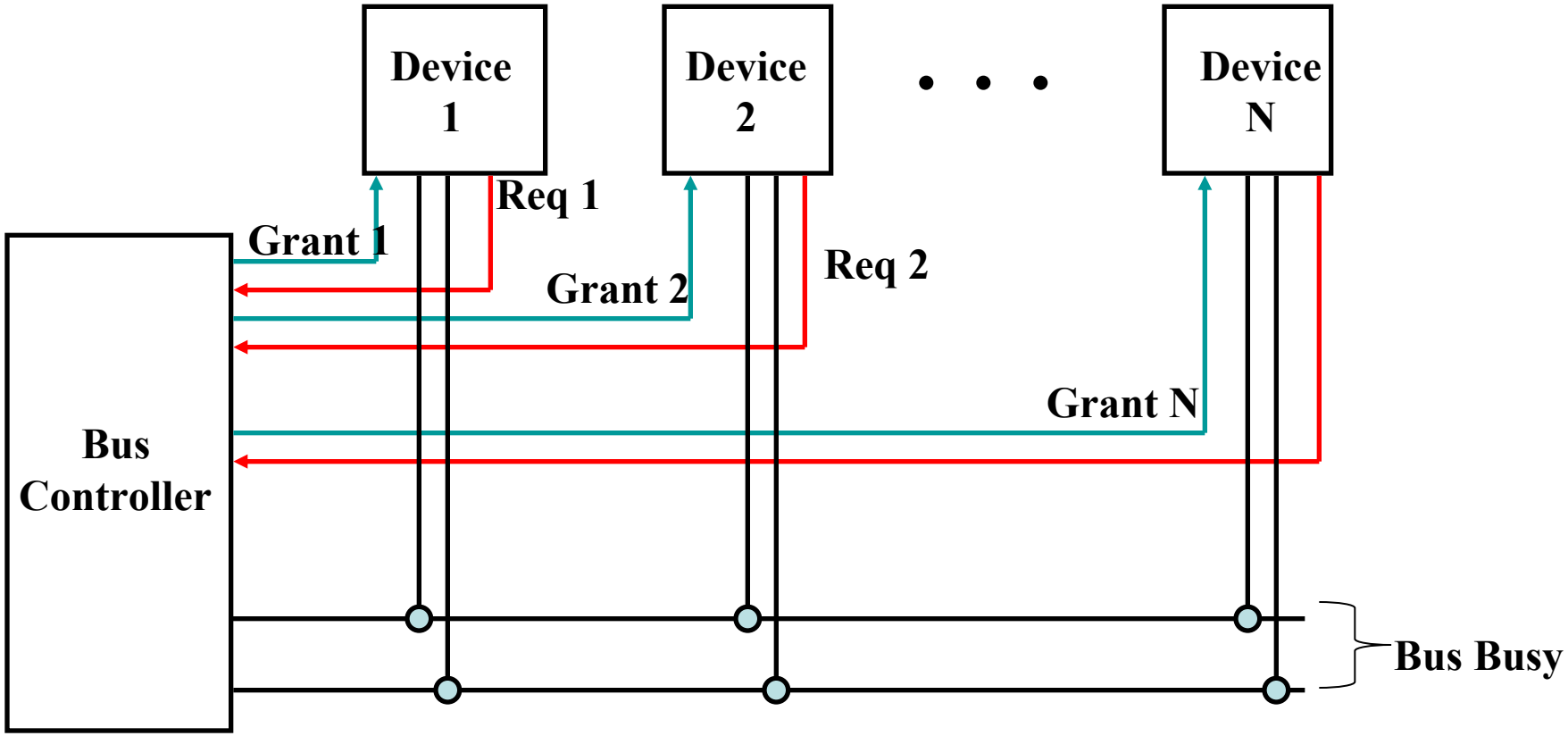
Polling Arbitration



Polling Arbitration (Contd.)

- Bus **grant line** of daisy chaining gets replaced by a **set of lines called poll count**
- On getting bus req. line **bus controller generates a sequence of addressing** on the poll count line in a predefined order
- Each **device compares its address** with that put on **the poll count line**
- If **equal**, the corresponding device **raises bus busy line** and **uses the bus**
- The bus controller responds by terminating the polling process

Independent Request Arbitration



Independent Request Arbitration (Contd.)

- **Separate bus request and bus grant line** for every unit sharing the bus
- Provide bus controller with immediate identification of all requesting units and enables it to request for bus access
- Main drawback
  - 2n bus request and bus grant line must be connecting to the bus controller in order to control n device

Questions

Thanks a lot!