

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

DWG NO	92-105229-01	SHT 138	REV A0
REVISION			
REV	ECO	DESCRIPTION	
A0	EA576148	RELEASE TO PRODUCTION	

1RU SUNDOWN1 MIN FW1201 ASIC  
48-PORTS SFP+ AND 6-PORTS QSFP

## MFG PART NUMBERS

AN1

---

SNPNLBL

VISHAY BOM

**SUPERFUZZ**  
NEW SUNDOWN1 FW1201 AND NEW PI  
BOM NUMBER 73-102931-01  
SCHEMATIC NUMBER 92-105229-01  
FAB NUMBER 28-102746-01  
ASSY PROCEDURE 61-106157-01  
ASSY NUMBER 60-105172-01

REV	DATE	DESCRIPTION
A0		RELEASE TO PRODUCTION BASE ON ELYSIAN P4 WITH NEW SUNDOWN1 MIN FW1201
P2		VRM CHANGES + OSC DUAL FOOTPRINT DUE TO SUPPLY SHORTAGE



QTY REQD	PART OR IDENTIFYING NO.			NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION		
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION DECIM ANGLES + <sup>xx</sup> <sub>xxx</sub> . <sup>+01</sup> <sub>.005</sub> ± <sup>1°</sup>			APPROVALS	DATE					
DRAWN BY BEYENE LULSEGED	CAD SHAHBAZ MAHMOOD								
MATERIAL	MECH JOSEPH PANG		TITLE: 1 RU TOR ELYSIAN/SUPERFUZZ 48 SFP28 AND 6 QSFP28 PORTS						
FINISH	ENGR BEYENE LULSEGED								
DO NOT SCALE DWG	TEST ?		SIZE <b>B</b>	CLASS CODE	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>	SCALE	DATE: Mon Mar 14 11:03:16 2022	1 OF 138

## TABLE OF CONTENTS

1	TITLE PAGE
3	BLOCK DIAGRAM
4	DATA CARD CONNECTOR
5	SYSTEM POWER CONNECTOR
6	POWER LEDS, HEADERS
7	MIFPGA: BANK 3, MIROM1, JTAG HDR
8	MIFPGA: BANK 5B & 6A
9	MIFPGA: BANK 4A & 5A
10	MIFPGA: BANK 7 & 8, DBG HDR/LEDS
11	MIFPGA: CONFIG, REFCLK, SERDES
12	MIFPGA: POWER & GROUND
13	IO EXPANDER CPLD 1
14	IO EXPANDER CPLD 2
15	IO EXPANDER CPLD 3
16	IO EXPANDER CPLD 4
17	ACT2, IDPROM
18	RFID, SIROM, TEMP SENSOR
19	MTG HOLES
20	SUNDOWN PORTS
21	SUNDOWN1 PCIE \ CLK
22	SUNDOWN POWER JTAG
23	SNDN IO LEVEL SHIFTER
24	SUNDOWN1 GPIO / MISC
25	RETIMER SFP <15:0>
26	RETIMER SFP <31:16>
27	RETIMER SFP <47:32>
28	RETIMER QSFP <3:0>
29	RETIMER QSFP <5:4>
30	CLOCK BLOCK DIAGRAM
31	ASIC CLOCKS
32	CLK156M25 AND CLK212M ASIC
33	CLK156M25 RETIMER
34	SYNCE PLL
35	SYNCE PLL POWER
36	103M JITTER ATTENUATOR
37	TOD PORT
38	GNSS CONNECTOR
39	GNSS POWER
40	ASIC CLOCK BUF
41	SFP SERDES MAPPING <15:0>
42	SFP SERDES MAPPING <31:16>
43	SFP SERDES MAPPING <47:32>
44	QSFP SERDES MAPPING <3:0>
45	QSFP SERDES MAPPING <5:4>
46	CLK BUF SHIFT REG
47	SFP TX RATE SEL (0..47) SHIFT REG
48	SFP RX RATE SEL (0..47) SHIFT REG
49	SFP+ HIERARCHY INSTANCIATION
50	QSFP+ UPLINK PORT
51	PWR, SUBDESIGNS/3P3V/3P3_SFP/5V
52	PWR, SUNDOWN1 POWER
53	PWR, A DOMAIN,P1V8

## TABLE OF CONTENTS

54	PWR, RETIMER DVDD AVDD
55	PWR, RETIMER P2V5RT
56	STATUS AND ENV LEDs
57	JTAG HEADER\BUFFER
58	JTAG HEADER\BUFFER 2
59	(SUNDOWN1) TITLE PAGE
61	(SUNDOWN1) SNDN_HS0_TO_HS8_N_S0
62	(SUNDOWN1) SNDN_HS9_TO_HS17_N_S0
63	(SUNDOWN1) SNDN_PCIE_CLK_JTAG_MISC
64	(SUNDOWN1) SNDN STRAP OPTIONS
65	(SUNDOWN1) SNDN_VDDA / VDDHA
66	(SUNDOWN1) SNDN_VDD / VDDIO
67	(SUNDOWN1) SNDN_GND
68	(SUNDOWN1) SNDN_DECAP_1
69	(SUNDOWN1) SNDN_DECAP_2
70	(SUNDOWN1) SNDN_DECAP_3
71	(SUNDOWN1) TITLE PAGE
73	(SUNDOWN1) SNDN_HS0_TO_HS8_N_S0
74	(SUNDOWN1) SNDN_HS9_TO_HS17_N_S0
75	(SUNDOWN1) SNDN_PCIE_CLK_JTAG_MISC
76	(SUNDOWN1) SNDN_STRAP_OPTIONS
77	(SUNDOWN1) SNDN_VDDA / VDDHA
78	(SUNDOWN1) SNDN_VDD / VDDIO
79	(SUNDOWN1) SNDN_GND
80	(SUNDOWN1) SNDN_DECAP_1
81	(SUNDOWN1) SNDN_DECAP_2
82	(SUNDOWN1) SNDN_DECAP_3
83	(SUNDOWN1) TITLE PAGE
85	(SUNDOWN1) SNDN_HS0_TO_HS8_N_S0
86	(SUNDOWN1) SNDN_HS9_TO_HS17_N_S0
87	(SUNDOWN1) SNDN_PCIE_CLK_JTAG_MISC
88	(SUNDOWN1) SNDN_STRAP_OPTIONS
89	(SUNDOWN1) SNDN_VDDA / VDDHA
90	(SUNDOWN1) SNDN_VDD / VDDIO
91	(SUNDOWN1) SNDN_GND
92	(SUNDOWN1) SNDN_DECAP_1
93	(SUNDOWN1) SNDN_DECAP_2
94	(SUNDOWN1) SNDN_DECAP_3
95	(SUNDOWN1) TITLE PAGE
97	(SUNDOWN1) SNDN_HS0_TO_HS8_N_S0
98	(SUNDOWN1) SNDN_HS9_TO_HS17_N_S0
99	(SUNDOWN1) SNDN_PCIE_CLK_JTAG_MISC
100	(SUNDOWN1) SNDN_STRAP_OPTIONS
101	(SUNDOWN1) SNDN_VDDA / VDDHA
102	(SUNDOWN1) SNDN_VDD / VDDIO
103	(SUNDOWN1) SNDN_GND
104	(SUNDOWN1) SNDN_DECAP_1
105	(SUNDOWN1) SNDN_DECAP_2
106	(SUNDOWN1) SNDN_DECAP_3
107	(BEARVALLEYX2_SUB) TITLE
108	(BEARVALLEYX2_SUB) BEARVALLEY-1
109	(BEARVALLEYX2_SUB) BEARVALLEY-2

## TABLE OF CONTENTS

110	(BEARVALLEYX2_SUB) BEARVALLEY-3
111	(BEARVALLEYX2_SUB) BEARVALLEY-4
112	(BEARVALLEYX2_SUB) TITLE
113	(BEARVALLEYX2_SUB) BEARVALLEY-1
114	(BEARVALLEYX2_SUB) BEARVALLEY-2
115	(BEARVALLEYX2_SUB) BEARVALLEY-3
116	(BEARVALLEYX2_SUB) BEARVALLEY-4
117	(BEARVALLEYX2_SUB) TITLE
118	(BEARVALLEYX2_SUB) BEARVALLEY-1
119	(BEARVALLEYX2_SUB) BEARVALLEY-2
120	(BEARVALLEYX2_SUB) BEARVALLEY-3
121	(BEARVALLEYX2_SUB) BEARVALLEY-4
122	(BEARVALLEYX2_SUB) TITLE
123	(BEARVALLEYX2_SUB) BEARVALLEY-1
124	(BEARVALLEYX2_SUB) BEARVALLEY-2
125	(BEARVALLEYX2_SUB) BEARVALLEY-3
126	(BEARVALLEYX2_SUB) BEARVALLEY-4
127	(BEARVALLEY_SUB) TITLE
128	(BEARVALLEY_SUB) BEARVALLEY-1
129	(BEARVALLEY_SUB) BEARVALLEY-2
130	(5V2_XV) CONTROLLER
131	(SFP2X12_SUB) TITLE
132	(SFP2X12_SUB) PORT_0-3
133	(SFP2X12_SUB) PORT_4-7
134	(SFP2X12_SUB) PORT_8-11
135	(SFP2X12_SUB) PORT_12-15
136	(SFP2X12_SUB) PORT_16-19
137	(SFP2X12_SUB) PORT_20-23
138	(SFP2X12_SUB) TITLE
139	(SFP2X12_SUB) PORT_0-3
140	(SFP2X12_SUB) PORT_4-7
141	(SFP2X12_SUB) PORT_8-11
142	(SFP2X12_SUB) PORT_12-15
143	(SFP2X12_SUB) PORT_16-19
144	(SFP2X12_SUB) PORT_20-23
145	(QSFP_SUB) QSFP_PORT_1-2
146	(QSFP_SUB) QSFP_PORT_1-2
147	(QSFP_SUB) QSFP_PORT_1-2
161	(FPGA3RAIL_9A_3A_3A) CONTROLLER
164	(MP_PS_LV) MULTI-PHASE POWER STAGE
165	(MP_PS_LV) MULTI-PHASE POWER STAGE
166	(MP_PS_LV) MULTI-PHASE POWER STAGE
167	(MP_PS_LV) MULTI-PHASE POWER STAGE
168	(MP_PS_LV) MULTI-PHASE POWER STAGE
169	(MP_PS_LV) MULTI-PHASE POWER STAGE
170	(MP_PS_LV) MULTI-PHASE POWER STAGE
171	(MP_PS_LV) MULTI-PHASE POWER STAGE
172	(MP_PS_LV) MULTI-PHASE POWER STAGE
173	(MP_PS_LV) MULTI-PHASE POWER STAGE
174	(MP_PS_LV) MULTI-PHASE POWER STAGE

TOC

		
SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE:	Mon Jul 1 21:22:14 2019
		2 OF 138

D

D

C

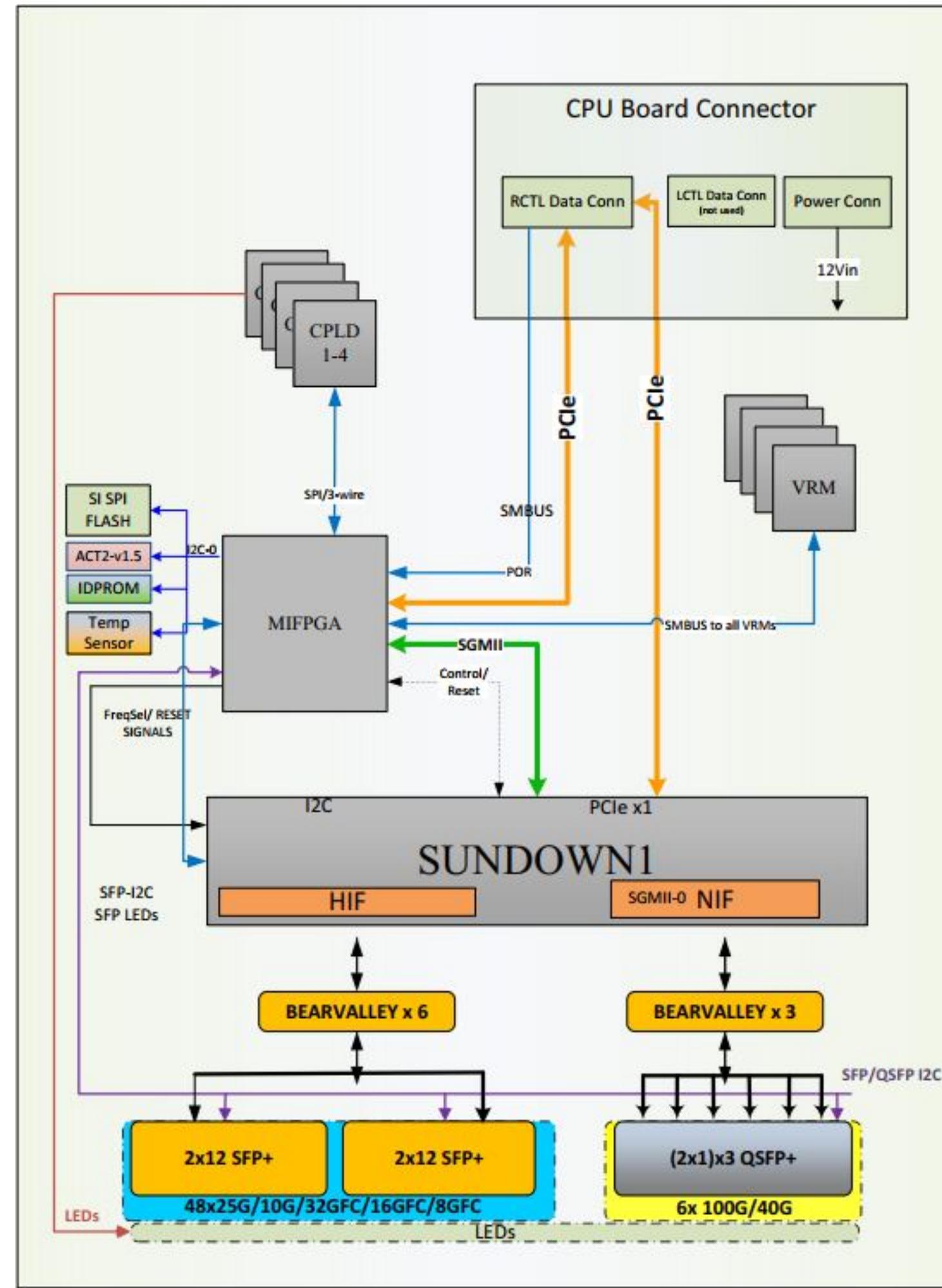
C

B

B

A

A



8

7

6

5

4

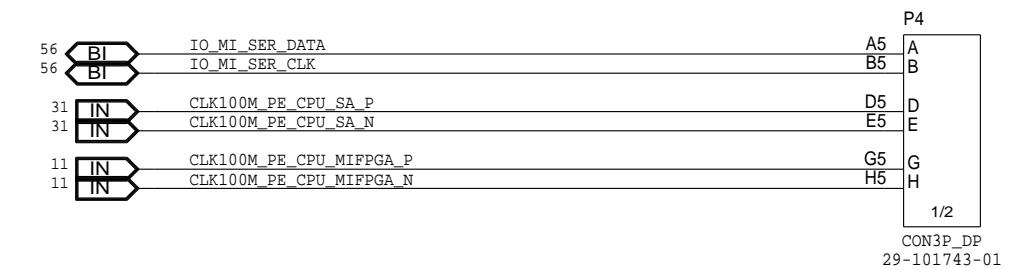
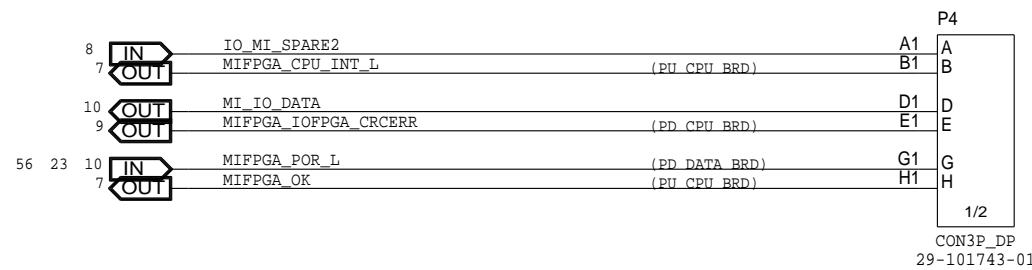
3

2

1

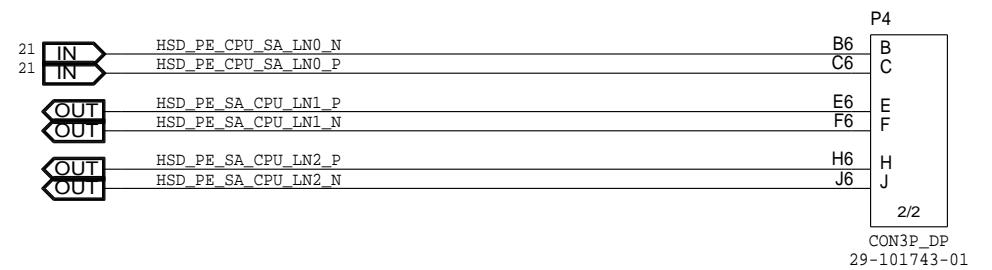
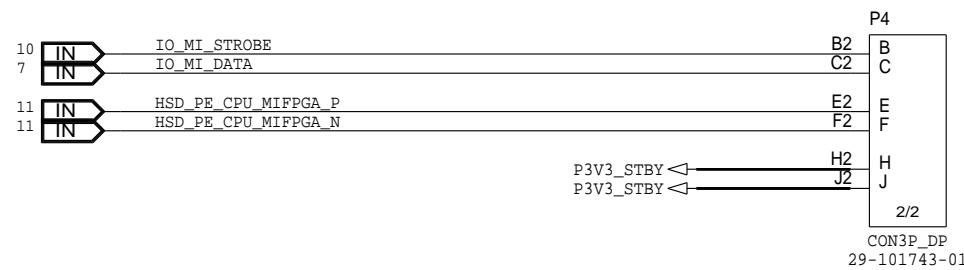
D

D



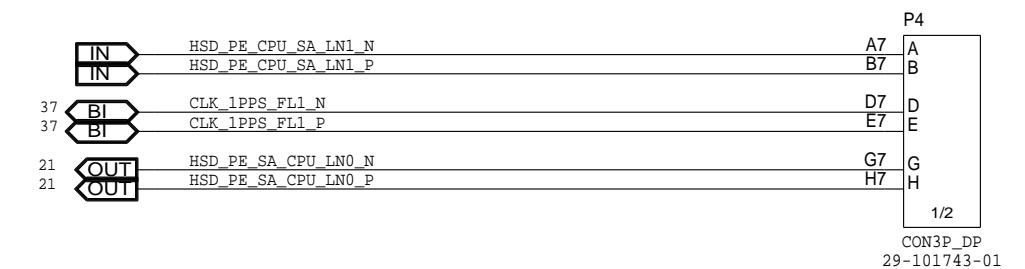
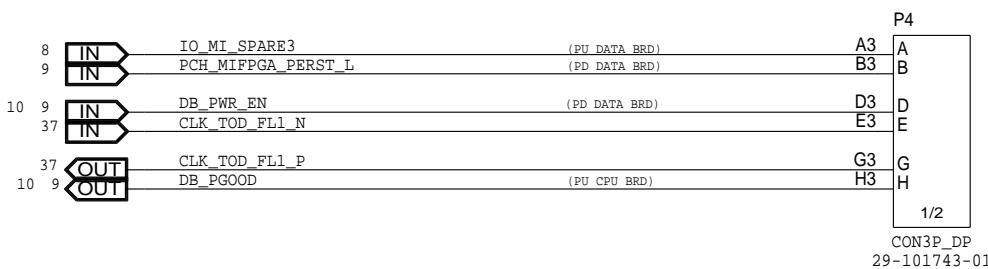
C

C



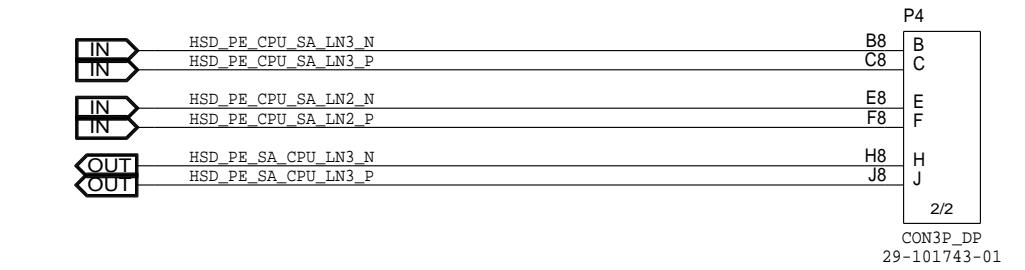
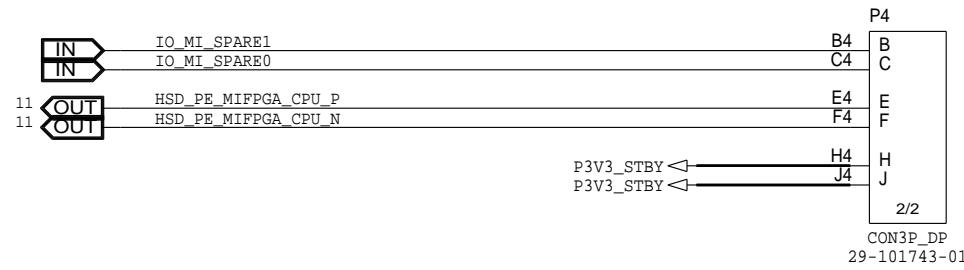
B

B



A

A



DATA CARD CONNECTOR



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE:	Mon Mar 14 11:03:16 2022	4 OF 138

8

7

6

5

4

3

2

1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

12V CAPACITANCE LOADING 2200UF TO 10000UF  
12V STDBY CAPACITANCE LOADING 200UF TO 1000UF  
NEED 5,000UF FOR 12MS HOLD UP TIME

D

D

C

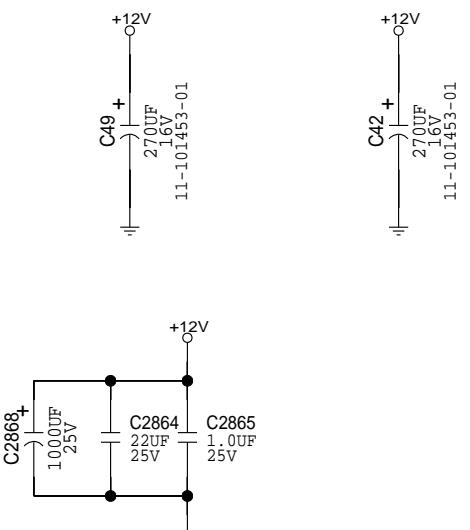
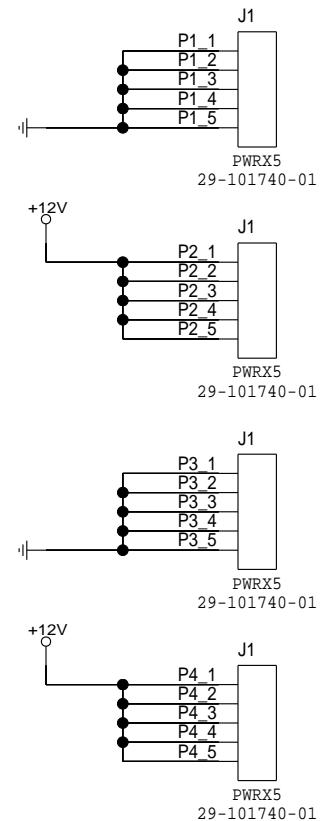
C

B

B

A

A



SYSTEM POWER CONNECTOR



SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0

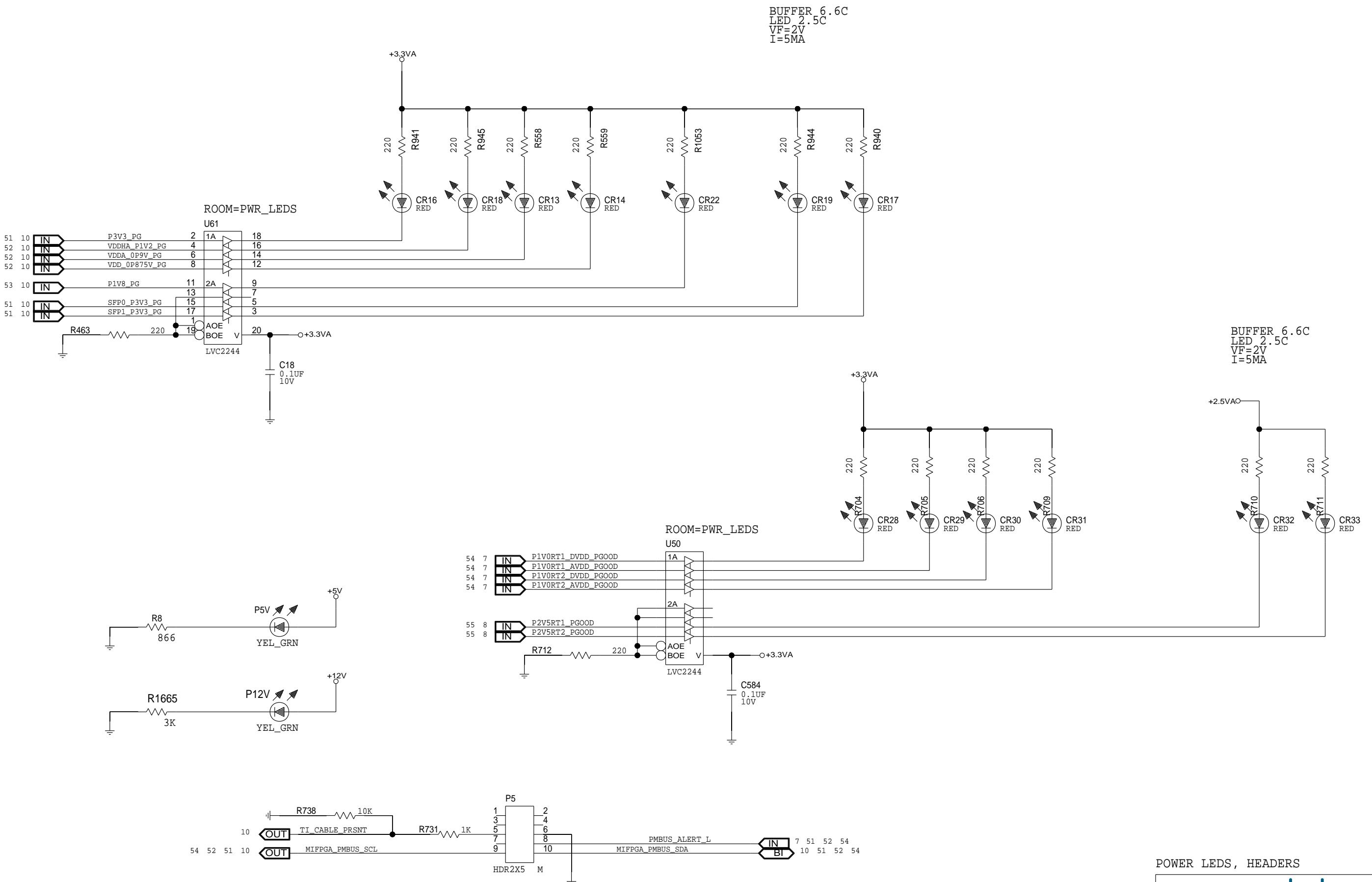
SCALE DATE: Mon Mar 14 11:03:15 2022 5 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

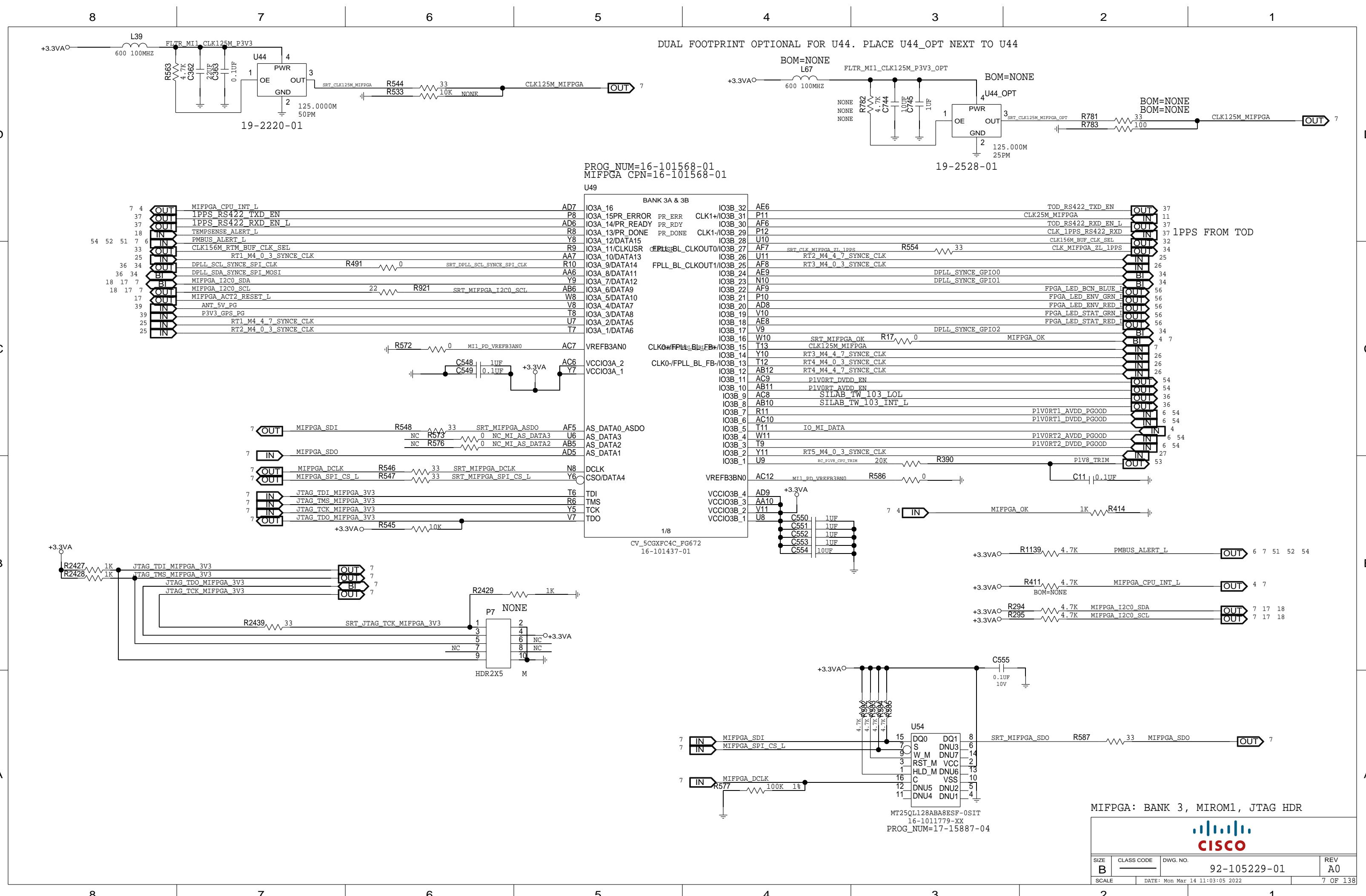


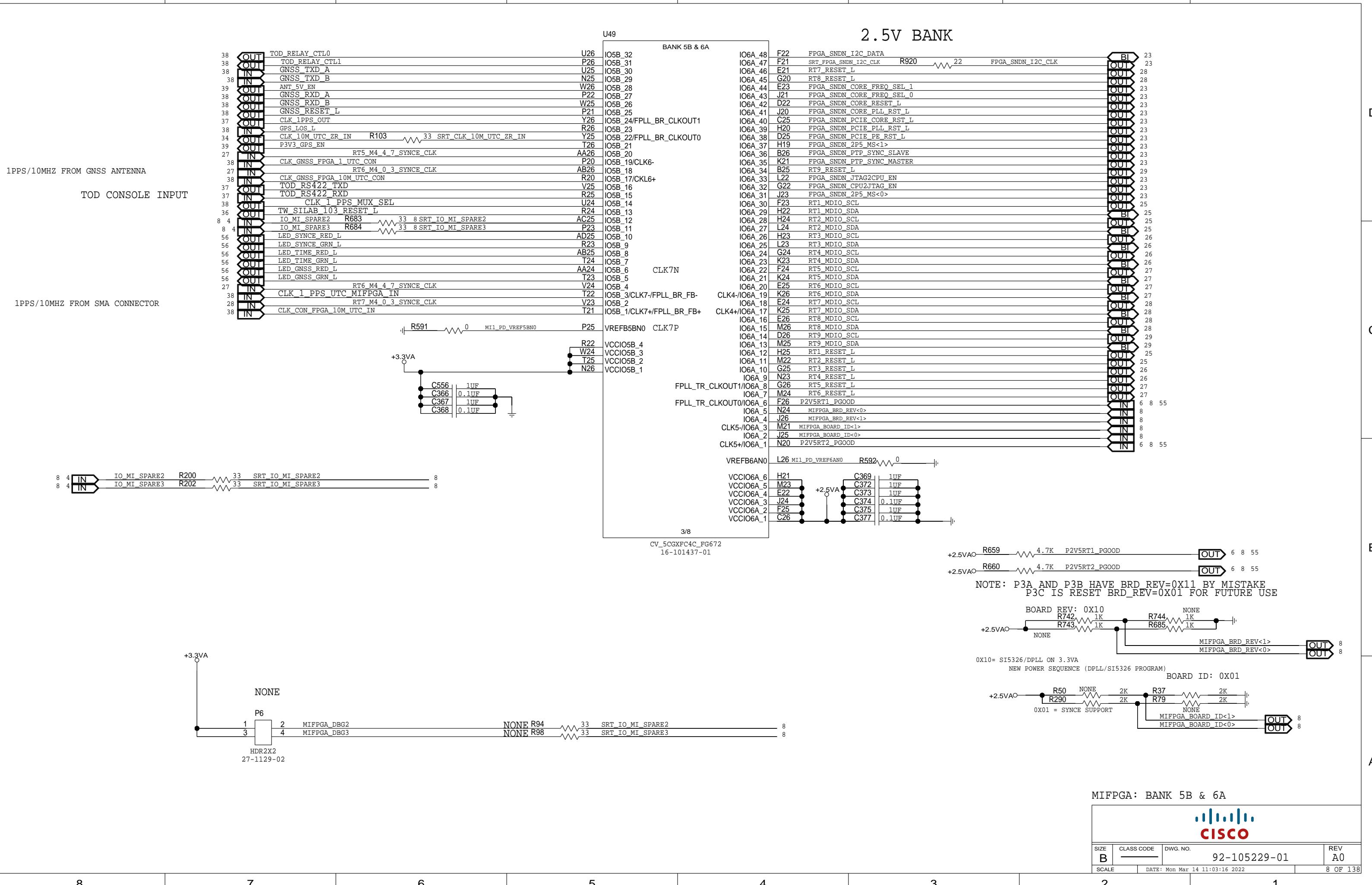
POWER LEDS, HEADERS

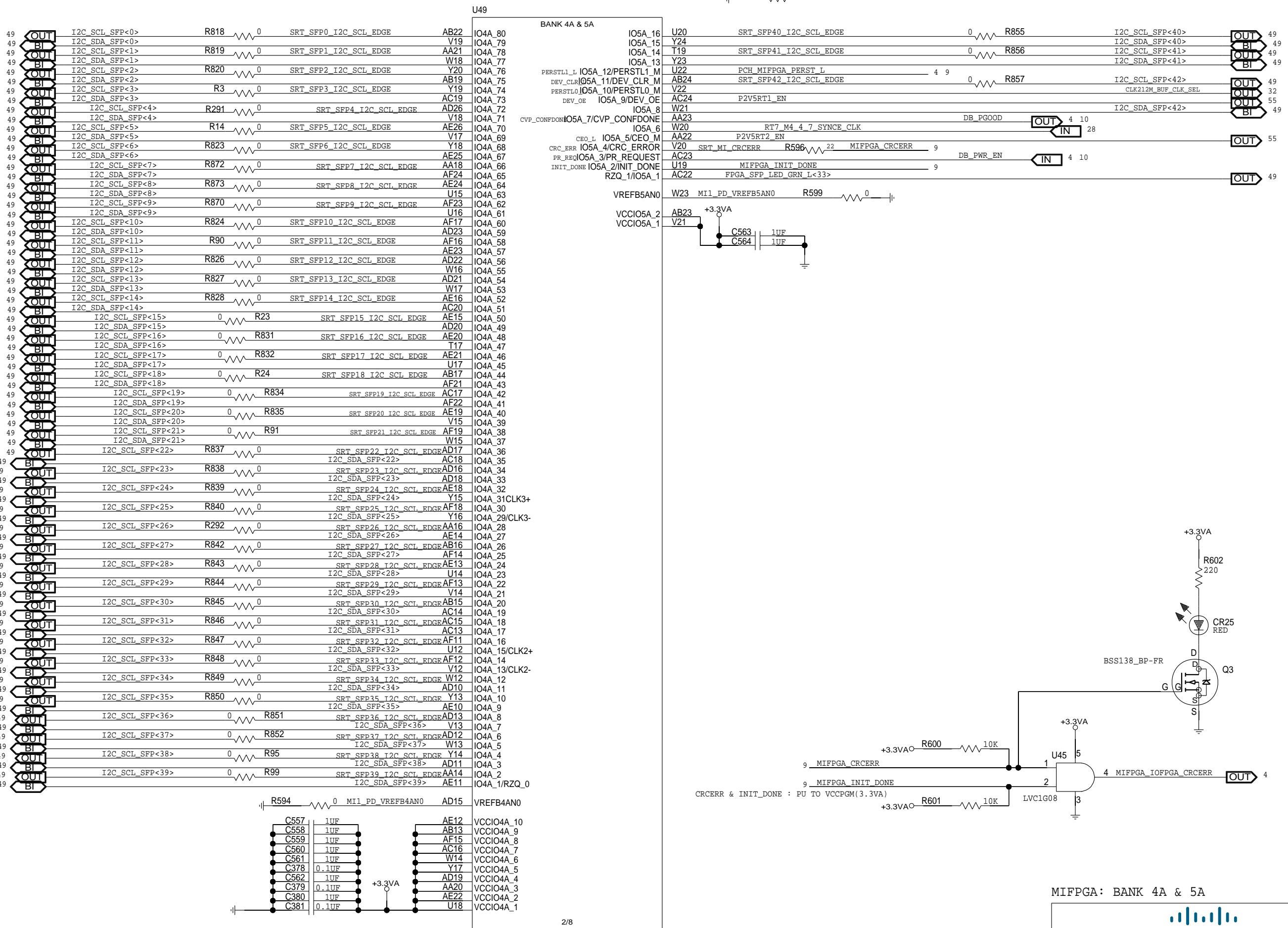


SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:05 2022	REV A0

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1







D

D

C

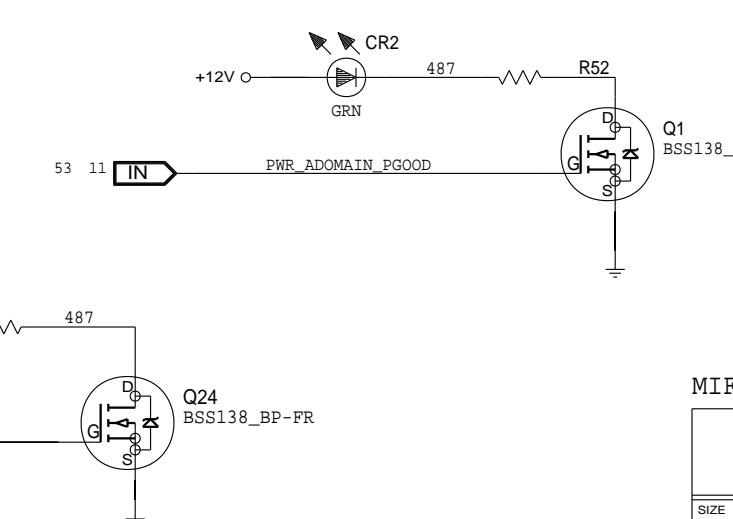
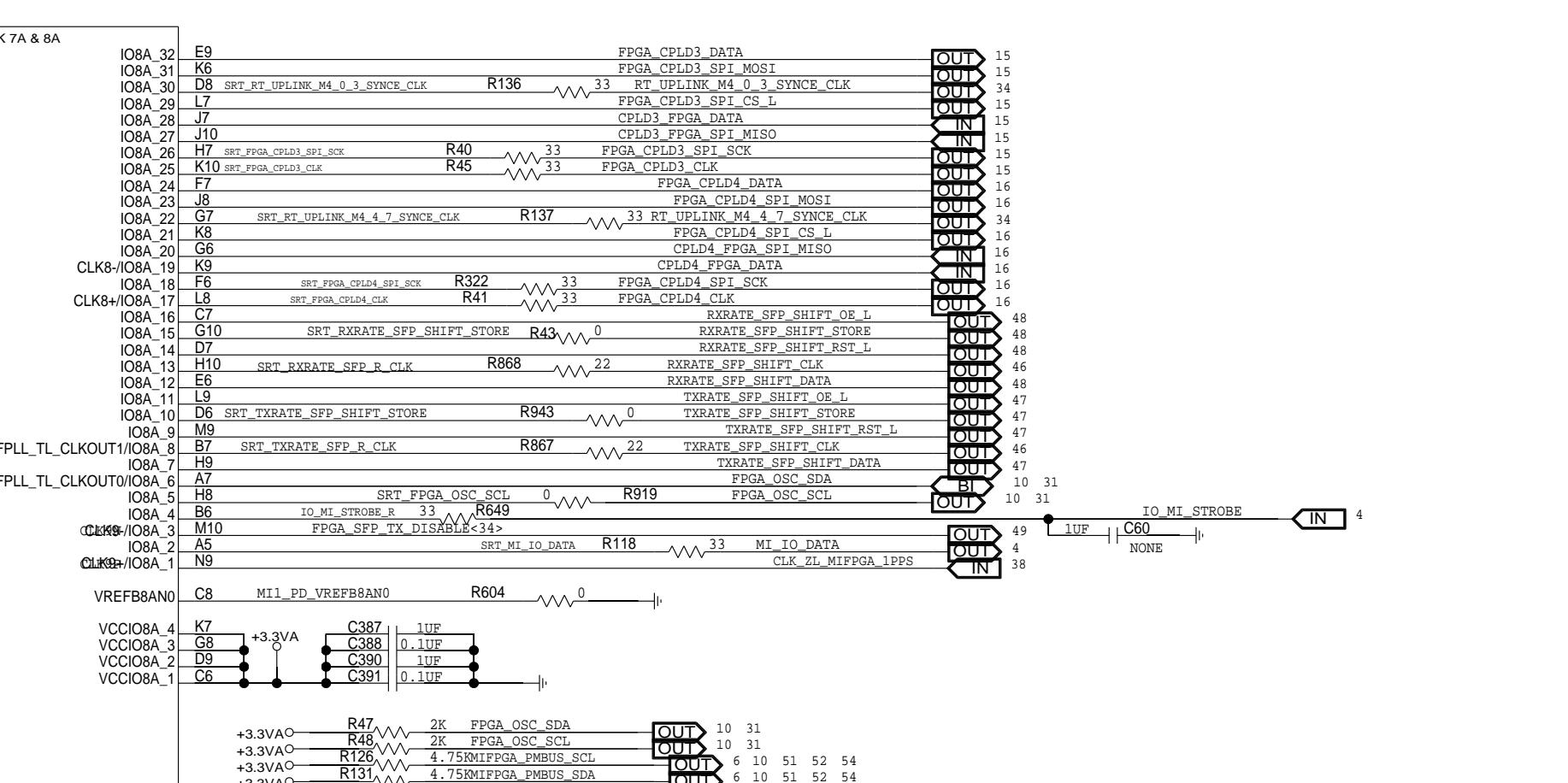
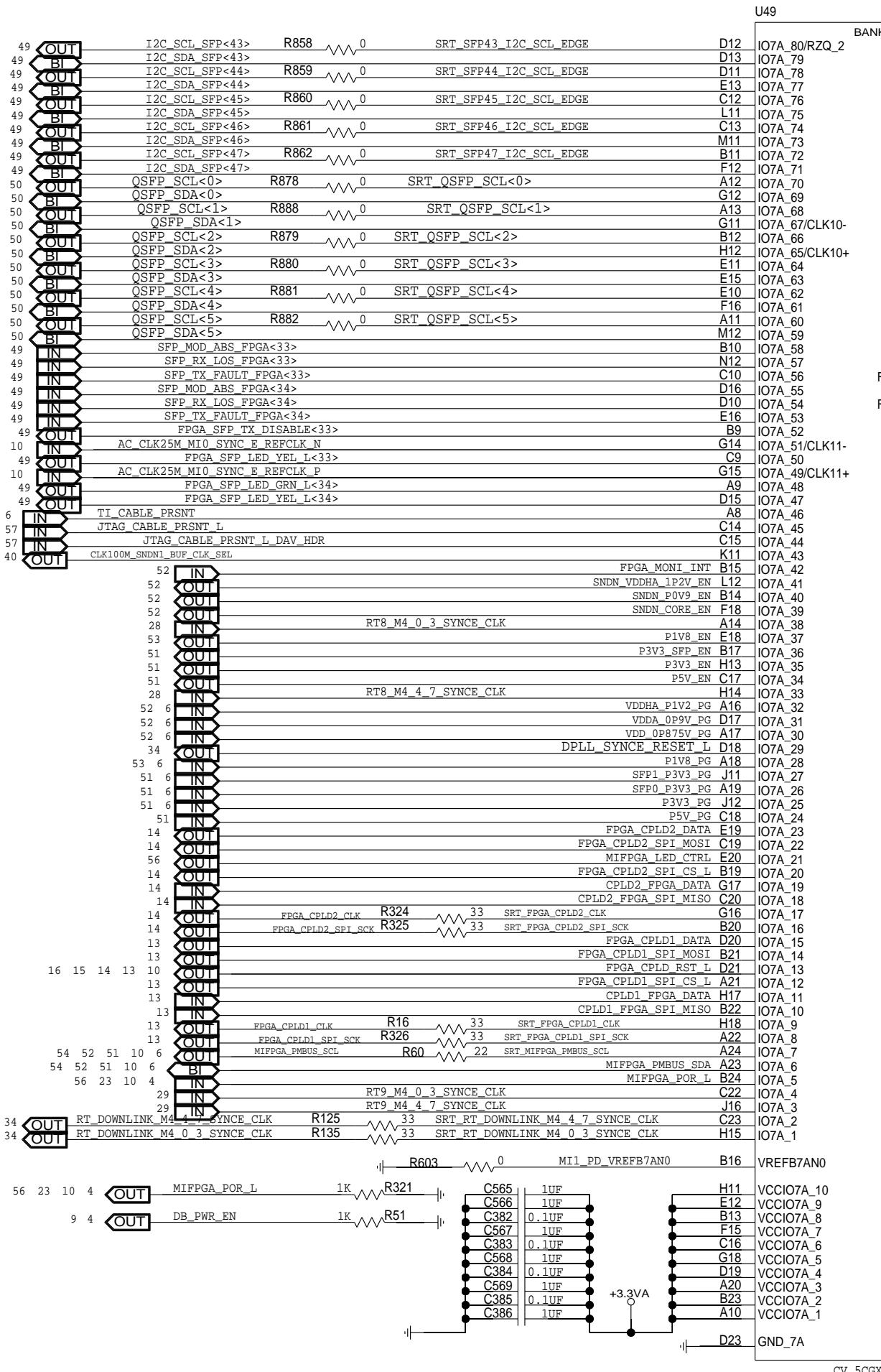
C

B

B

A

A



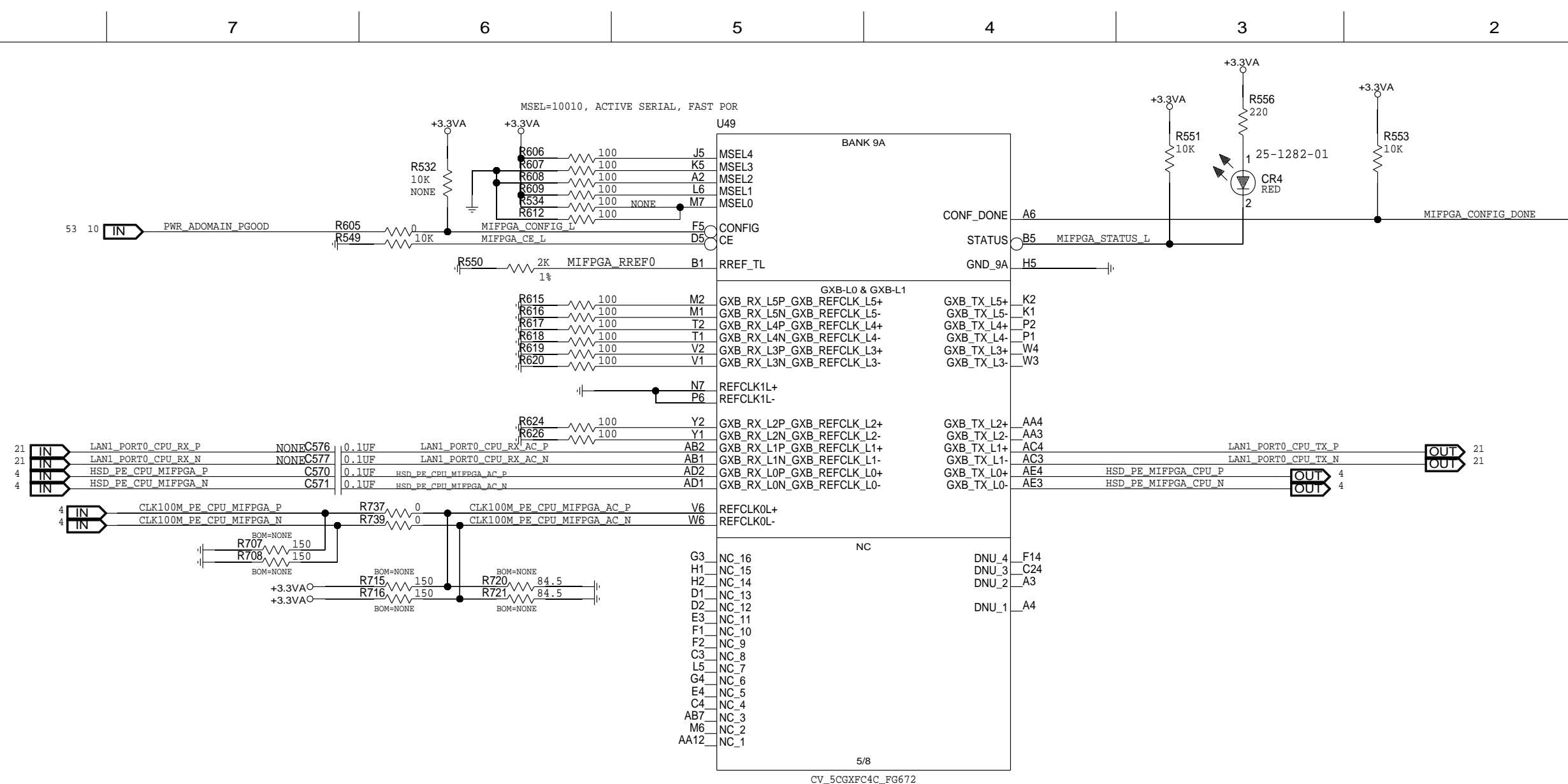
MIFPGA: BANK 7 &amp; 8, DBG HDR/LEDS



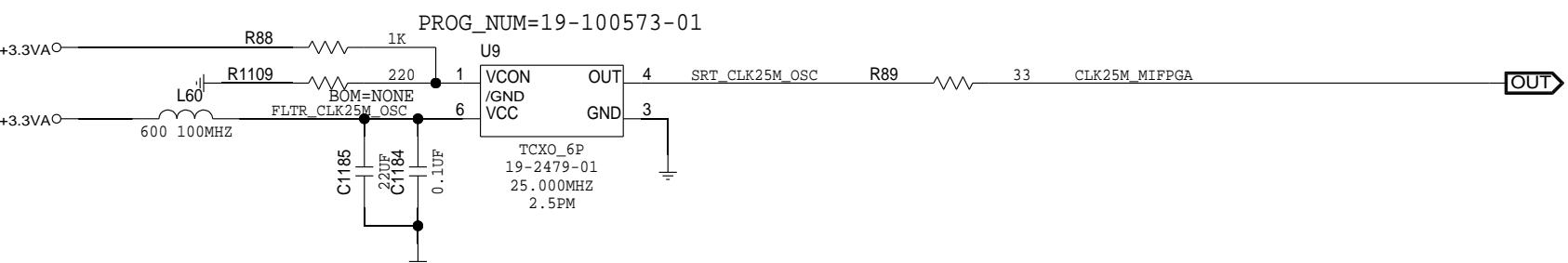
SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:06 2022	10 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D



WE CAN BOM NONE THIS  
USE THE 125MHZ FOR FPGA LOGIC



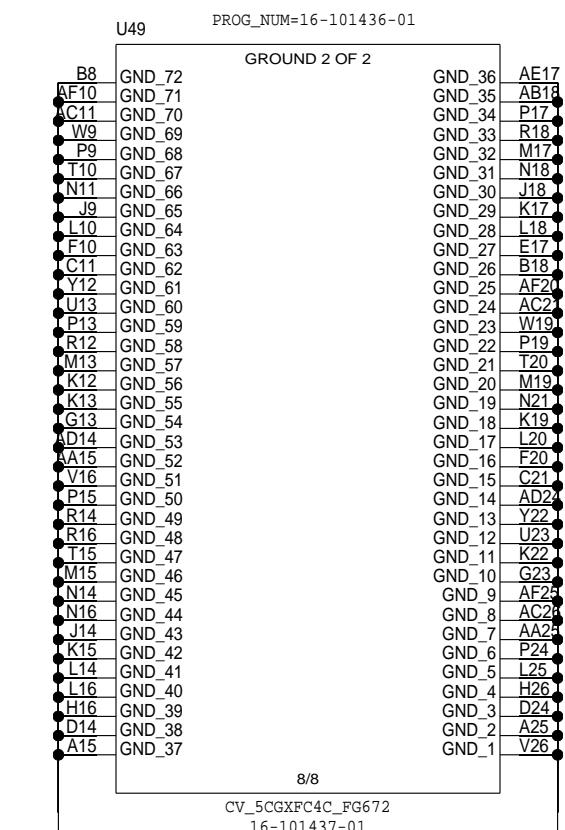
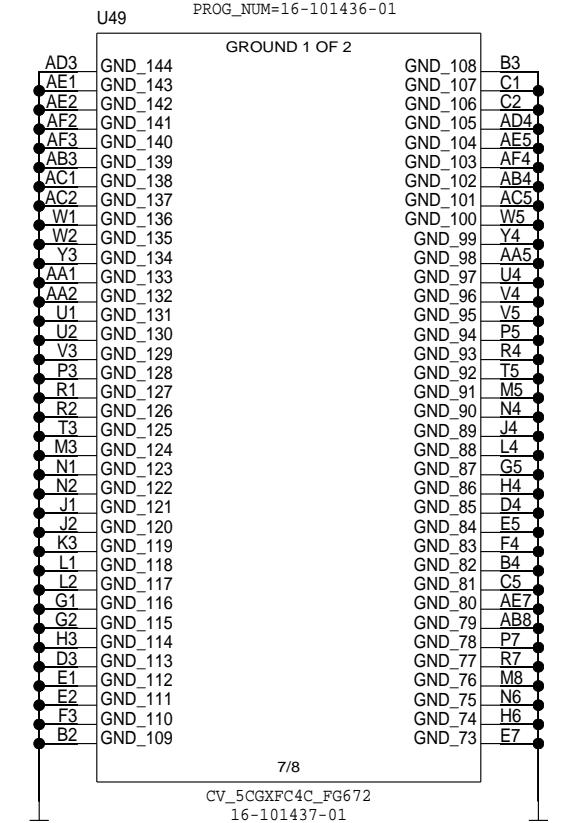
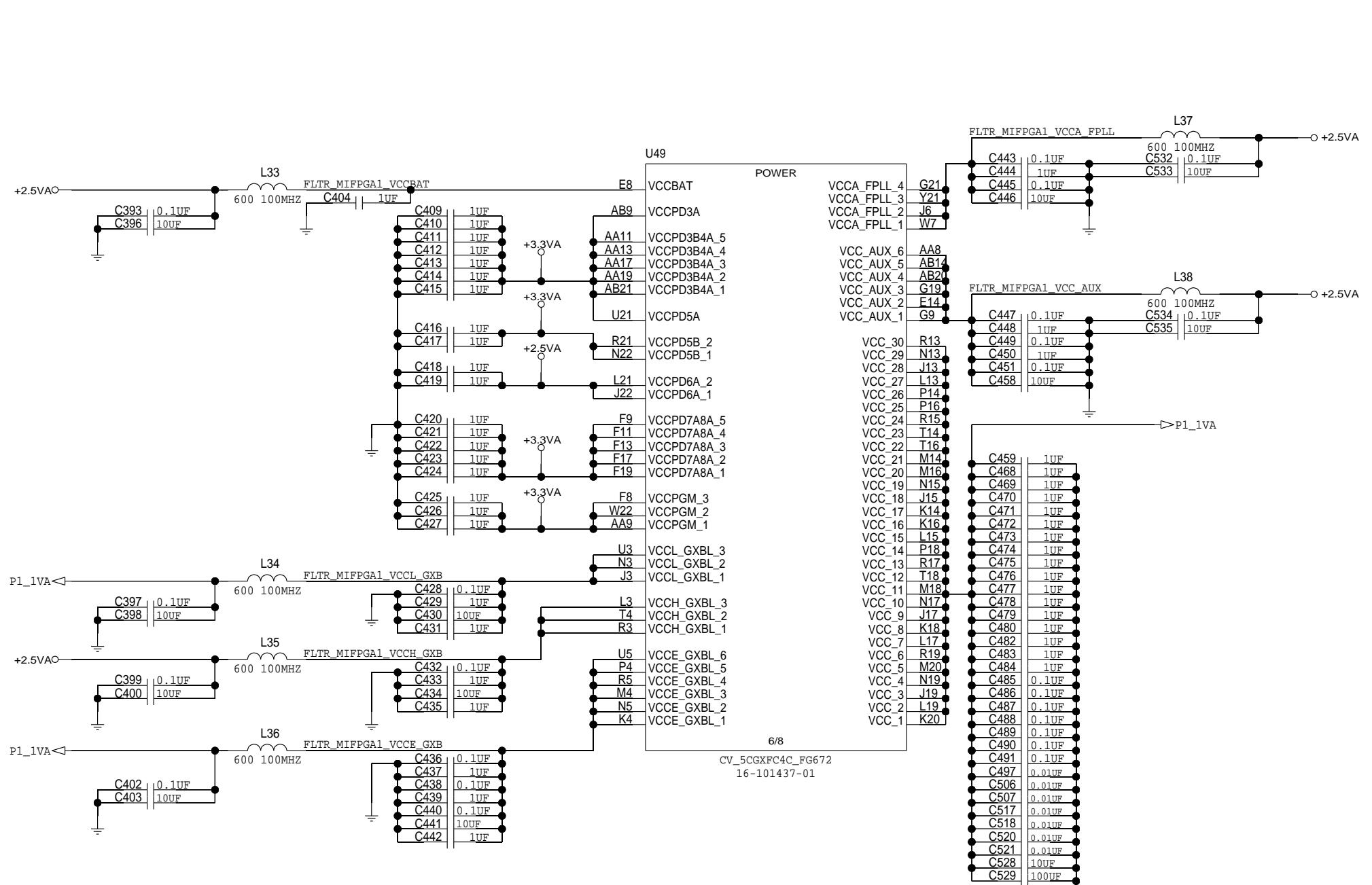
MIFPGA: CONFIG, REFCLK, SERDES



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:08 2022	REV A0

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

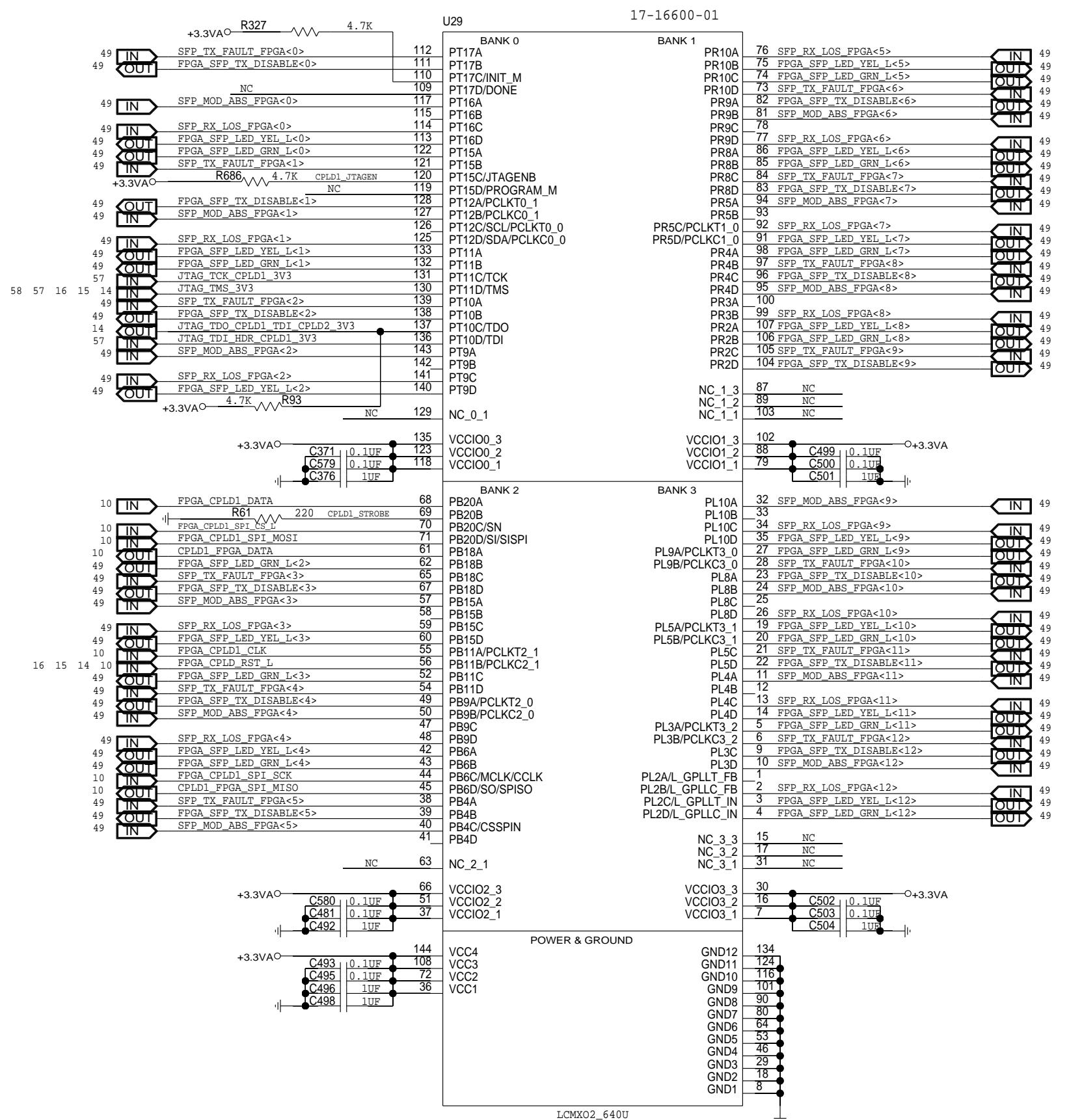
11 OF 138



## MIFPGA: POWER & GROUND



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Mon Mar 14 11:03:14 2022		12 OF 138



IO EXPANDER CPLD 1



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Mon Mar 14 11:03:10 2022		13 OF 138

D

D

C

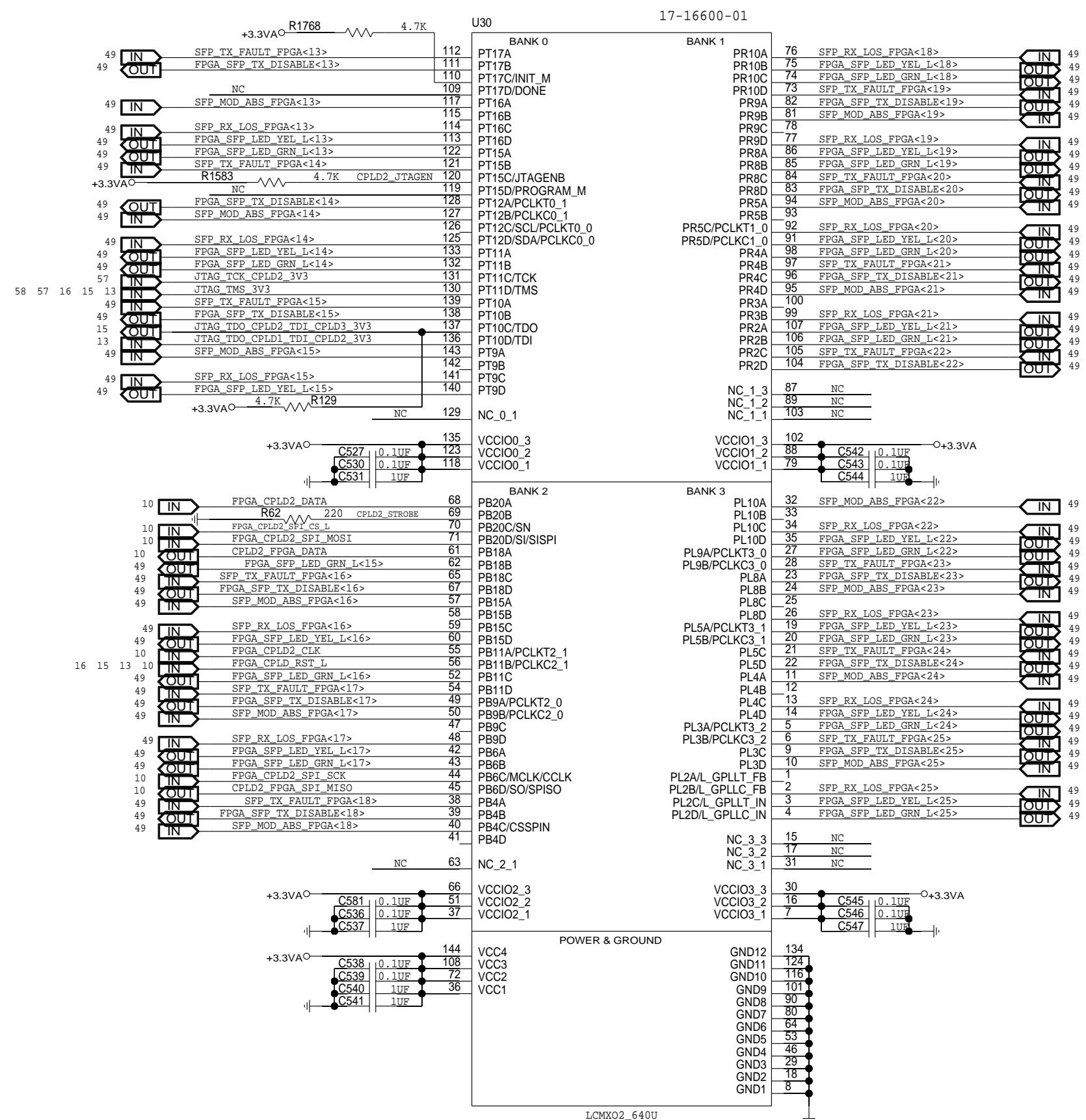
C

B

B

A

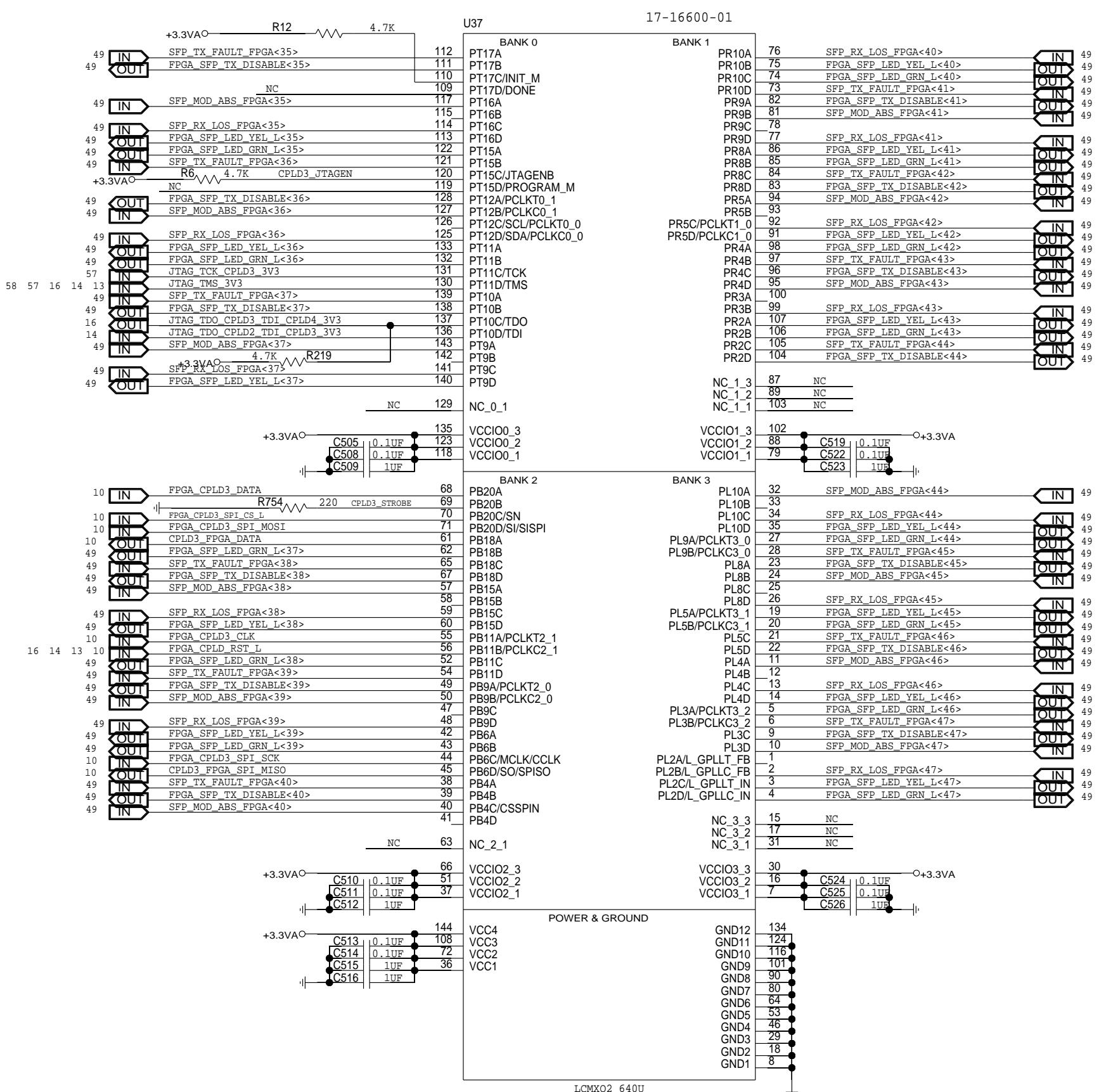
A



IO EXPANDER CPLD 2



SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Mon Mar 14 11:03:10 2022	REV A0 14 OF 138



IO EXPANDER CPLD 3



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Mon Mar 14 11:03:10 2022		15 OF 138

D

D

C

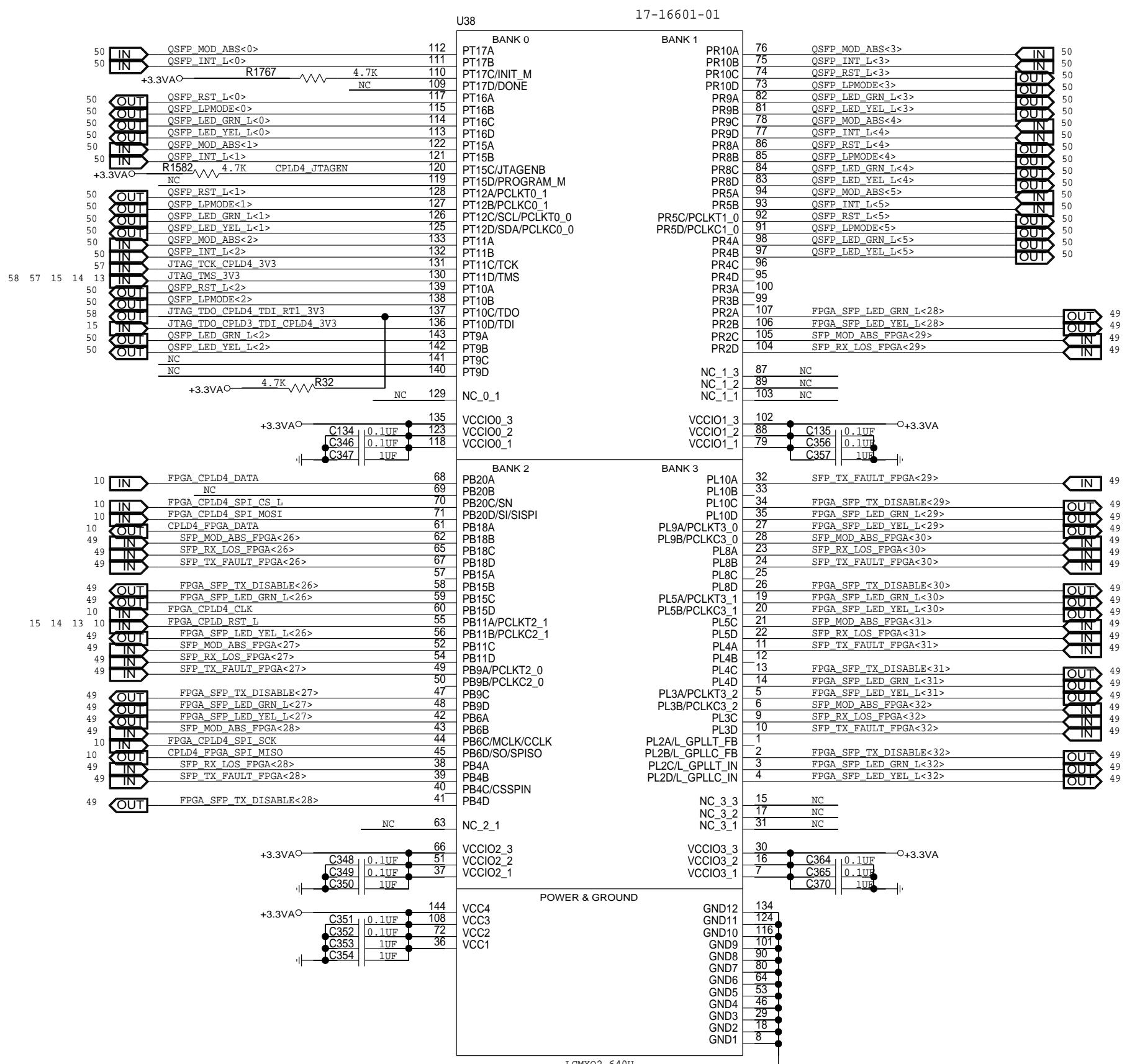
C

B

B

A

A



IO EXPANDER CPLD 4



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:09 2022	REV A0 16 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

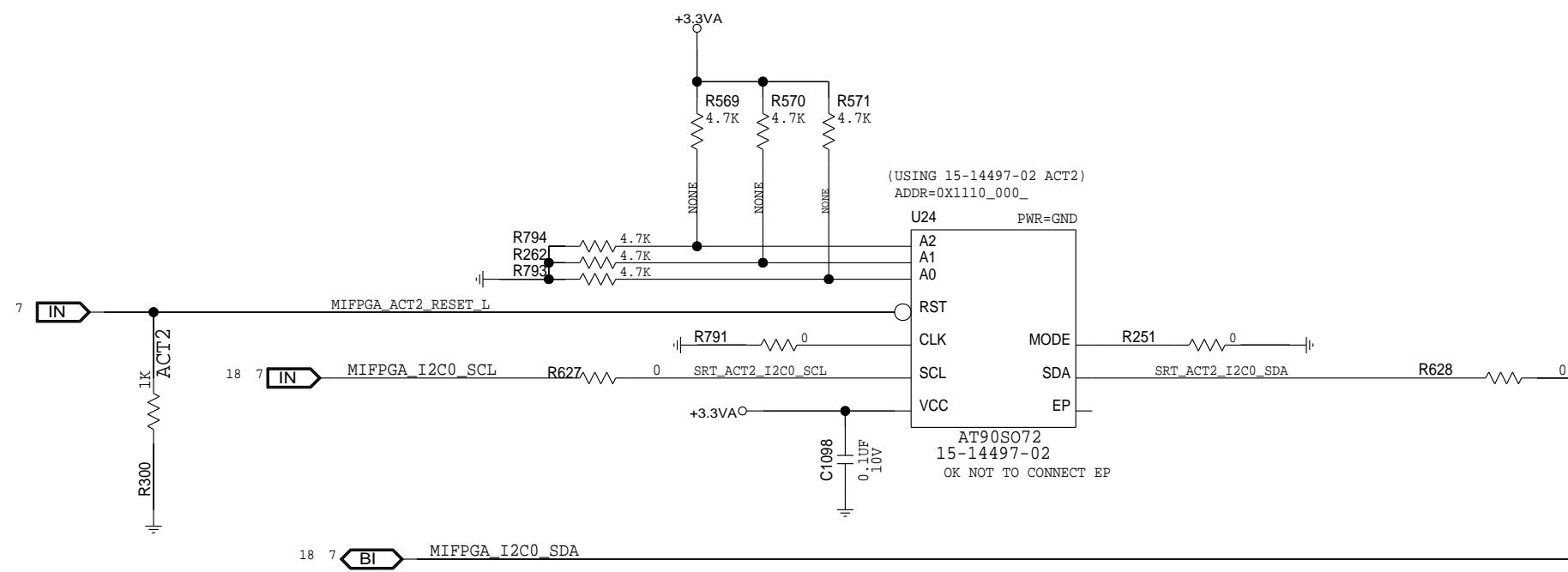
C

B

B

A

A



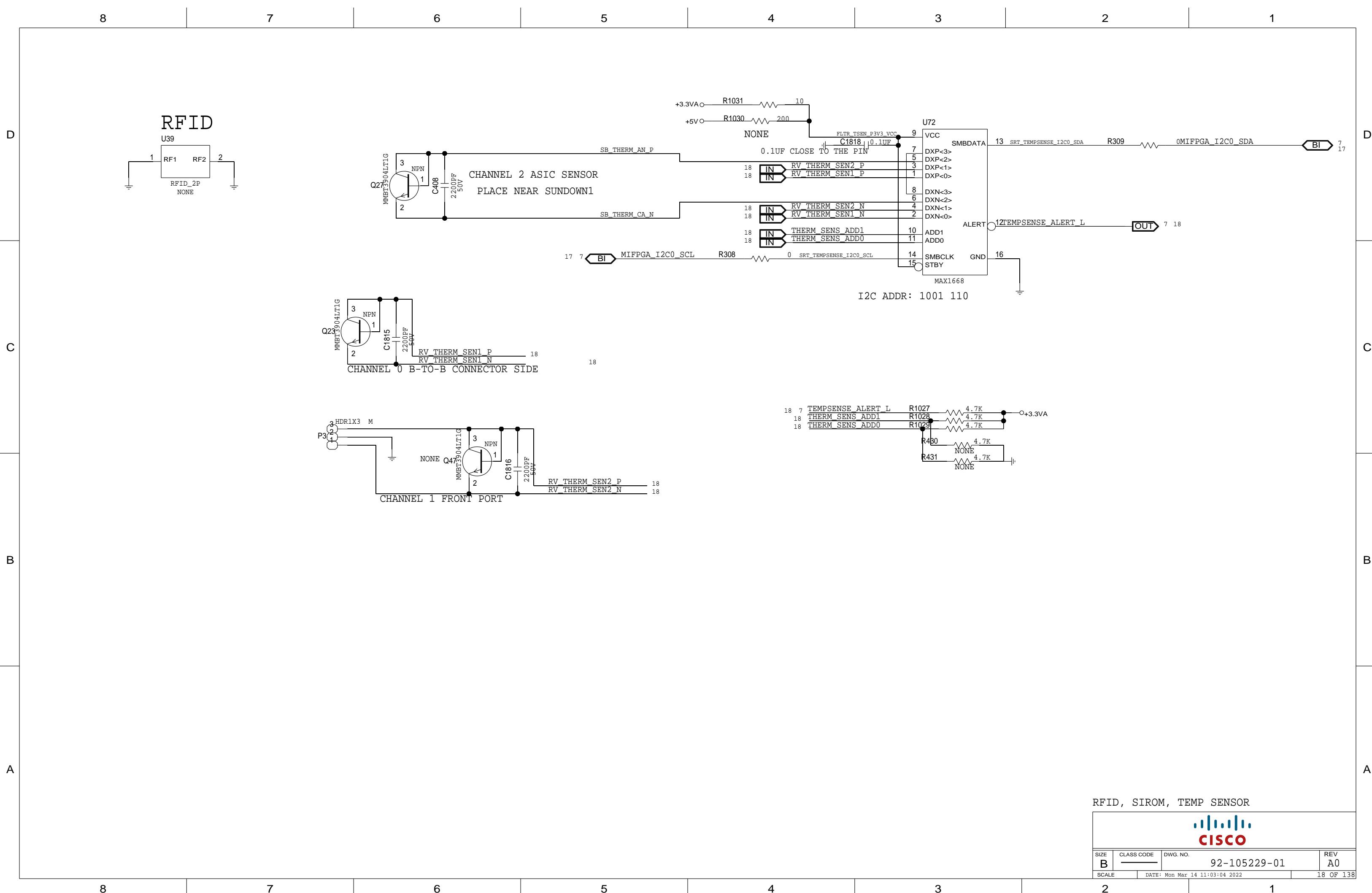
ACT2



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0

SCALE DATE: Mon Mar 14 11:03:09 2022 17 OF 138

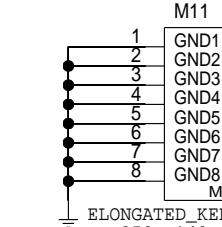
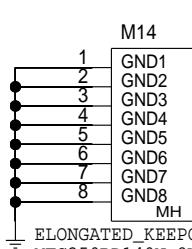
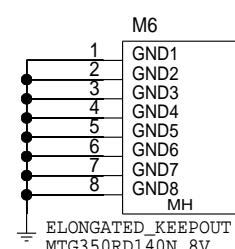
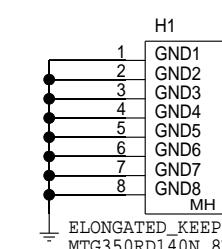
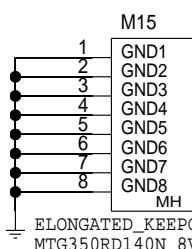
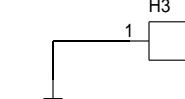
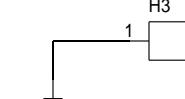
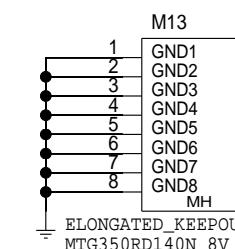
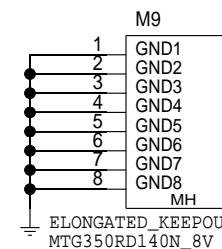
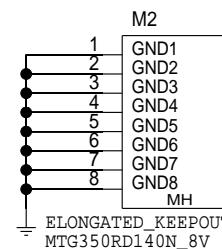
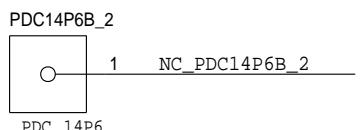
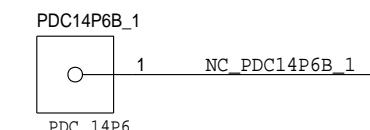
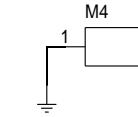
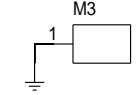
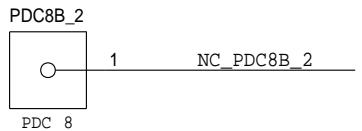
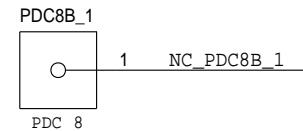
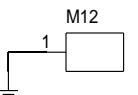
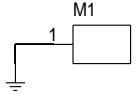
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D



MTG HOLES



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:14 2022		19 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

A

A

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

I1  
SUBDESIGN\_SUFFIX=3

SUNDOWN1\_MINFW1201\_CDS\_491059270

104 45	SNDN_HS0_RX_S0_P<3..0>	HS0_RX_S0_P<3..0>
104 45	SNDN_HS0_RX_S0_N<3..0>	HS0_RX_S0_N<3..0>
104 45	SNDN_HS1_RX_S0_P<3..0>	HS1_RX_S0_P<3..0>
104 45	SNDN_HS1_RX_S0_N<3..0>	HS1_RX_S0_N<3..0>
104 44	SNDN_HS2_RX_S0_P<3..0>	HS2_RX_S0_P<3..0>
104 44	SNDN_HS2_RX_S0_N<3..0>	HS2_RX_S0_N<3..0>
104 44	SNDN_HS3_RX_S0_P<3..0>	HS3_RX_S0_P<3..0>
104 44	SNDN_HS3_RX_S0_N<3..0>	HS3_RX_S0_N<3..0>
104 44	SNDN_HS4_RX_S0_P<3..0>	HS4_RX_S0_P<3..0>
104 44	SNDN_HS4_RX_S0_N<3..0>	HS4_RX_S0_N<3..0>
104 44	SNDN_HS5_RX_S0_P<3..0>	HS5_RX_S0_P<3..0>
104 44	SNDN_HS5_RX_S0_N<3..0>	HS5_RX_S0_N<3..0>
104 43	SNDN_HS6_RX_S0_P<3..0>	HS6_RX_S0_P<3..0>
104 43	SNDN_HS6_RX_S0_N<3..0>	HS6_RX_S0_N<3..0>
104 43	SNDN_HS7_RX_S0_P<3..0>	HS7_RX_S0_P<3..0>
104 43	SNDN_HS7_RX_S0_N<3..0>	HS7_RX_S0_N<3..0>
104 43	SNDN_HS8_RX_S0_P<3..0>	HS8_RX_S0_P<3..0>
104 43	SNDN_HS8_RX_S0_N<3..0>	HS8_RX_S0_N<3..0>
105 43	SNDN_HS9_RX_S0_P<3..0>	HS9_RX_S0_P<3..0>
105 43	SNDN_HS9_RX_S0_N<3..0>	HS9_RX_S0_N<3..0>
105 42	SNDN_HS10_RX_S0_P<3..0>	HS10_RX_S0_P<3..0>
105 42	SNDN_HS10_RX_S0_N<3..0>	HS10_RX_S0_N<3..0>
105 42	SNDN_HS11_RX_S0_P<3..0>	HS11_RX_S0_P<3..0>
105 42	SNDN_HS11_RX_S0_N<3..0>	HS11_RX_S0_N<3..0>
105 42	SNDN_HS12_RX_S0_P<3..0>	HS12_RX_S0_P<3..0>
105 42	SNDN_HS12_RX_S0_N<3..0>	HS12_RX_S0_N<3..0>
105 42	SNDN_HS13_RX_S0_P<3..0>	HS13_RX_S0_P<3..0>
105 42	SNDN_HS13_RX_S0_N<3..0>	HS13_RX_S0_N<3..0>
105 41	SNDN_HS14_RX_S0_P<3..0>	HS14_RX_S0_P<3..0>
105 41	SNDN_HS14_RX_S0_N<3..0>	HS14_RX_S0_N<3..0>
105 41	SNDN_HS15_RX_S0_P<3..0>	HS15_RX_S0_P<3..0>
105 41	SNDN_HS15_RX_S0_N<3..0>	HS15_RX_S0_N<3..0>
105 41	SNDN_HS16_RX_S0_P<3..0>	HS16_RX_S0_P<3..0>
105 41	SNDN_HS16_RX_S0_N<3..0>	HS16_RX_S0_N<3..0>
105 41	SNDN_HS17_RX_S0_P<3..0>	HS17_RX_S0_P<3..0>
105 41	SNDN_HS17_RX_S0_N<3..0>	HS17_RX_S0_N<3..0>

sundown1\_minfw1201

HS0_RX_S0_P<3..0>	SNDN_HS0_RX_S0_P<3..0>	45 104
HS0_RX_S0_N<3..0>	SNDN_HS0_RX_S0_N<3..0>	45 104
HS1_RX_S0_P<3..0>	SNDN_HS1_RX_S0_P<3..0>	45 104
HS1_RX_S0_N<3..0>	SNDN_HS1_RX_S0_N<3..0>	45 104
HS2_RX_S0_P<3..0>	SNDN_HS2_RX_S0_P<3..0>	44 104
HS2_RX_S0_N<3..0>	SNDN_HS2_RX_S0_N<3..0>	44 104
HS3_RX_S0_P<3..0>	SNDN_HS3_RX_S0_P<3..0>	44 104
HS3_RX_S0_N<3..0>	SNDN_HS3_RX_S0_N<3..0>	44 104
HS4_RX_S0_P<3..0>	SNDN_HS4_RX_S0_P<3..0>	44 104
HS4_RX_S0_N<3..0>	SNDN_HS4_RX_S0_N<3..0>	44 104
HS5_RX_S0_P<3..0>	SNDN_HS5_RX_S0_P<3..0>	44 104
HS5_RX_S0_N<3..0>	SNDN_HS5_RX_S0_N<3..0>	44 104
HS6_RX_S0_P<3..0>	SNDN_HS6_RX_S0_P<3..0>	43 104
HS6_RX_S0_N<3..0>	SNDN_HS6_RX_S0_N<3..0>	43 104
HS7_RX_S0_P<3..0>	SNDN_HS7_RX_S0_P<3..0>	43 104
HS7_RX_S0_N<3..0>	SNDN_HS7_RX_S0_N<3..0>	43 104
HS8_RX_S0_P<3..0>	SNDN_HS8_RX_S0_P<3..0>	43 104
HS8_RX_S0_N<3..0>	SNDN_HS8_RX_S0_N<3..0>	43 104
HS9_RX_S0_P<3..0>	SNDN_HS9_RX_S0_P<3..0>	43 105
HS9_RX_S0_N<3..0>	SNDN_HS9_RX_S0_N<3..0>	43 105
HS10_RX_S0_P<3..0>	SNDN_HS10_RX_S0_P<3..0>	42 105
HS10_RX_S0_N<3..0>	SNDN_HS10_RX_S0_N<3..0>	42 105
HS11_RX_S0_P<3..0>	SNDN_HS11_RX_S0_P<3..0>	42 105
HS11_RX_S0_N<3..0>	SNDN_HS11_RX_S0_N<3..0>	42 105
HS12_RX_S0_P<3..0>	SNDN_HS12_RX_S0_P<3..0>	42 105
HS12_RX_S0_N<3..0>	SNDN_HS12_RX_S0_N<3..0>	42 105
HS13_RX_S0_P<3..0>	SNDN_HS13_RX_S0_P<3..0>	42 105
HS13_RX_S0_N<3..0>	SNDN_HS13_RX_S0_N<3..0>	42 105
HS14_RX_S0_P<3..0>	SNDN_HS14_RX_S0_P<3..0>	41 105
HS14_RX_S0_N<3..0>	SNDN_HS14_RX_S0_N<3..0>	41 105
HS15_RX_S0_P<3..0>	SNDN_HS15_RX_S0_P<3..0>	41 105
HS15_RX_S0_N<3..0>	SNDN_HS15_RX_S0_N<3..0>	41 105
HS16_RX_S0_P<3..0>	SNDN_HS16_RX_S0_P<3..0>	41 105
HS16_RX_S0_N<3..0>	SNDN_HS16_RX_S0_N<3..0>	41 105
HS17_RX_S0_P<3..0>	SNDN_HS17_RX_S0_P<3..0>	41 105
HS17_RX_S0_N<3..0>	SNDN_HS17_RX_S0_N<3..0>	41 105

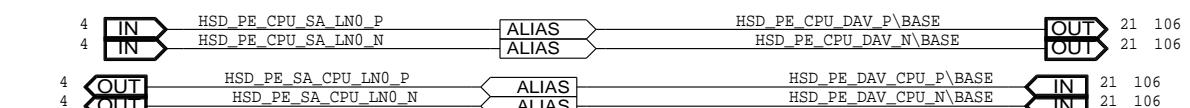
## SUNDOWN PORTS



SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Tue Jan 19 17:14:32 2021	20 OF 138	

8 7 6 5 4 3 2 1

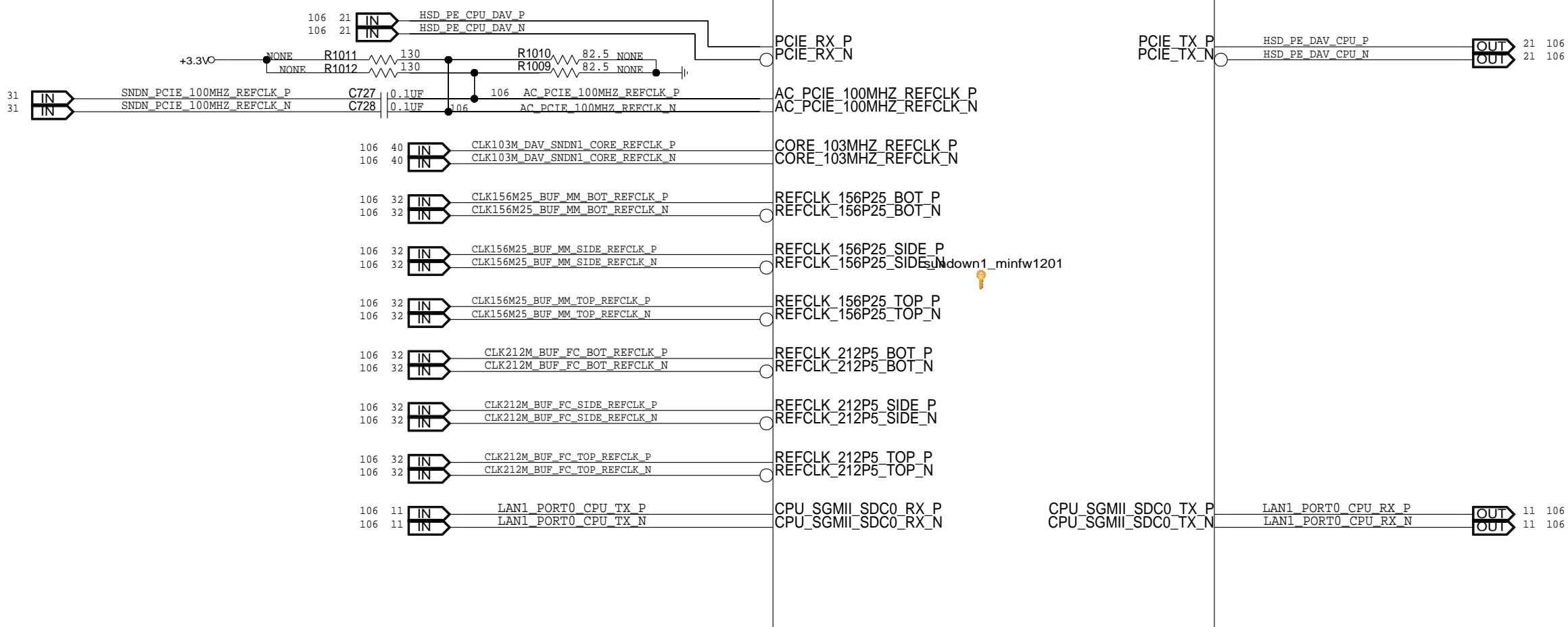
## PCIE BUS CONNECTOR NETNAME ALIAS "CPU&lt;&gt;&gt;SNDN1"



I74

SUBDESIGN\_SUFFIX=3

SUNDOWN1\_MINFW1201\_CDS\_491059270



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:13 2022		21 OF 138

8 7 6 5 4 3 2 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

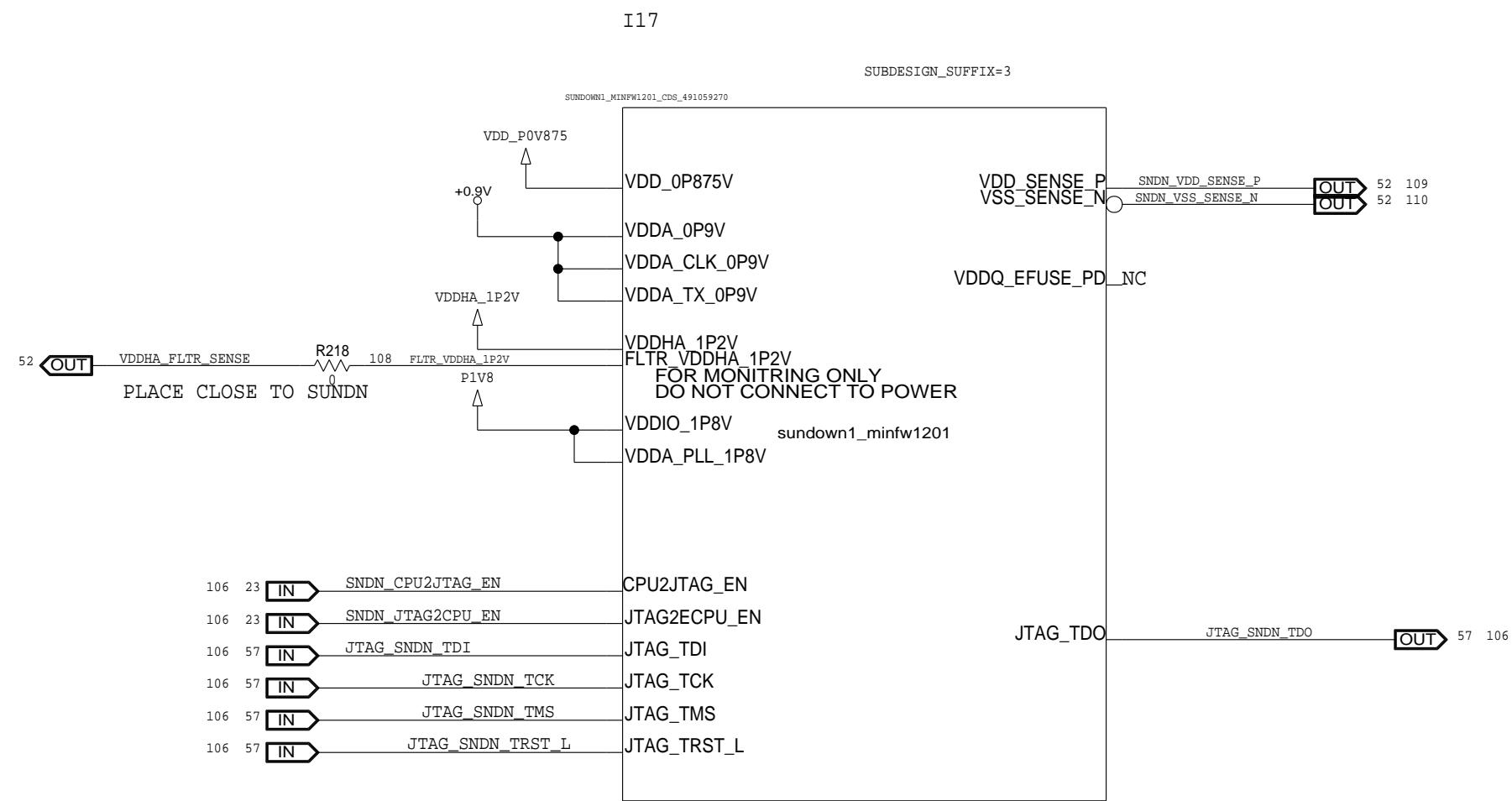
C

B

B

A

A



CISCO

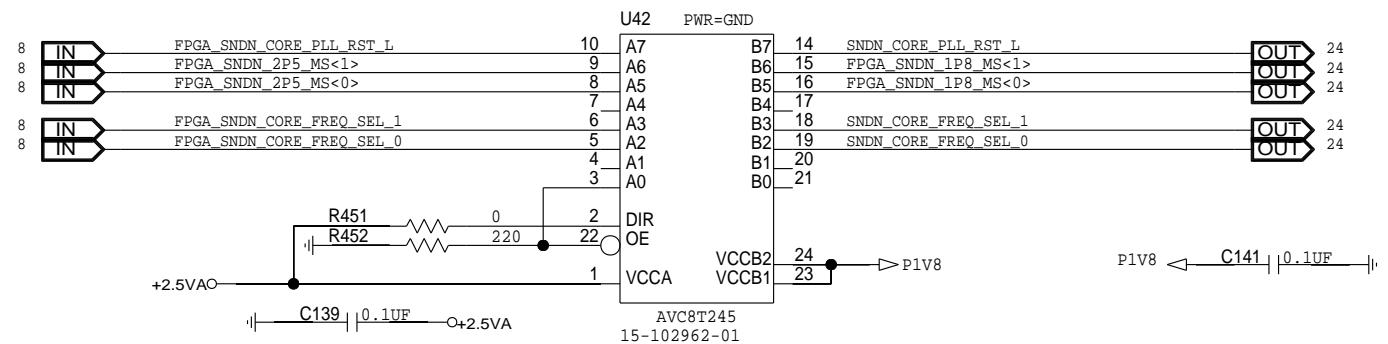
SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:15 2022		22 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

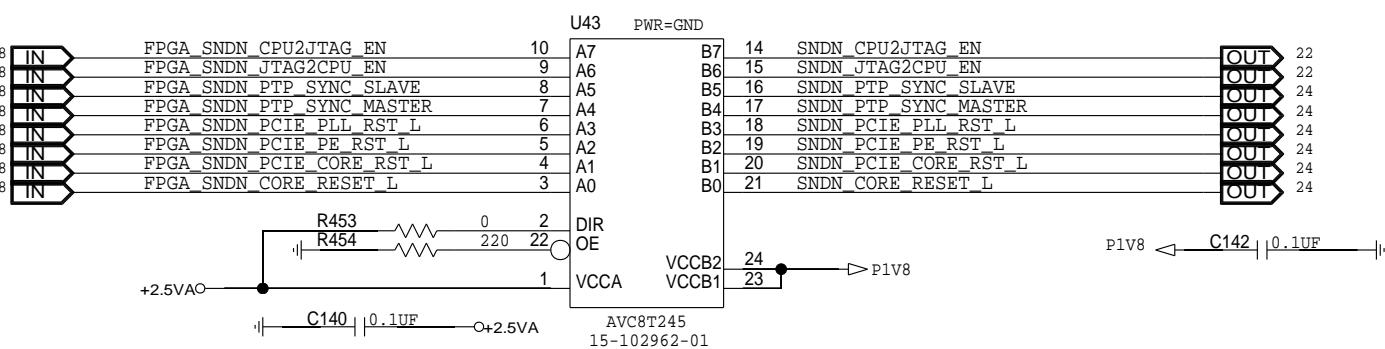
D

D



C

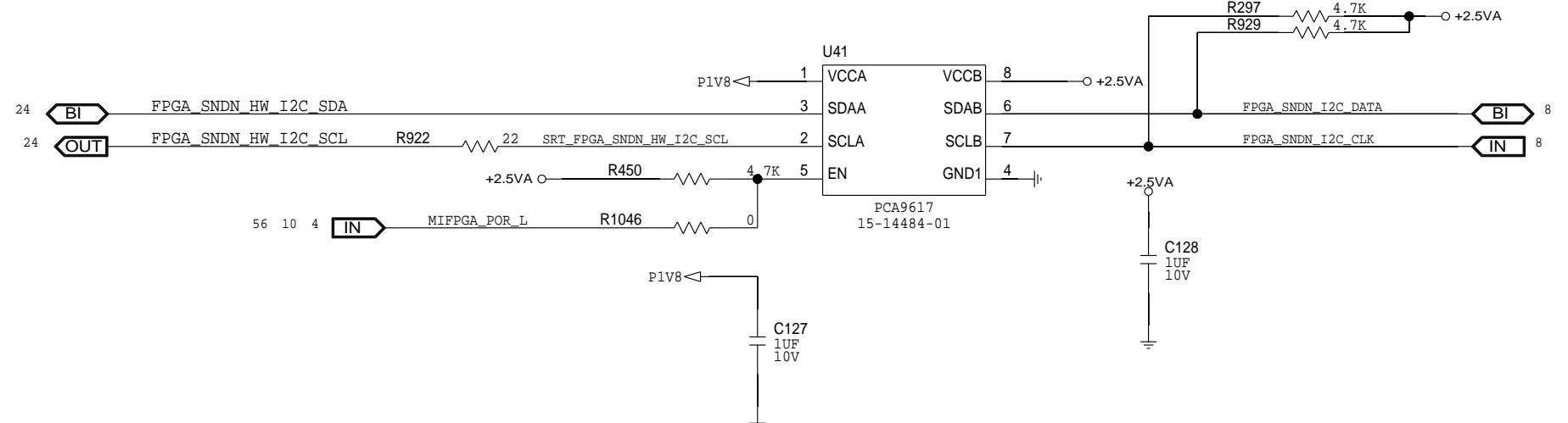
C



CHANGE RAIL LEVEL TO 2.5

B

B



A

A

SNDN IO LEVEL shifter



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Mon Mar 14 11:03:04 2022	23 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

I75  
SUBDESIGN\_SUFFIX=3

SUNDOWN1\_MINFW1201\_CDS\_491059270

PCIE\_RREF TERMINATED IN SUBDESIGN

106 23 [IN] SNDN_PTP_SYNC_SLAVE	PTP_SYNC_SLAVE
106 23 [IN] SNDN_PTP_SYNC_MASTER	PTP_SYNC_MASTER
106 [IN] SNDN_PCIE_RREF	PCIE_RREF
106 [IN] SNDN_USR_DRV_EN	PCIE_USR_DRV_EN
106 23 [IN] SNDN_PCIE_PLL_RST_L	PCIE_PLL_RST_L
106 [IN] SNDN_PCIE_PLL_BYP	PCIE_PLL_BYP
106 23 [IN] SNDN_PCIE_PE_RST_L	PCIE_PE_RST_L
106 23 [IN] SNDN_PCIE_CORE_RST_L	PCIE_CORE_RST_L
106 [IN] SNDN_EXTLOOP_EN	EXTLOOP_EN
106 23 [IN] SNDN_CORE_PLL_RST_L	CORE_PLL_RST_L
106 [IN] SNDN_CORE_PLL_BYP	CORE_PLL_BYP
106 23 [IN] SNDN_CORE_RESET_L	CORE_RESET_L
106 23 [IN] SNDN_CORE_FREQ_SEL_1	CORE_FREQ_SEL_1
106 23 [IN] SNDN_CORE_FREQ_SEL_0	CORE_FREQ_SEL_0

sundown1\_minfw1201

106 23 [IN] SNDN_PTP_SYNC_SLAVE	PTP_SYNC_SLAVE
106 23 [IN] SNDN_PTP_SYNC_MASTER	PTP_SYNC_MASTER
106 [IN] SNDN_PCIE_RREF	PCIE_RREF
106 [IN] SNDN_USR_DRV_EN	PCIE_USR_DRV_EN
106 23 [IN] SNDN_PCIE_PLL_RST_L	PCIE_PLL_RST_L
106 [IN] SNDN_PCIE_PLL_BYP	PCIE_PLL_BYP
106 23 [IN] SNDN_PCIE_PE_RST_L	PCIE_PE_RST_L
106 23 [IN] SNDN_PCIE_CORE_RST_L	PCIE_CORE_RST_L
106 [IN] SNDN_EXTLOOP_EN	EXTLOOP_EN
106 23 [IN] SNDN_CORE_PLL_RST_L	CORE_PLL_RST_L
106 [IN] SNDN_CORE_PLL_BYP	CORE_PLL_BYP
106 23 [IN] SNDN_CORE_RESET_L	CORE_RESET_L
106 23 [IN] SNDN_CORE_FREQ_SEL_1	CORE_FREQ_SEL_1
106 23 [IN] SNDN_CORE_FREQ_SEL_0	CORE_FREQ_SEL_0

MS1	FPGA_SNDN_1P8_MS<1>	[IN] 23 106
MS0	FPGA_SNDN_1P8_MS<0>	[IN] 23 106
HW_I2C_SDA	FPGA_SNDN_HW_I2C_SDA	[BI] 23 106
HW_I2C_SCL	FPGA_SNDN_HW_I2C_SCL	[IN] 23 106
GPIO21	FPGA_SNDN_GPIO21	[BI] 106
GPIO20	FPGA_SNDN_GPIO20	[BI] 106
GPIO19	FPGA_SNDN_GPIO19	[BI] 106
GPIO18	FPGA_SNDN_GPIO18	[BI] 106
GPIO17	FPGA_SNDN_GPIO17	[BI] 106
GPIO16	FPGA_SNDN_GPIO16	[BI] 106
GPIO15	FPGA_SNDN_GPIO15	[BI] 106
GPIO14	FPGA_SNDN_GPIO14	[BI] 106
GPIO13	FPGA_SNDN_GPIO13	[BI] 106
GPIO12	FPGA_SNDN_GPIO12	[BI] 106
GPIO11	FPGA_SNDN_GPIO11	[BI] 106
GPIO10	FPGA_SNDN_GPIO10	[BI] 106
GPIO9	FPGA_SNDN_GPIO09	[BI] 106
GPIO8	FPGA_SNDN_GPIO08	[BI] 106
GPIO7	FPGA_SNDN_GPIO07	[BI] 106
GPIO6	FPGA_SNDN_GPIO06	[BI] 106
GPIO5	FPGA_SNDN_GPIO05	[BI] 106
FUSE_FSRC		



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE:	Tue Jan 19 17:14:01 2021	24 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

A

A

C

C

B

B

A

A

D

D

C

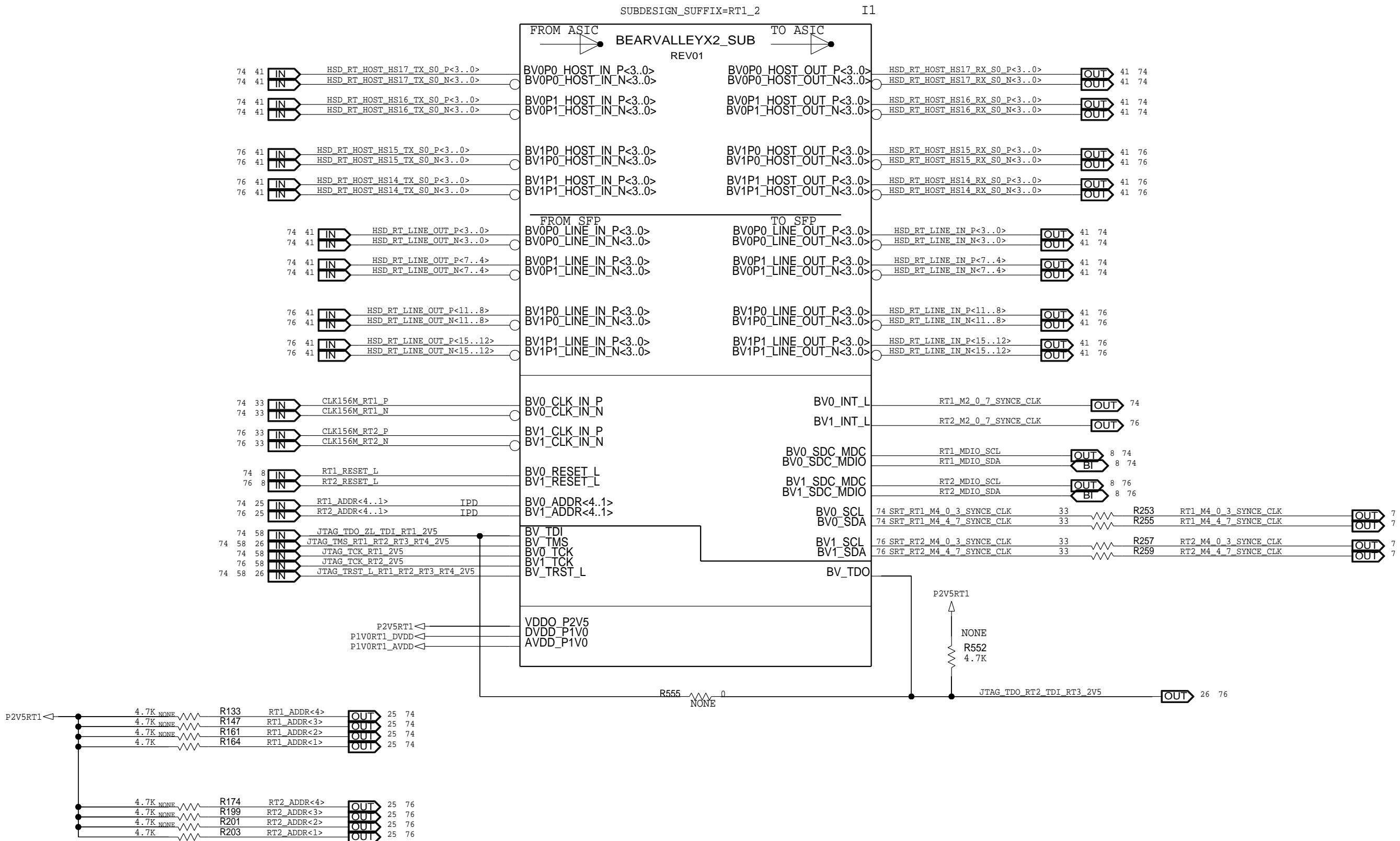
C

B

B

A

A

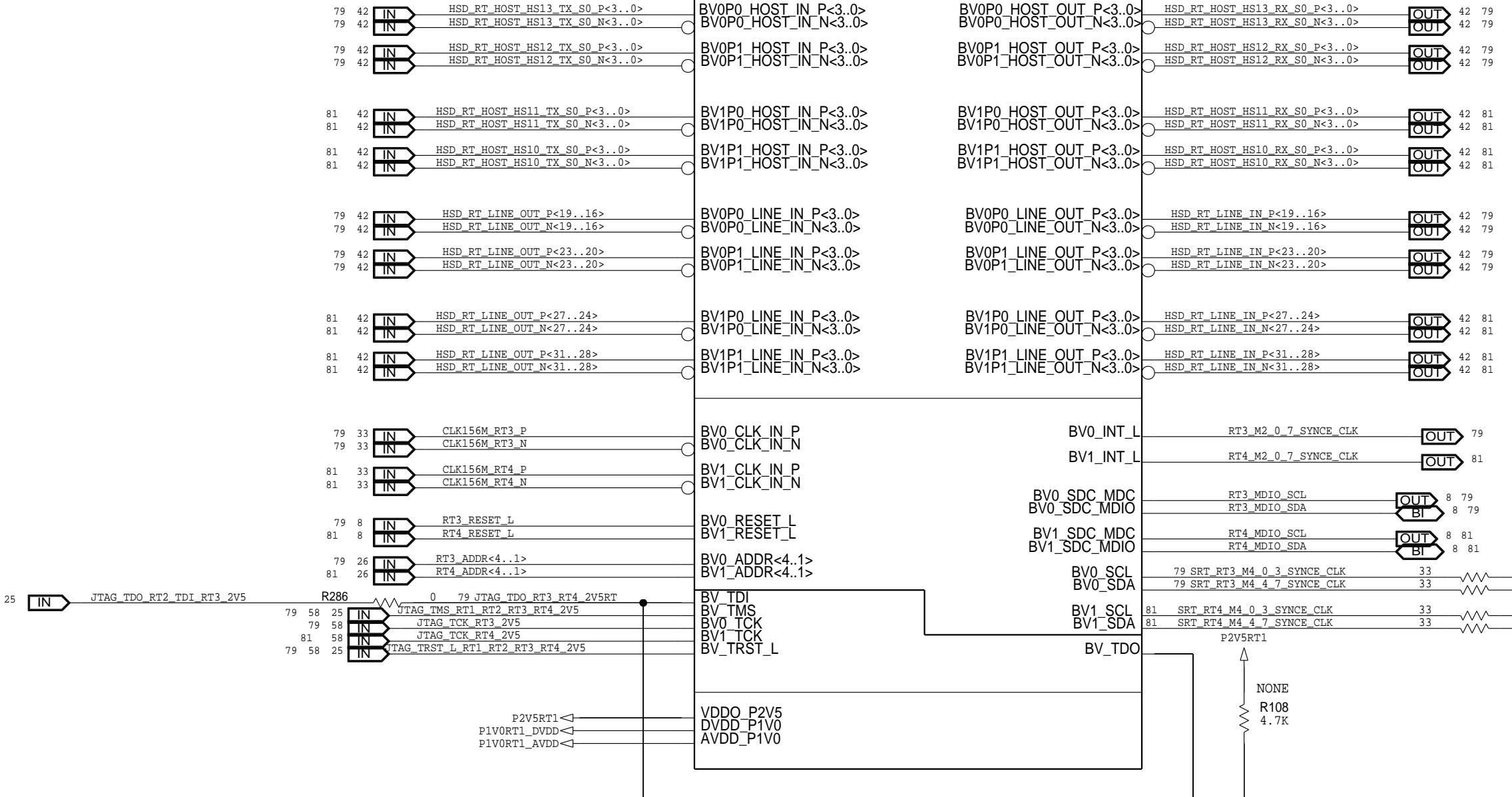


D

D

SUBDESIGN\_SUFFIX=RT3\_4

I1

BEARVALLEYX2\_SUB  
REV01

C

C

B

B

A

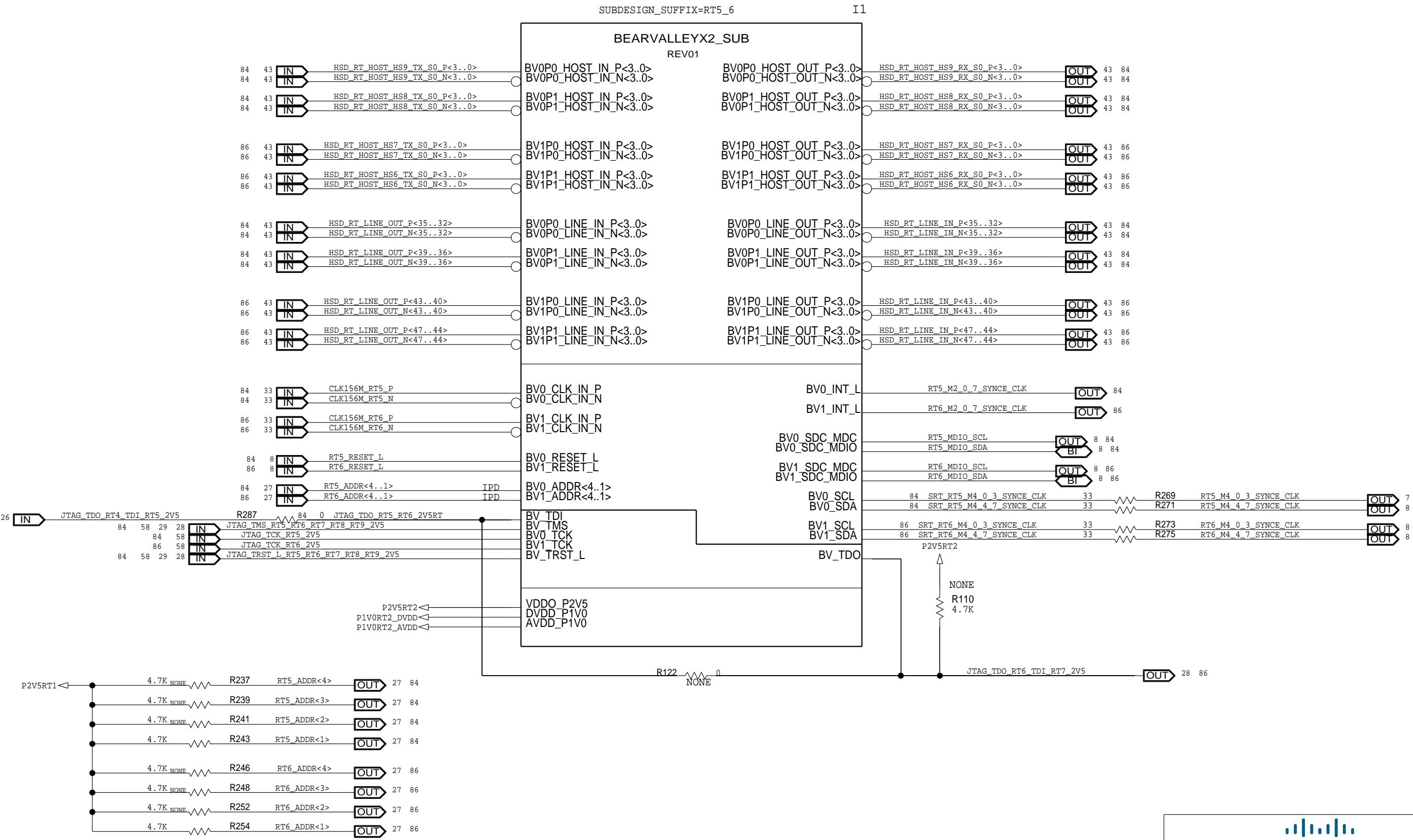
A



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:11 2022		26 OF 138

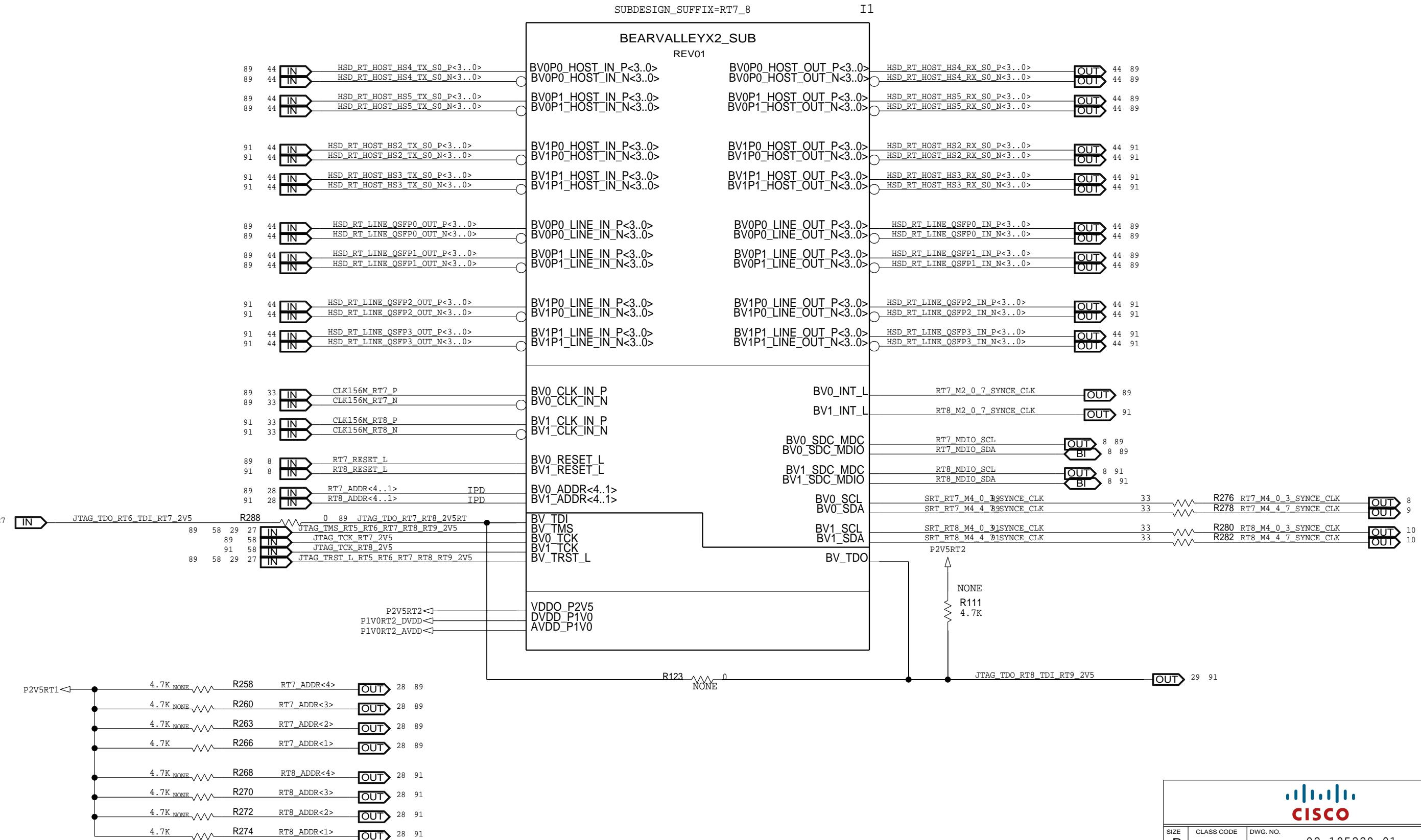
D

D



D

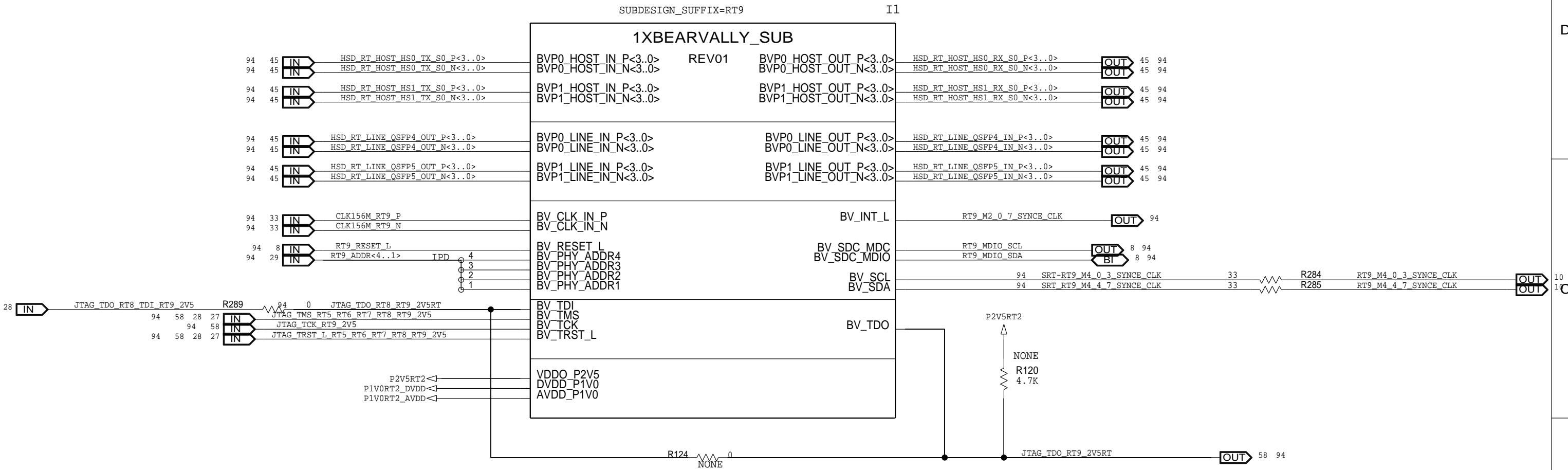
D



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

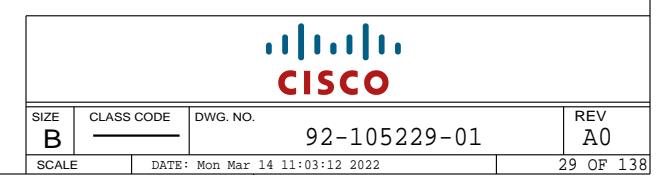


B

B

A

A



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

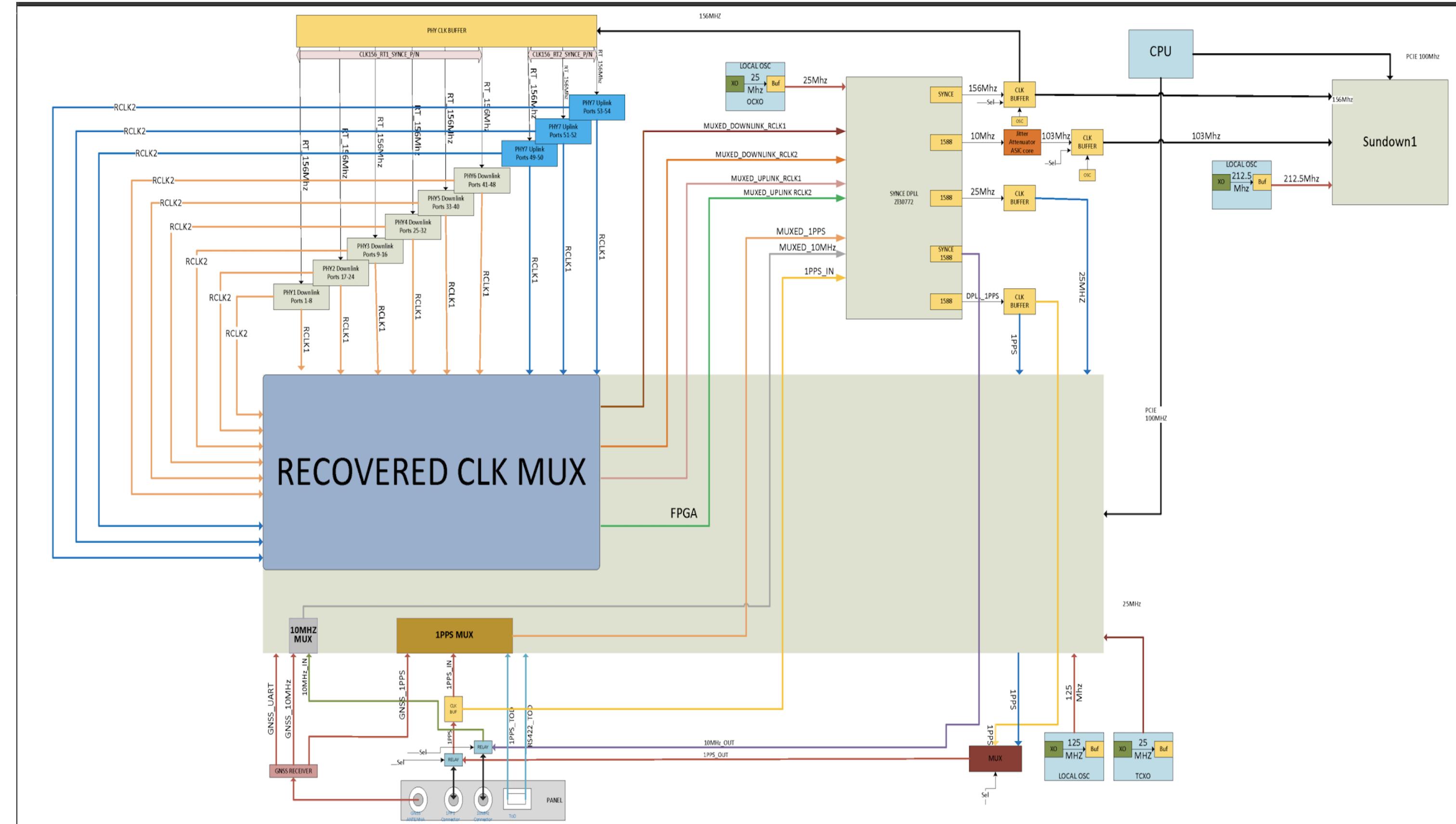
C

B

B

A

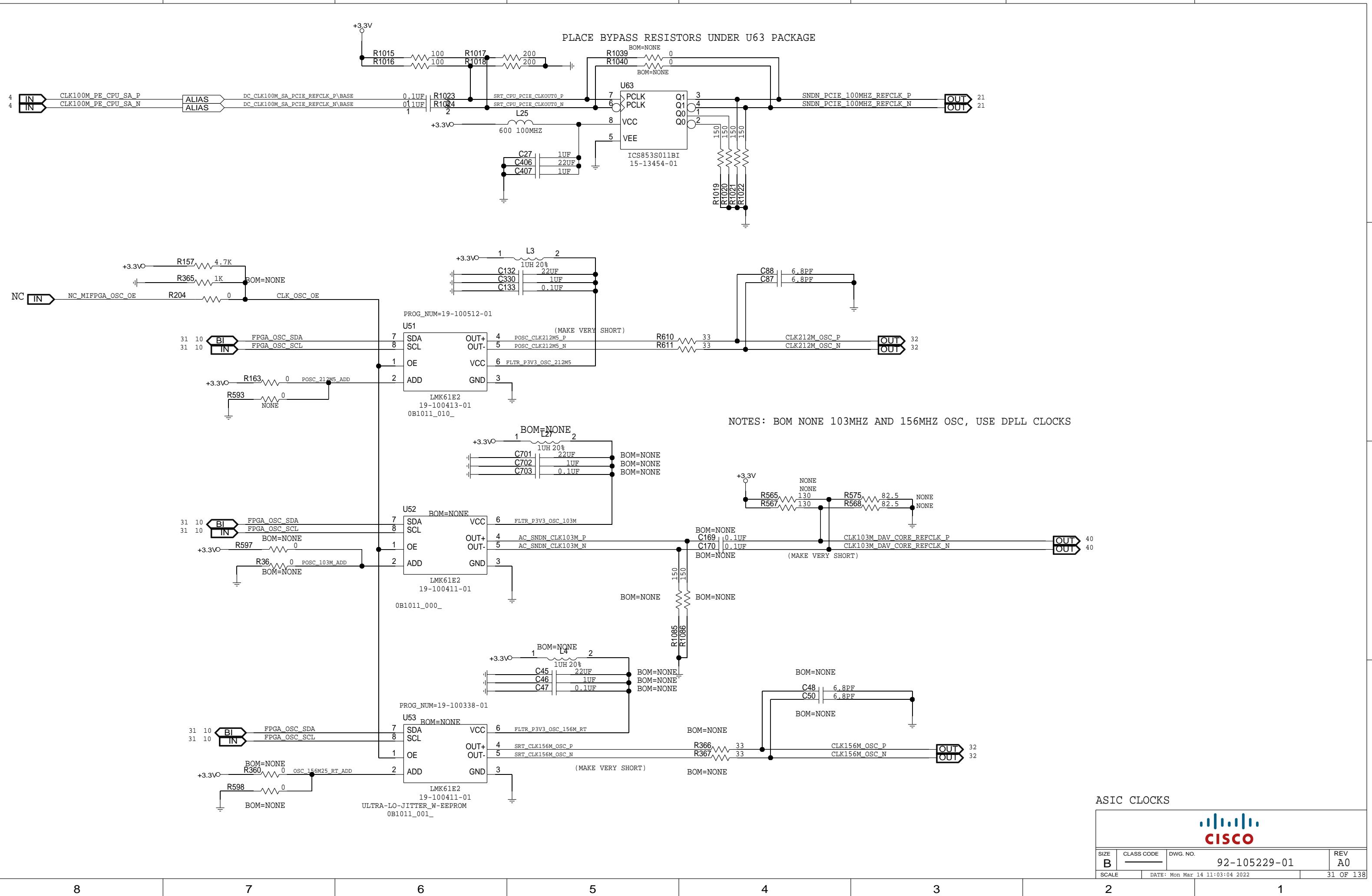
A



CISCO

SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Thu Dec 5 17:45:43 2019	REV A0
30 OF 138		

8 7 6 5 4 3 2 1



8

7

6

5

4

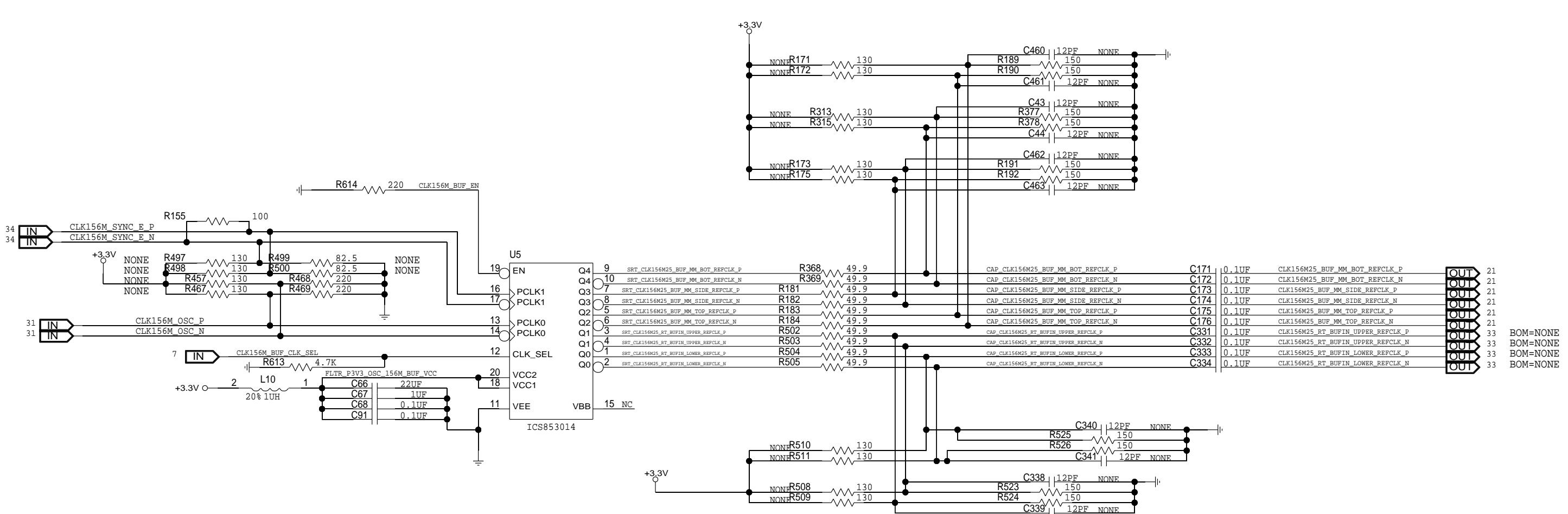
3

2

1

D

D



NC

B

A

A

B

B

C

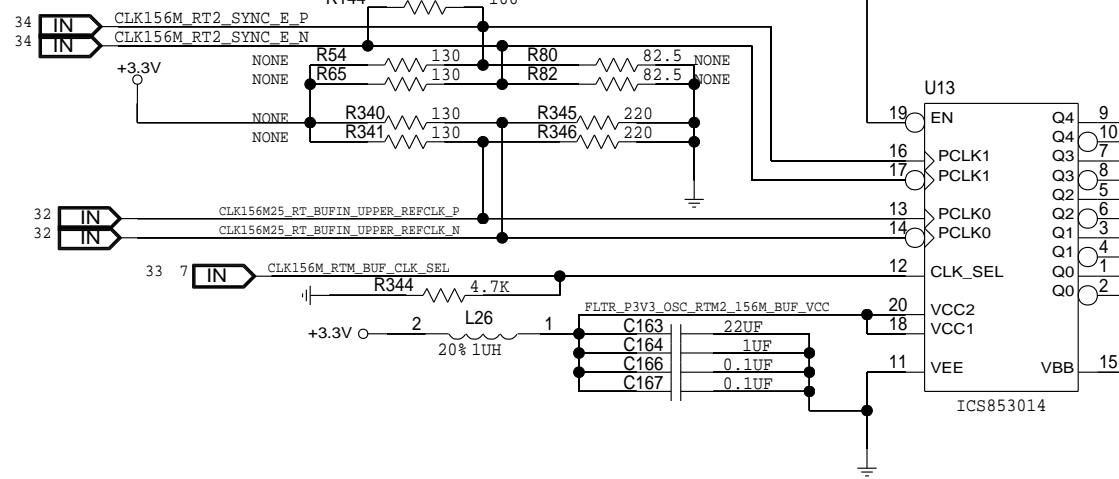
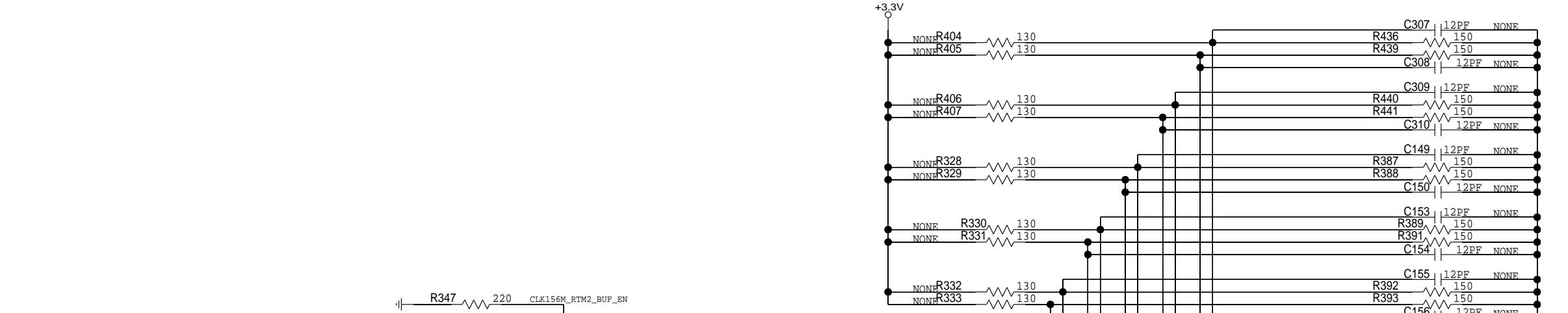
C

D

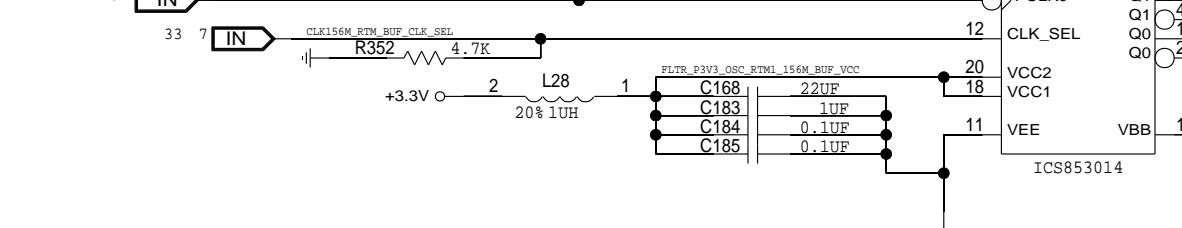
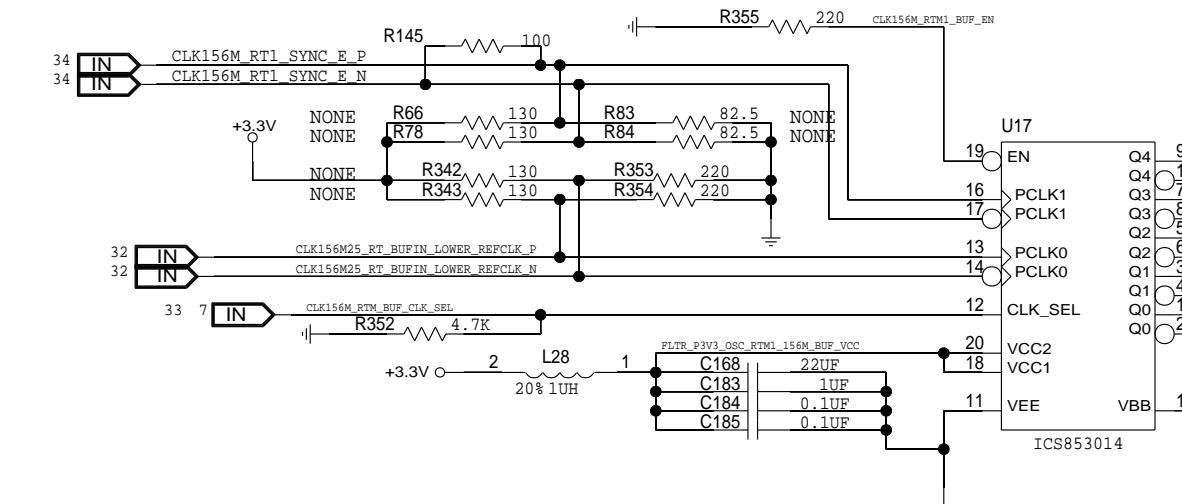
D

D

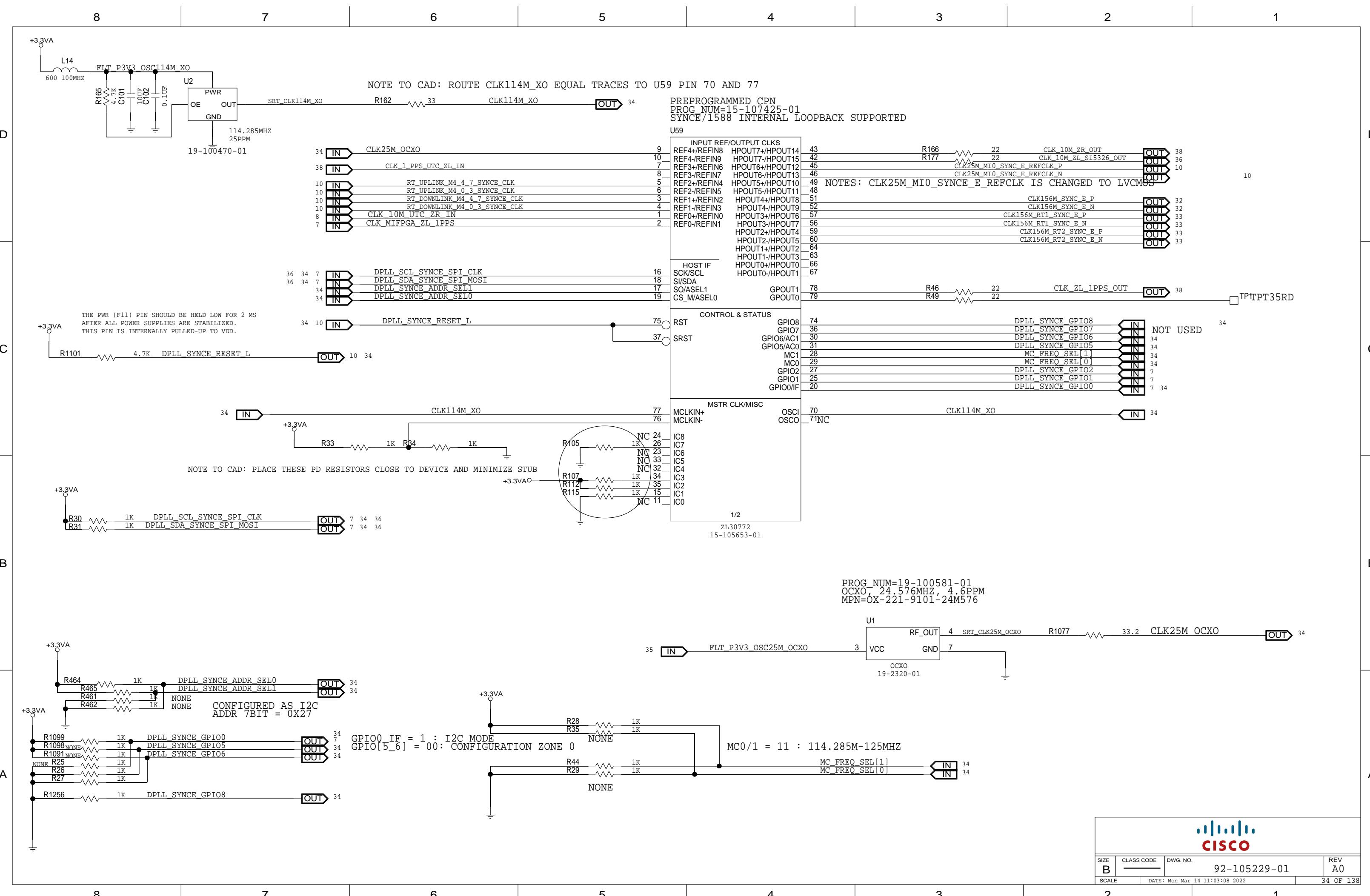
D

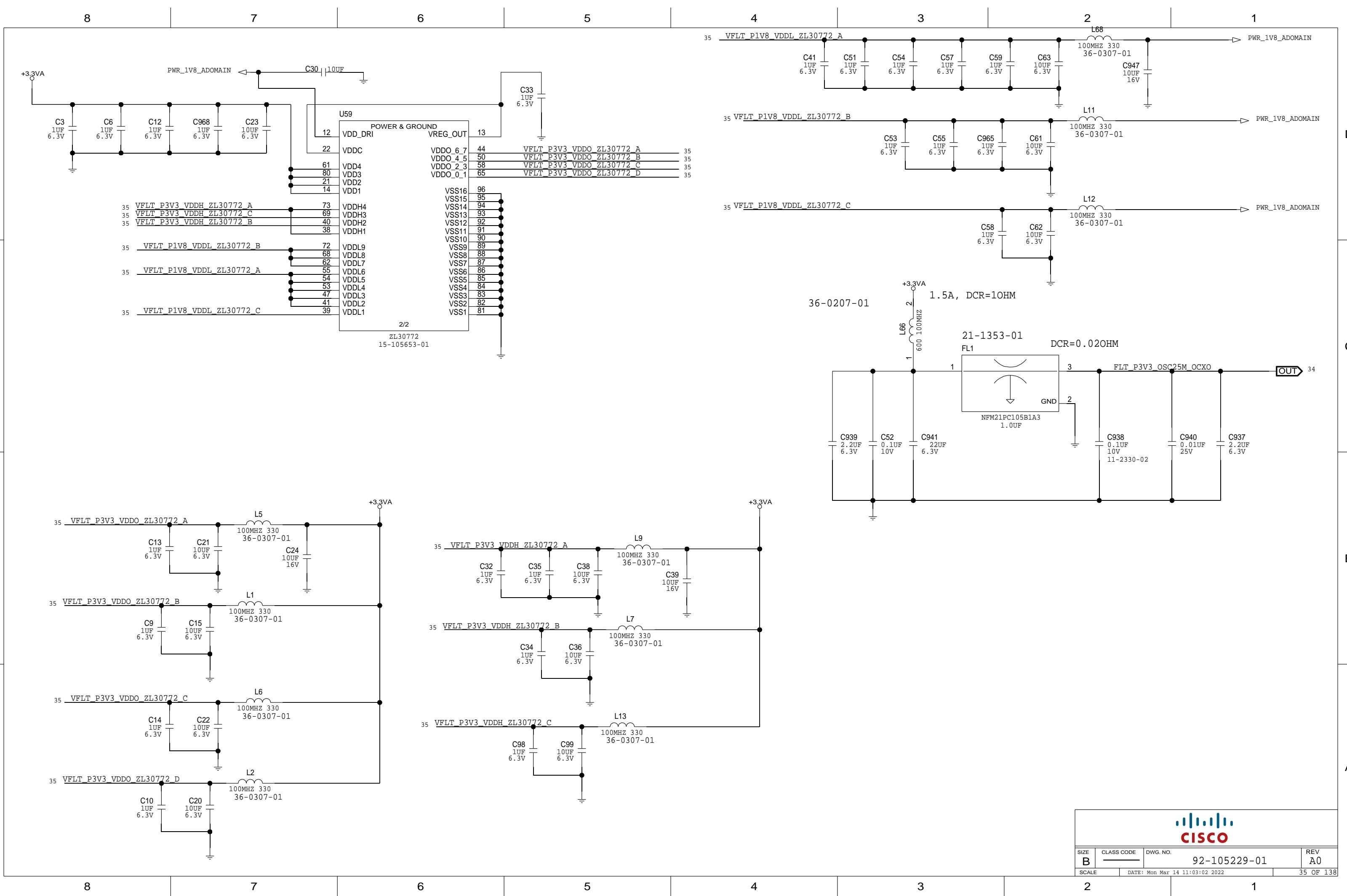


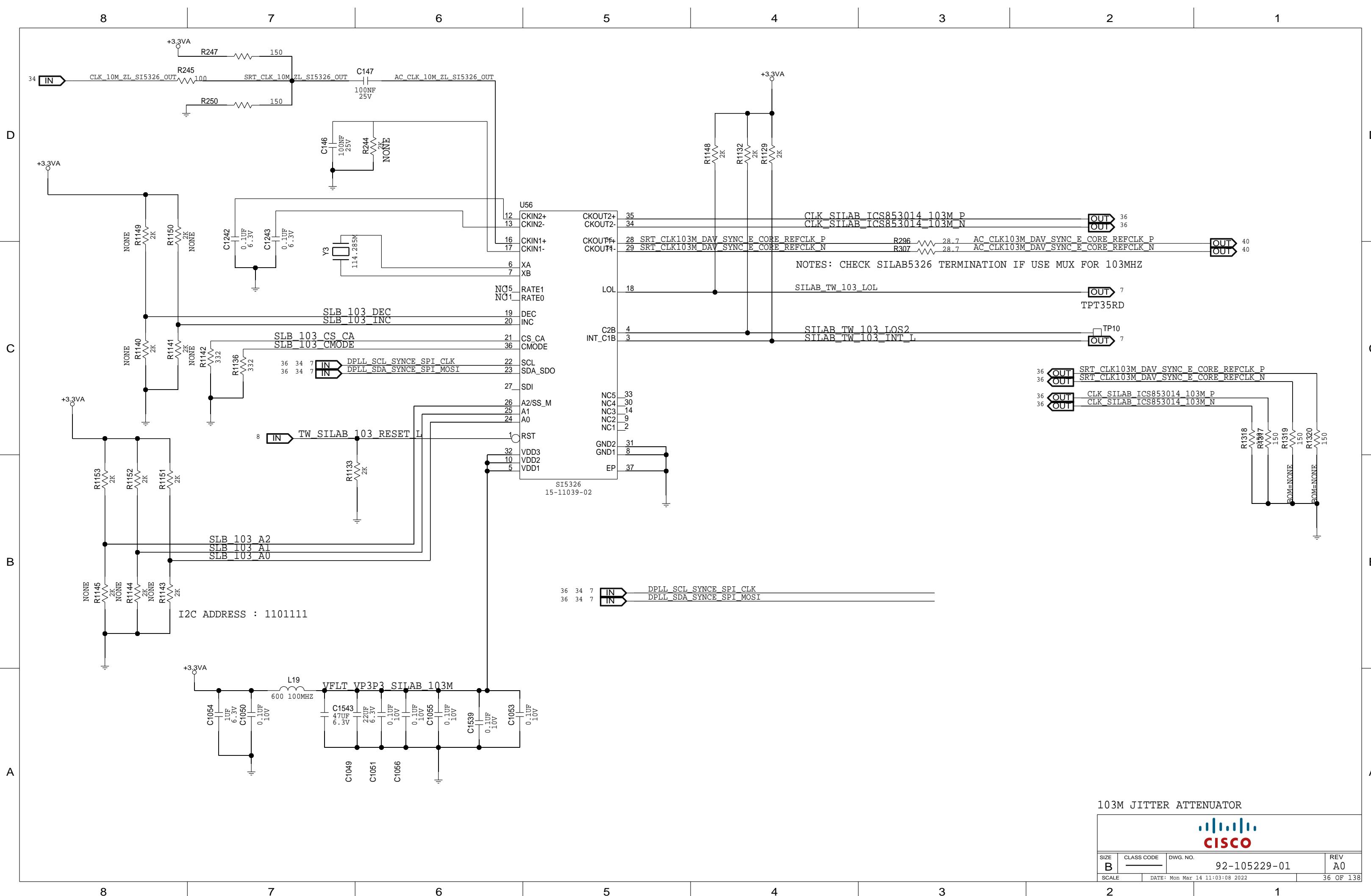
NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTORS AS SHORT AS POSSIBLE



CISCO

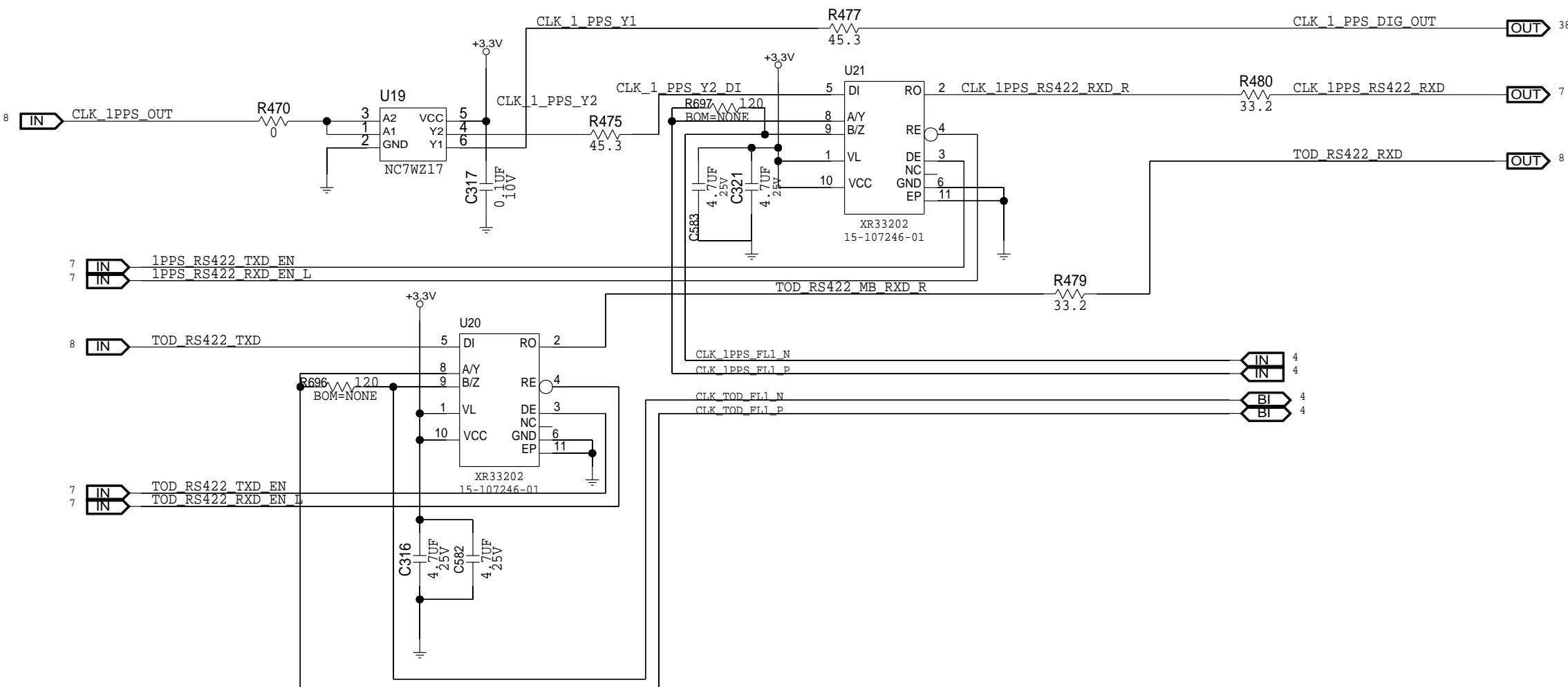






8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

TOD  
ONLY RS422 AND 1PPS / REMOVE RS232

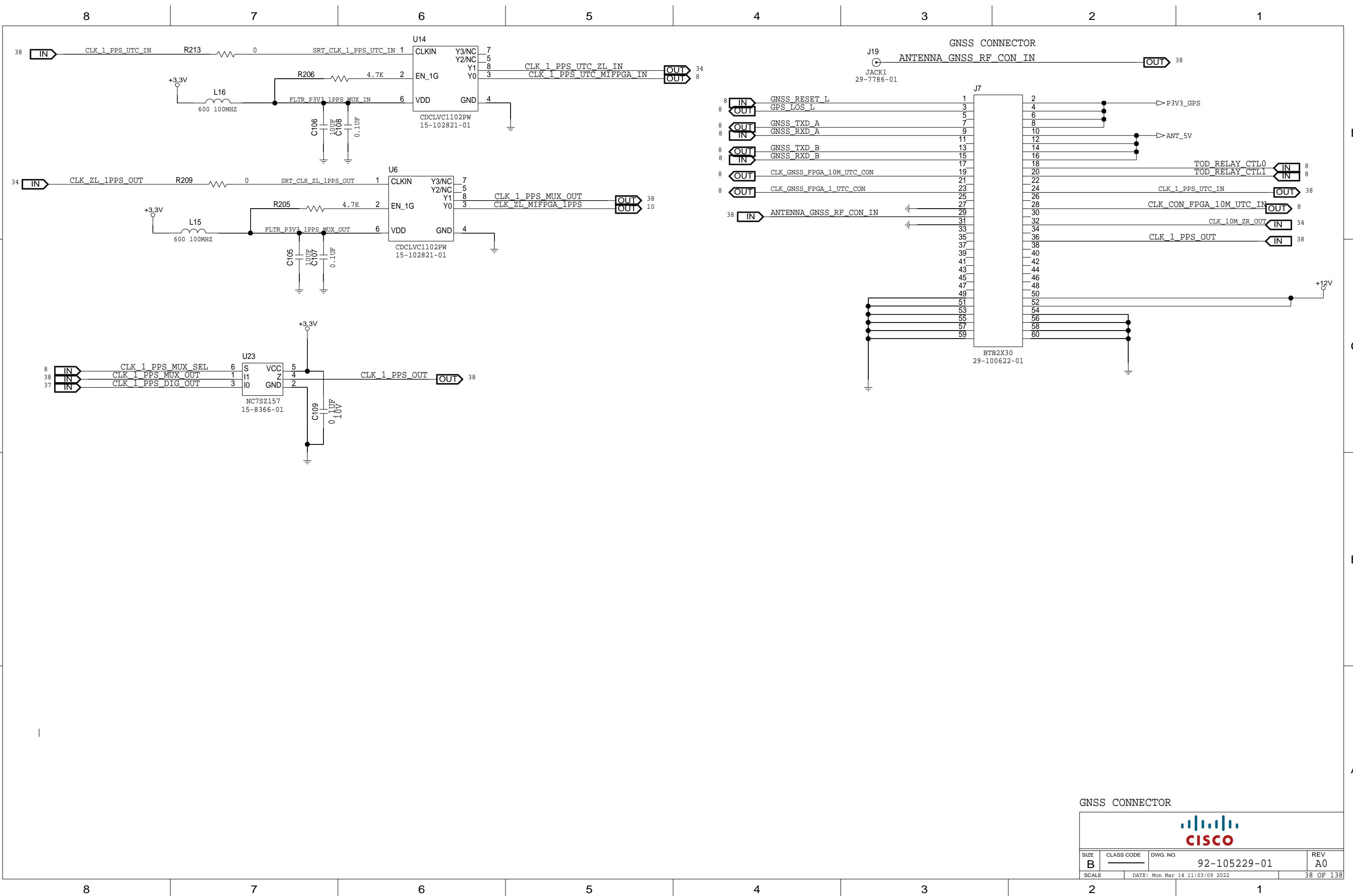


ToD PORT

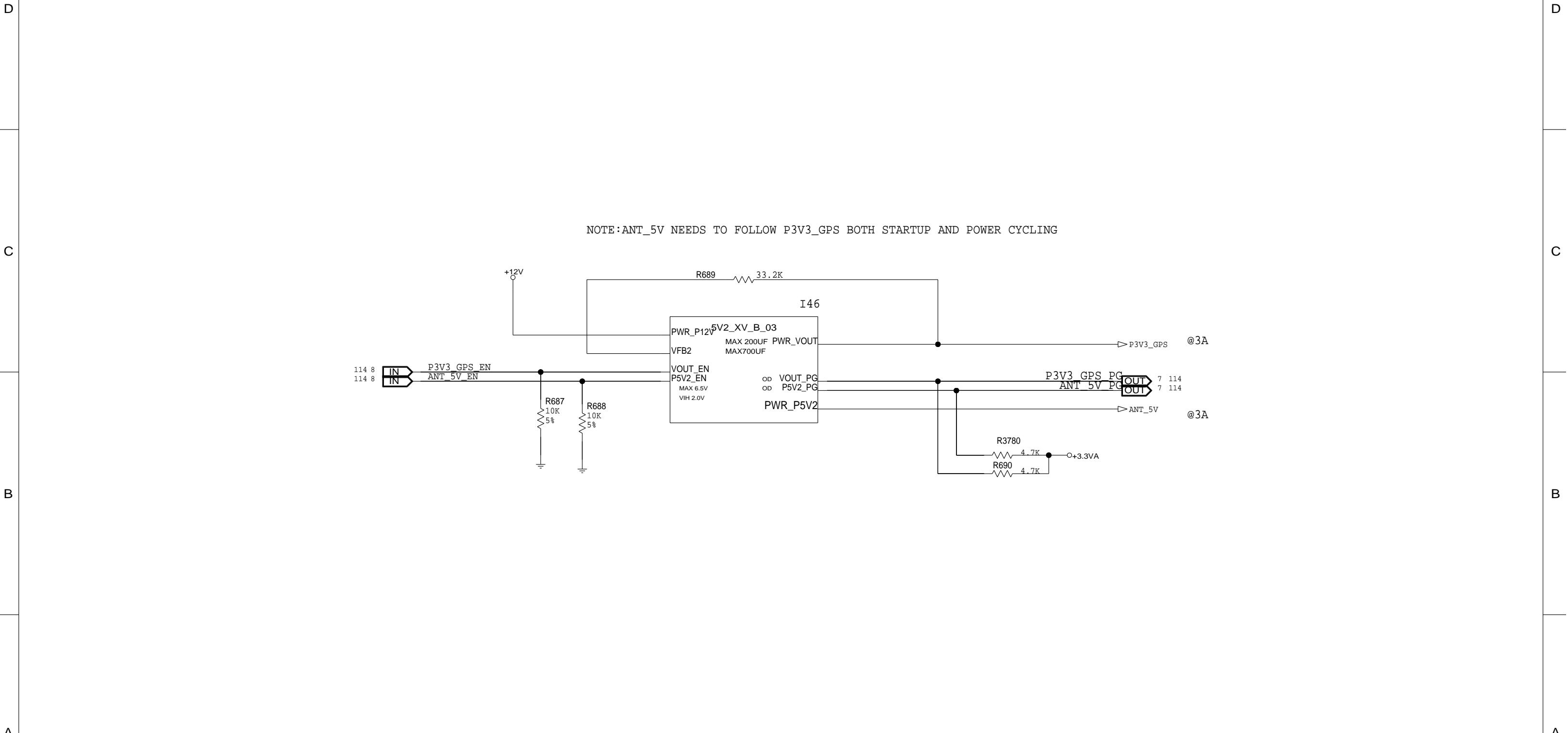


SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:03 2022		37 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



GNSS POWER			
SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:07 2022	39 OF 138	

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

C

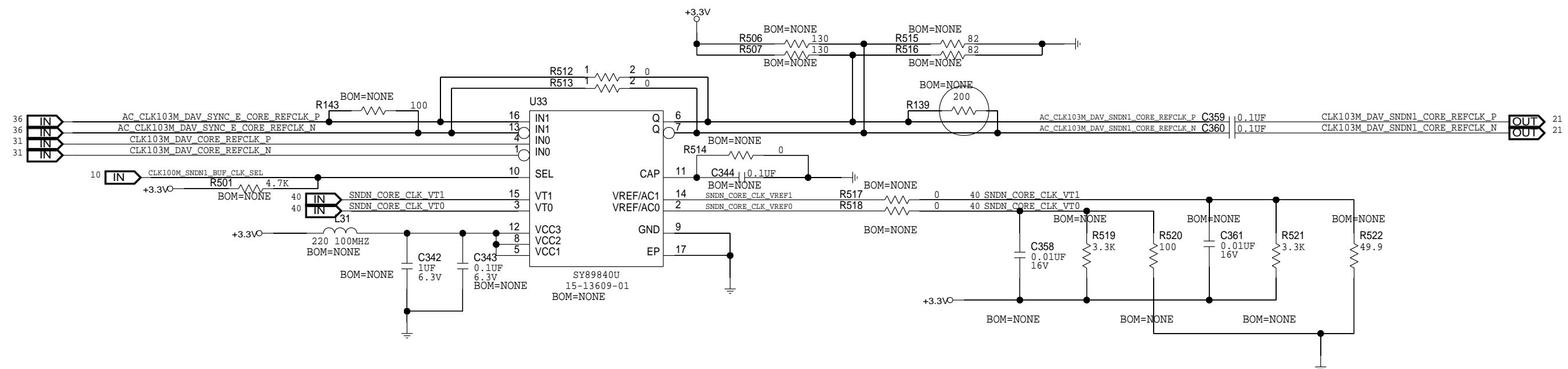
B

B

A

A

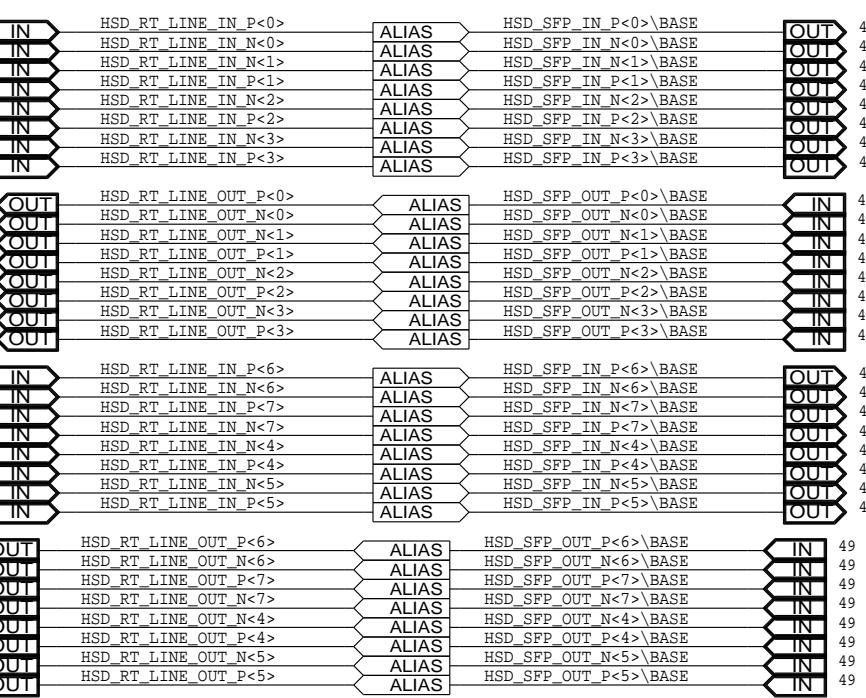
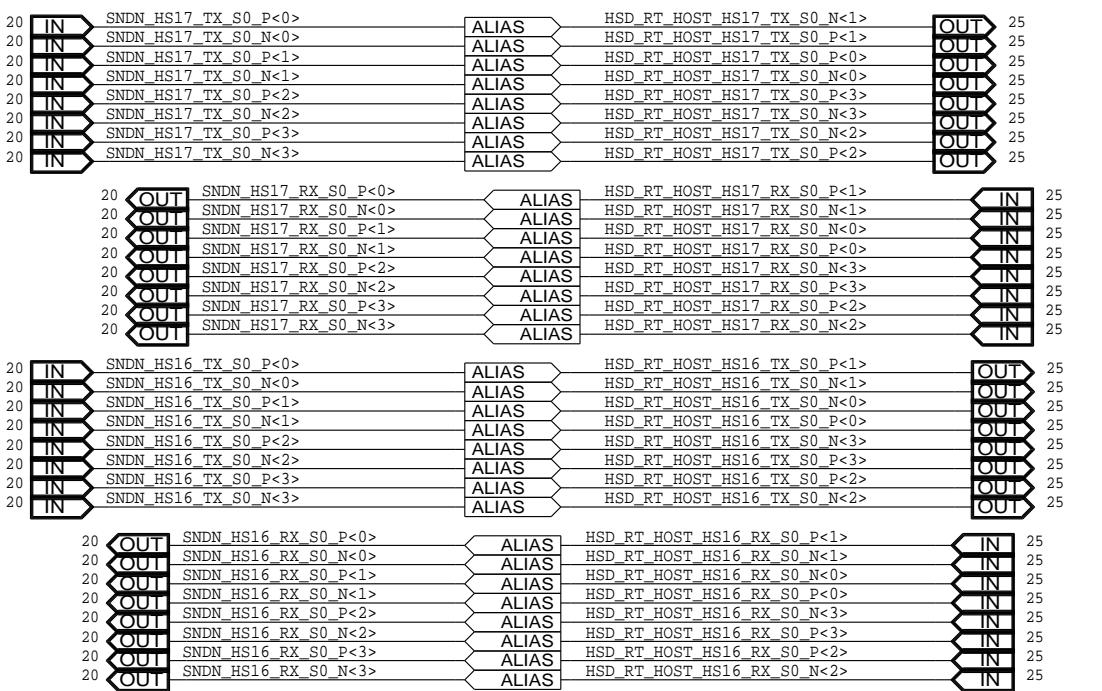
NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTOR AS SHORT AS POSSIBLE  
 NOTE TO CAD: ROUTE NETS OF R512,513 UNDERNEATH U33 ON TOP LAYER  
 NOTES: BYPASS CLOCK MUX



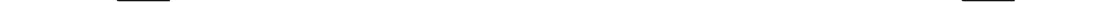
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:02 2022		40 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

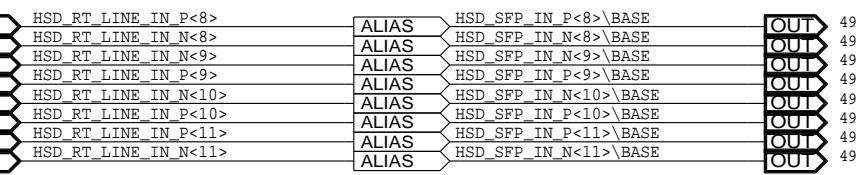
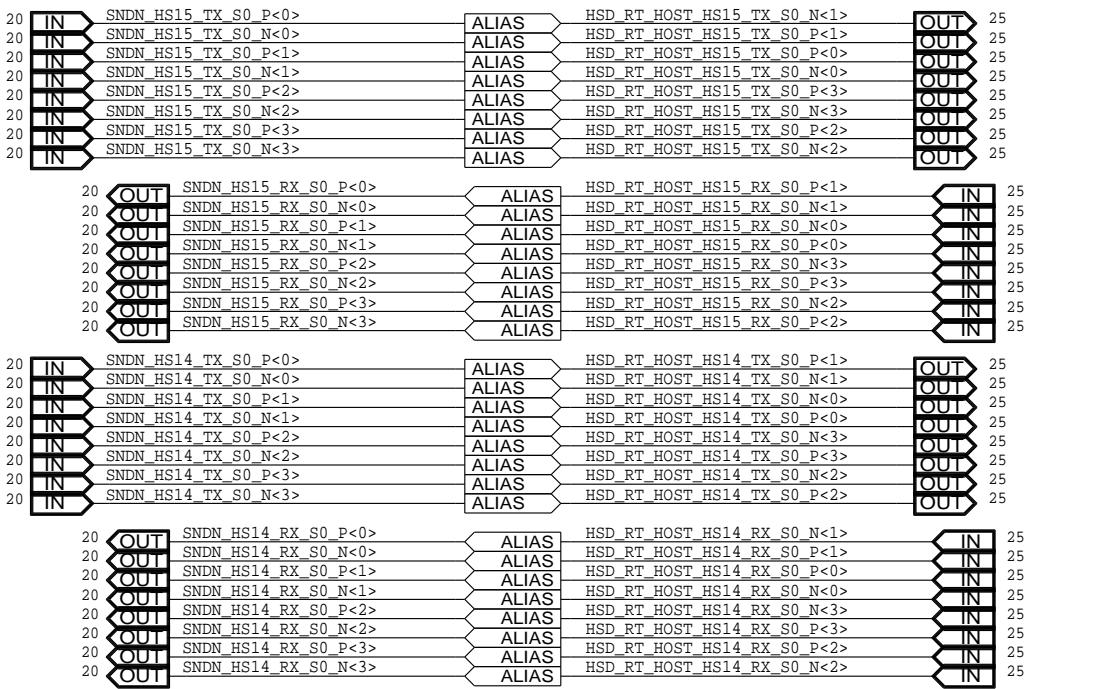
D



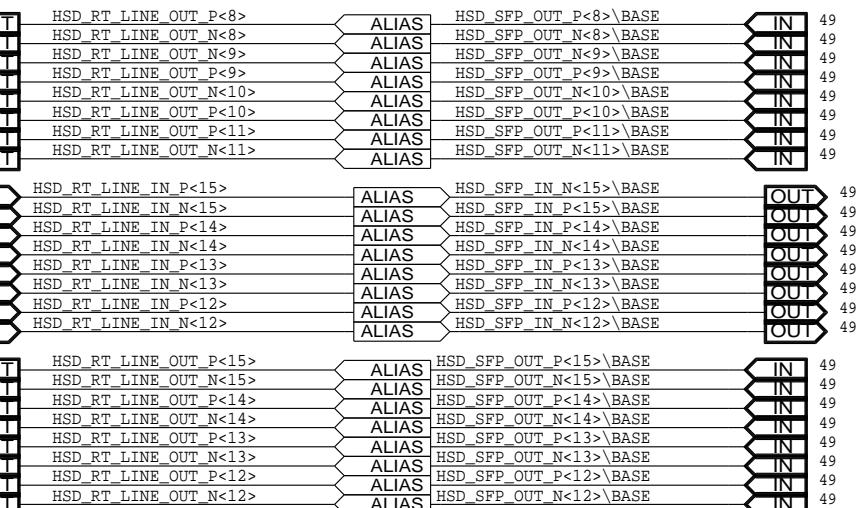
C



B



A

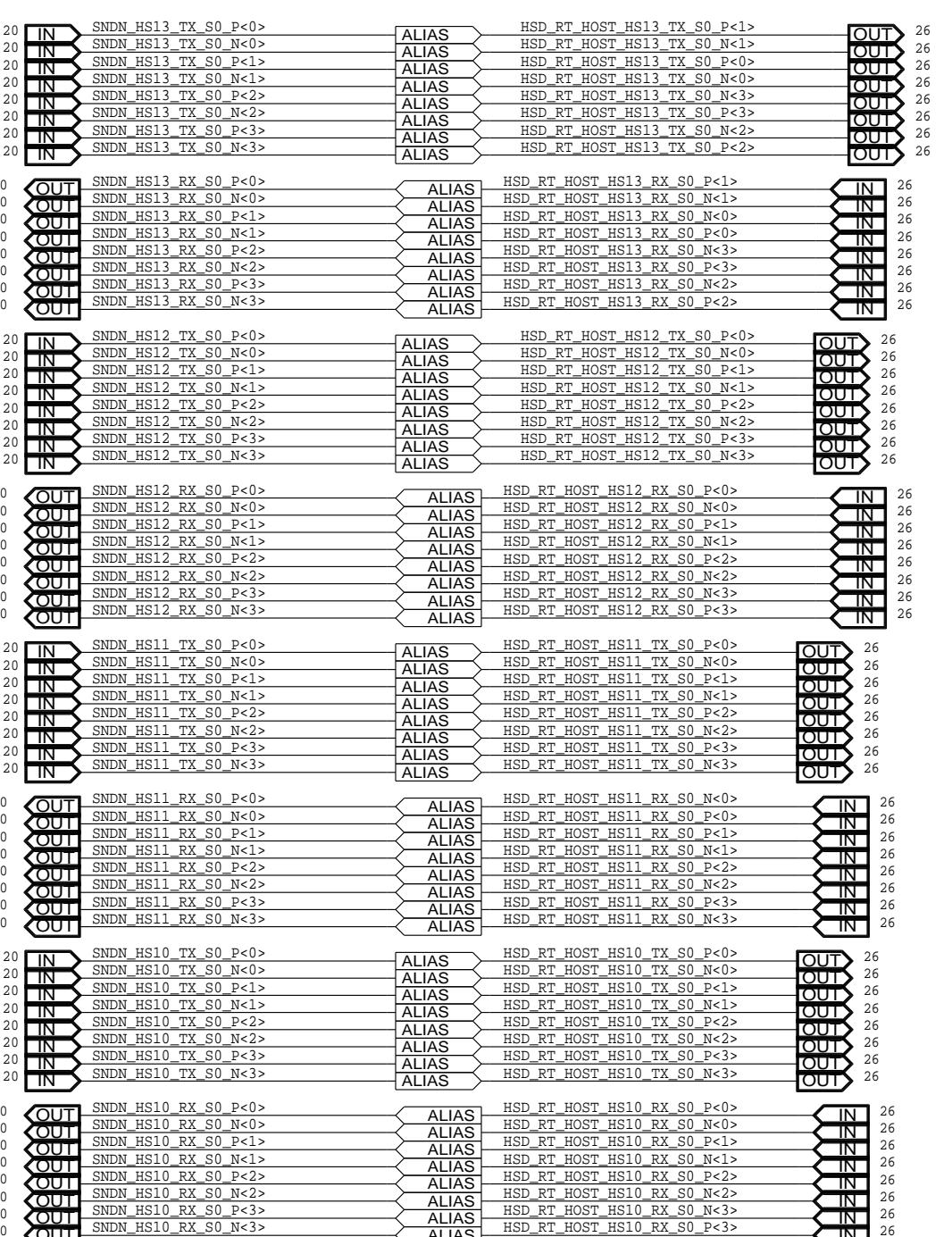


## SFP SERDES MAPPING &lt;15:0&gt;



SIZE	CLASS CODE	DWG. NO.
B	—	92-105229-01
SCALE	DATE: Wed Jun 5 13:37:46 2019	REV A0 41 OF 138

D



13

C

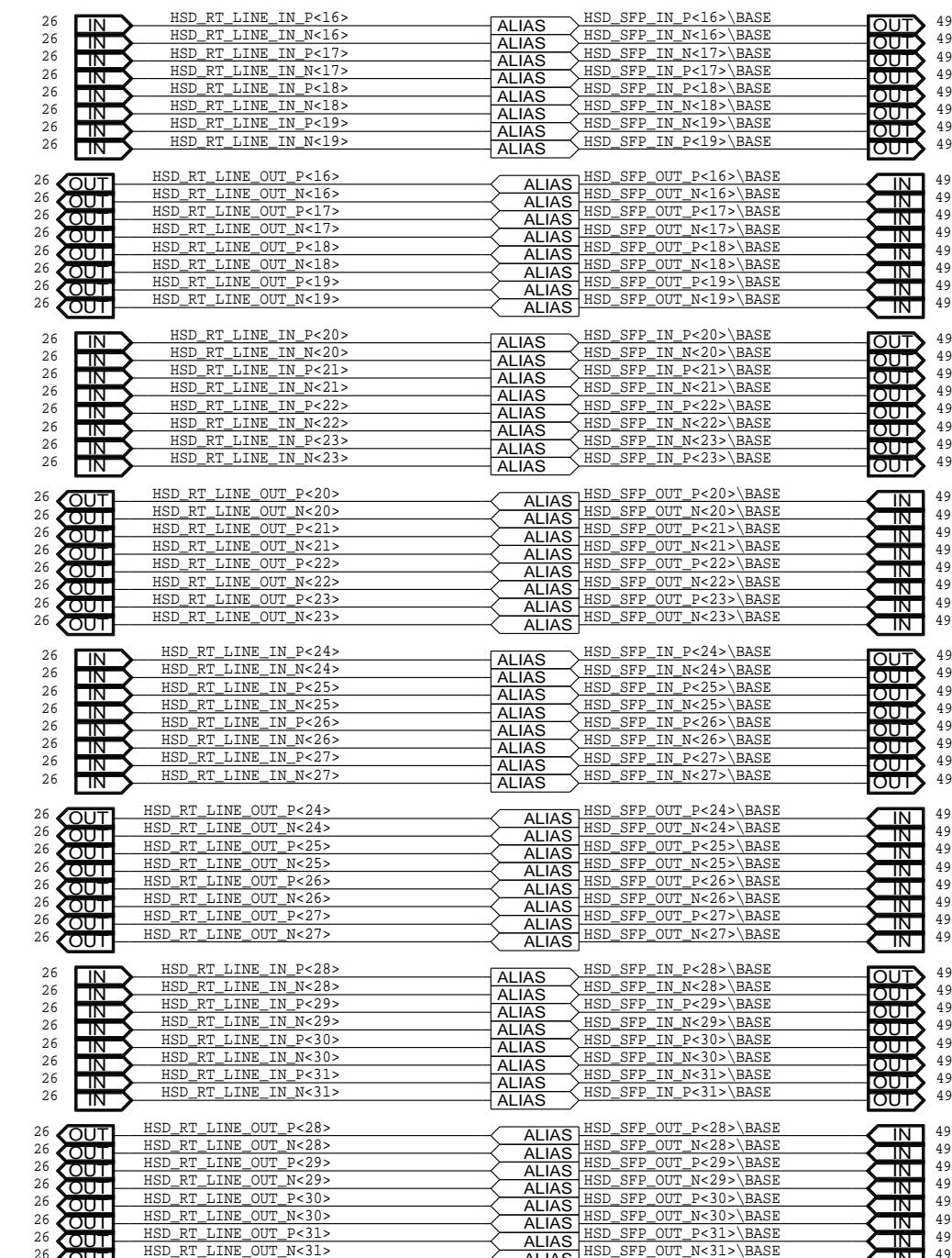
12

B

11

10

A

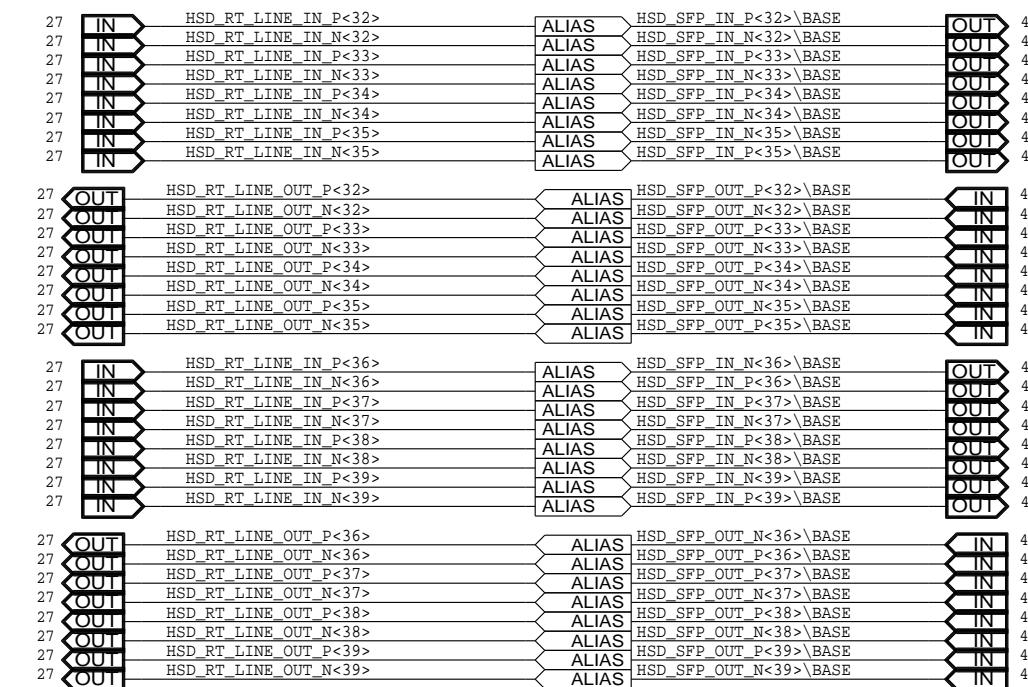
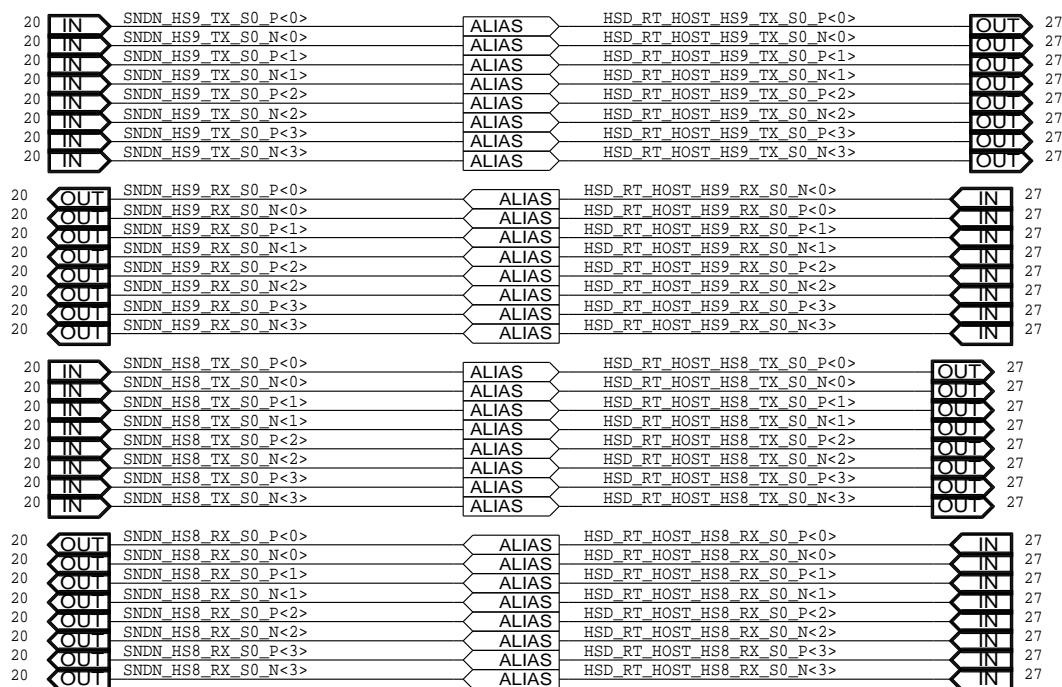


## SFP SERDES MAPPING &lt;31:16&gt;

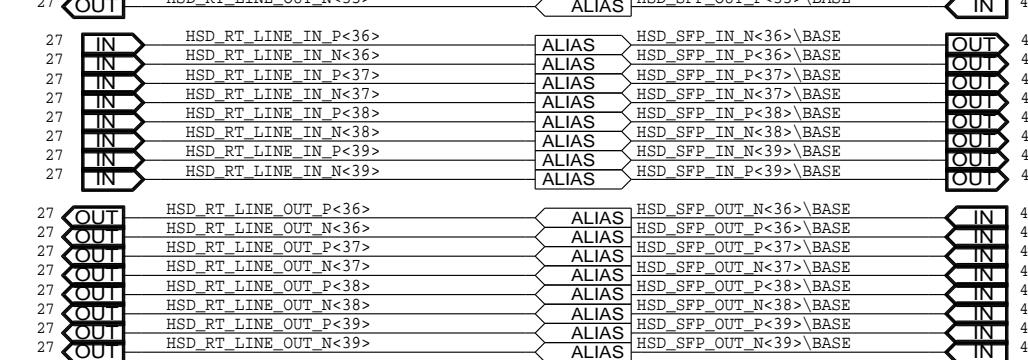
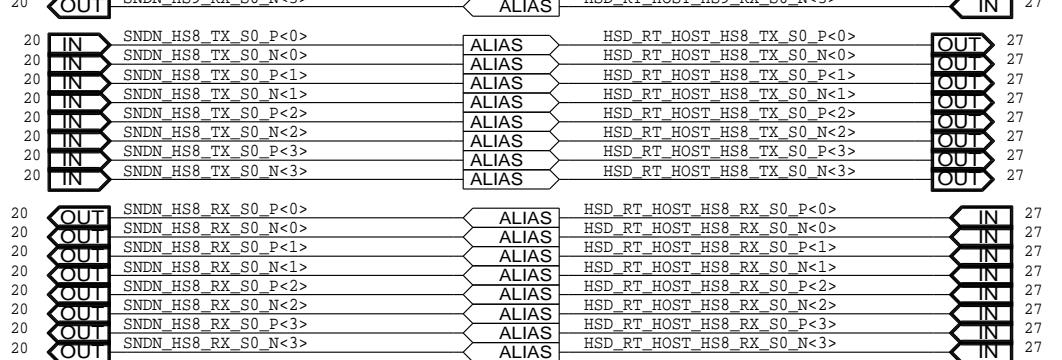


SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Wed Jun 5 13:38:47 2019	REV A0

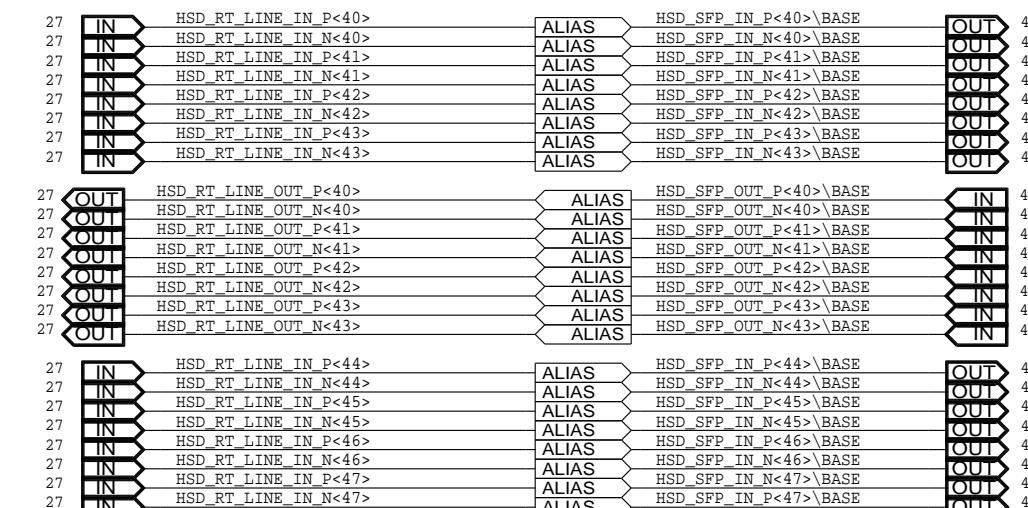
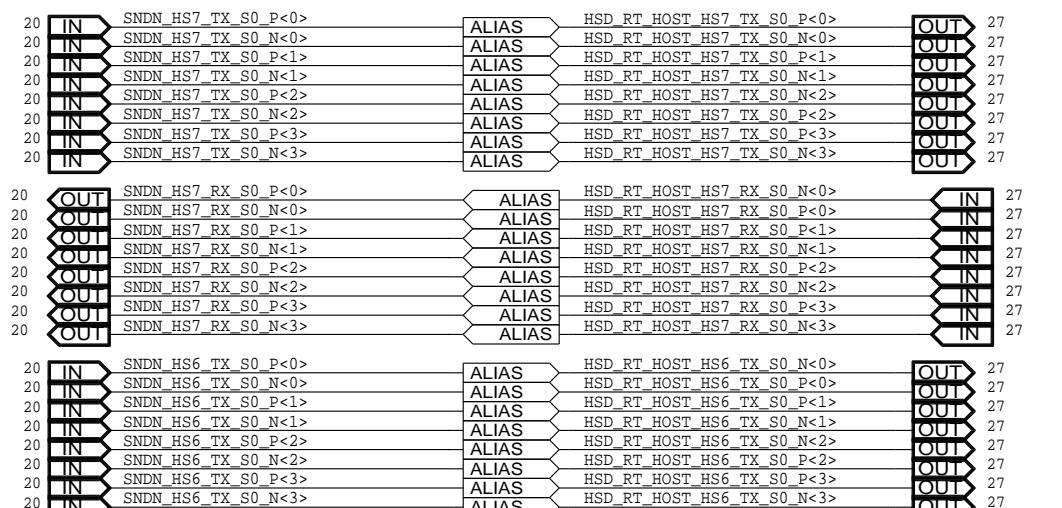
D



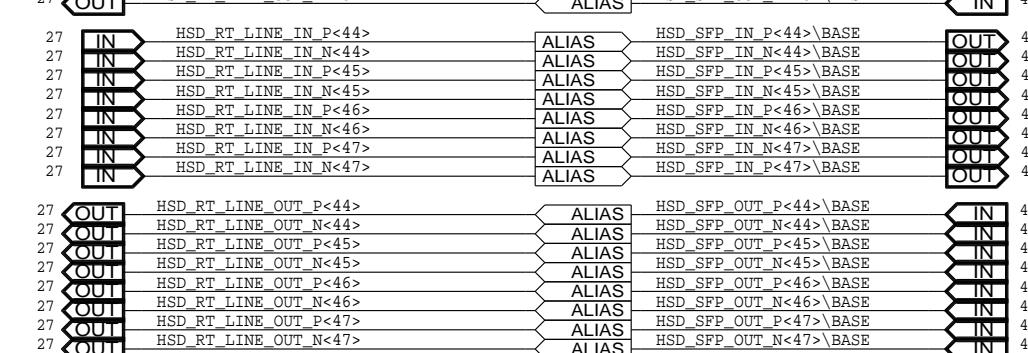
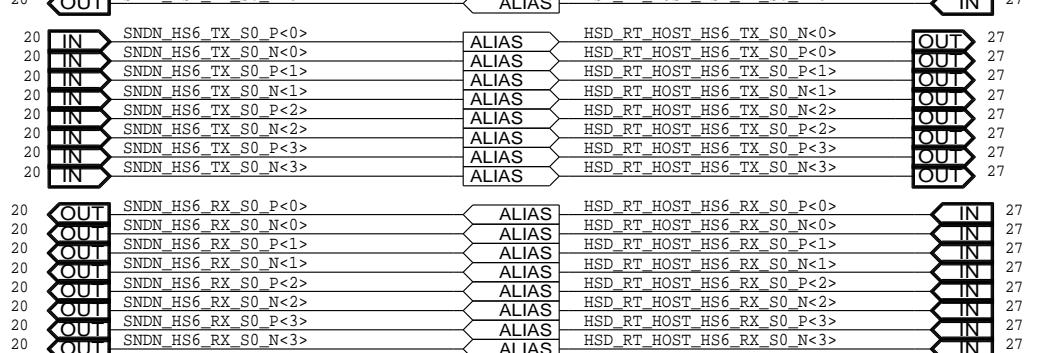
C



B



A

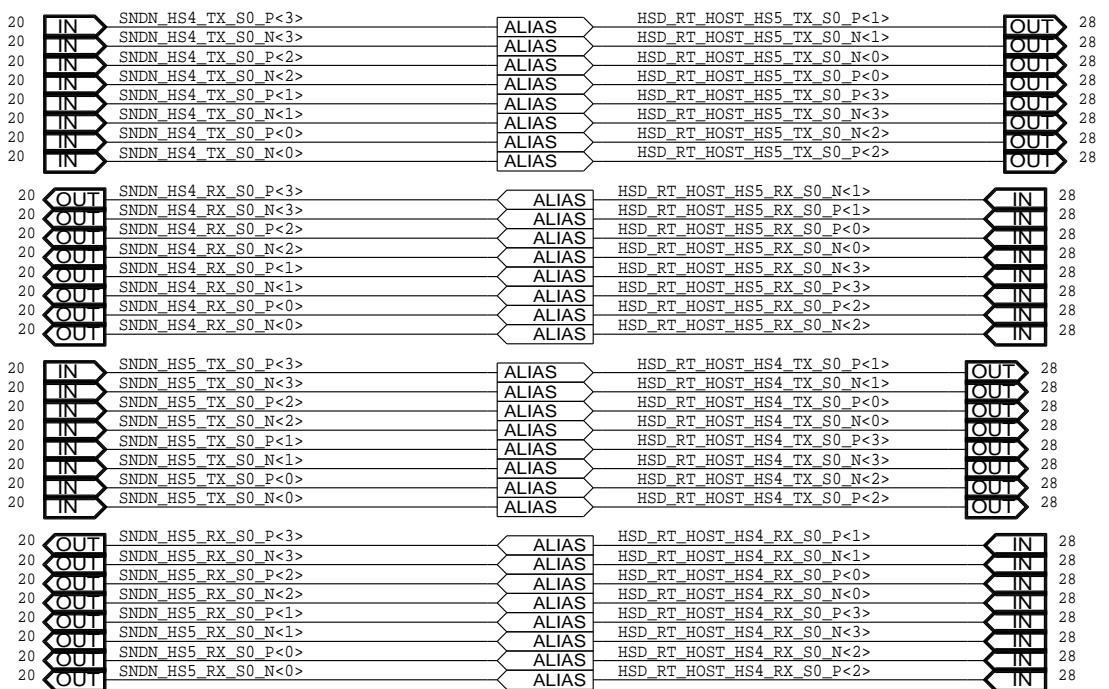


## SFP SERDES MAPPING &lt;47:32&gt;

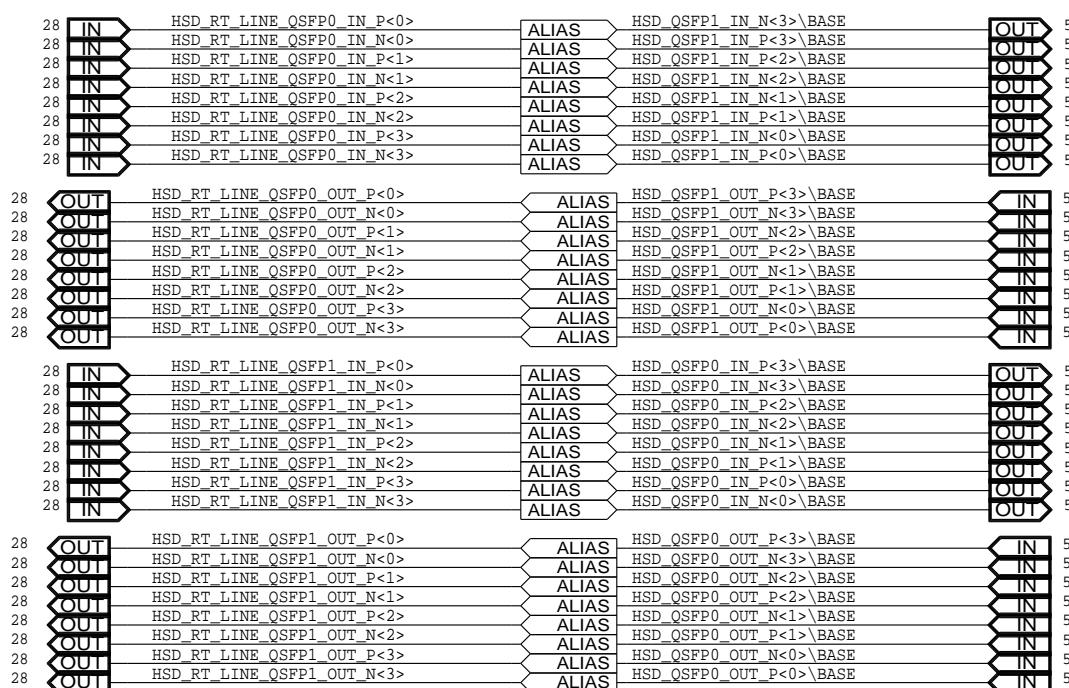


SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Tue Apr 23 20:37:56 2019	REV A0

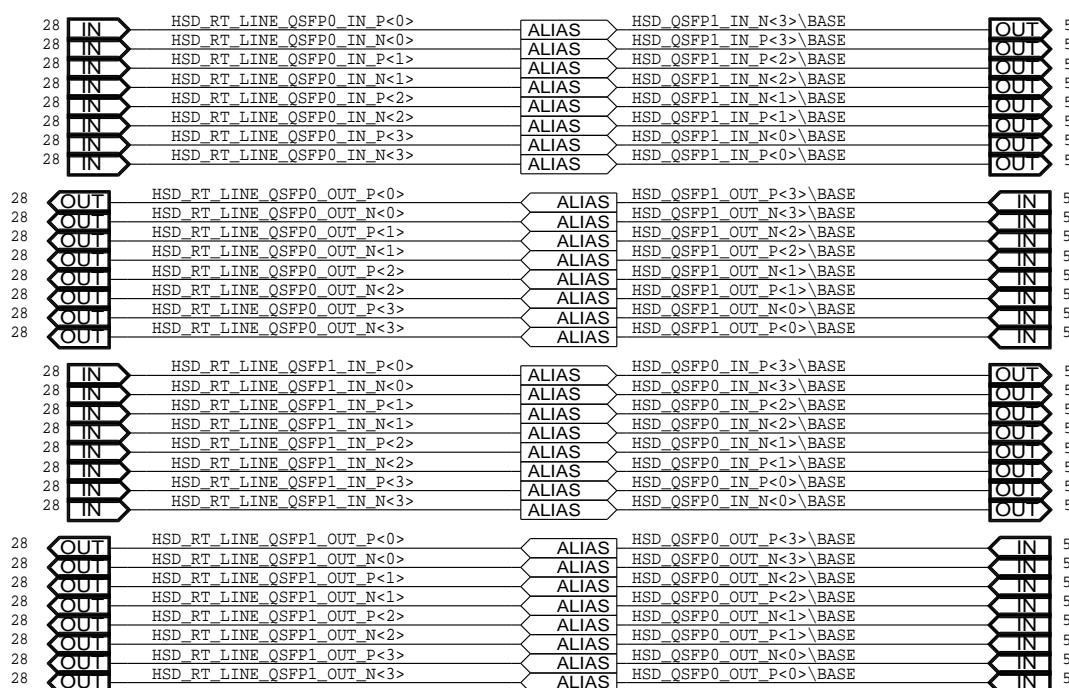
D



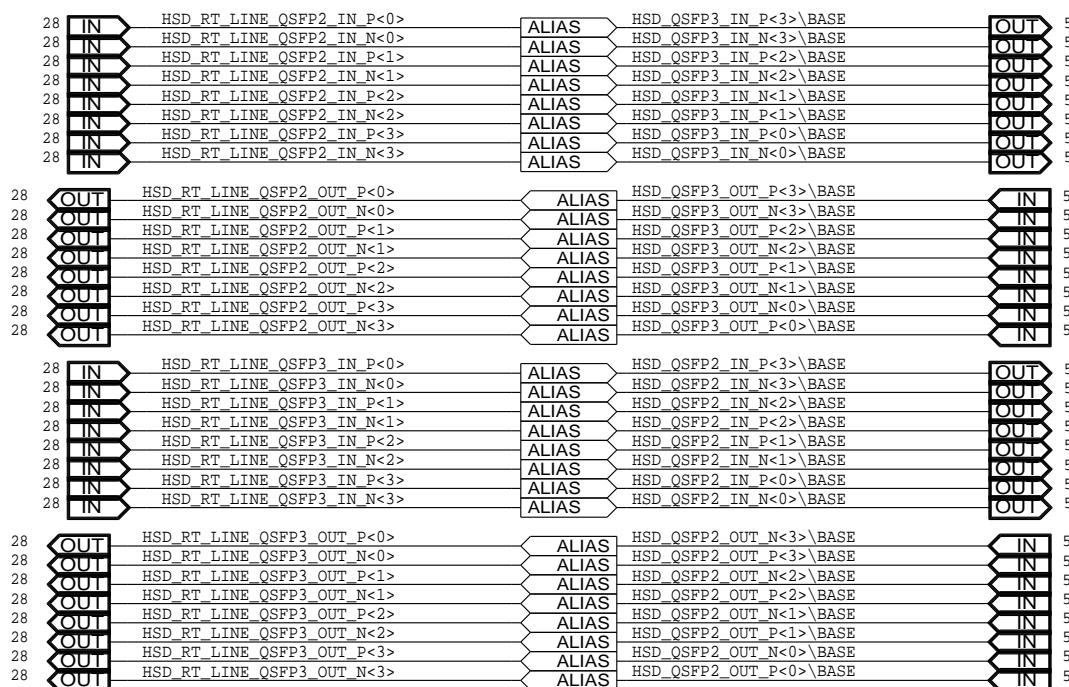
C



D

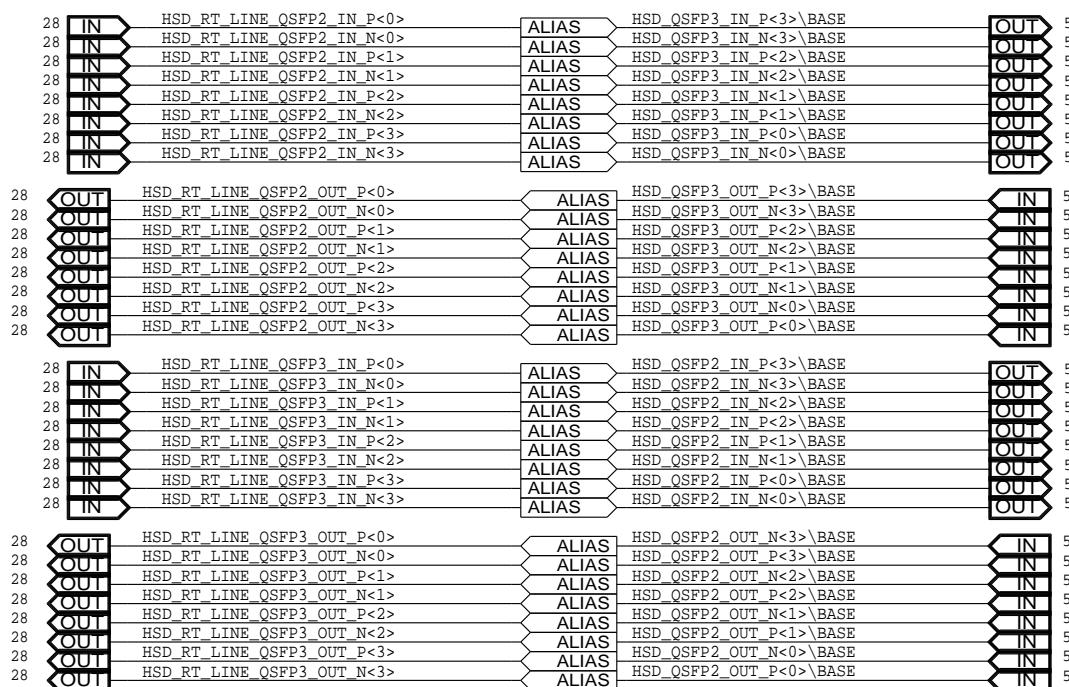


B



B

A



A

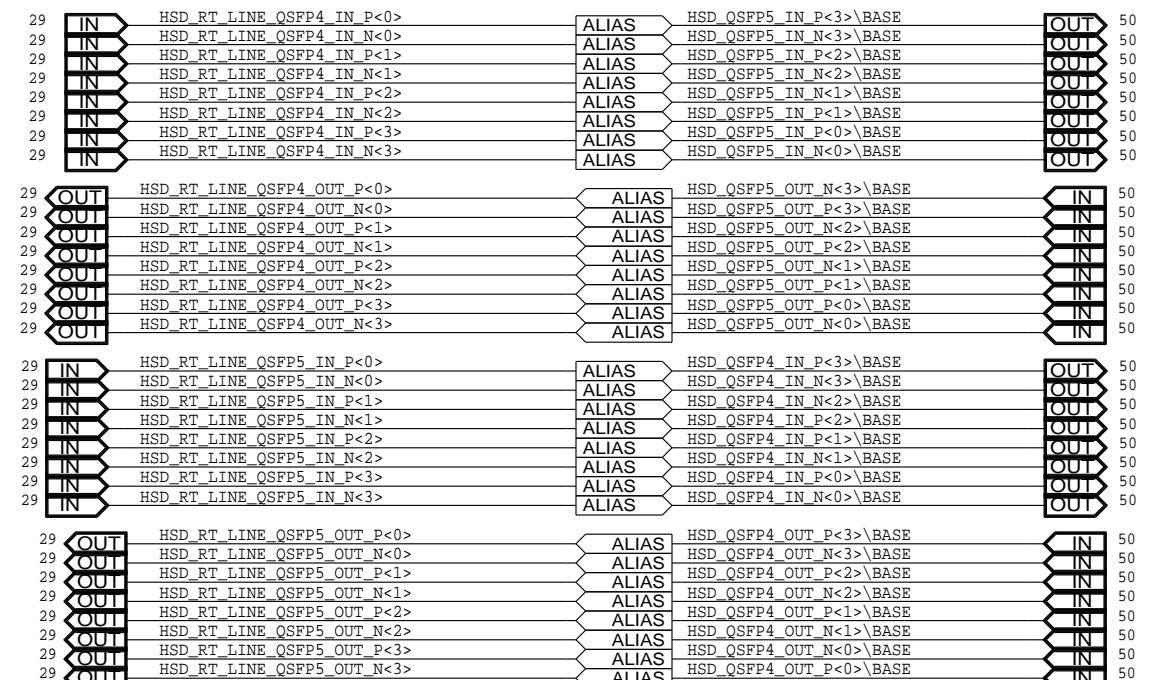
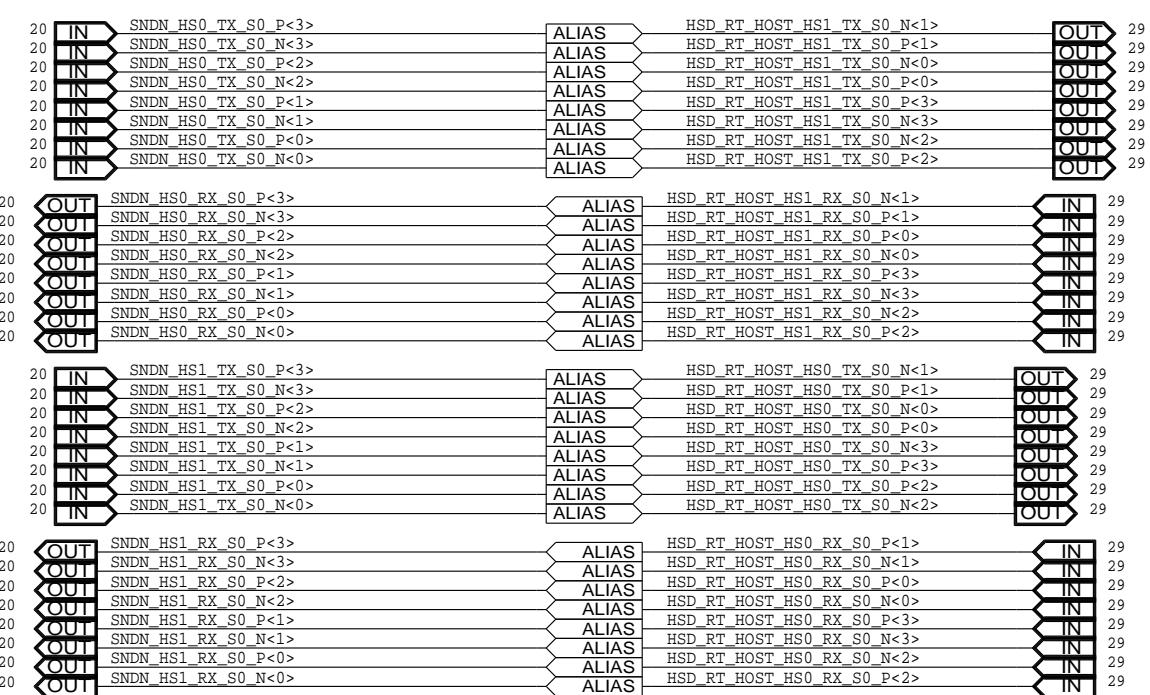
## QSFP SERDES MAPPING &lt;3:0&gt;



SIZE	CLASS CODE	DWG. NO.
B	—	92-105229-01
SCALE	DATE: Tue Apr 23 20:37:57 2019	44 OF 138

D

D



1

C

A

A

## QSFP SERDES MAPPING <5:4>



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Tue Apr 23 20:37:58 2019		45 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

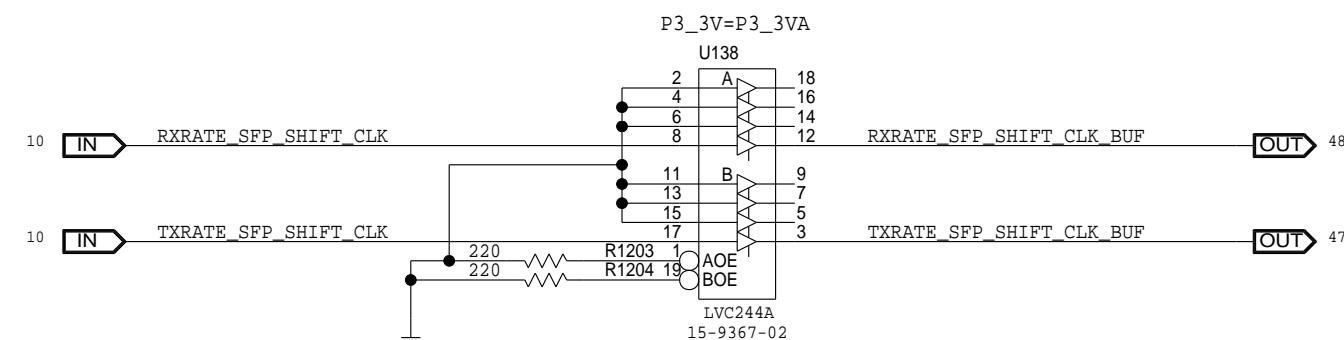
C

B

B

A

A



CLK BUF SHIFT REG



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0

SCALE DATE: Mon Mar 14 11:03:05 2022 46 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8

7

6

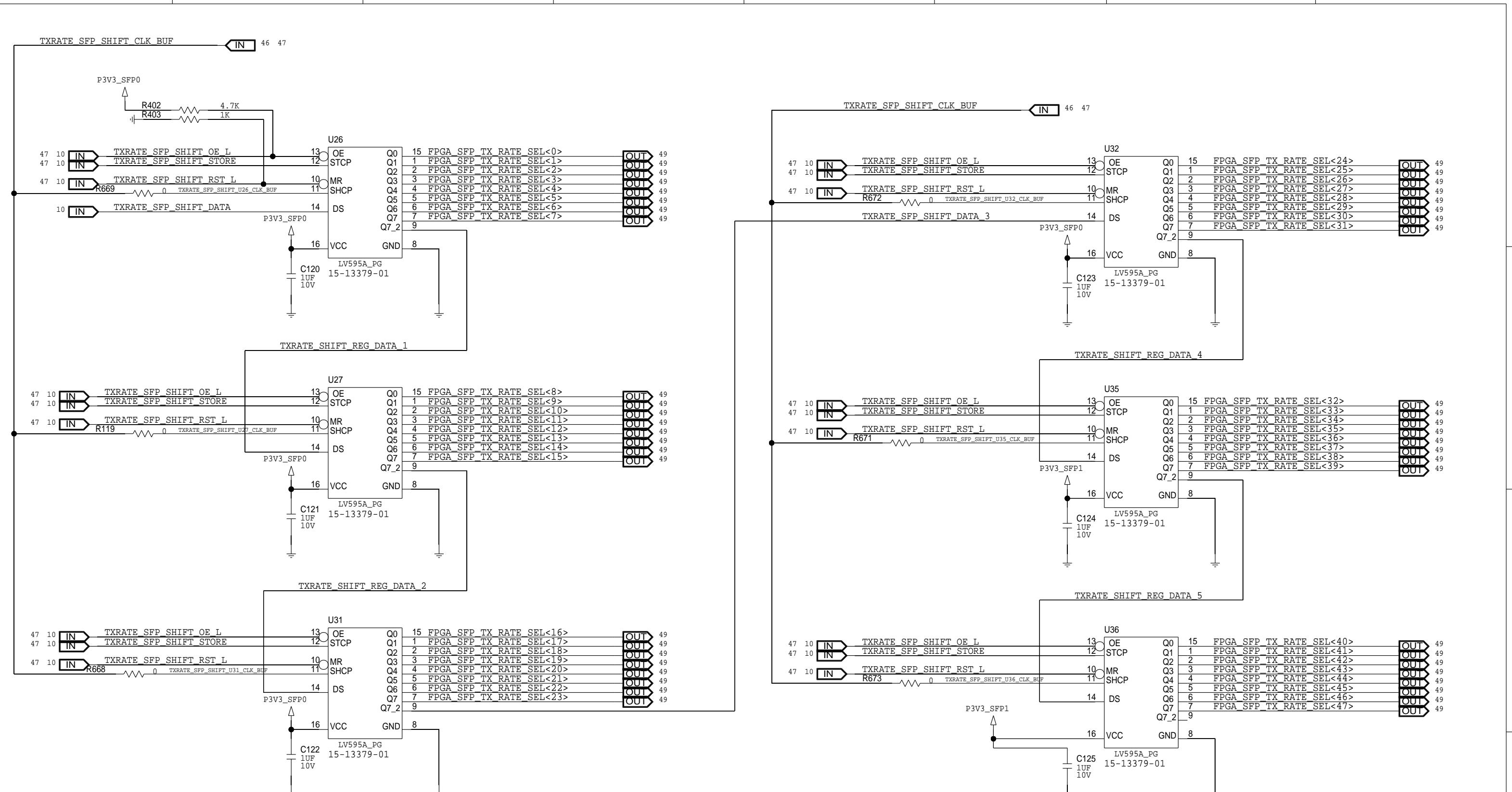
5

4

3

2

1



SFP TX RATE SEL (0..47) SHIFT REG



SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Mon Mar 14 11:03:15 2022	REV A0

8

7

6

5

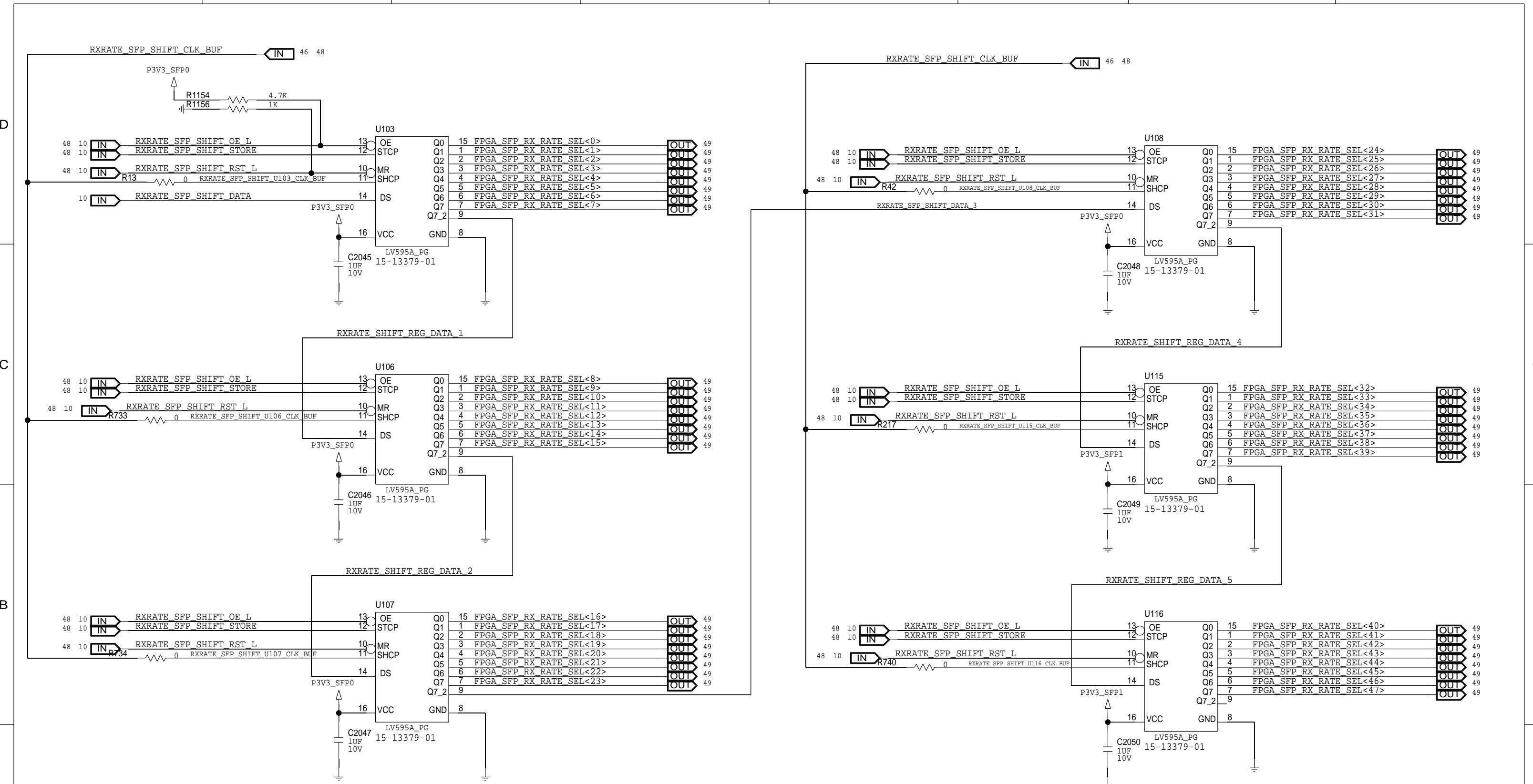
4

3

2

1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

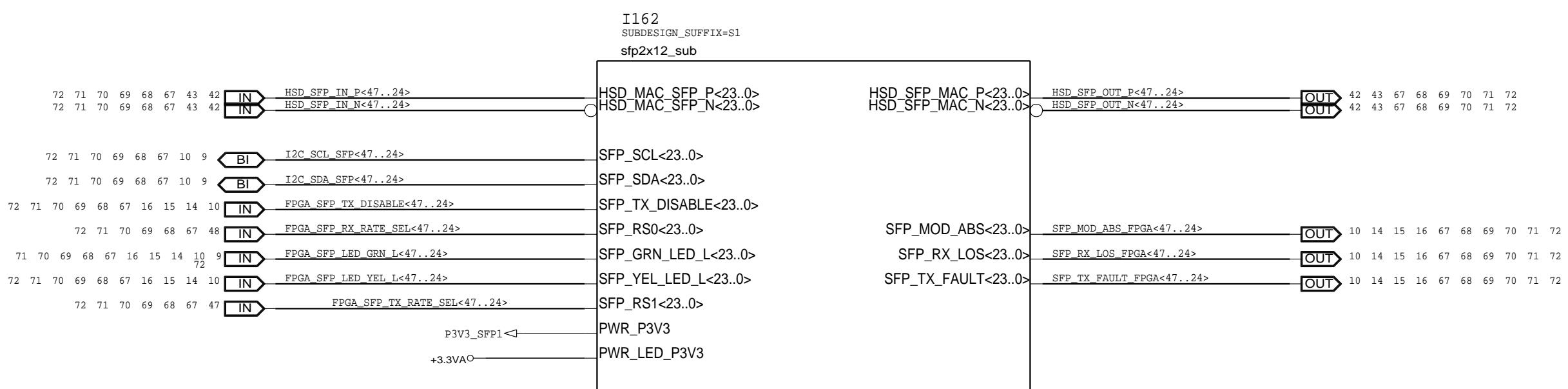
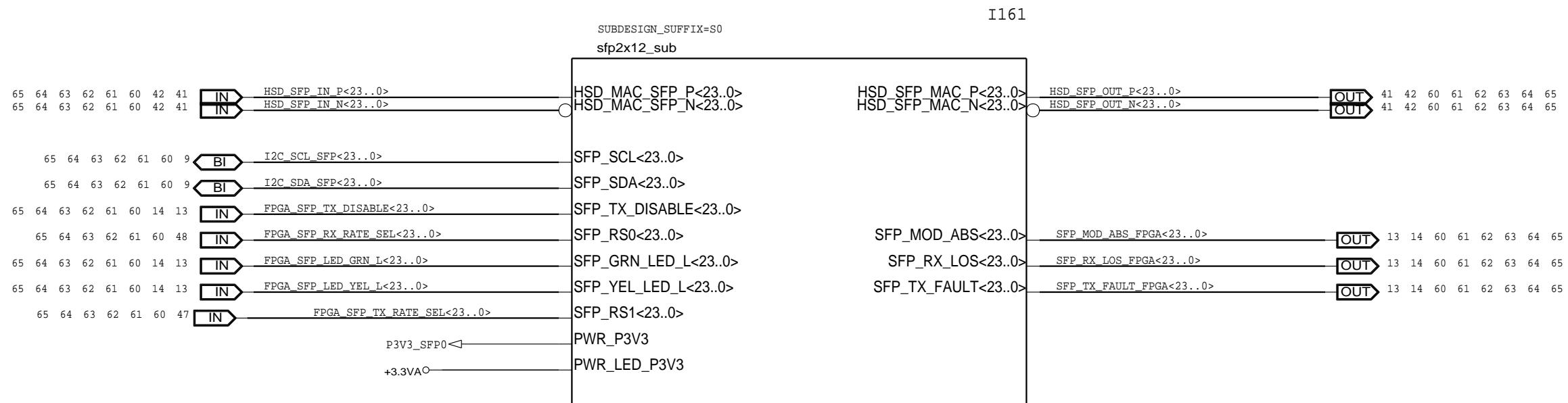


SFP RX RATE SEL (0..47) SHIFT REG



SIZE	CLASS CODE	DWG. NO.
B	—	92-105229-01
SCALE	DATE: Mon Mar 14 11:03:15 2022	REV A0 48 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



## SFP+ HIERARCHY INSTANCIATION

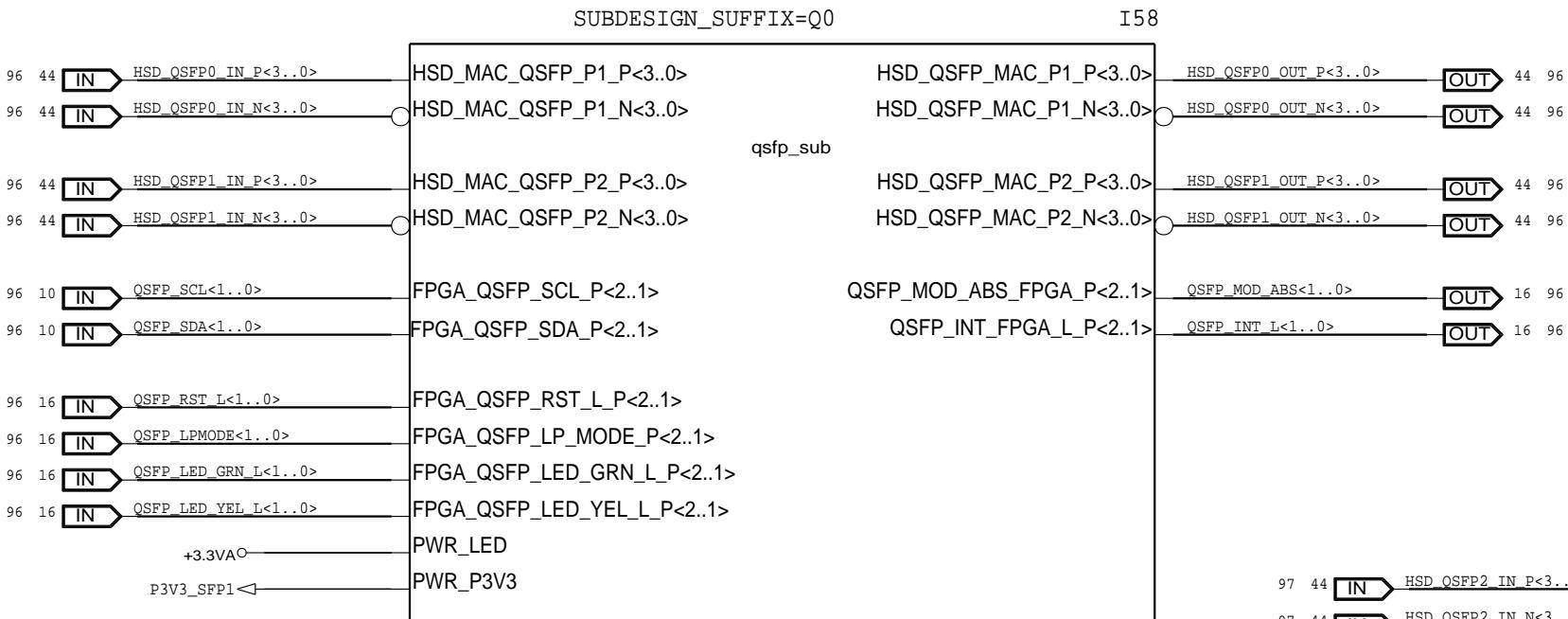


SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:57 2022		49 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

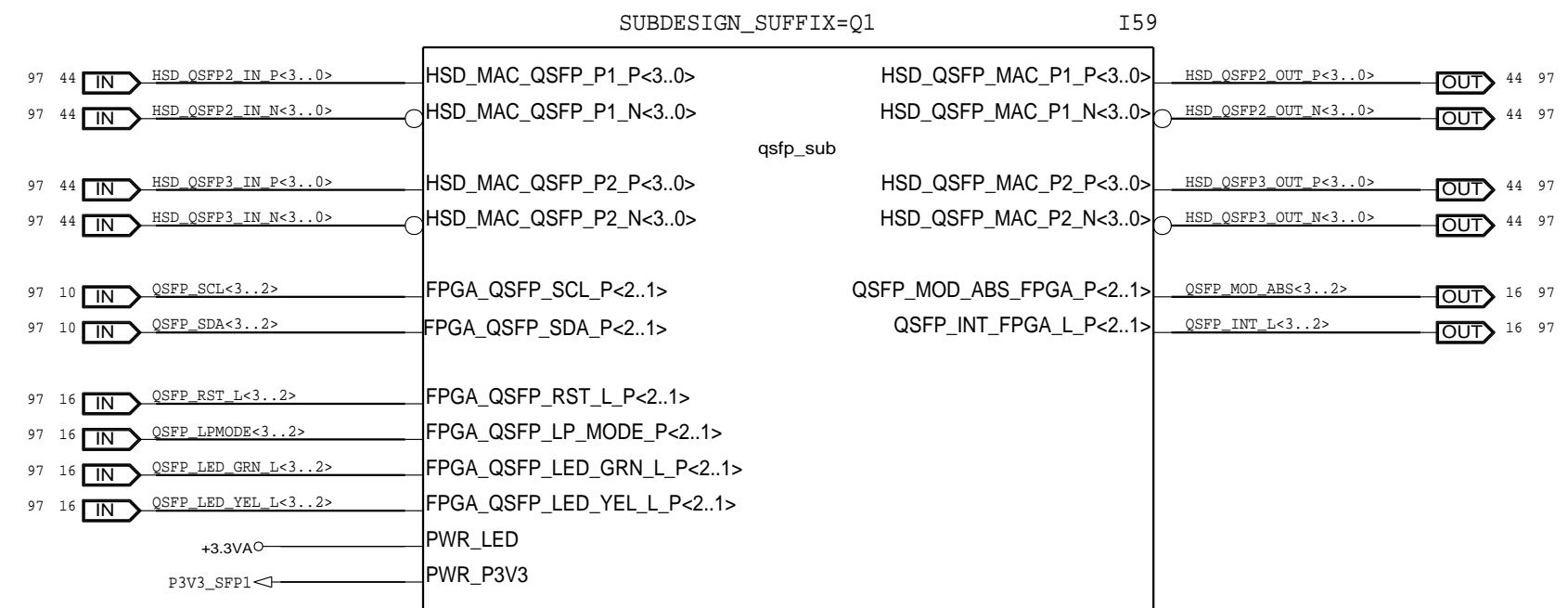
D

D



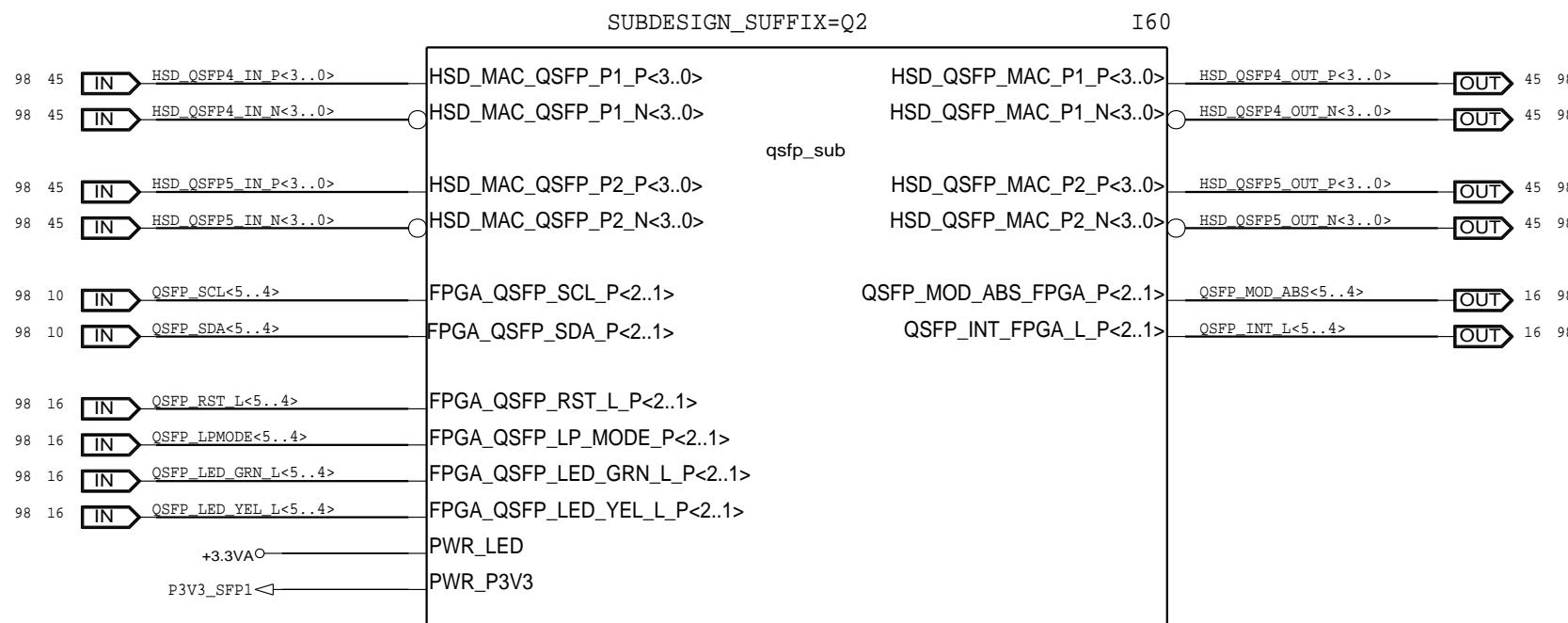
C

C



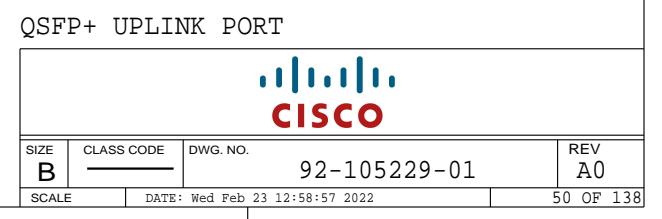
B

B



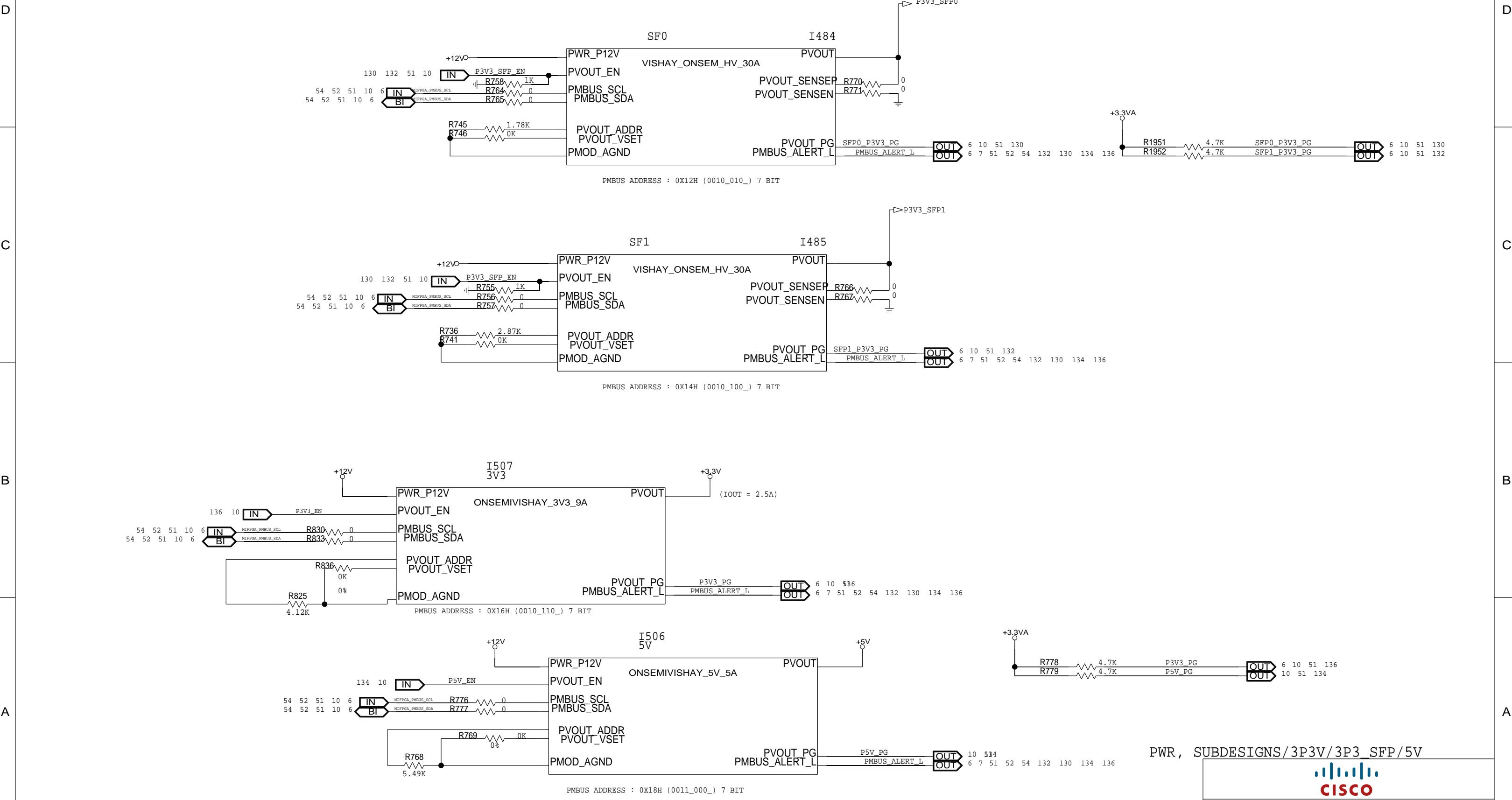
A

A



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# ALTERNATIVE CIRCUIT



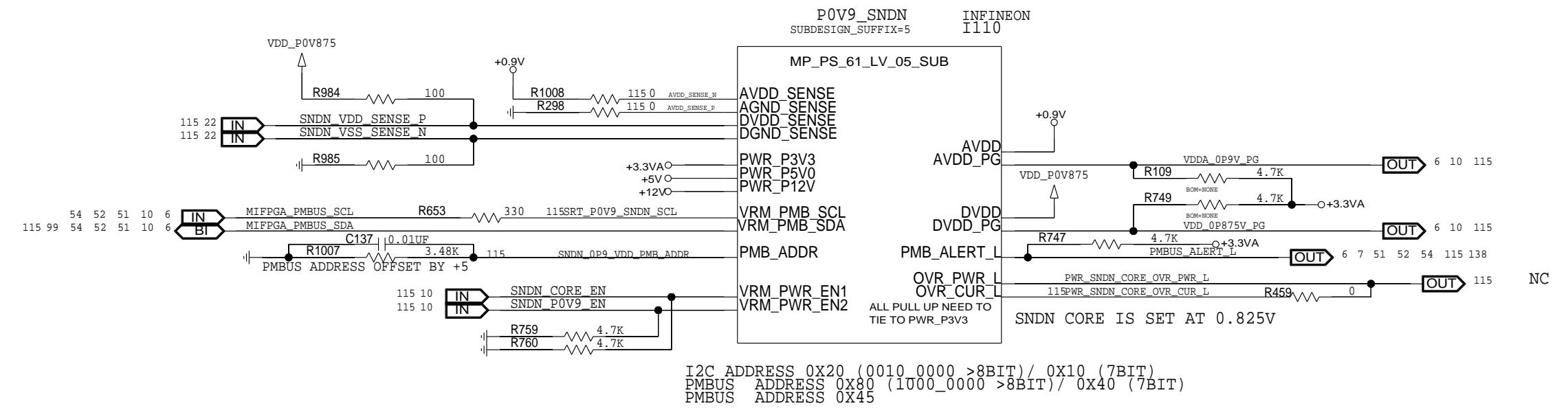
PWR , SUBDESIGNS/3P3V/3P3\_SFP/5V



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:11 2022	REV A0 51 OF 138

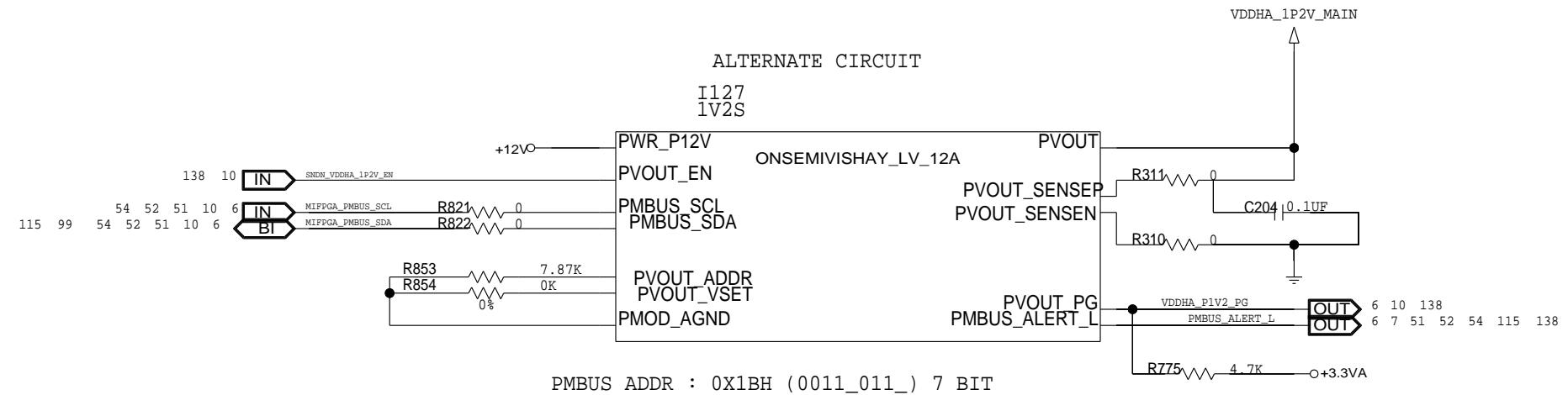
D

D



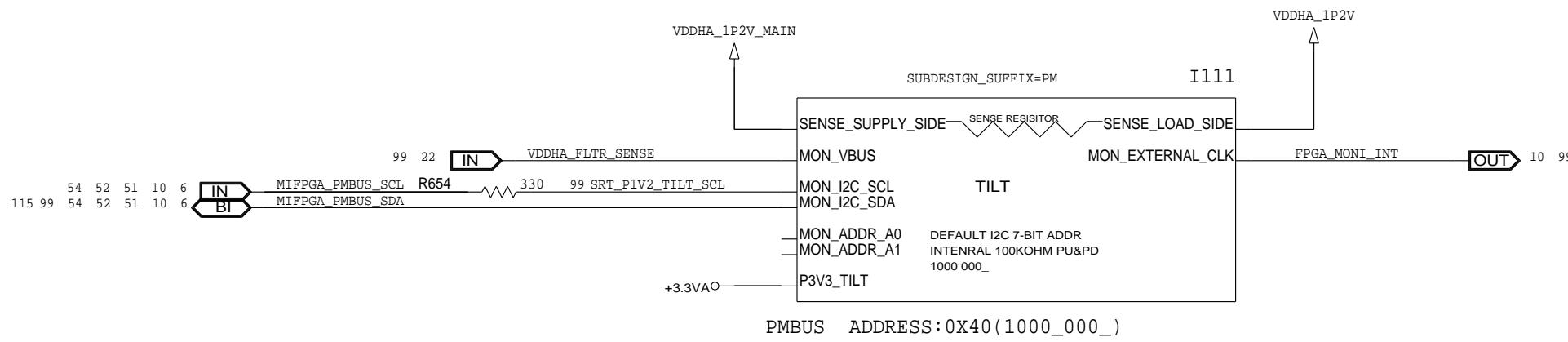
C

C



B

B



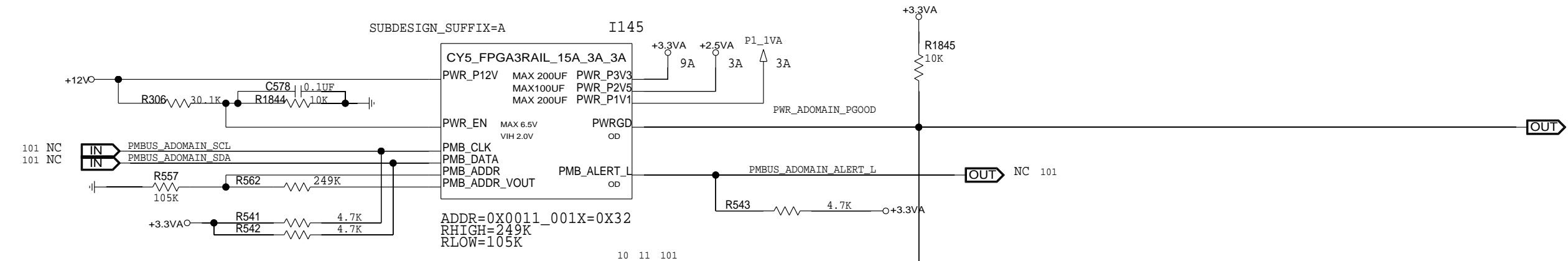
A

A

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

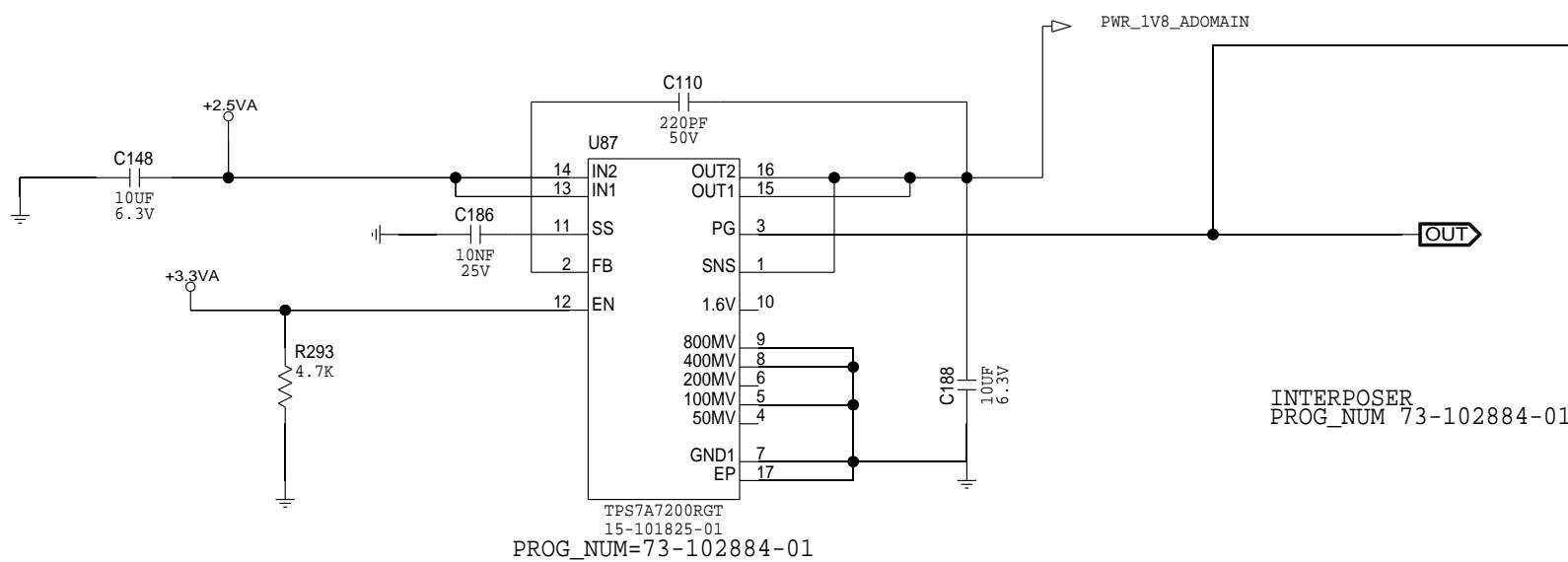
D

D



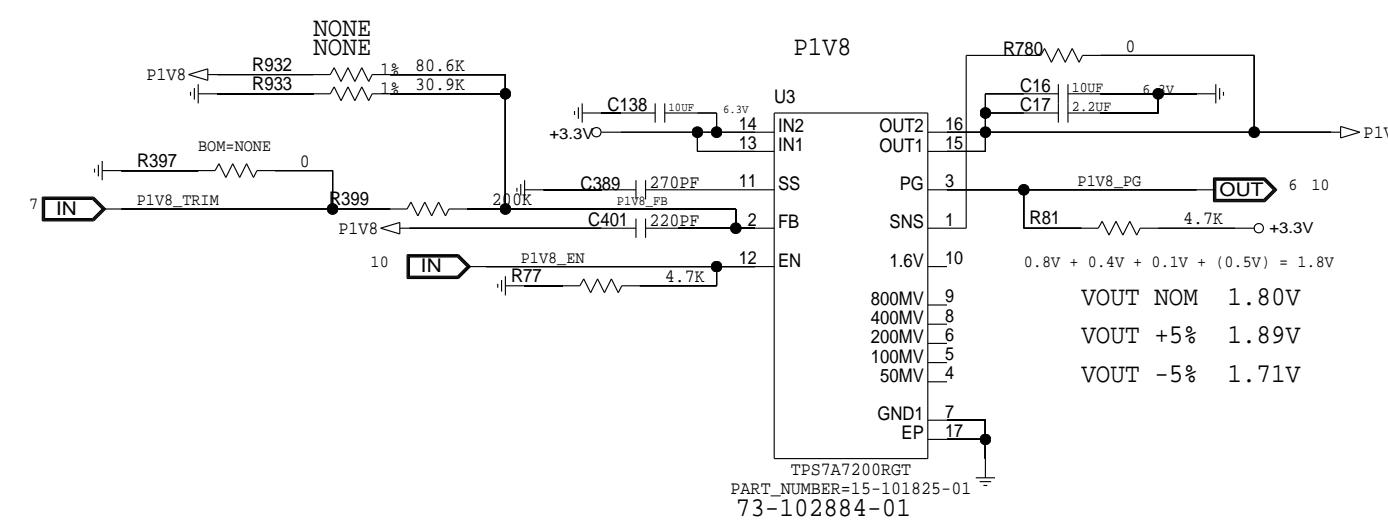
C

C



B

B



A

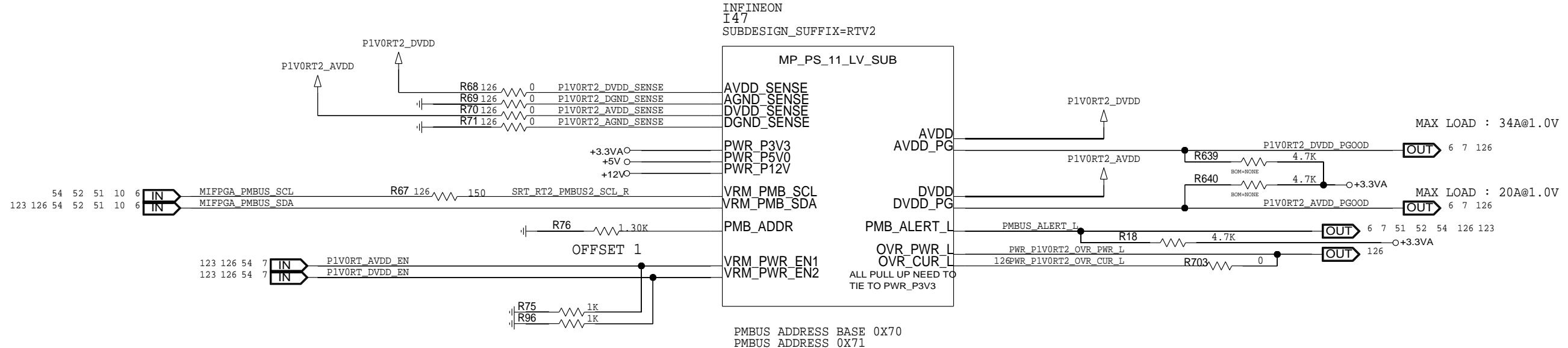
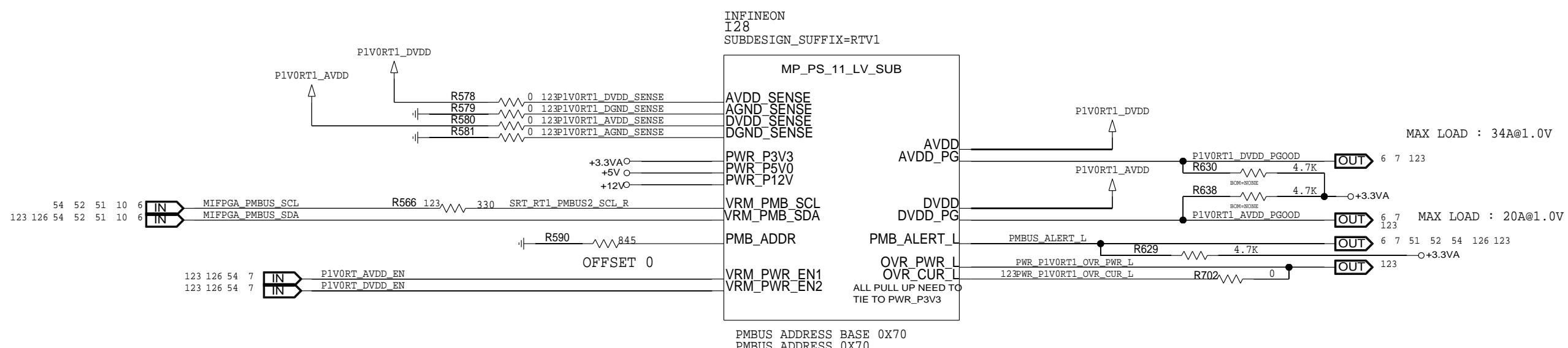
A

PWR, A DOMAIN, P1v8



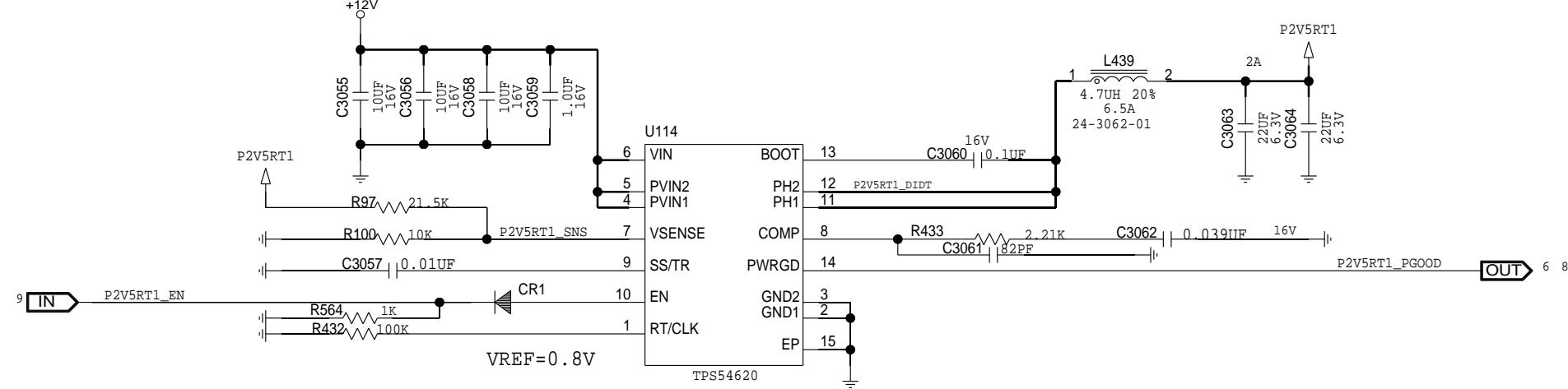
SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Mon Mar 14 11:03:07 2022	REV A0

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



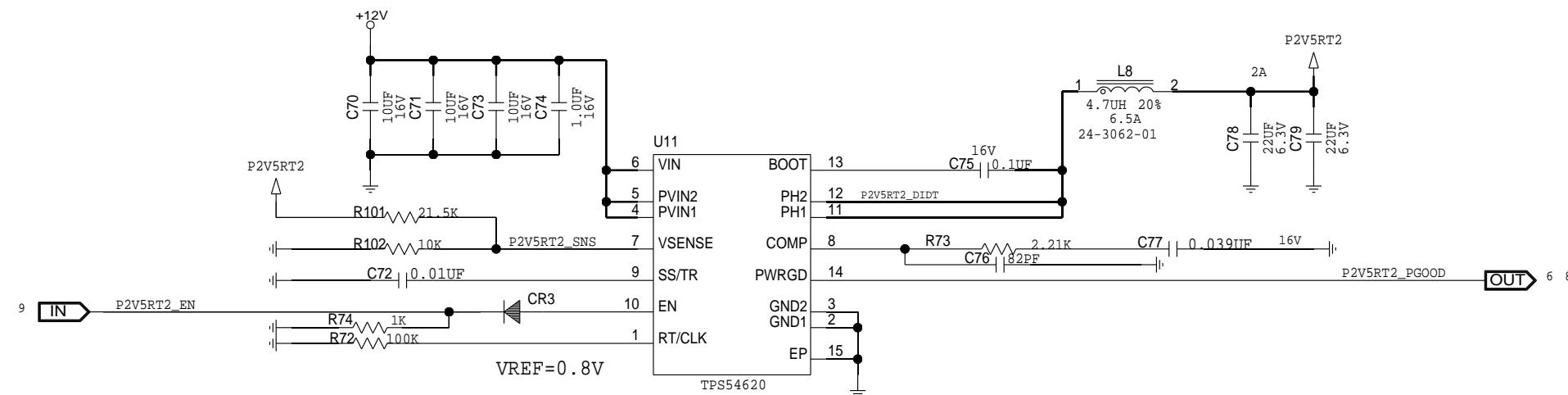
D

D



C

C

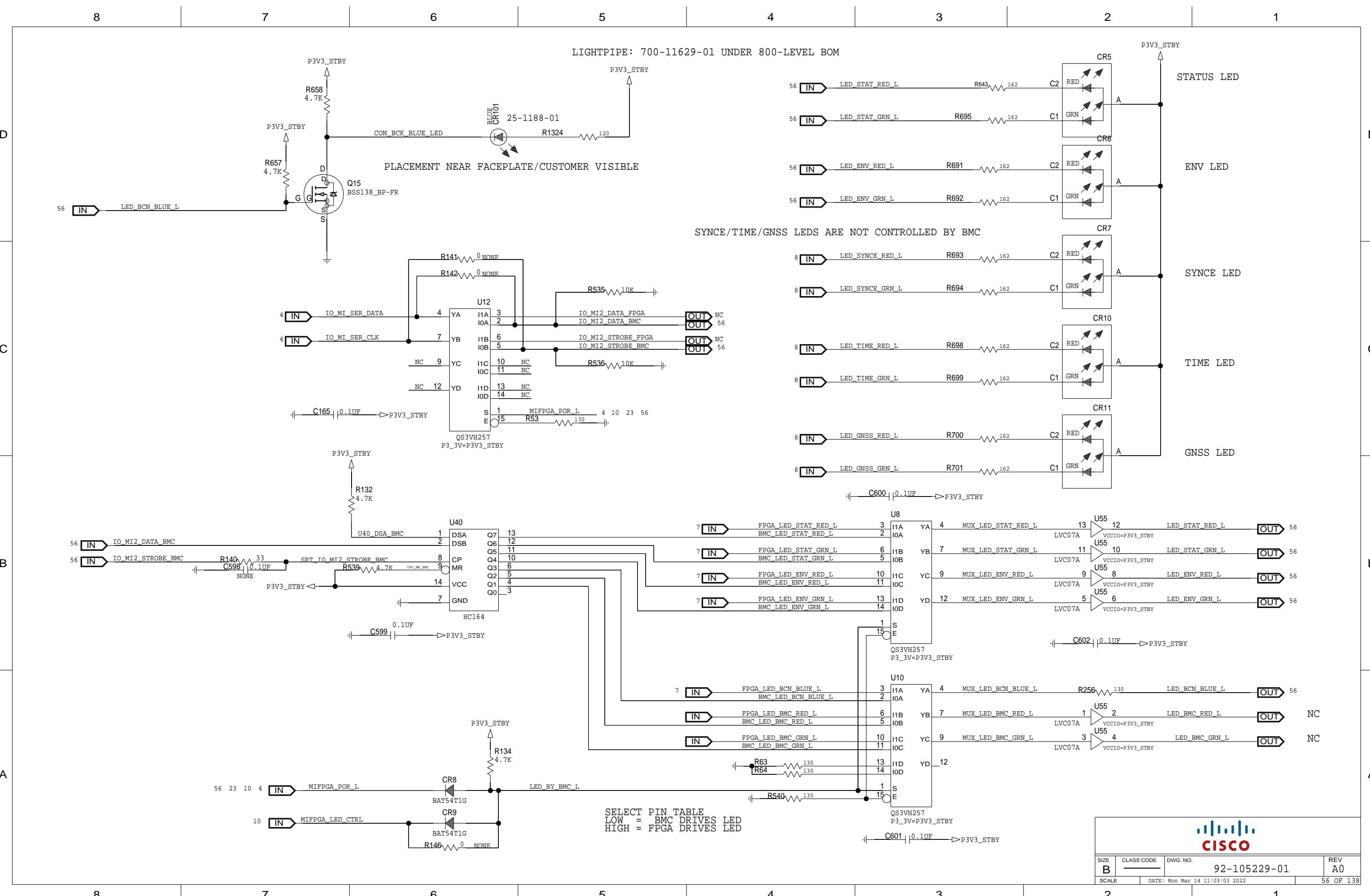


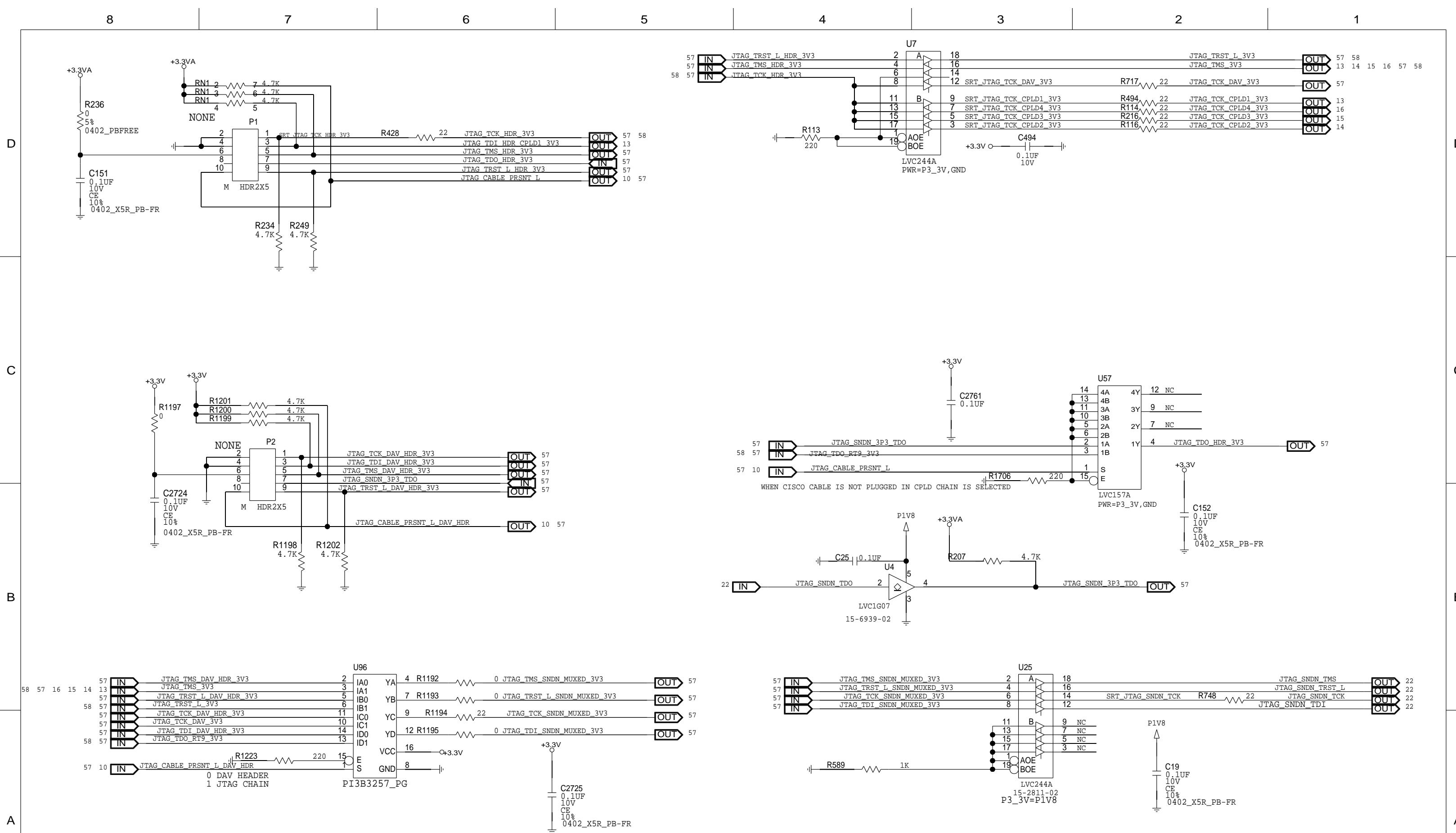
A

A

**CISCO**

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Mon Mar 14 11:03:03 2022		55 OF 138





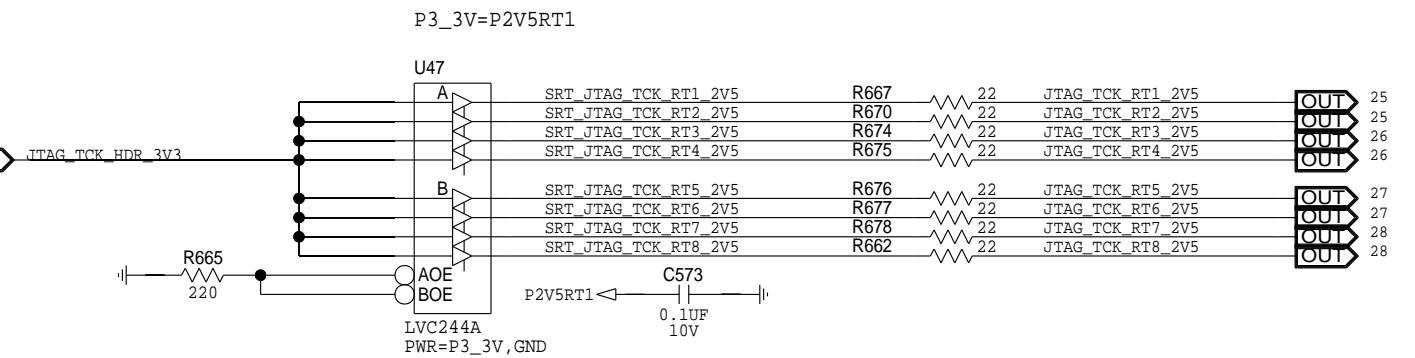
## JTAG HEADER\BUFFER



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Mon Mar 14 11:03:07 2022		57 OF 138

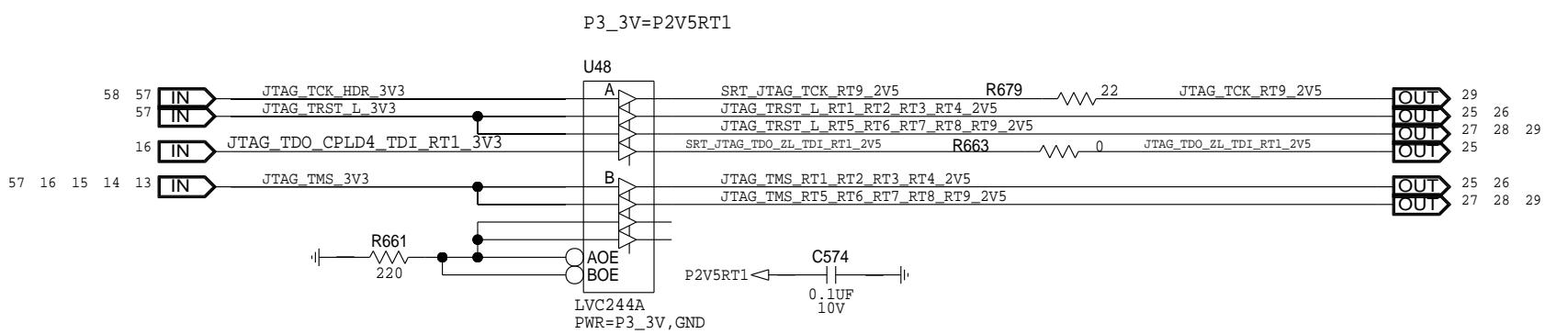
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D



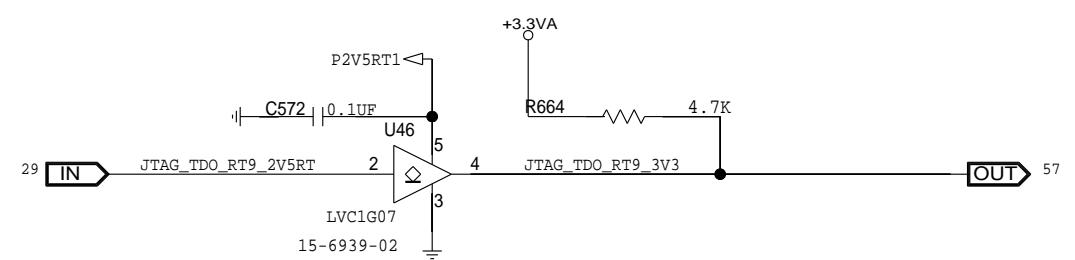
D

C



C

B



B

A

A

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

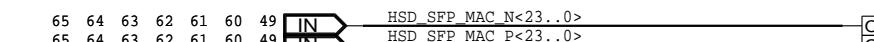
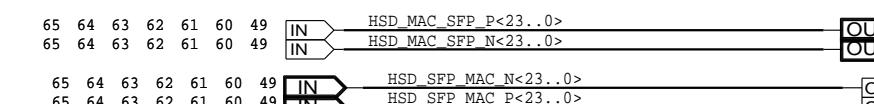
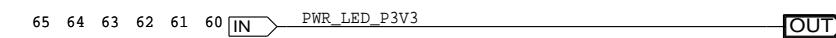
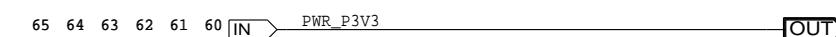
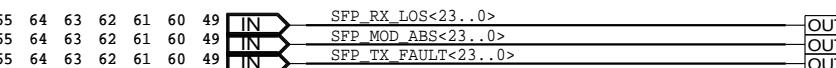
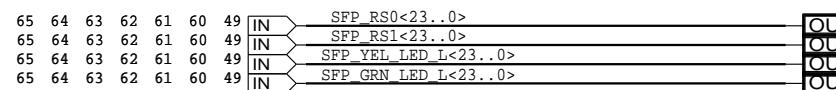
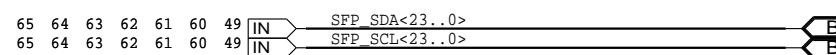
REVISION			APPROVALS		
REV	ECO	DESCRIPTION	DFTG	CHK	APVD

D

D

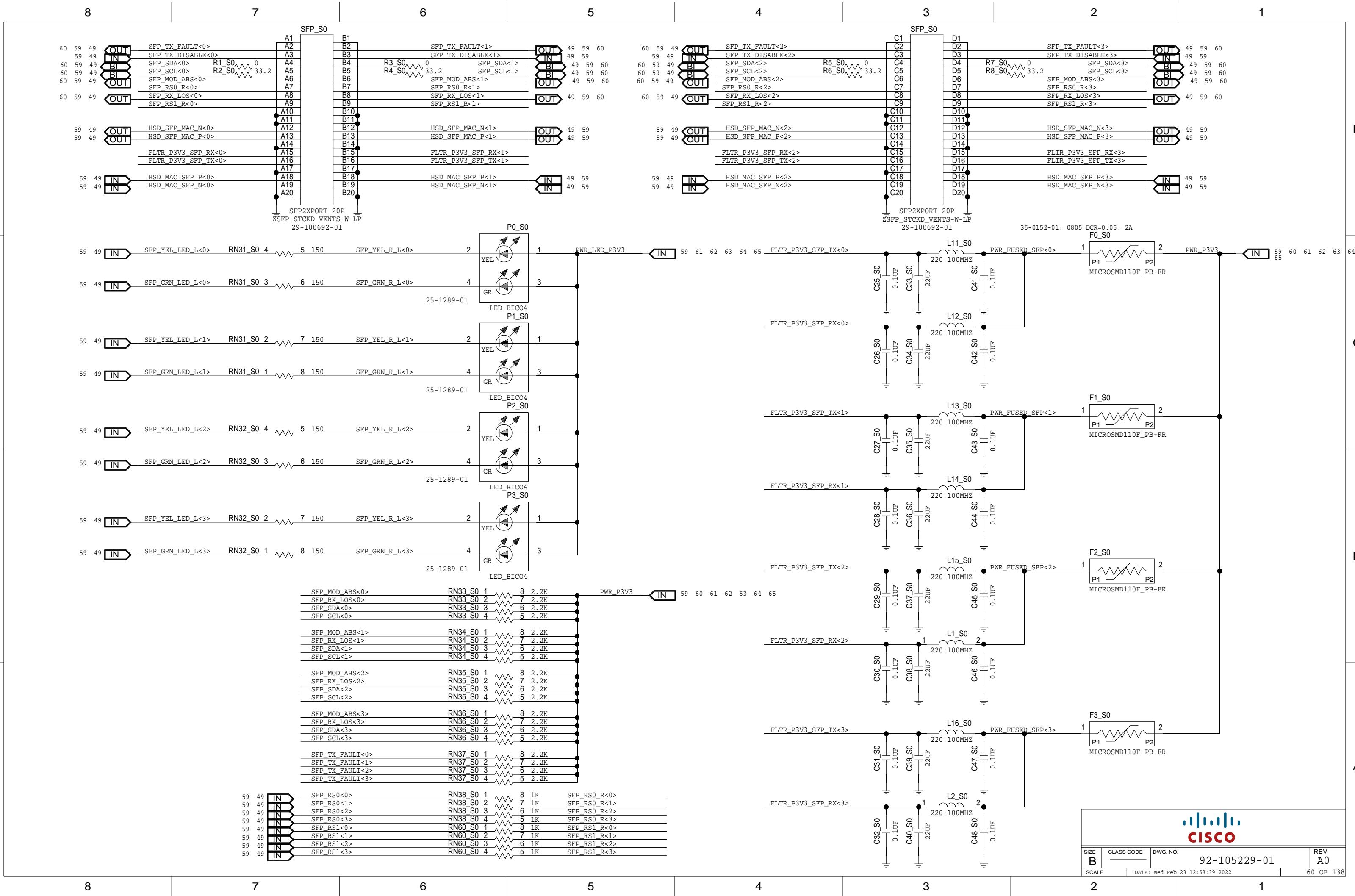
# 2X12 SFP W/O RE-TIMER SUBDESIGN 01

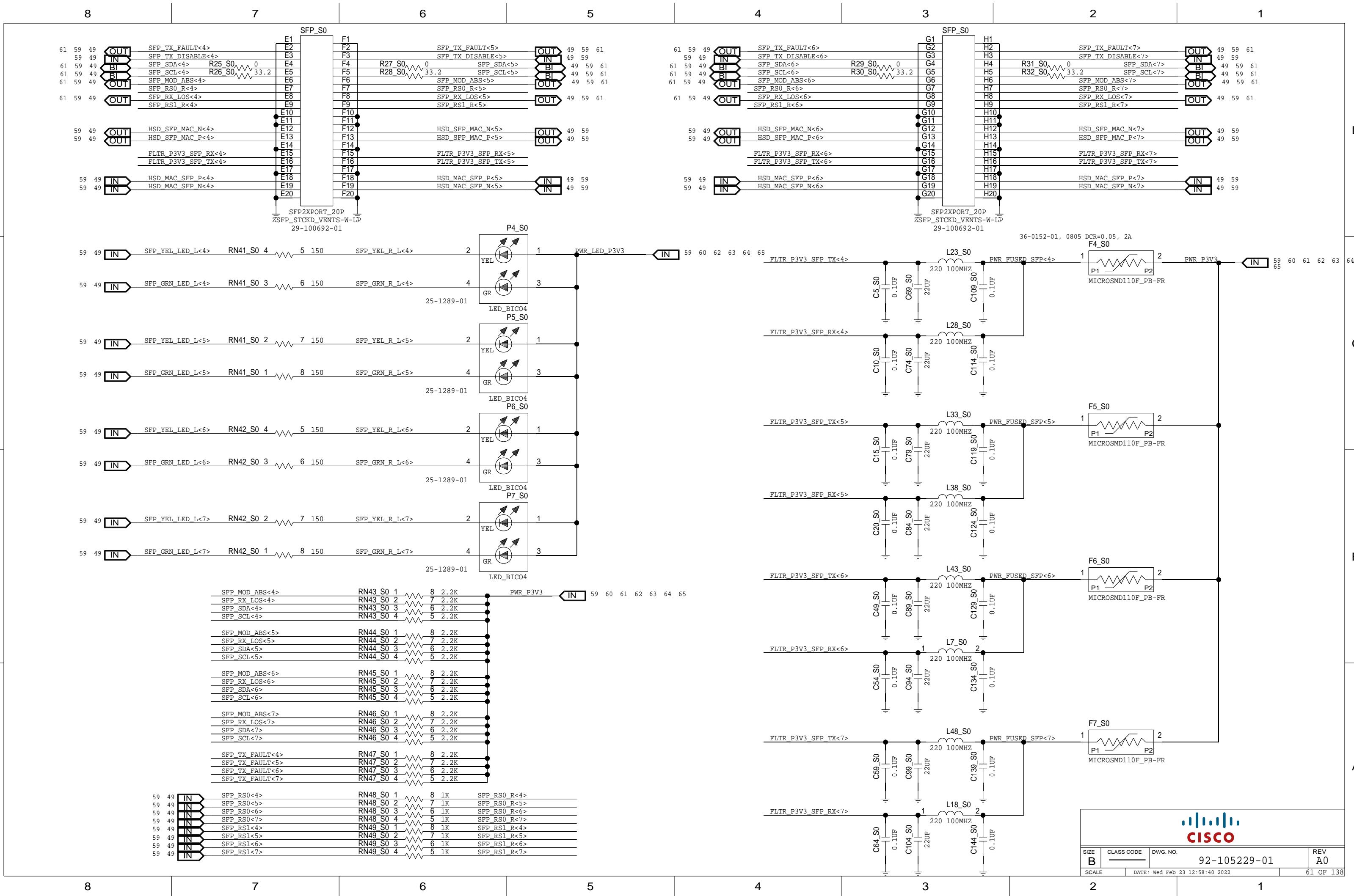
## CHANGE LOG:

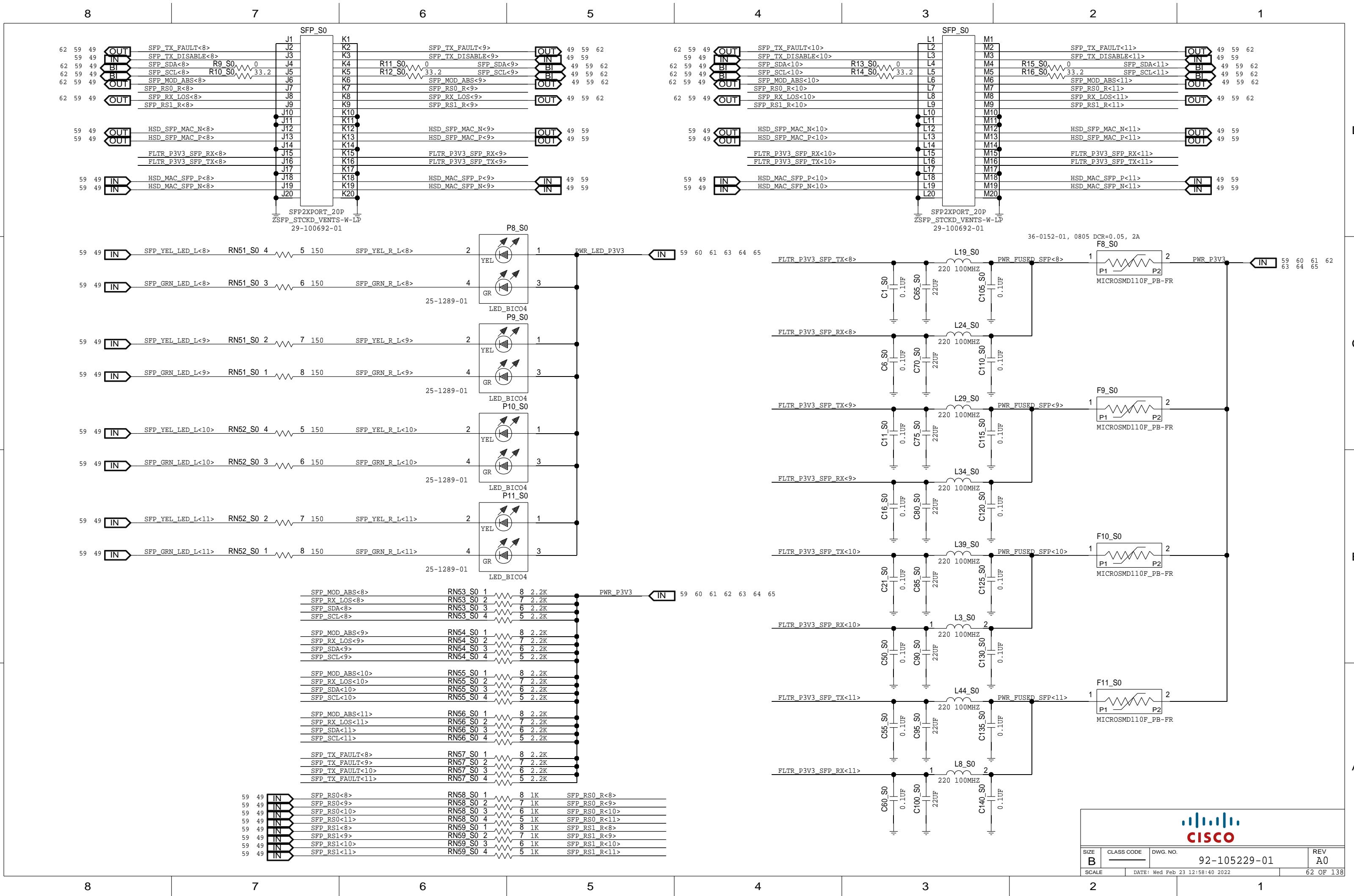


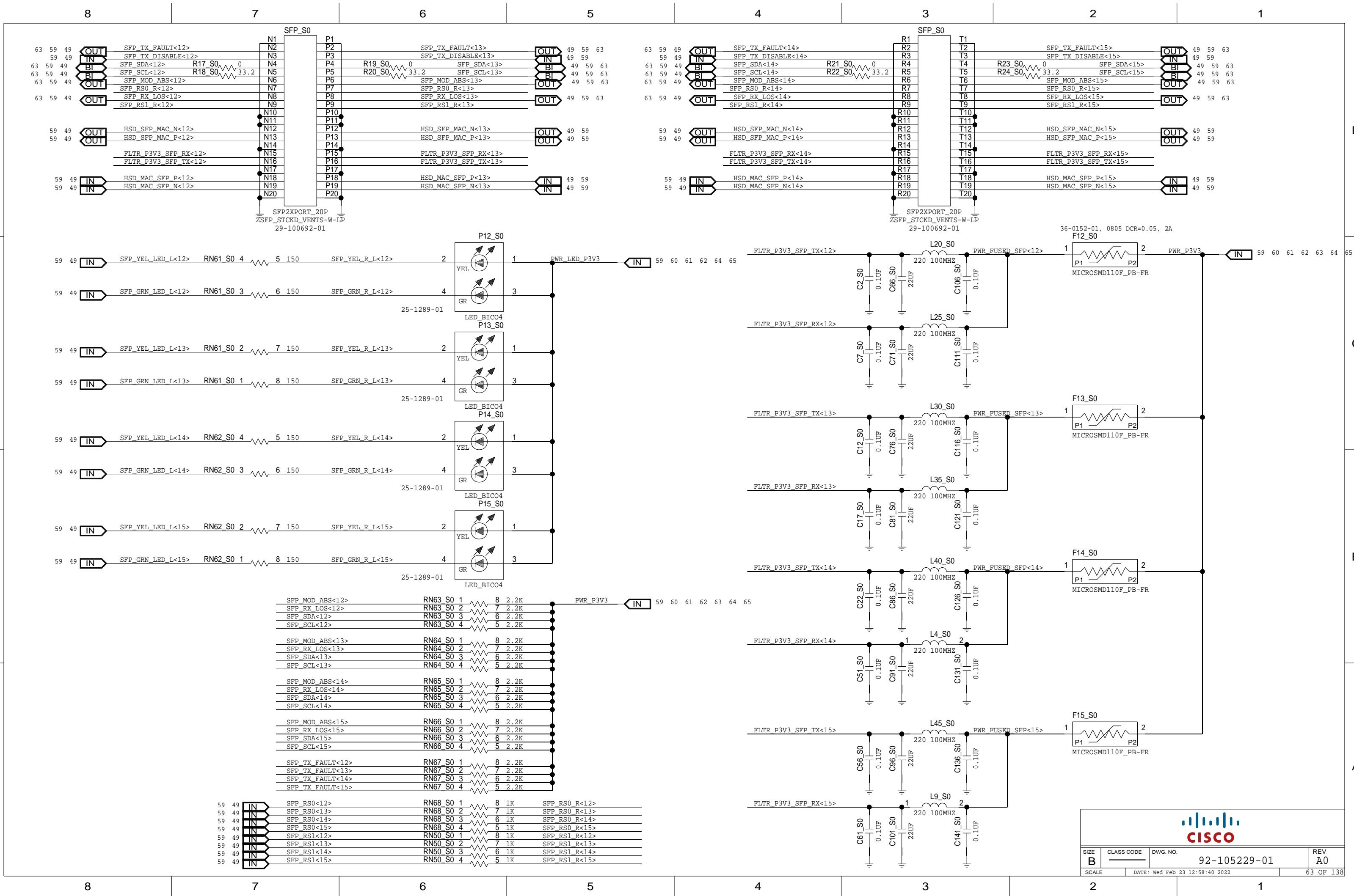
TITLE			NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION
QTY	REOD	PART OR IDENTIFYING NO.				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION .xx x.01 DECIM .xxx+.005	APPROVALS	DATE	DRAWN BY BCORDEIR			
‡ CAD						
MATERIAL	MECH		ENGR			
			BCORDEIR			
FINISH	MFG					
NEXT ASSY	USED ON	APPLICATION	DO NOT SCALE DWG	TEST		
SIZE B	CLASS CODE	DWG. NO. 92-XXXX-01	REV A0			
SCALE	DATE: Fri May 17 11:40:52 2019		59 OF 138			

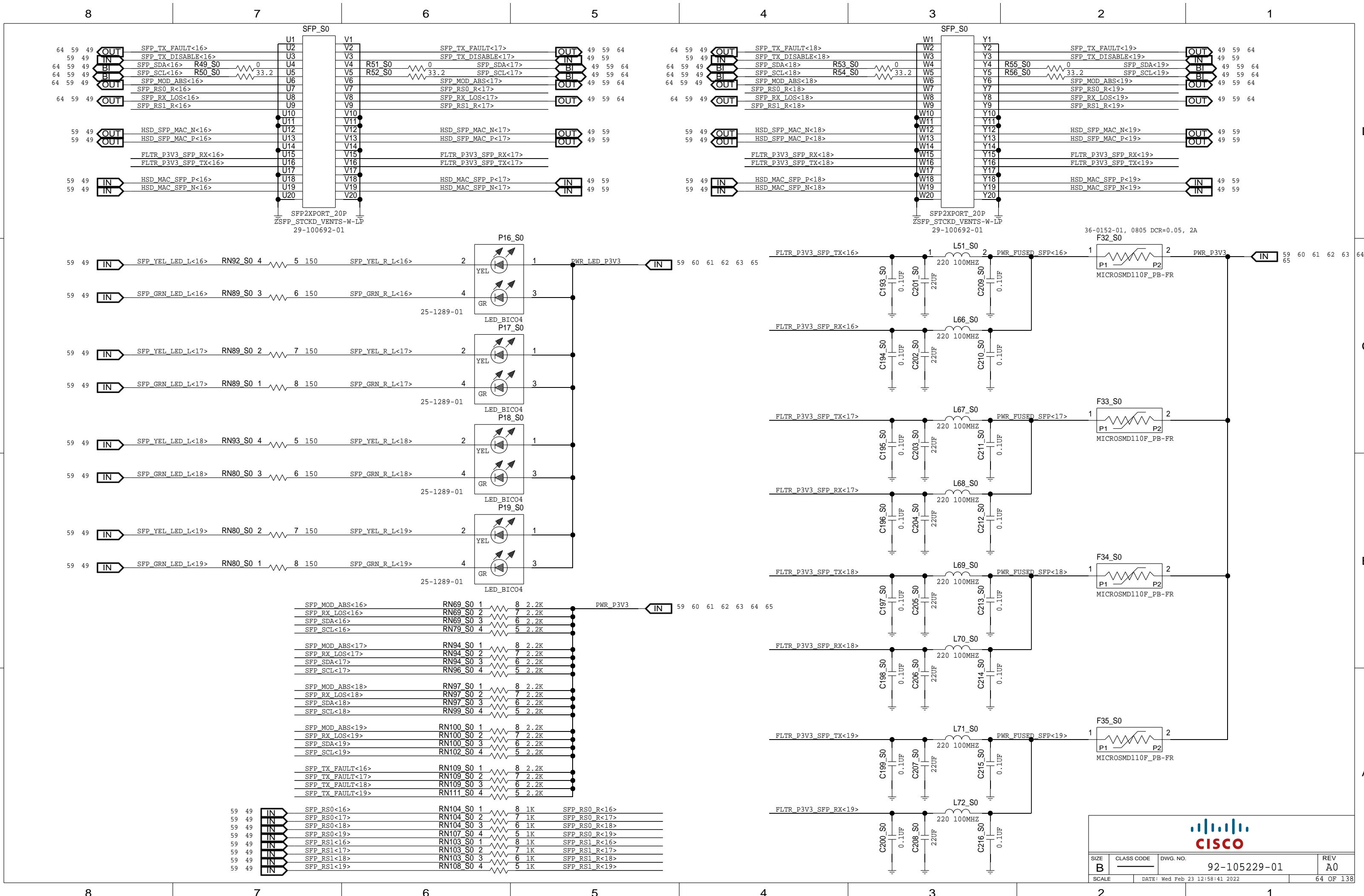


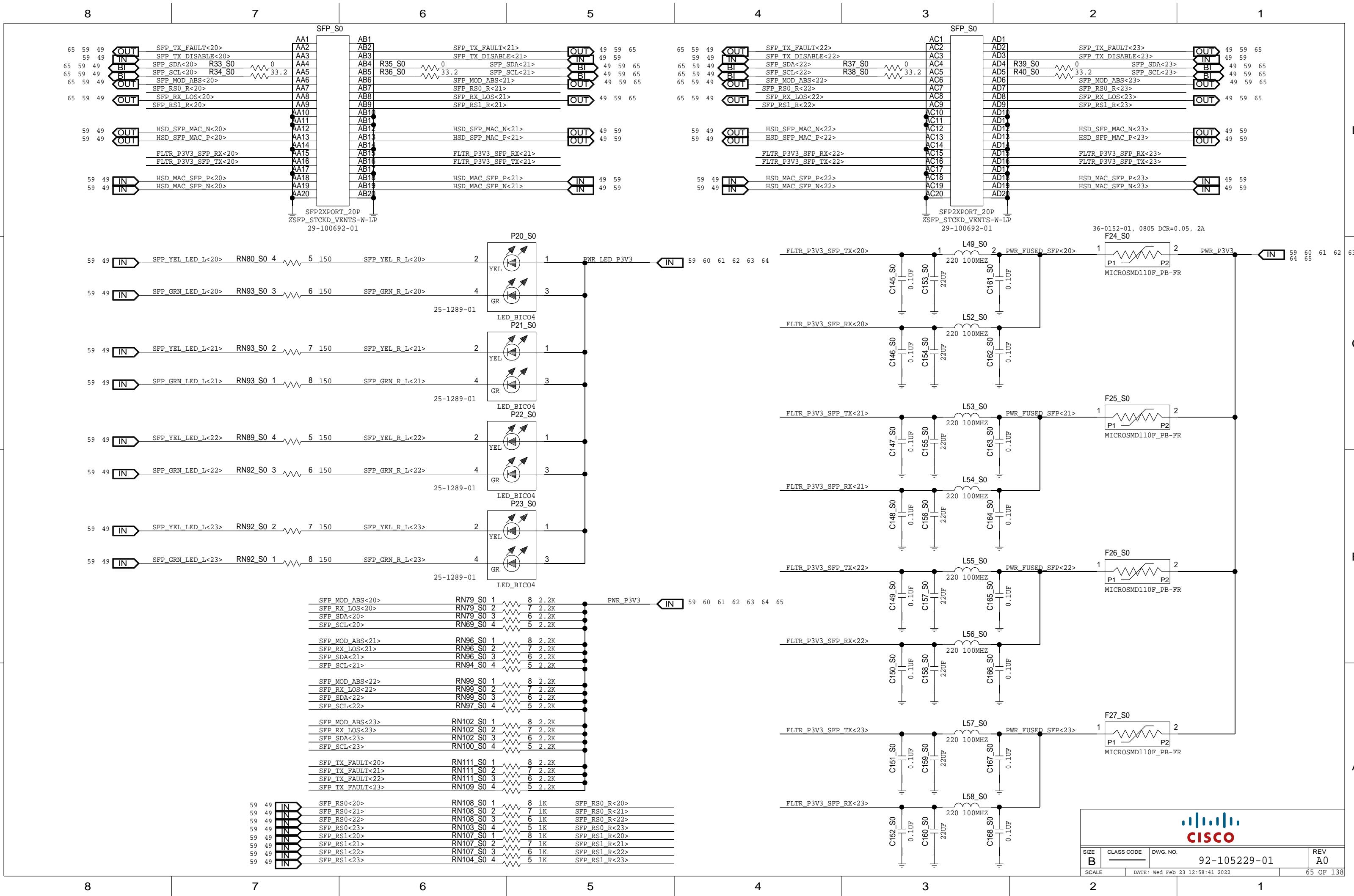










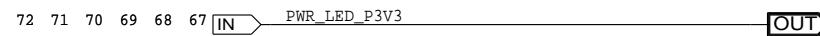
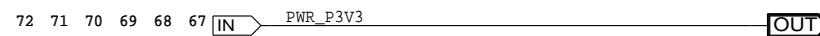
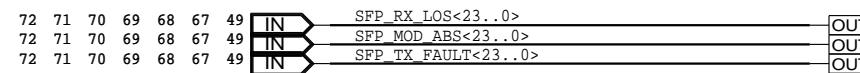
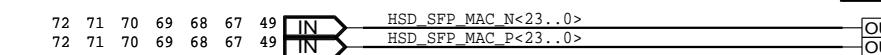
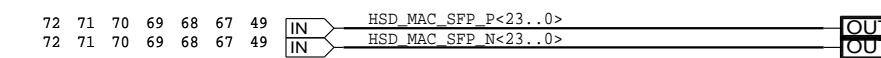
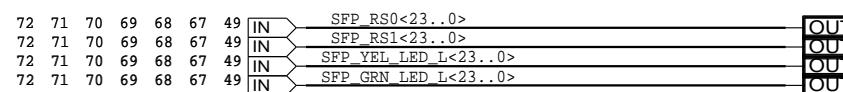
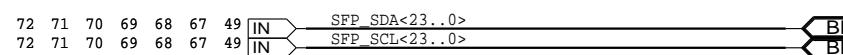


THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

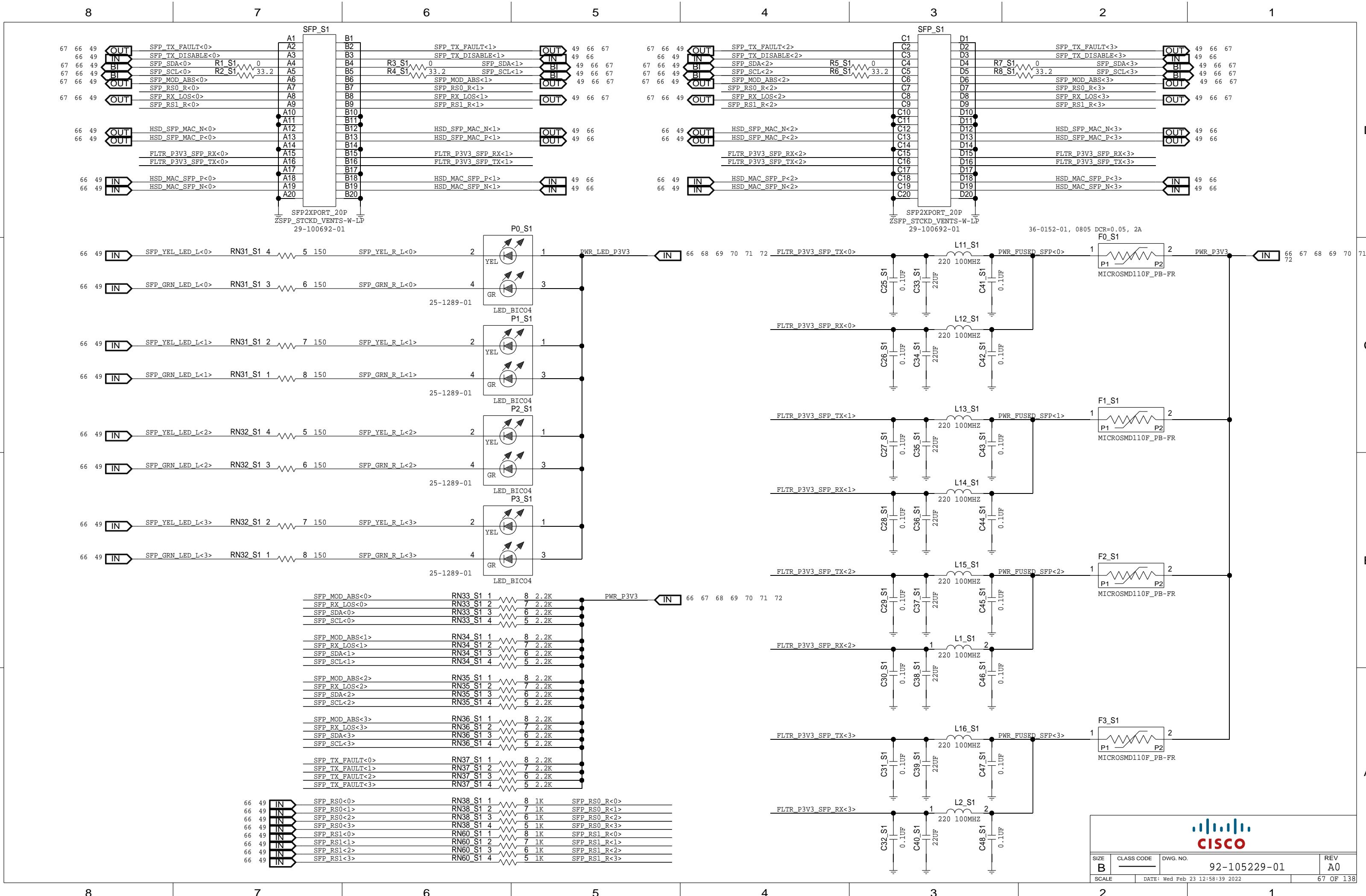
DWG NO	92-105229-01	SHT 138	REV A0	1
REVISION				
REV	ECO	DESCRIPTION	APPROVALS	
			DFTG	CHK
				APVD

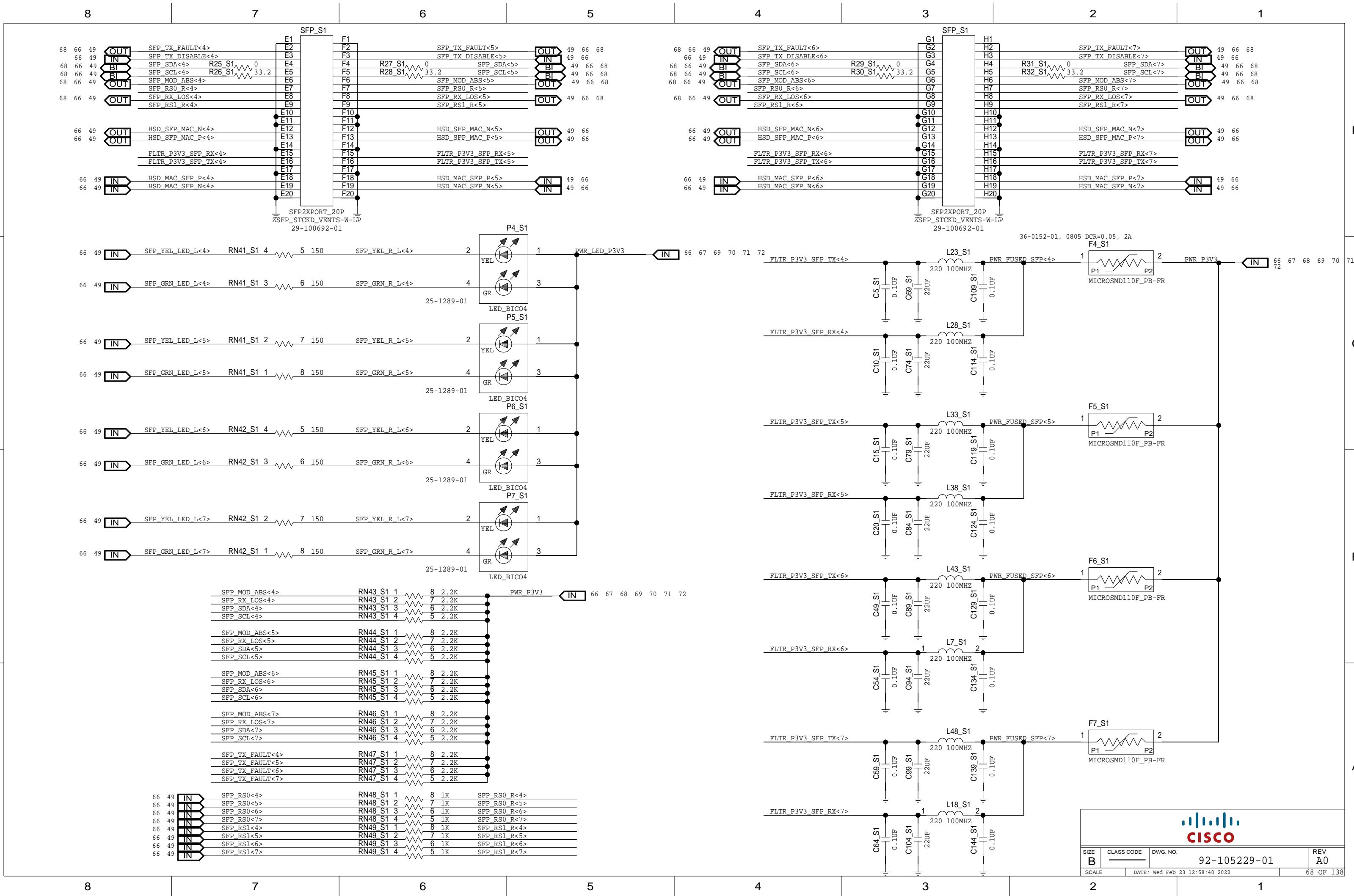
# 2X12 SFP W/O RE-TIMER SUBDESIGN 01

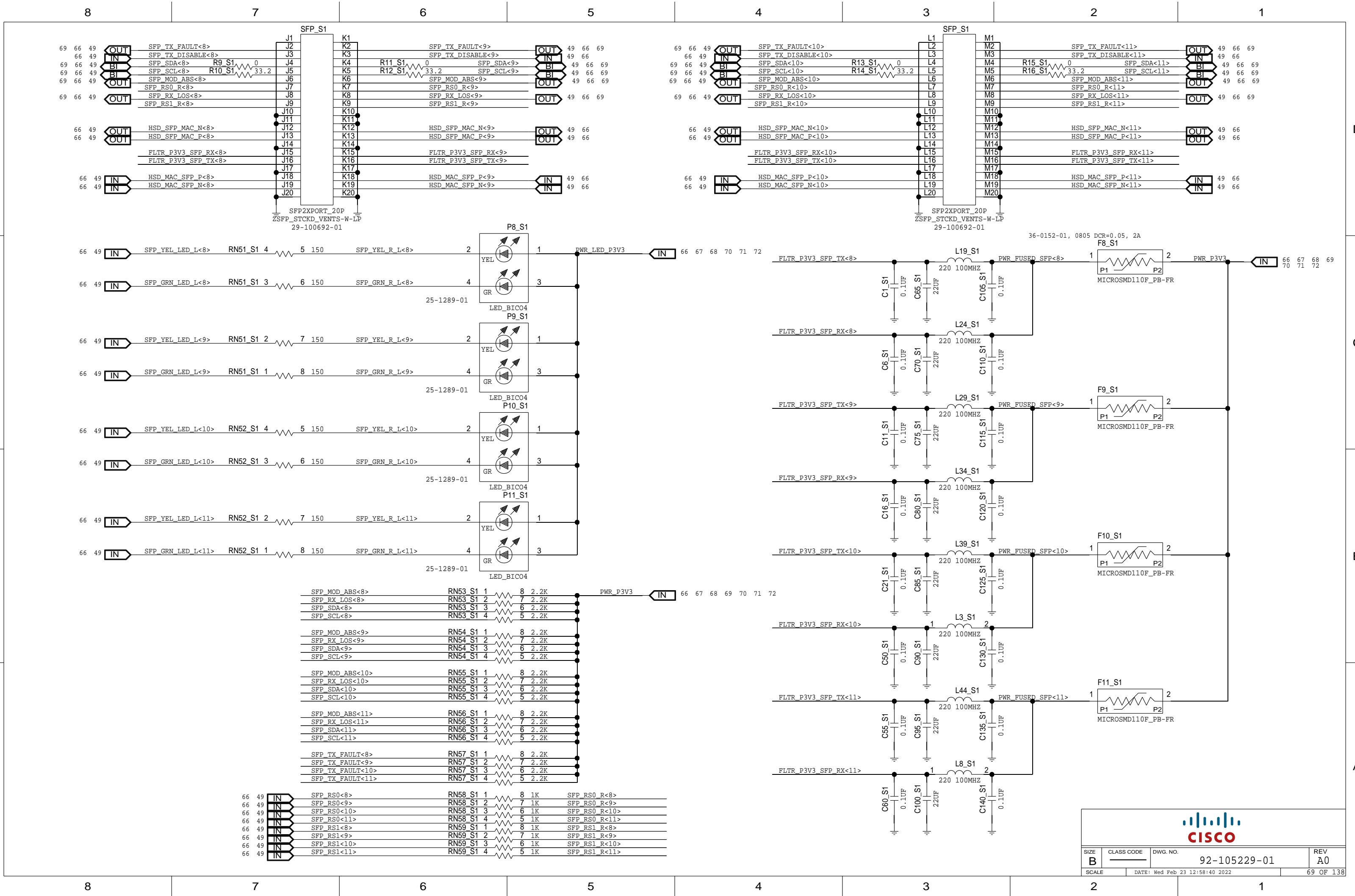
## CHANGE LOG

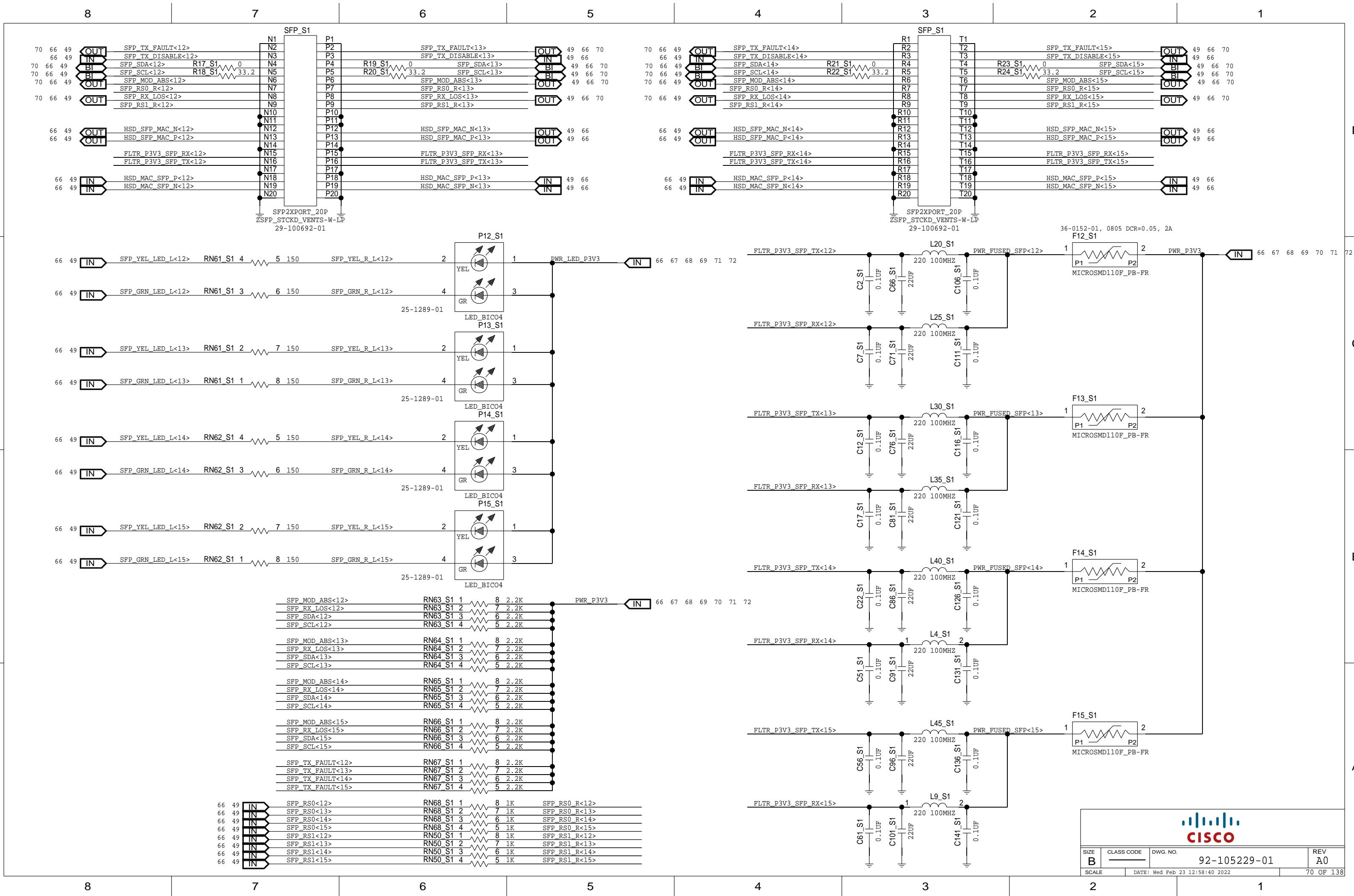


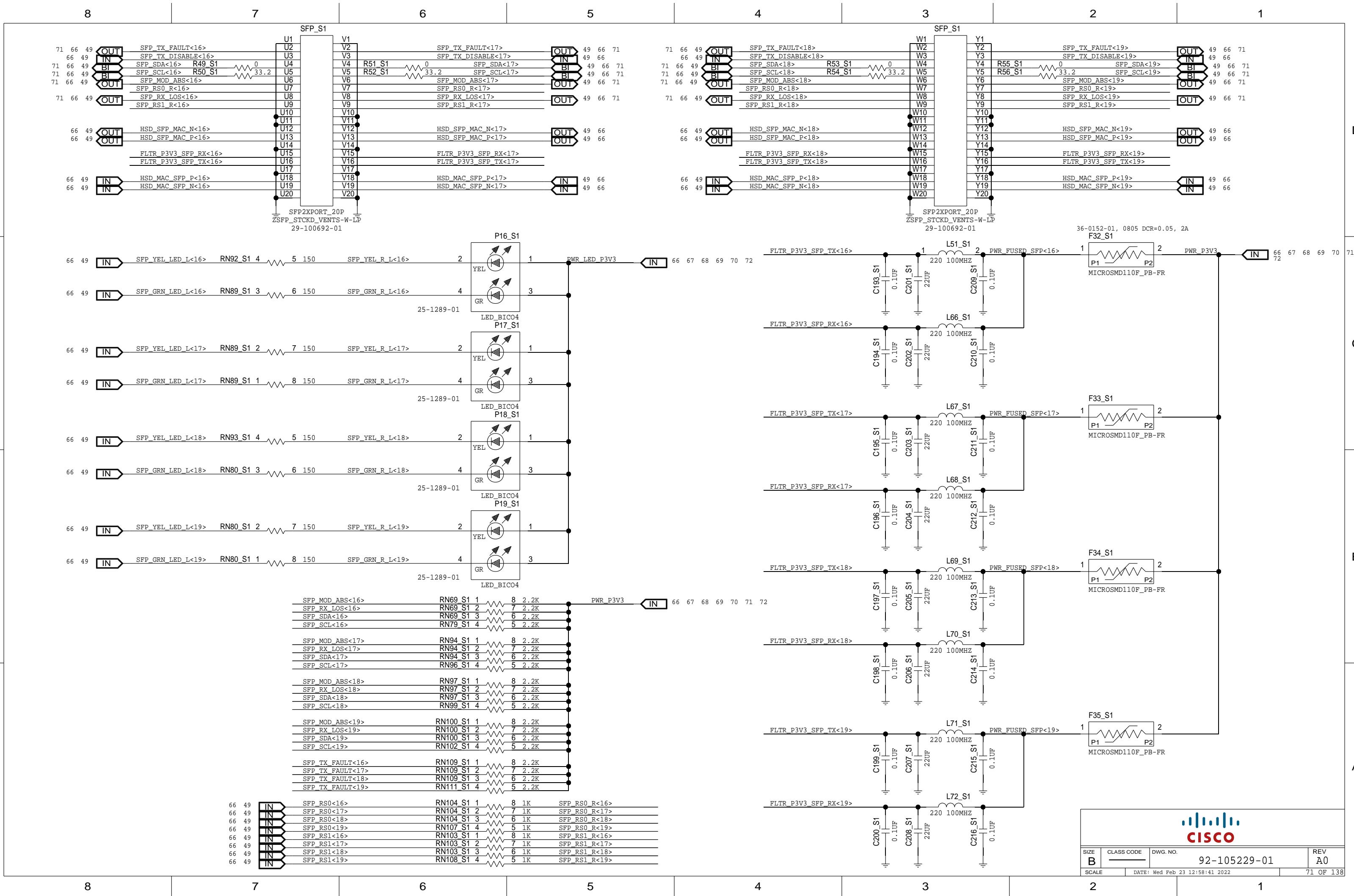
TITLE							
QTY REQD		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION	
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION    DECIM    ANGLES <del>xx +.01</del> <del>xxx+.005</del> <del>±1°</del> <del>CAD</del>		APPROVALS	DATE				
		DRAWN BY BCORDEIR					
		CAD					
MATERIAL		MECH		TITLE: SFP 2X12 W/O RETIMER			
		ENGR					
FINISH		BCORDEIR					
		MFG		SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-XXXX-01</b>	
DO NOT SCALE DWG		TEST		SCALE	DATE: Fri May 17 11:40:52 2019		66 OF 138

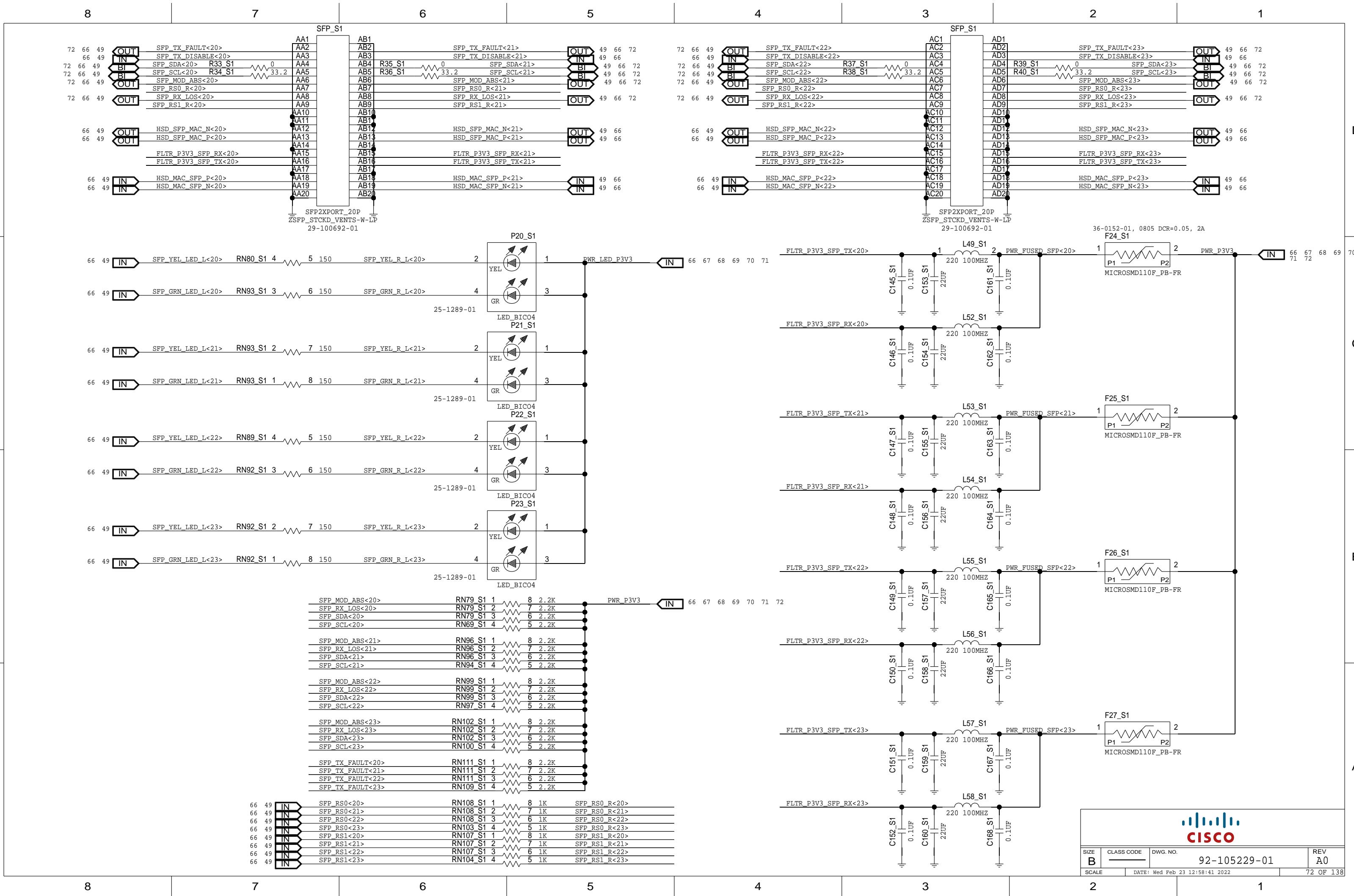












8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

# BEARVALLY SUBDESIGN REV05

## 2X BEARVALLY MODULE

### CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY

11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP

05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)  
REQUIRE CAD LAYOUT CHANGE

TITLE		
 <b>CISCO</b>		
SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>
SCALE	DATE: Mon Dec 21 20:28:30 2020	REV <b>A0</b>
		73 OF 138

8

7

6

5

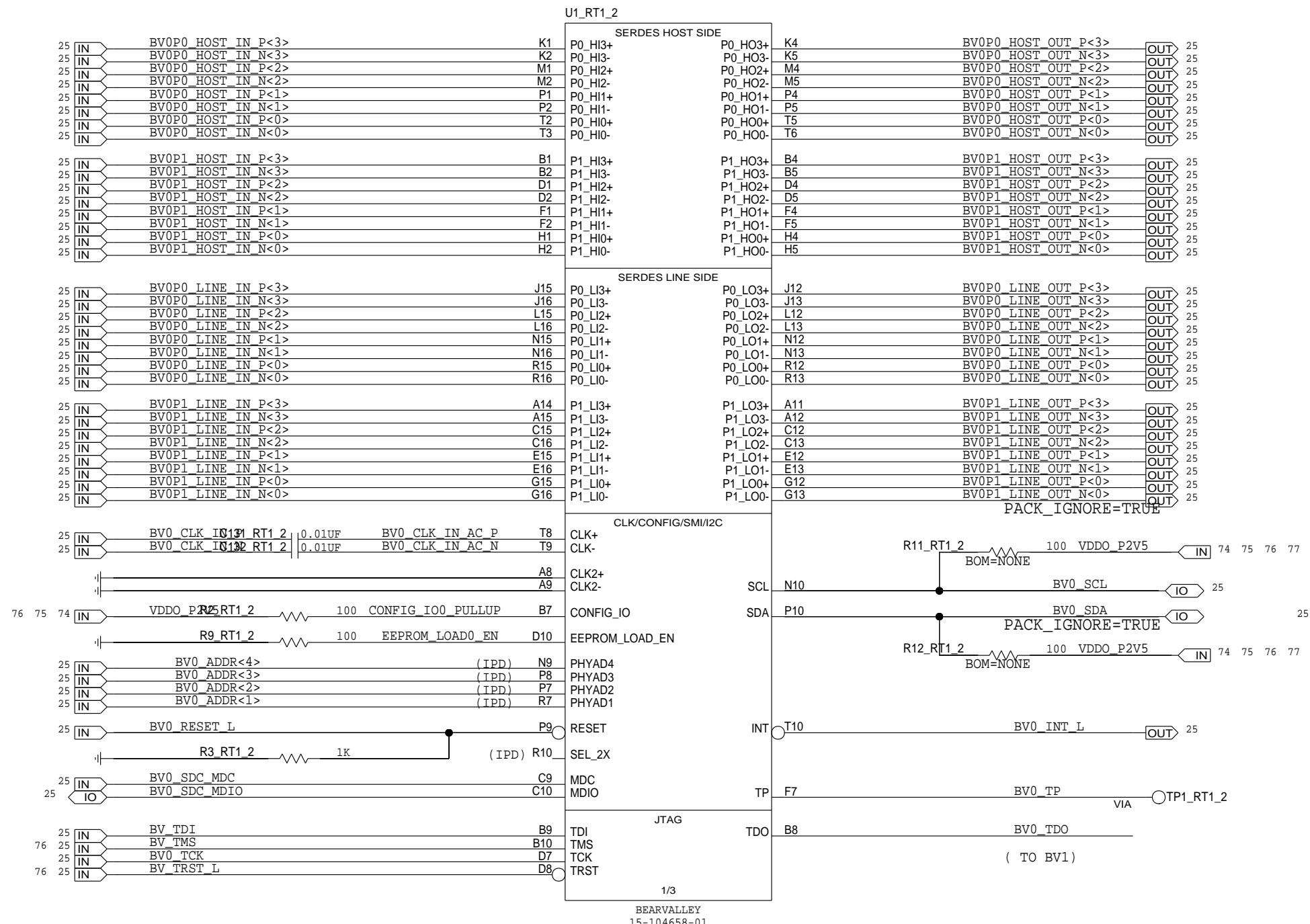
4

3

2

1

ADDCOMP=700-26993-01



BEARVALLEY-1



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Nov 4 15:26:15 2021		74 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

D

D

C

C

B

B

A

A

75

36-0212-01

L3\_RT1\_2

10A, 0.004OHM, 1612

C60\_RT1\_2

4V

C145\_RT1\_2

22UF

C61\_RT1\_2

6.3V

C41\_RT1\_2

22UF

C47\_RT1\_2

1UF

C19\_RT1\_2

1UF

C38\_RT1\_2

1UF

C50\_RT1\_2

1UF

C23\_RT1\_2

1UF

C62\_RT1\_2

1UF

C33\_RT1\_2

1UF

C64\_RT1\_2

1UF

C65\_RT1\_2

1UF

C134\_RT1\_2

1UF

C136\_RT1\_2

1UF

C138\_RT1\_2

1UF

0.1UF

FLTR\_BV0

AVDDH

2.05A (TYP DFE ON)

36-0212-01

L5\_RT1\_2

10A, 0.004OHM, 1612

C25\_RT1\_2

4V

C27\_RT1\_2

22UF

C8\_RT1\_2

1UF

C15\_RT1\_2

1UF

C21\_RT1\_2

1UF

C24\_RT1\_2

1UF

C13\_RT1\_2

1UF

C28\_RT1\_2

1UF

C30\_RT1\_2

1UF

C31\_RT1\_2

1UF

C38\_RT1\_2

1UF

C133\_RT1\_2

1UF

C28\_RT1\_2

1UF

C30\_RT1\_2

1UF

C135\_RT1\_2

1UF

C137\_RT1\_2

1UF

0.1UF

FLTR\_BV0

AVDDL

2.05A (TYP DFE ON)

BEARVALLEY  
15-104658-01

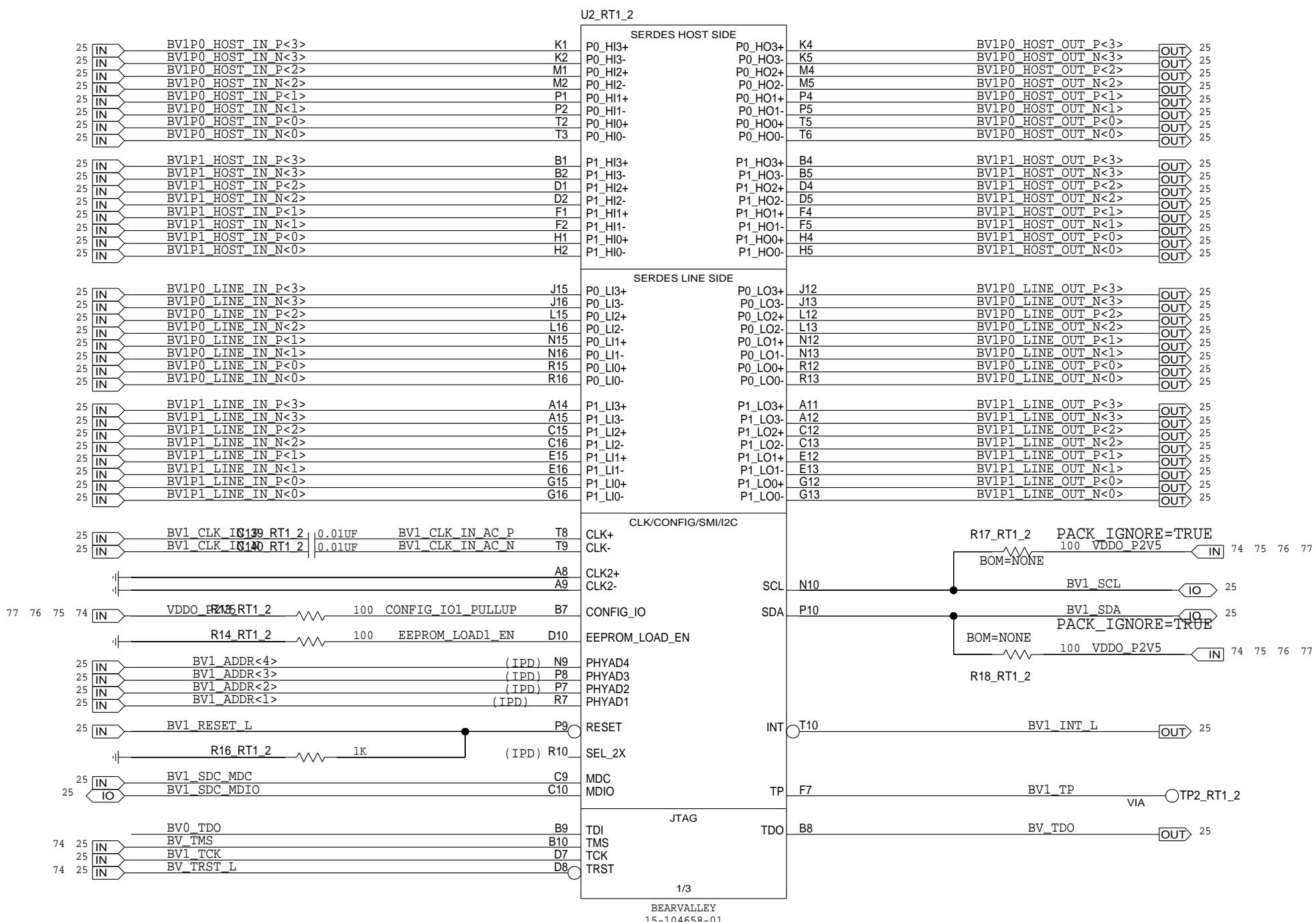
2/3

BEARVALLEY  
15-104658-01

3/3

BEARVALLEY  
15-104658-01

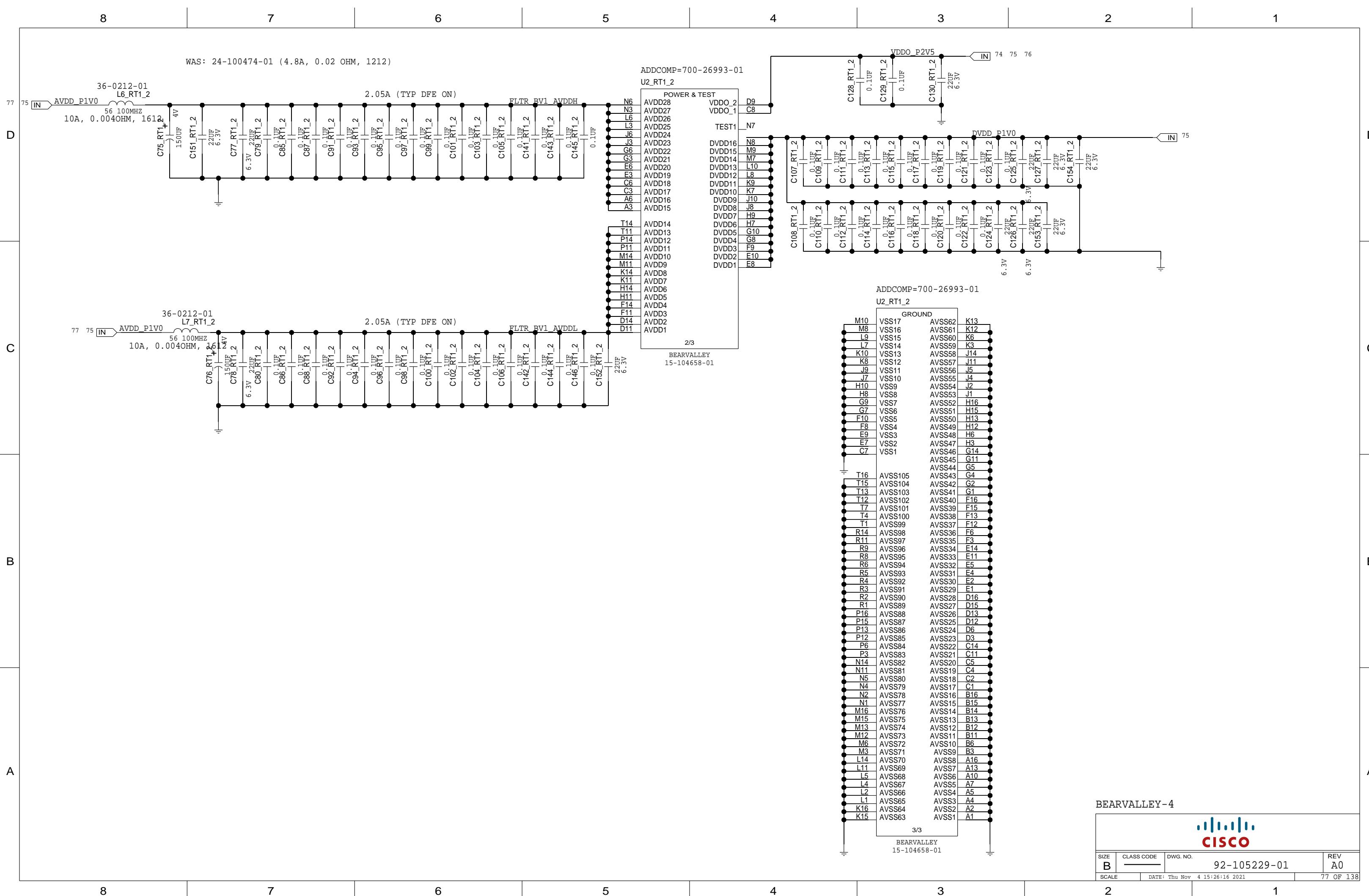
ADDCOMP=700-26993-01



BEARVALLEY-3



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:16 2021	76 OF 138



8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

# BEARVALLY SUBDESIGN REV05

## 2X BEARVALLY MODULE

### CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY

11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP

05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)  
REQUIRE CAD LAYOUT CHANGE

TITLE		
 <b>CISCO</b>		
SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>
SCALE	DATE: Mon Dec 21 20:28:30 2020	REV <b>A0</b>
		78 OF 138

8

7

6

5

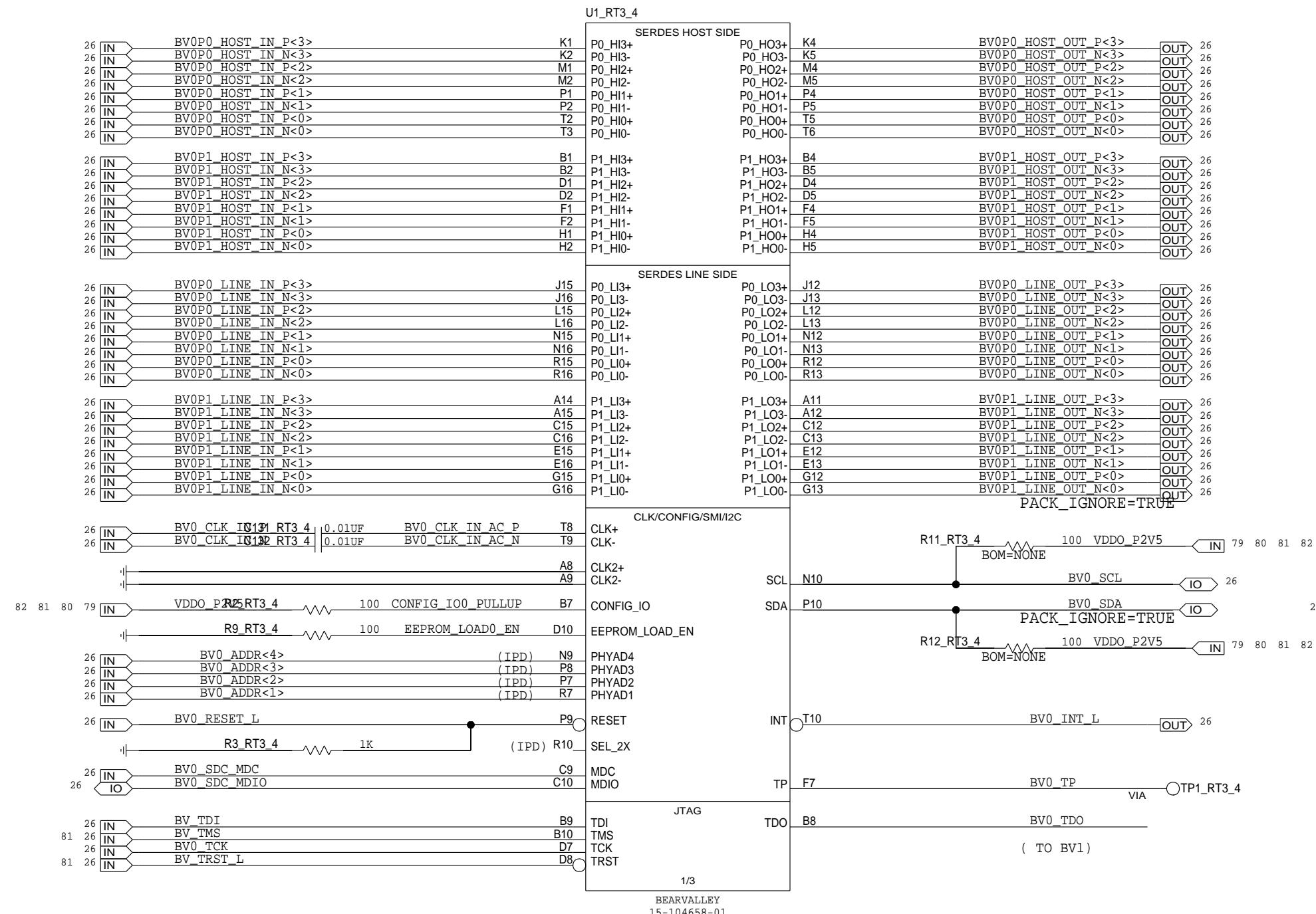
4

3

2

1

ADDCOMP=700-26993-01



BEARVALLEY  
15-104658-01

15-104658-01

BEARVALLEY-1



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Nov 4 15:26:15 2021		79 OF 138

8

7

6

5

4

3

2

1

D

D

C

C

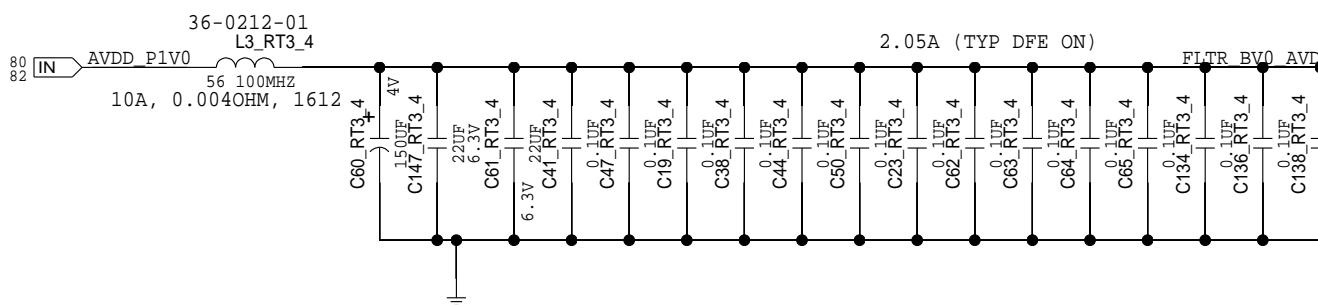
B

B

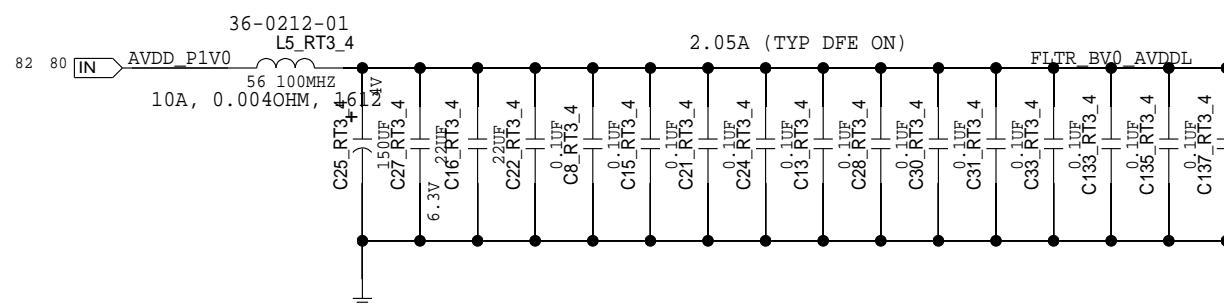
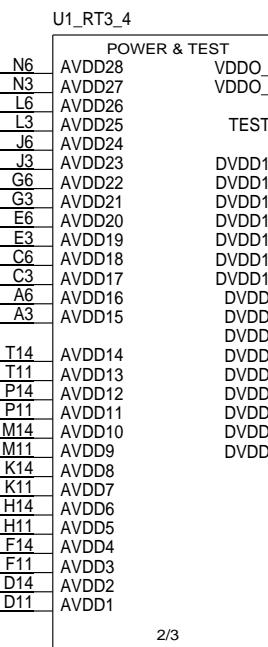
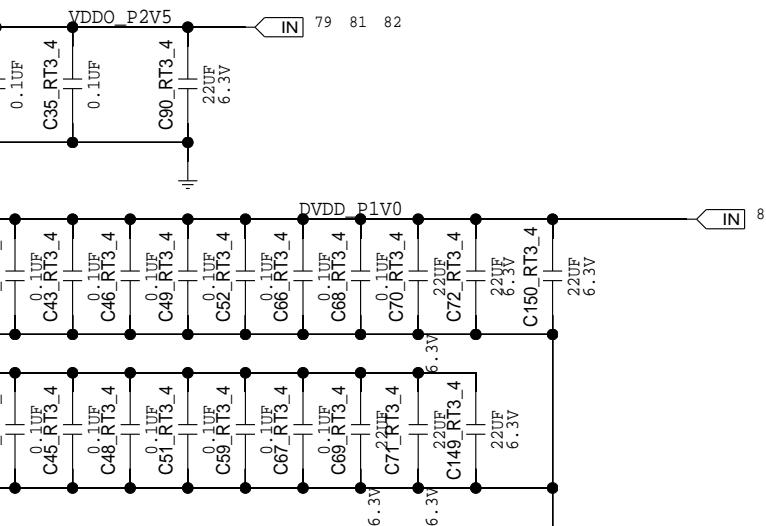
A

A

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)



ADDCOMP=700-26993-01

BEARVALLEY  
15-104658-01

ADDCOMP=700-26993-01

U1\_RT3\_4

GROUND

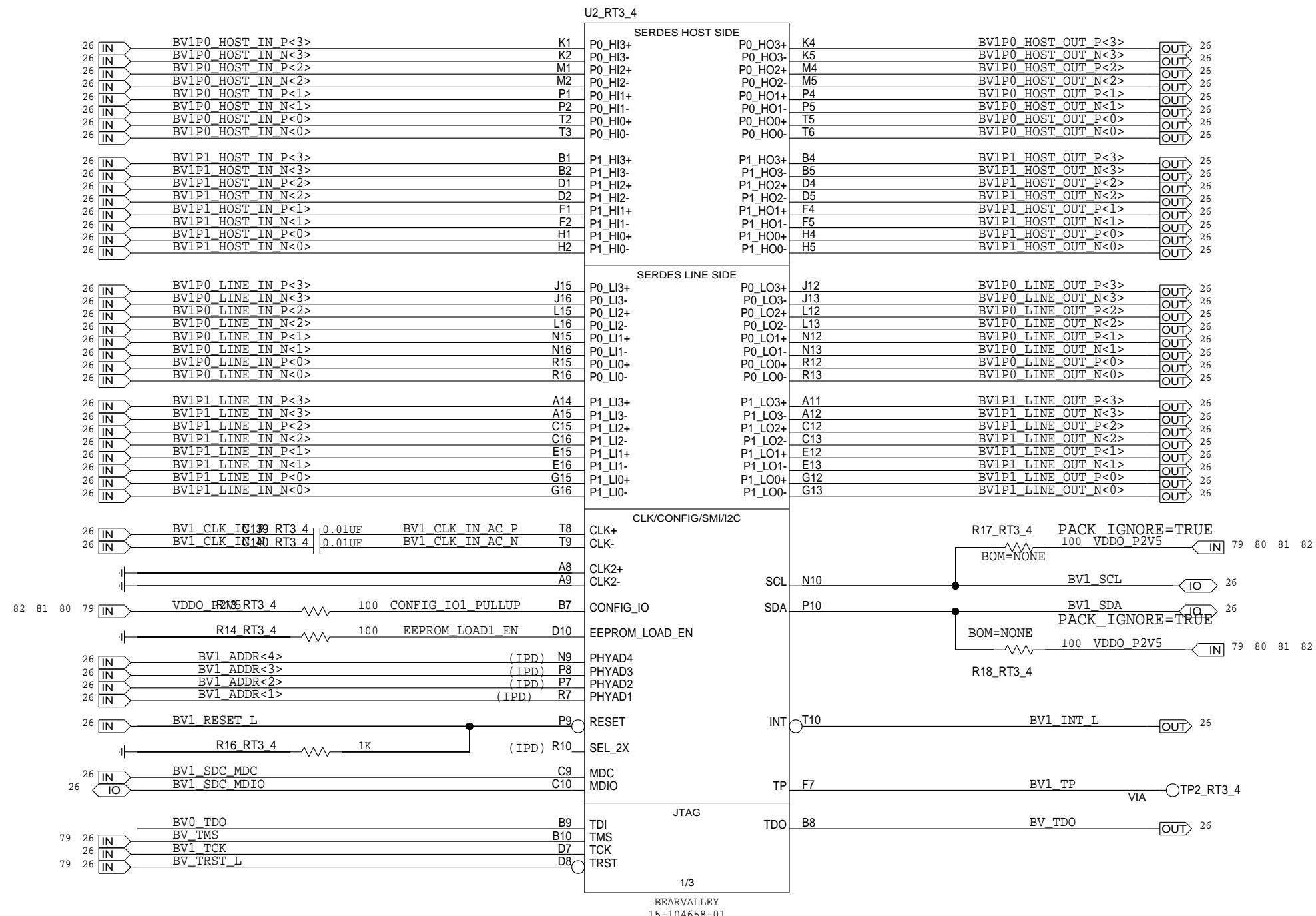
2/3

BEARVALLEY  
15-104658-01

3/3

BEARVALLEY  
15-104658-01

ADDCOMP=700-26993-01



BEARVALLE  
15-104658-

BEARVALLEY-3



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Nov 4 15:26:16 2021		81 OF 138

8

7

6

5

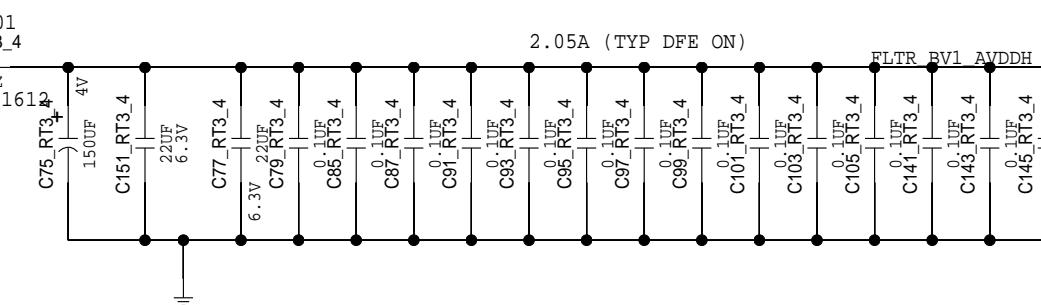
4

3

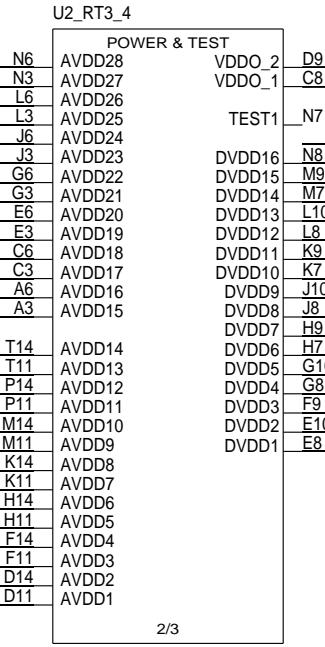
2

1

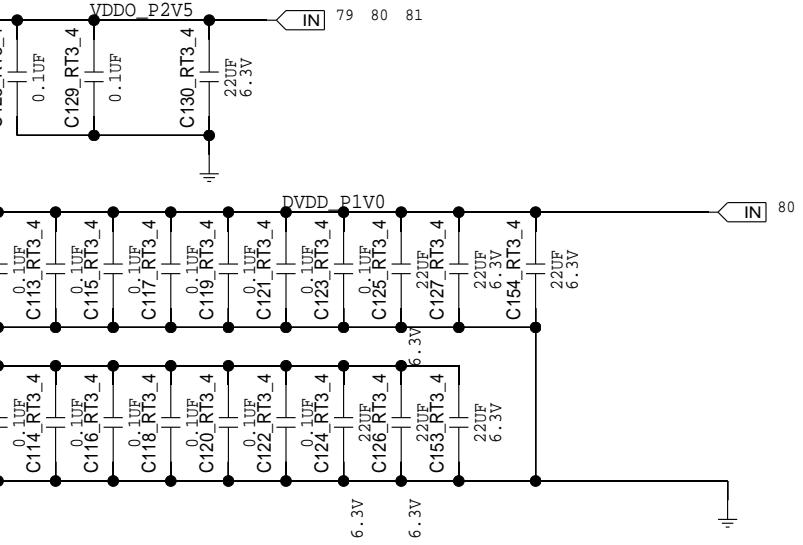
WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)



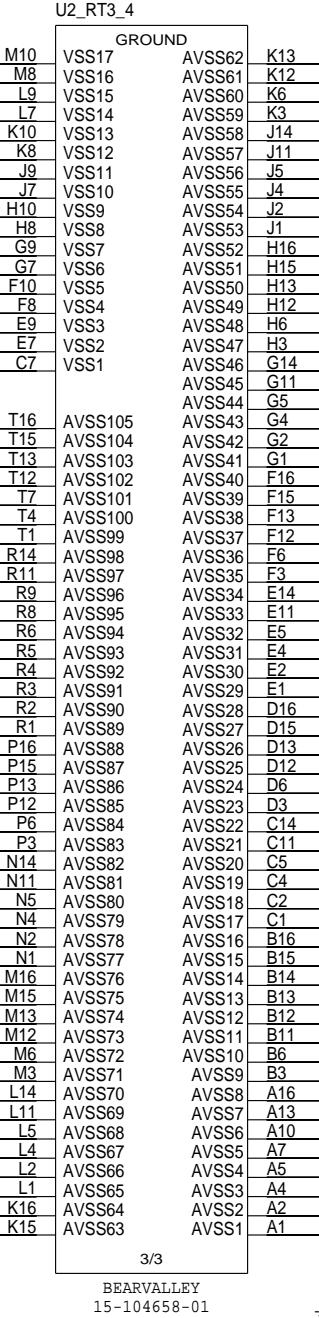
ADDCOMP=700-26993-01



2/3



ADDCOMP=700-26993-01



3/3

BEARVALLEY-4



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Thu Nov 4 15:26:16 2021	REV A0

1

82 OF 138

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

# BEARVALLY SUBDESIGN REV05

## 2X BEARVALLY MODULE

### CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY

11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP

05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)  
REQUIRE CAD LAYOUT CHANGE

TITLE		
 <b>CISCO</b>		
SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>
SCALE	DATE: Mon Dec 21 20:28:30 2020	REV <b>A0</b>
		83 OF 138

8

7

6

5

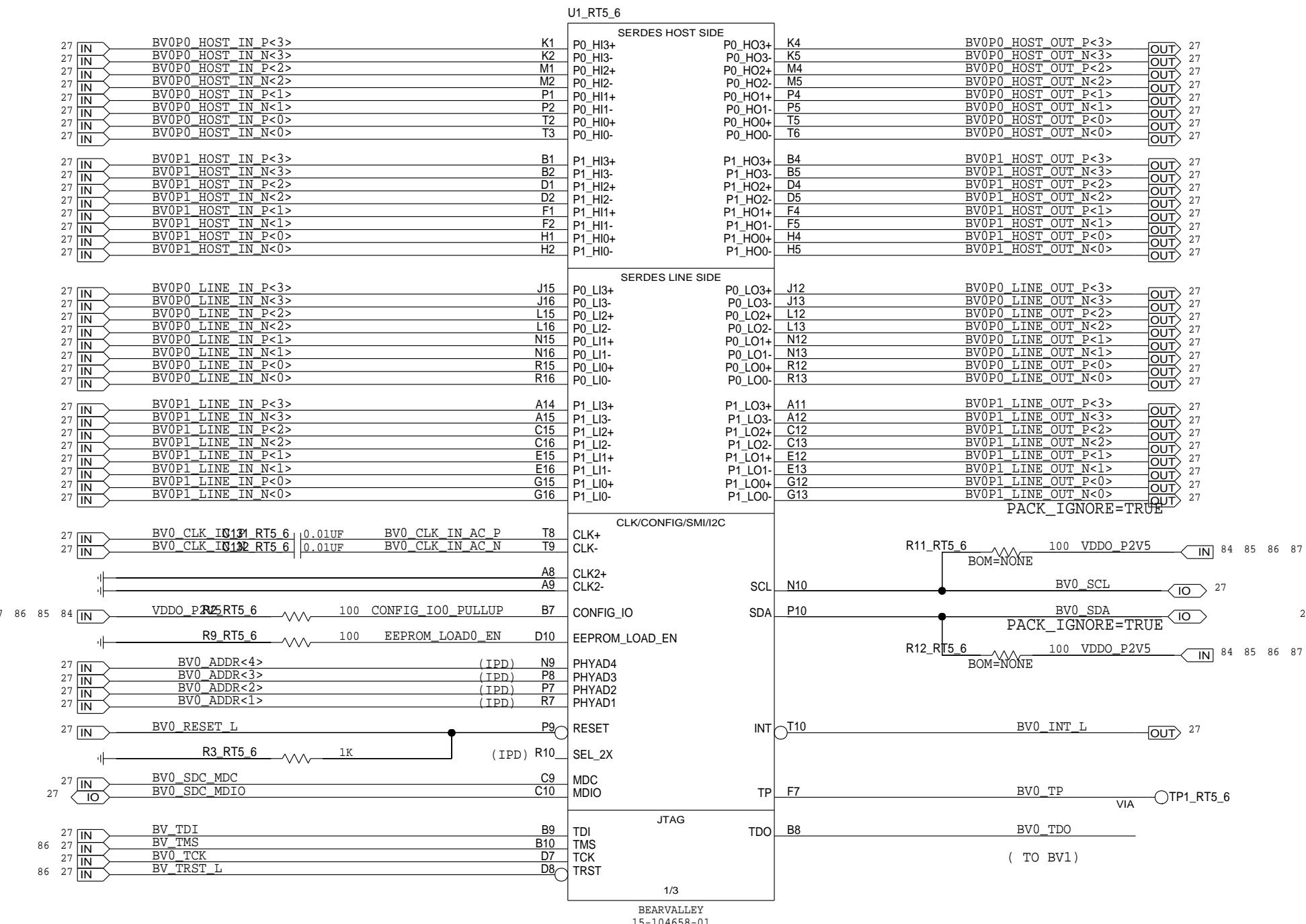
4

3

2

1

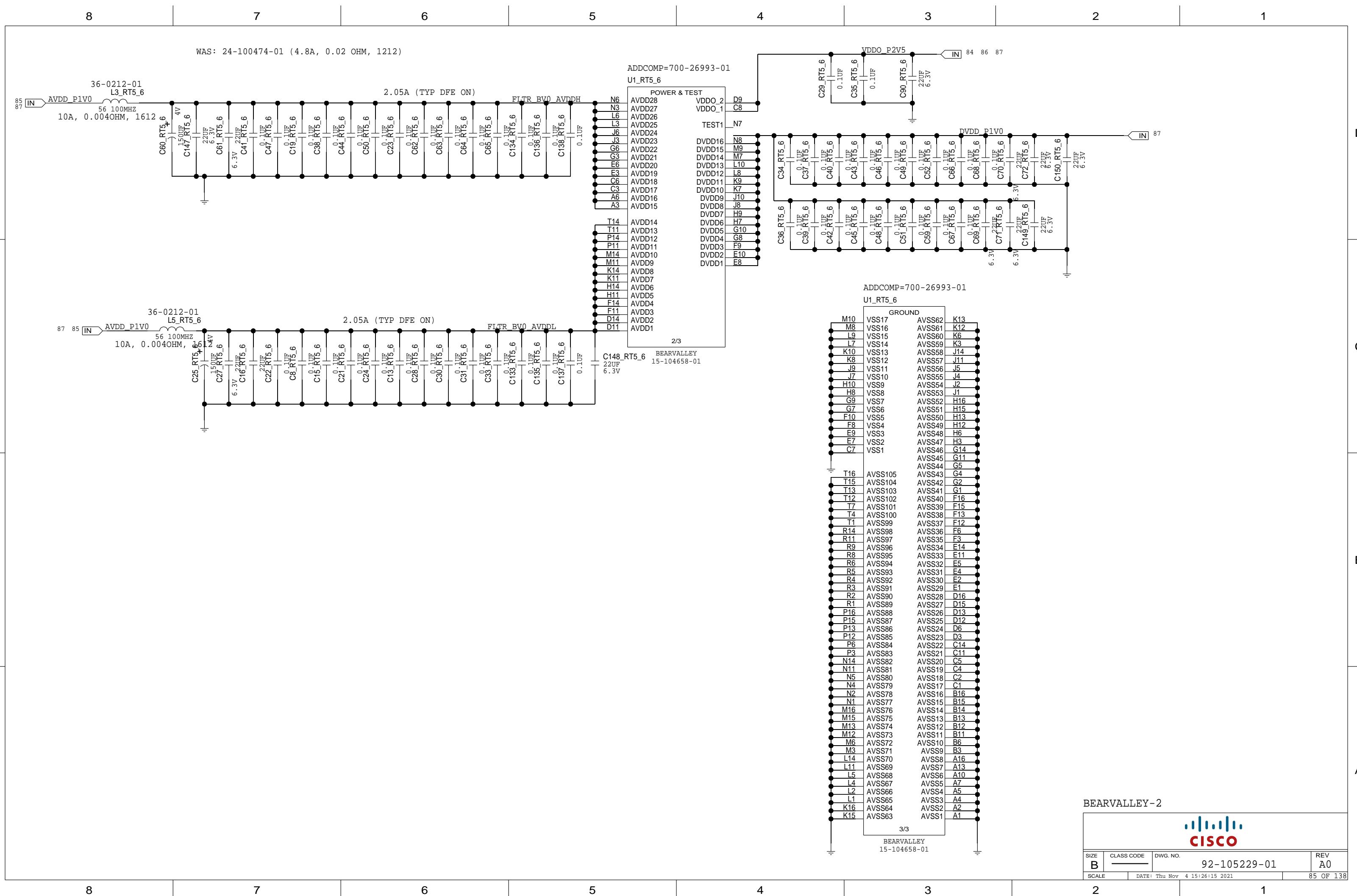
ADDCOMP=700-26993-01



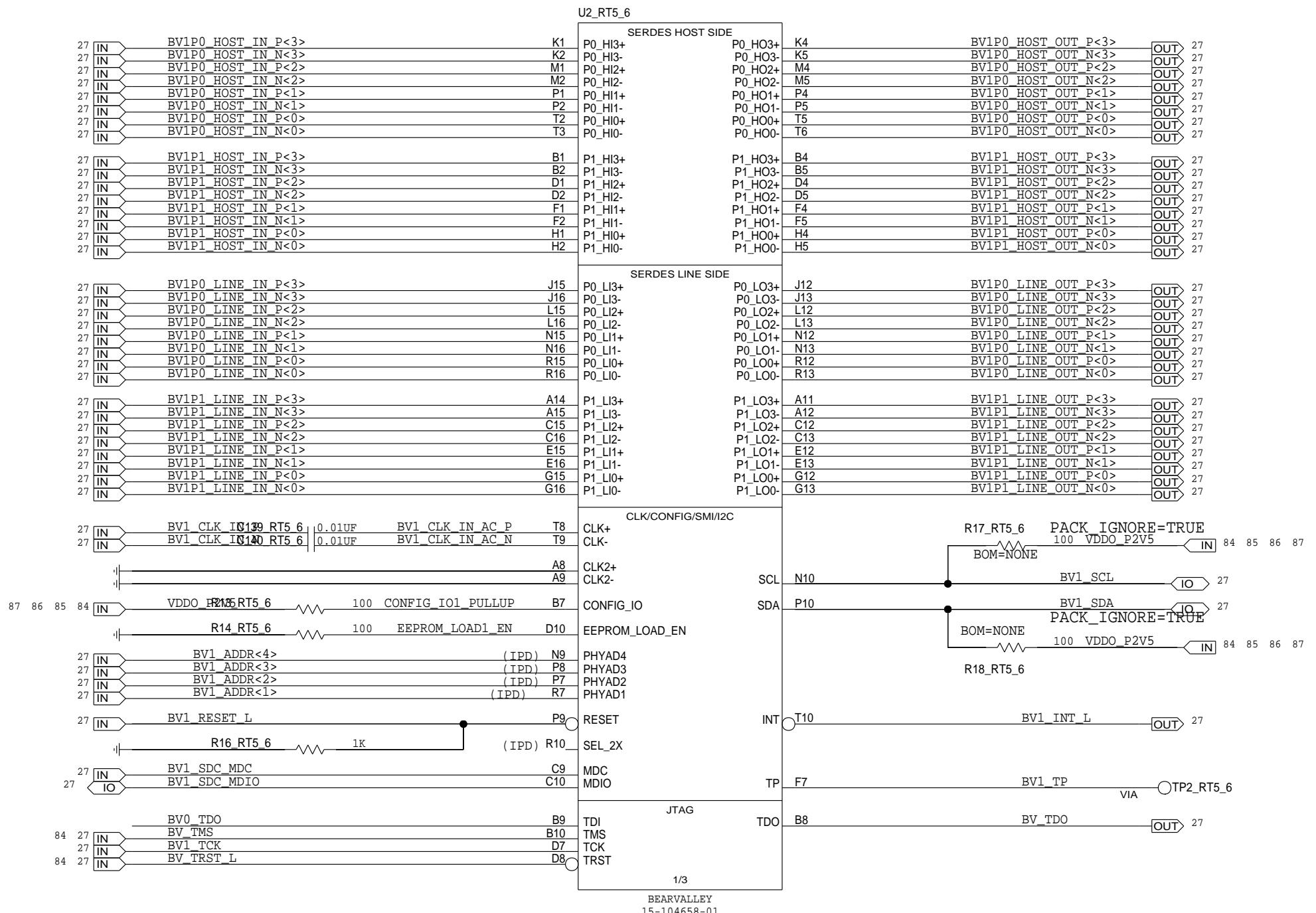
BEARVALLEY-1



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:15 2021	84 OF 138



ADDCOMP=700-26993-01



BEARVALLEY-3



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Nov 4 15:26:16 2021		86 OF 138

8

7

6

5

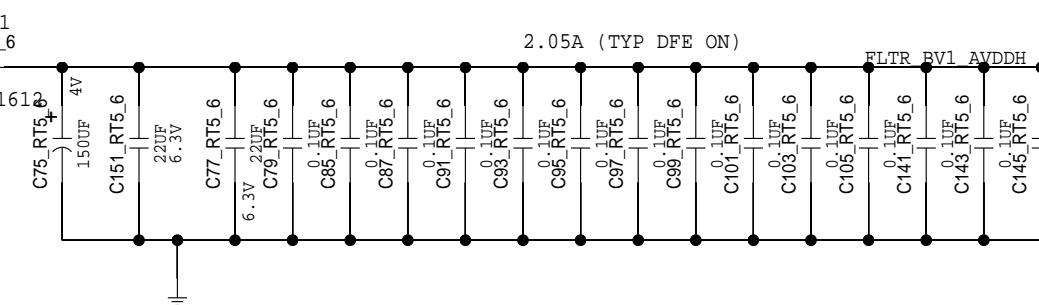
4

3

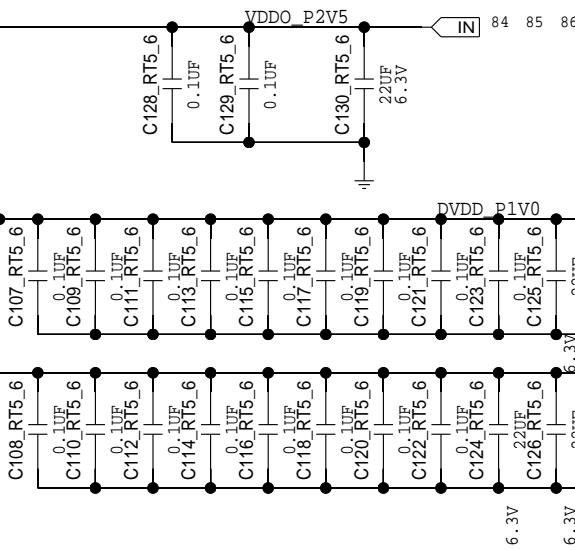
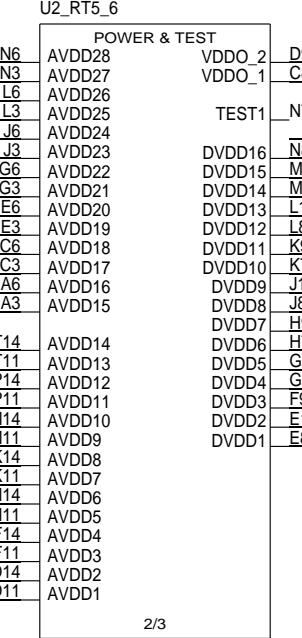
2

1

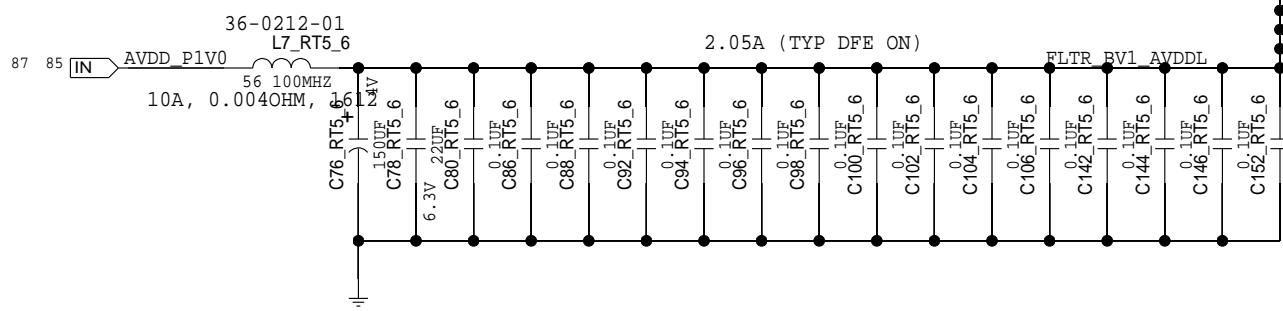
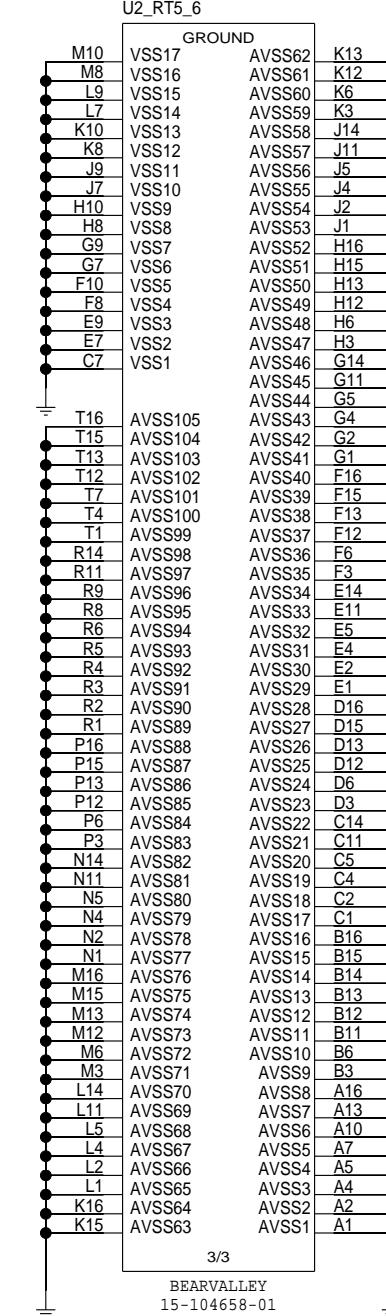
WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)



ADDCOMP=700-26993-01



ADDCOMP=700-26993-01



D

D

C

C

B

B

A

A

BEARVALLEY-4



92-105229-01

A0

SIZE CLASS CODE DWG. NO.

SCALE DATE: Thu Nov 4 15:26:16 2021

87 OF 138

8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

# BEARVALLY SUBDESIGN REV05

## 2X BEARVALLY MODULE

### CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY

11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP

05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)  
REQUIRE CAD LAYOUT CHANGE

TITLE		
 <b>CISCO</b>		
SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>
SCALE	DATE: Mon Dec 21 20:28:30 2020	REV <b>A0</b>
		88 OF 138

8

7

6

5

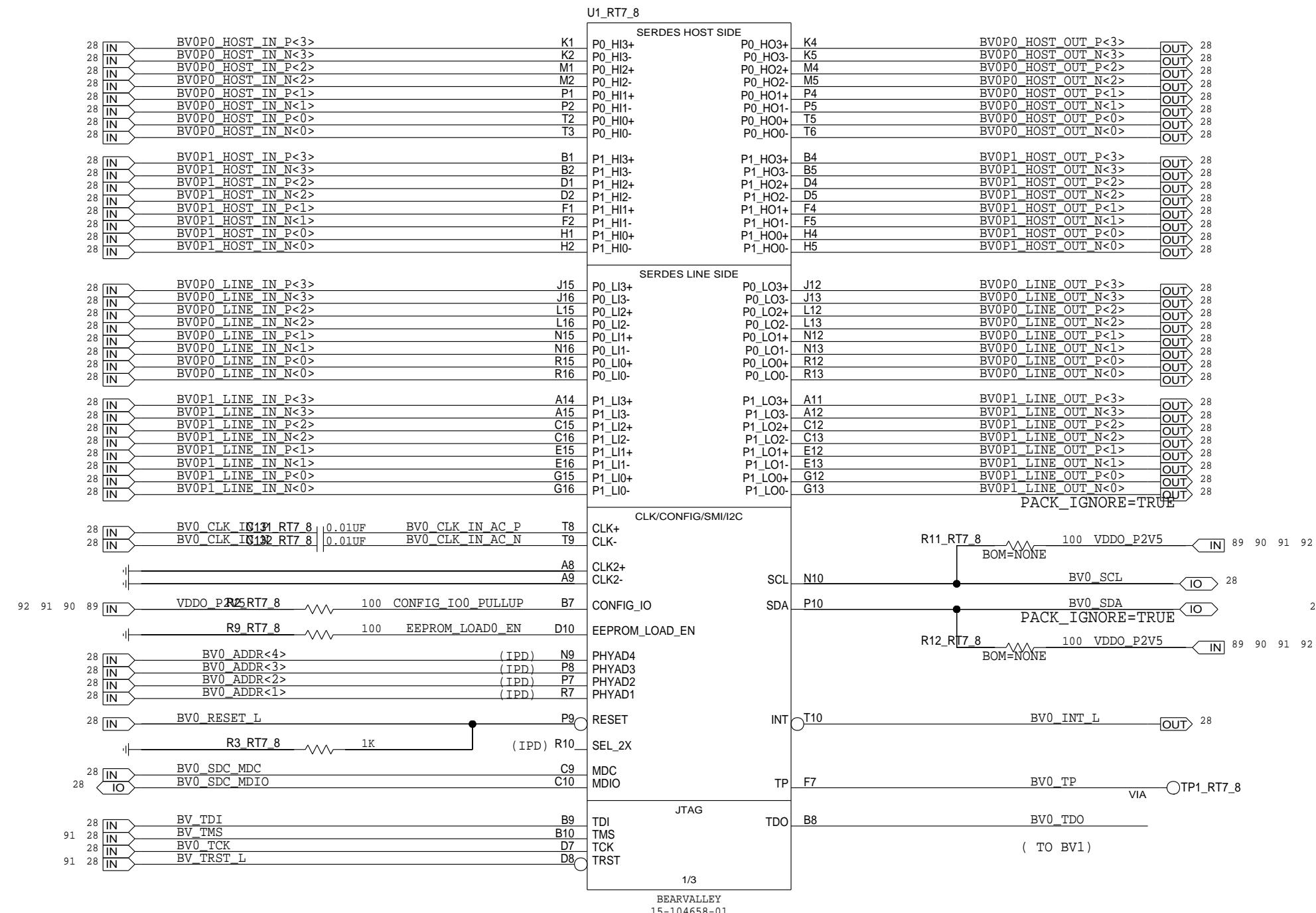
4

3

2

1

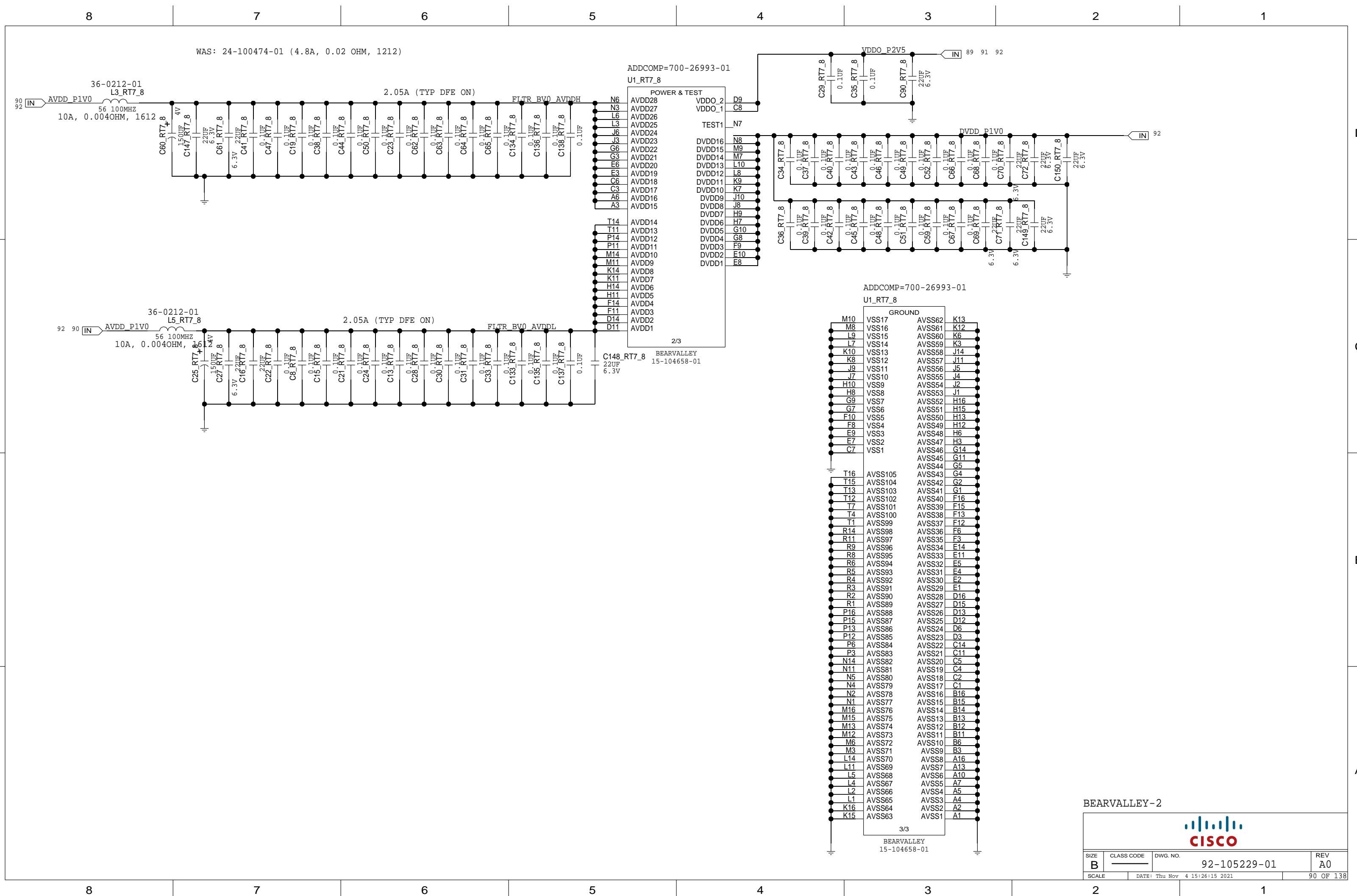
ADDCOMP=700-26993-01



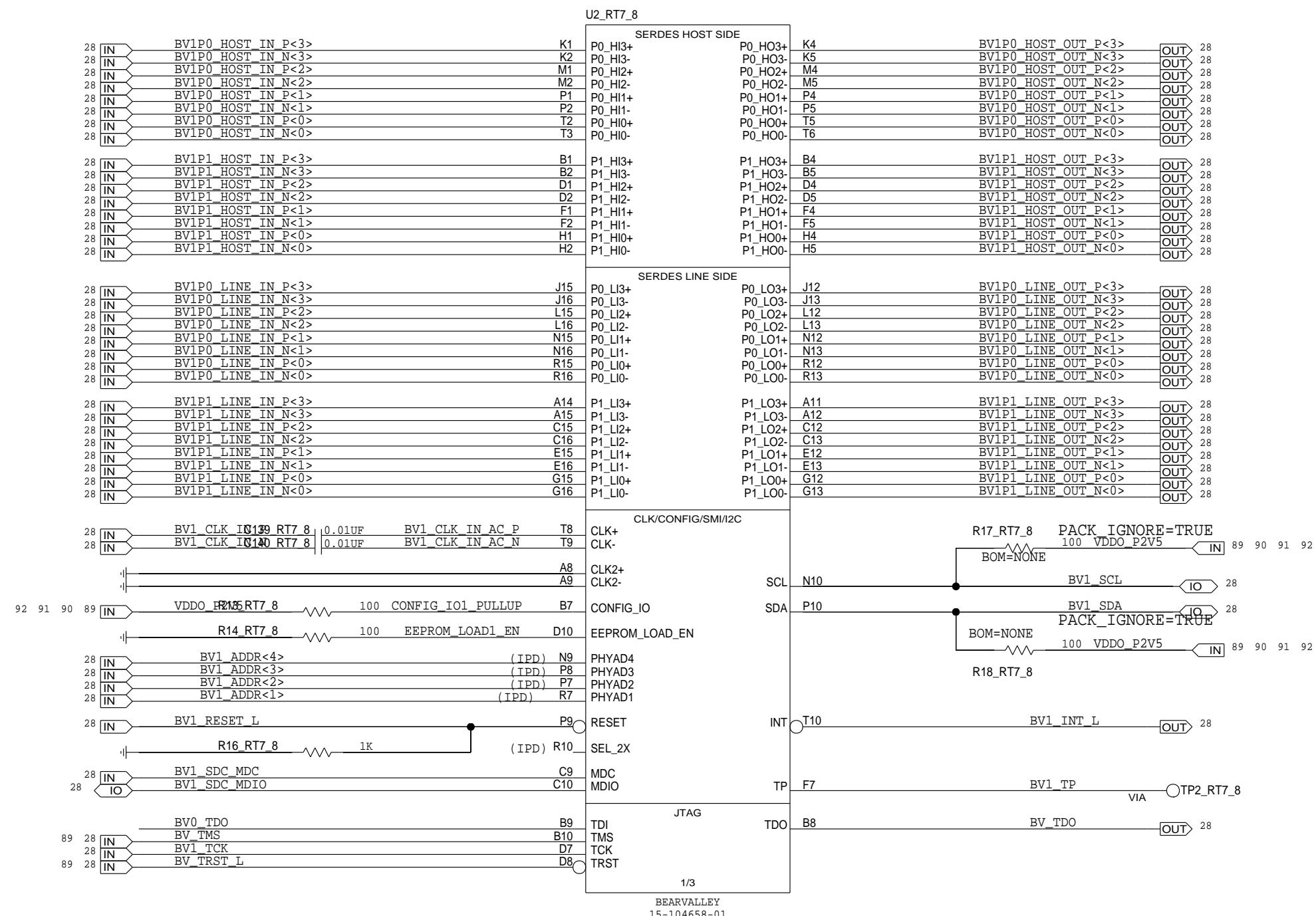
BEARVALLEY-1



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:15 2021	89 OF 138



ADDCOMP=700-26993-01



BEARVALLEY-3



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:16 2021	91 OF 138

8

7

6

5

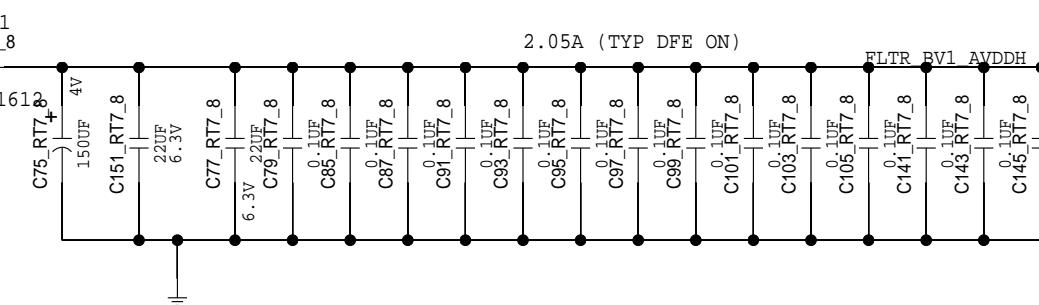
4

3

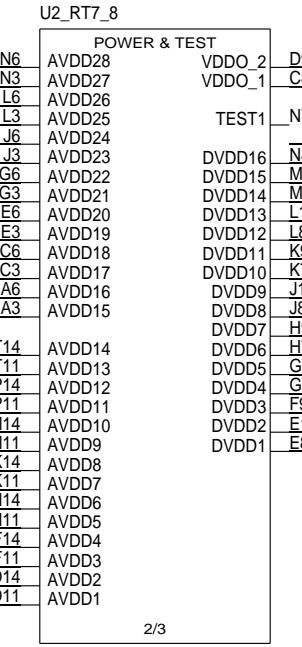
2

1

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

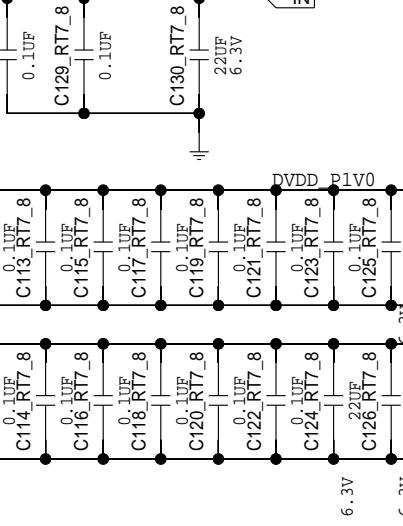


ADDCOMP=700-26993-01

BEARVALLEY  
15-104658-01

2/3

VDDO P2V5



ADDCOMP=700-26993-01

BEARVALLEY  
15-104658-01

3/3

BEARVALLEY-4



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Thu Nov 4 15:26:16 2021	REV A0

D

D

C

C

B

B

A

A

8

7

6

5

4

3

2

1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

C

B

B

A

A

# BEARVALLY SUBDESIGN REV08

## 1X BEARVALLY MODULE

REPLACED AVDD FILTER 0.02 OHM DCR INDUCTORS WITH 0.004 OHM DCR FERRITE BEADS TO REDUCE VOLTAGE DROP

REPLACED 47UF CAP 11-100179-01 WITH 11-3497-01 FOR BOM RISK

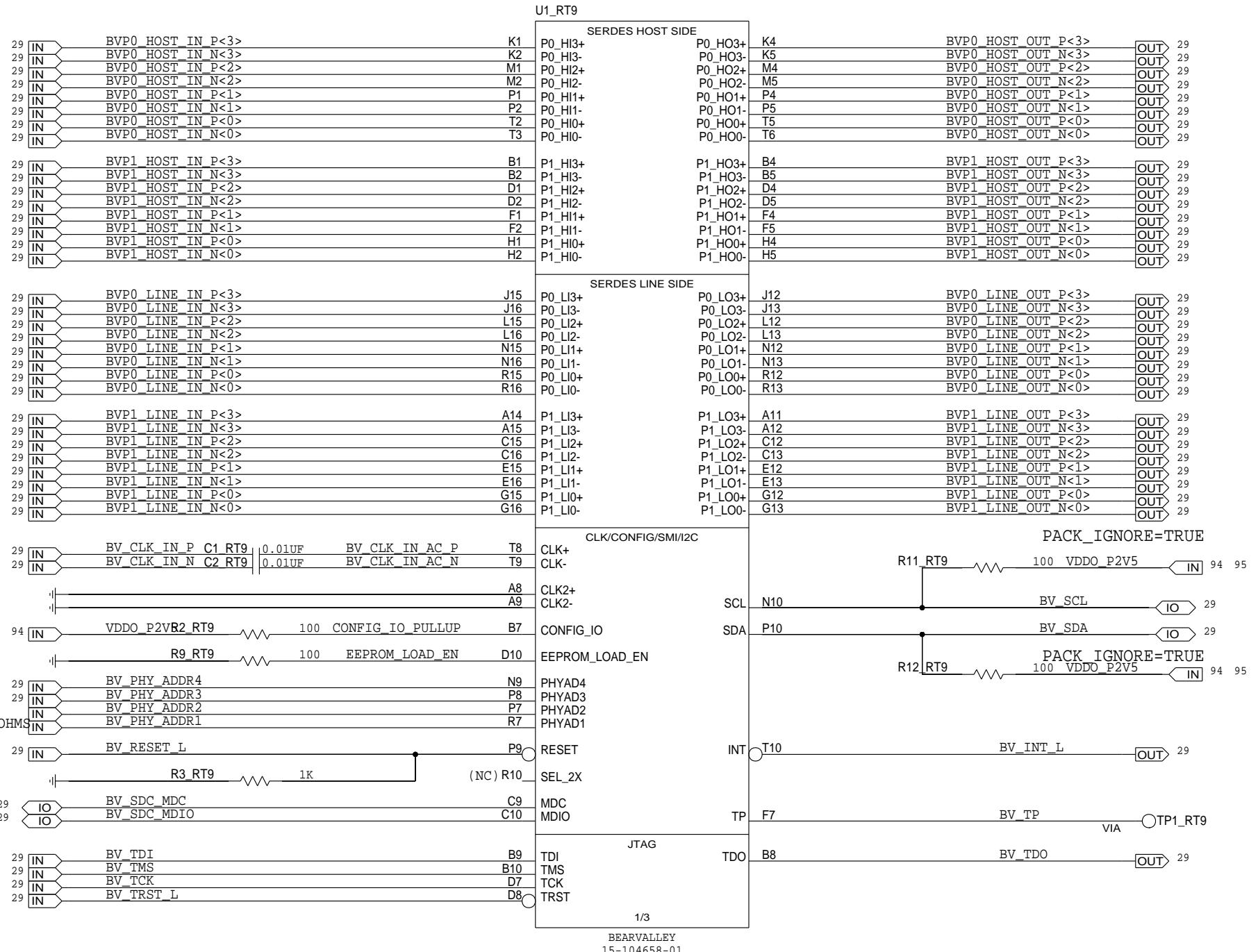
REPLACED 47UF CAP 11-3497-01 WITH 11-2686-04 FOR BOM RISK (ADD ADDITIONAL 11-2686-04 TO COMPENSATE CAPACITANCE)  
REQUIRE CAD LAYOUT CHANGE/RESPIN

TITLE			
SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Fri Jun 21 15:36:50 2019		93 OF 138



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

ADDCOMP=700-26993-01  
HEATSINK



PHYAD PINS HAVE AN INTERNAL  
PULL DOWN RESISTORS AT LIST

BEARVALLEY-1



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Nov 4 15:26:25 2021		94 OF 138

8

7

6

5

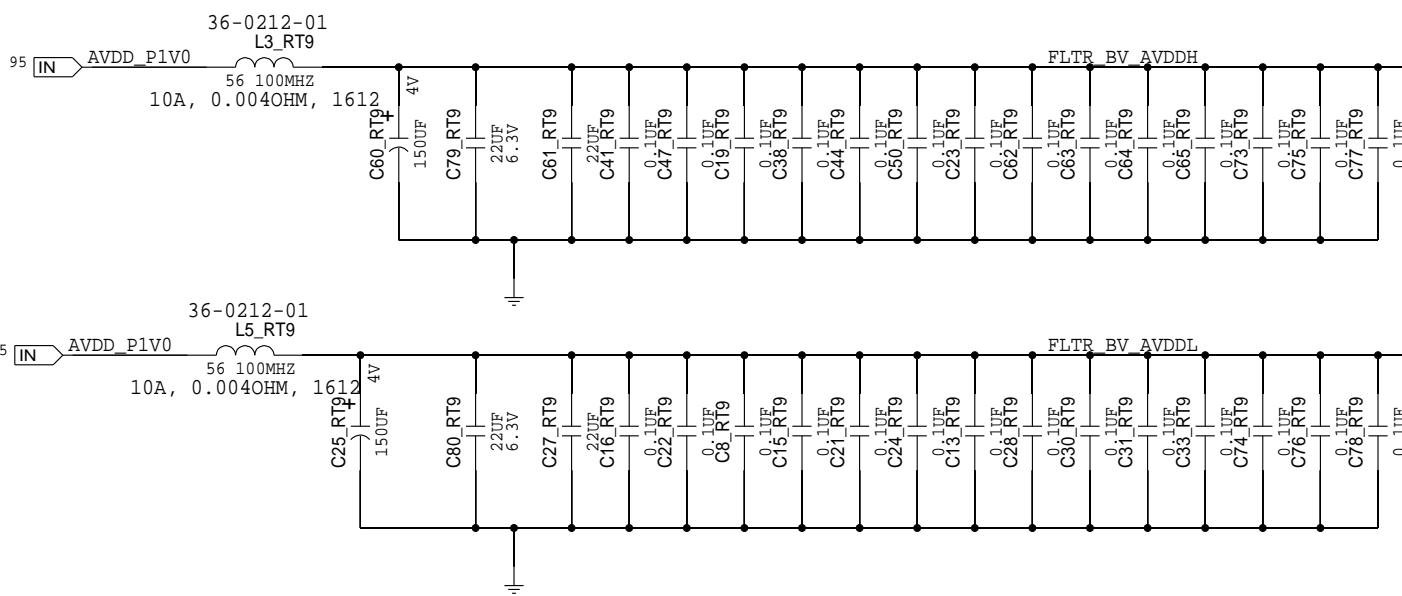
4

3

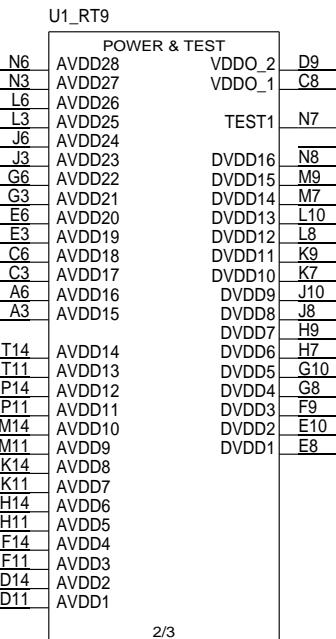
2

1

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

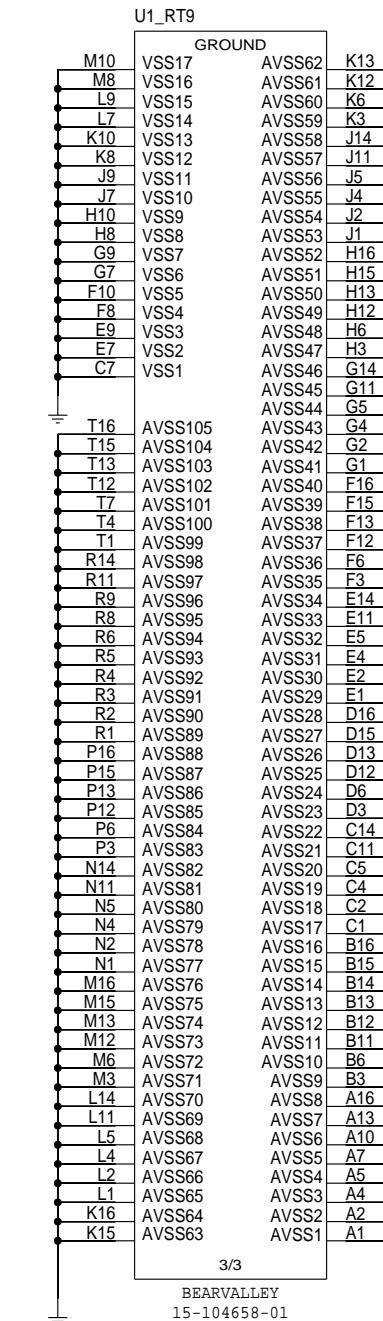


ADDCOMP=700-26993-01

BEARVALLEY  
15-104658-01

2/3

ADDCOMP=700-26993-01

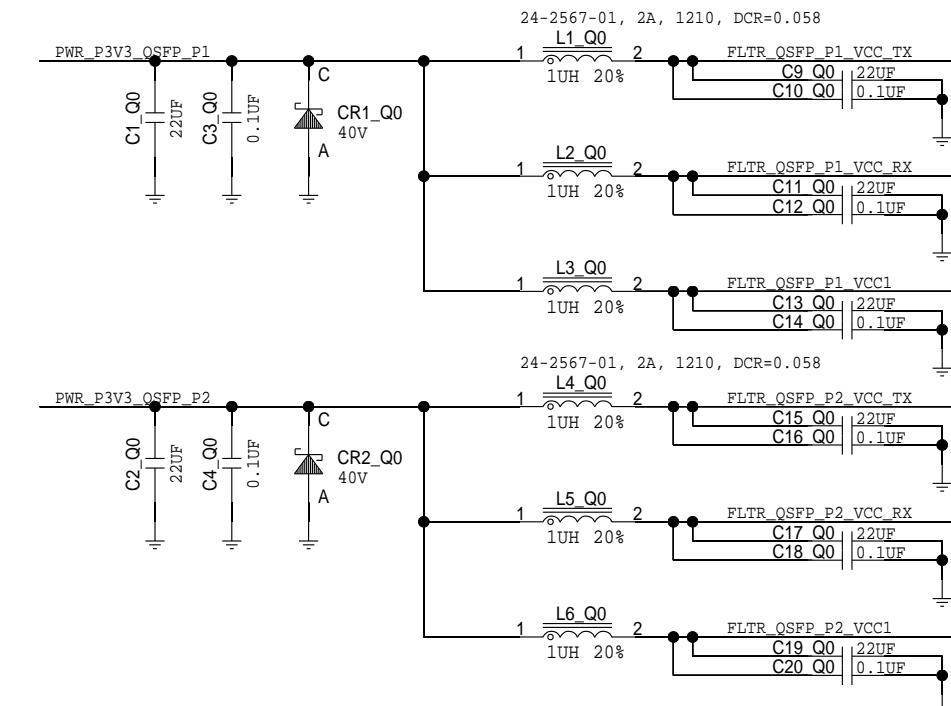
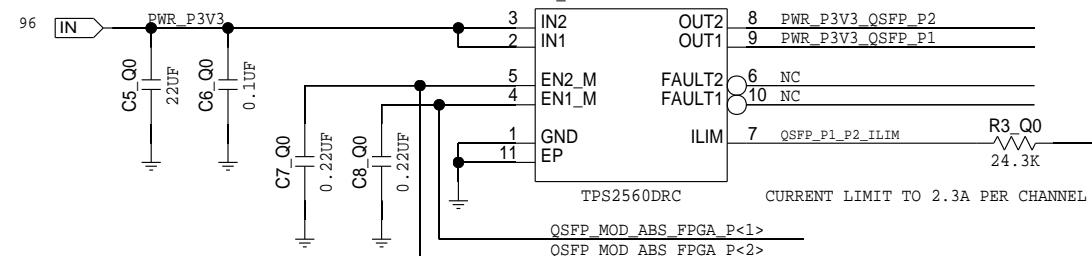
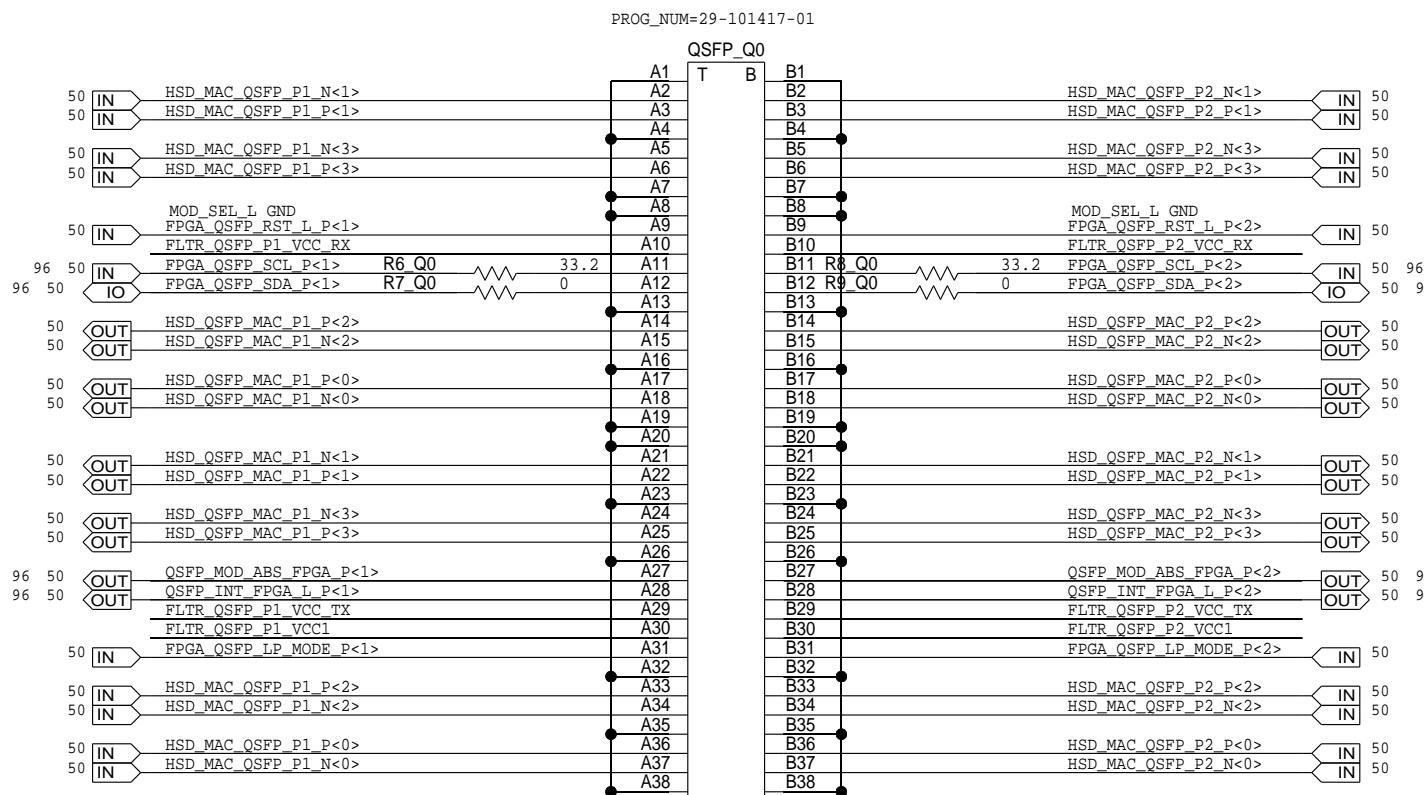
BEARVALLEY  
15-104658-01

3/3

BEARVALLEY-2

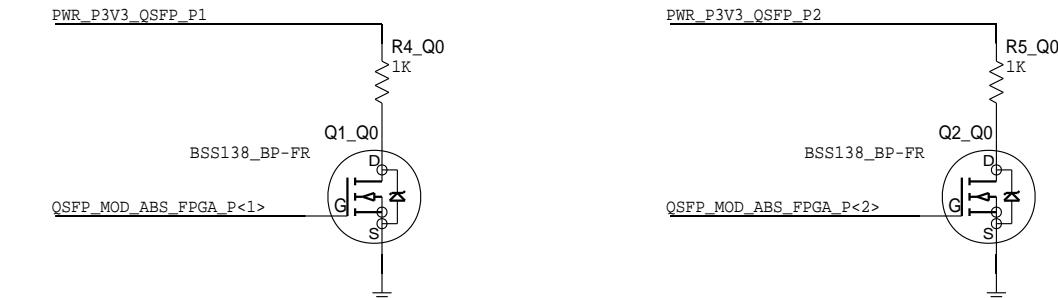


SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:25 2021	95 OF 138

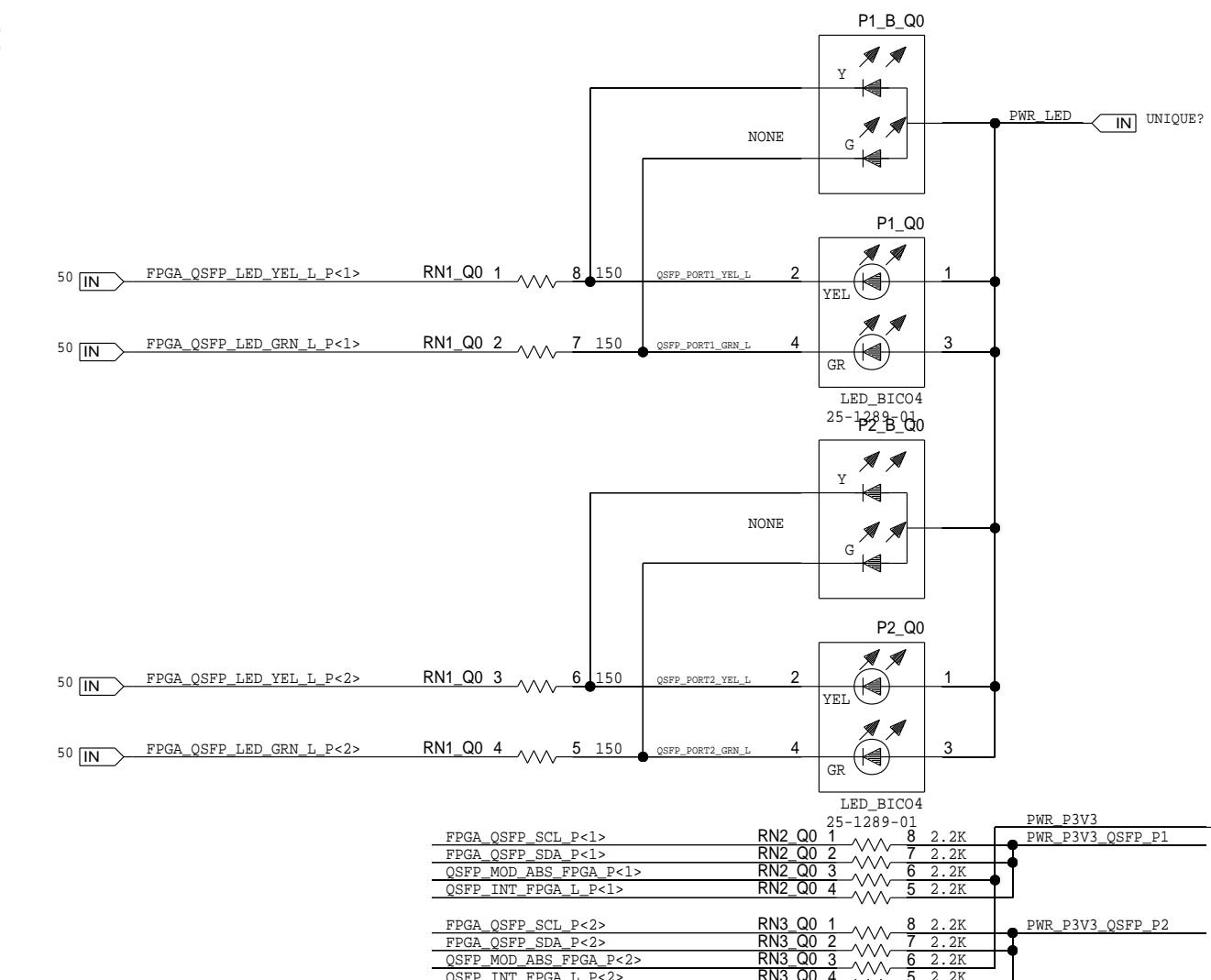


## 2X1 QSFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:  
05/23/2016: COPY FROM QSFP\_2X1\_DUAL\_LED\_PWR  
CHANGED QSFP CONNECTOR TO "REVC" VERSION  
CONDENSED SUBDESIGN TO 1 PAGE  
05/2017: ADDED DUAL FOOTPRINT TO USE BELLEVUE B2B CONNECTORS  
06/2017: CHANGED SHORT PROTECTION TO SOFTSTART UPON INSERTION  
07/2017: ADD SRT FOR I2C



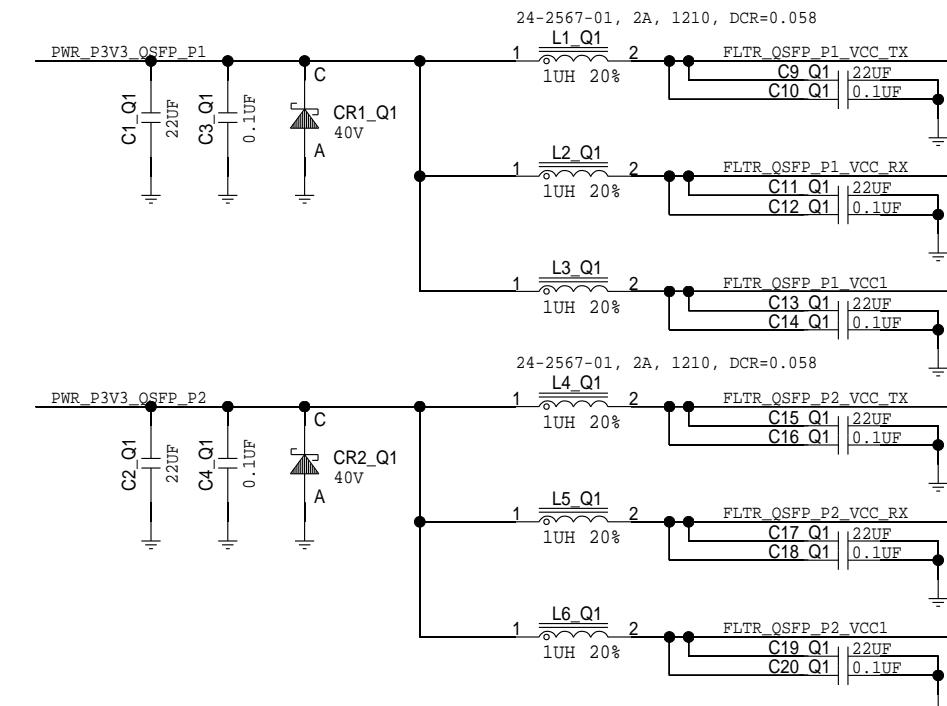
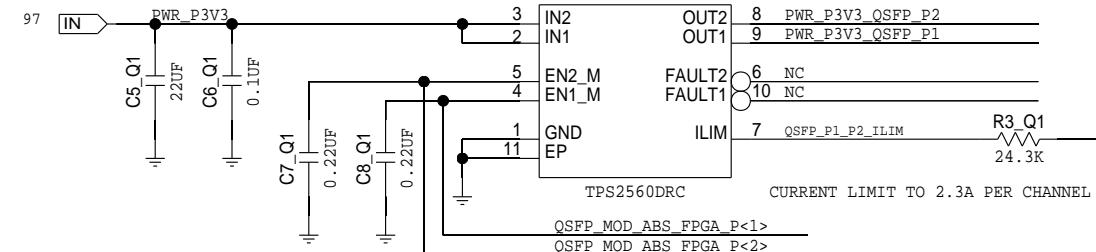
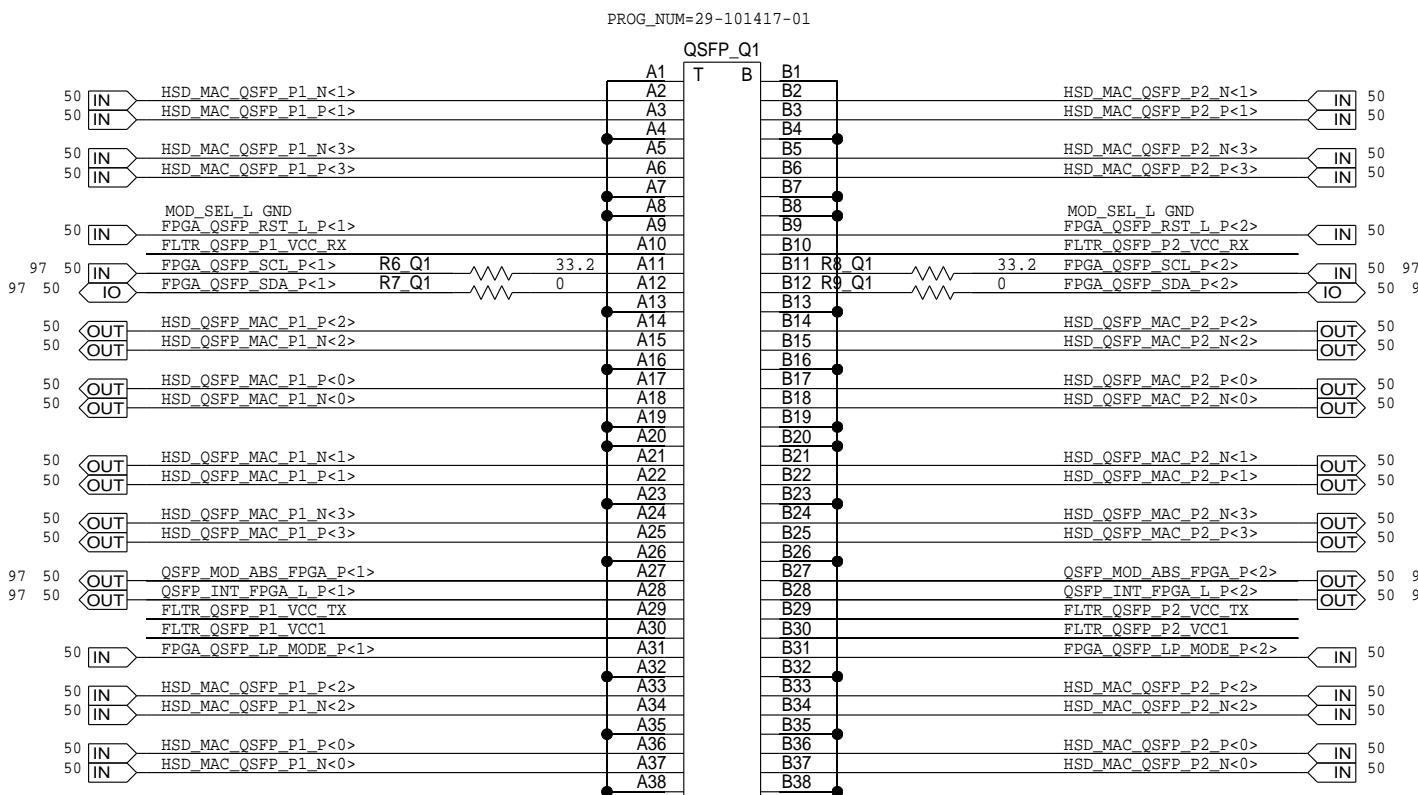
## TOP LEDS STUFFED



## QSFP PORT 1-2

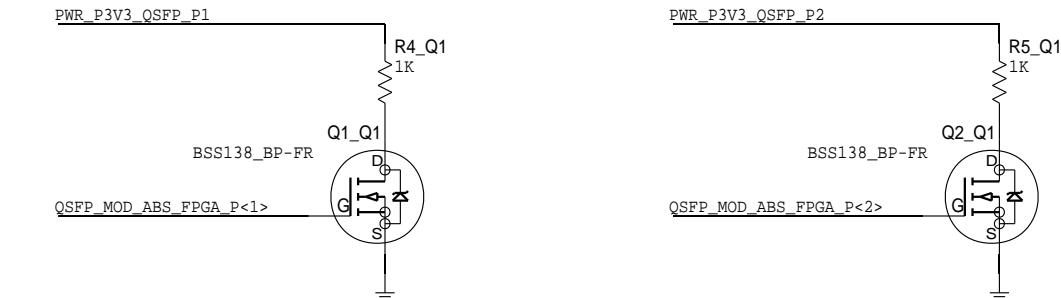


SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Fri Nov 5 15:07:38 2021	REV A0

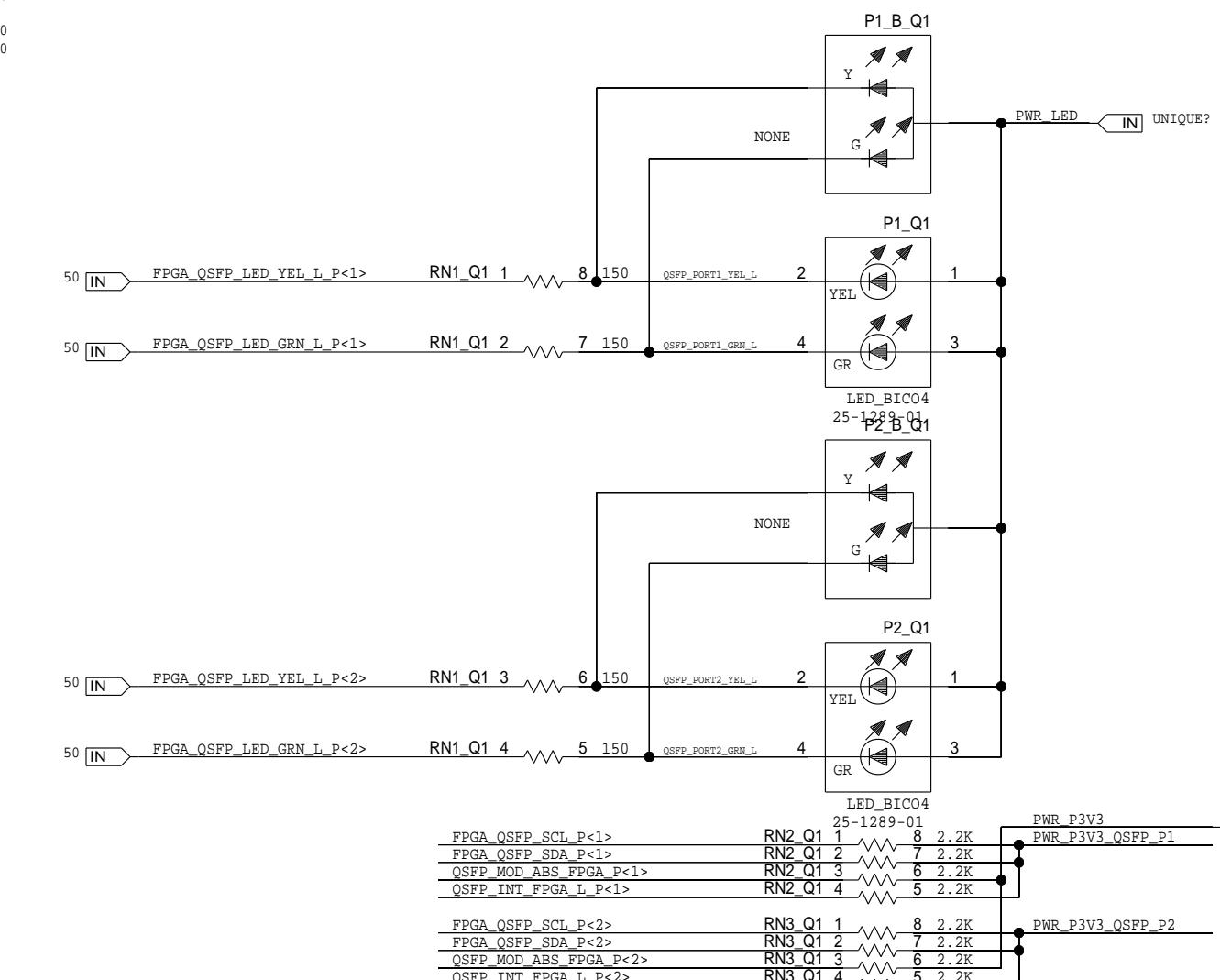


### 2X1 QSFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:  
05/23/2016: COPY FROM QSFP\_2X1\_DUAL\_LED\_PWR  
CHANGED QSFP CONNECTOR TO "REVC" VERSION  
CONDENSED SUBDESIGN TO 1 PAGE  
05/2017: ADDED DUAL FOOTPRINT TO USE BELLEVUE B2B CONNECTORS  
06/2017: CHANGED SHORT PROTECTION TO SOFTSTART UPON INSERTION  
07/2017: ADD SRT FOR I2C



### TOP LEDS STUFFED



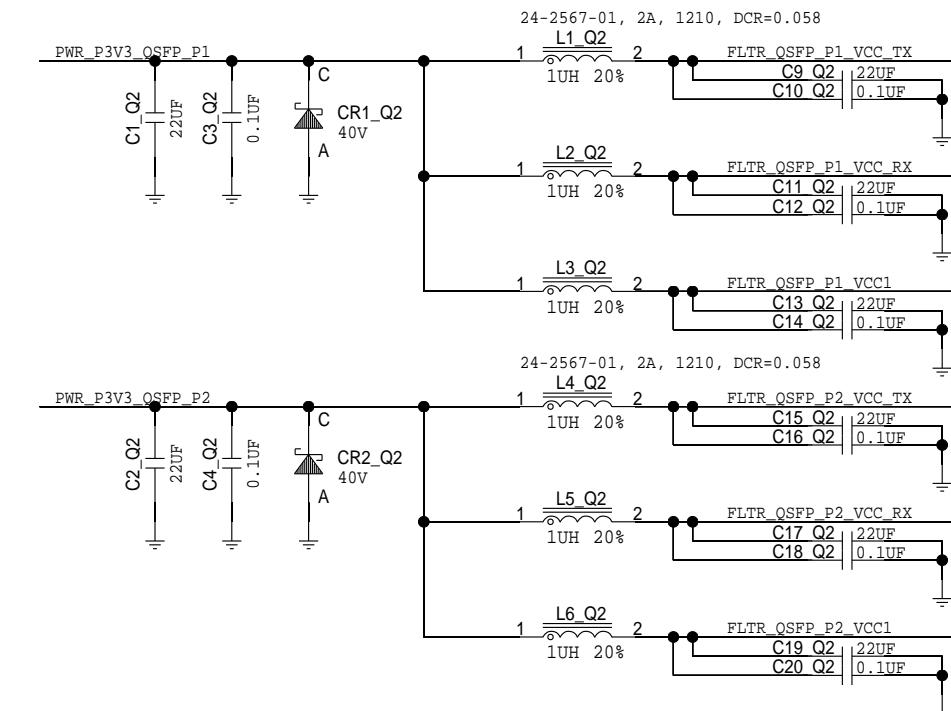
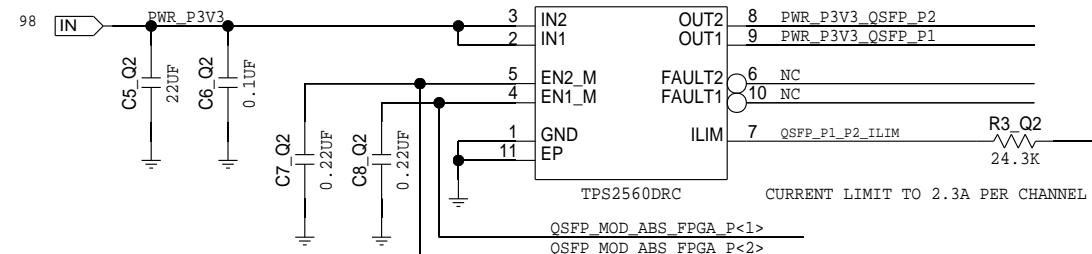
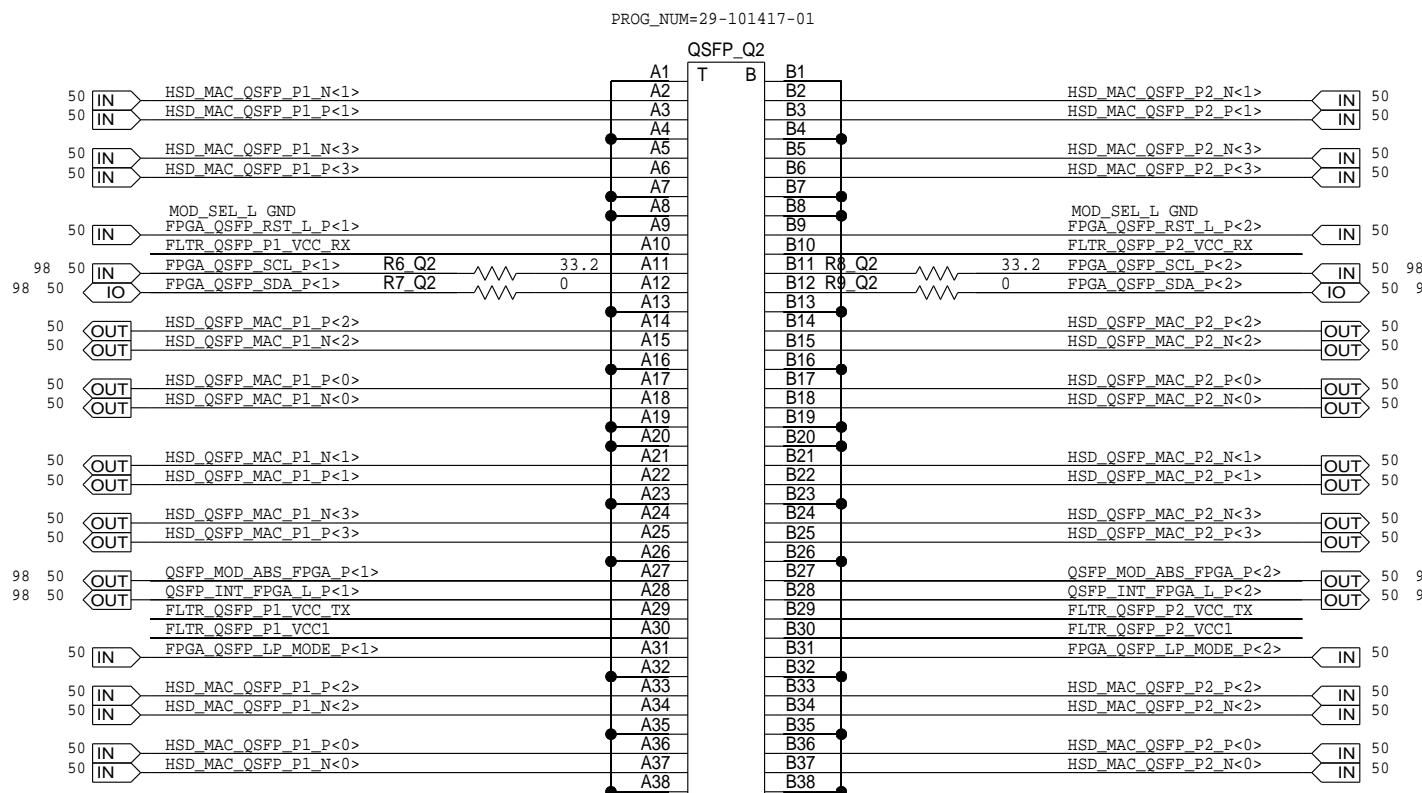
### QSFP PORT 1-2



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Fri Nov 5 15:07:38 2021	REV A0
97 OF 138		

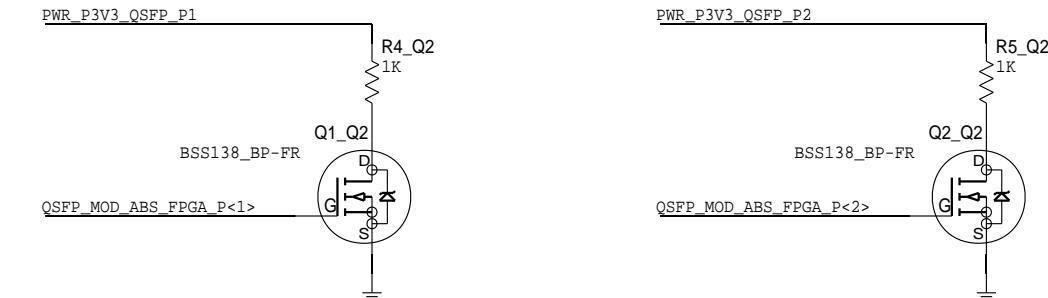
D

D

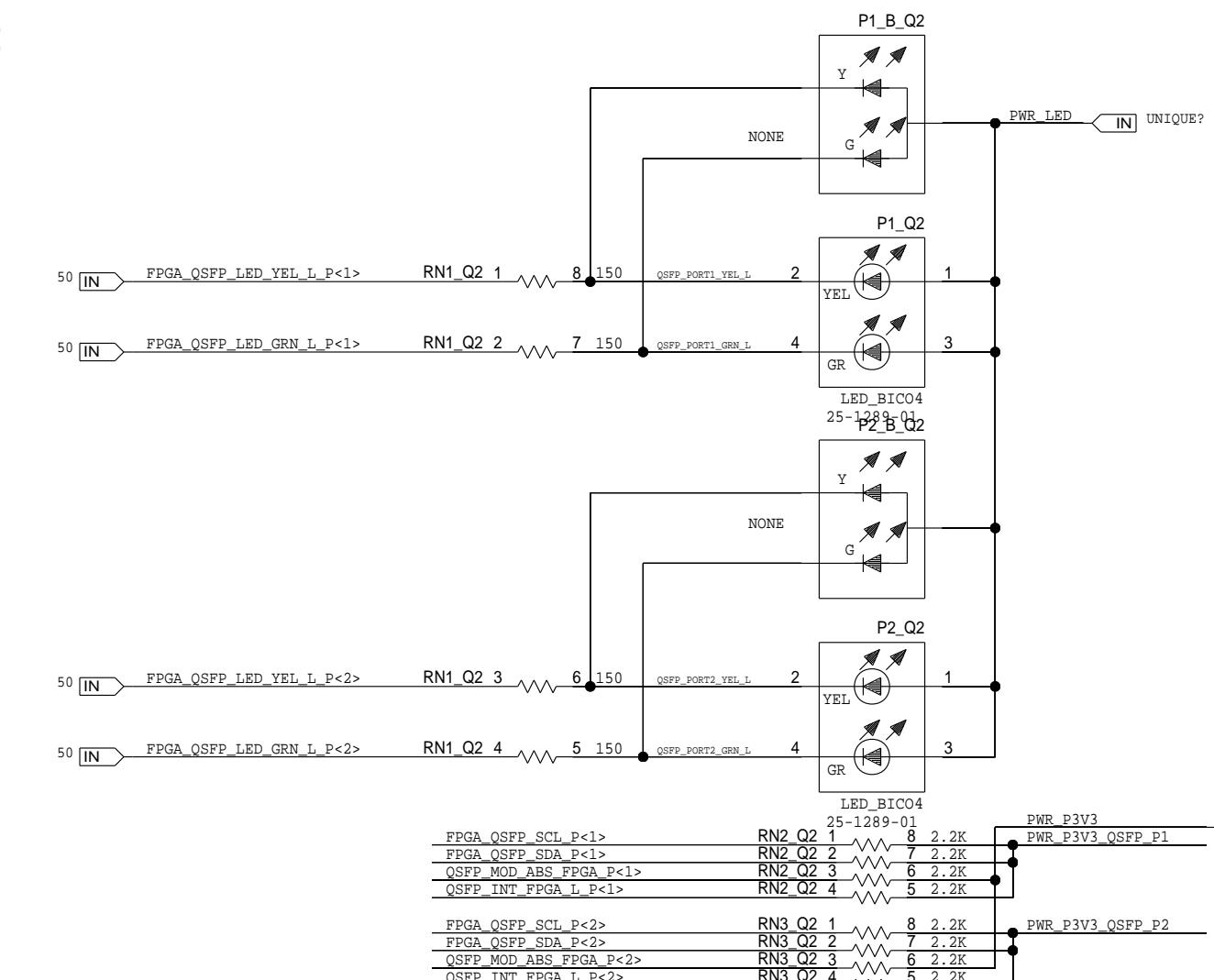


### 2X1 QSFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:  
05/23/2016: COPY FROM QSFP\_2X1\_DUAL\_LED\_PWR  
CHANGED QSFP CONNECTOR TO "REVC" VERSION  
CONDENSED SUBDESIGN TO 1 PAGE  
05/2017: ADDED DUAL FOOTPRINT TO USE BELLEVUE B2B CONNECTORS  
06/2017: CHANGED SHORT PROTECTION TO SOFTSTART UPON INSERTION  
07/2017: ADD SRT FOR I2C



### TOP LEDS STUFFED



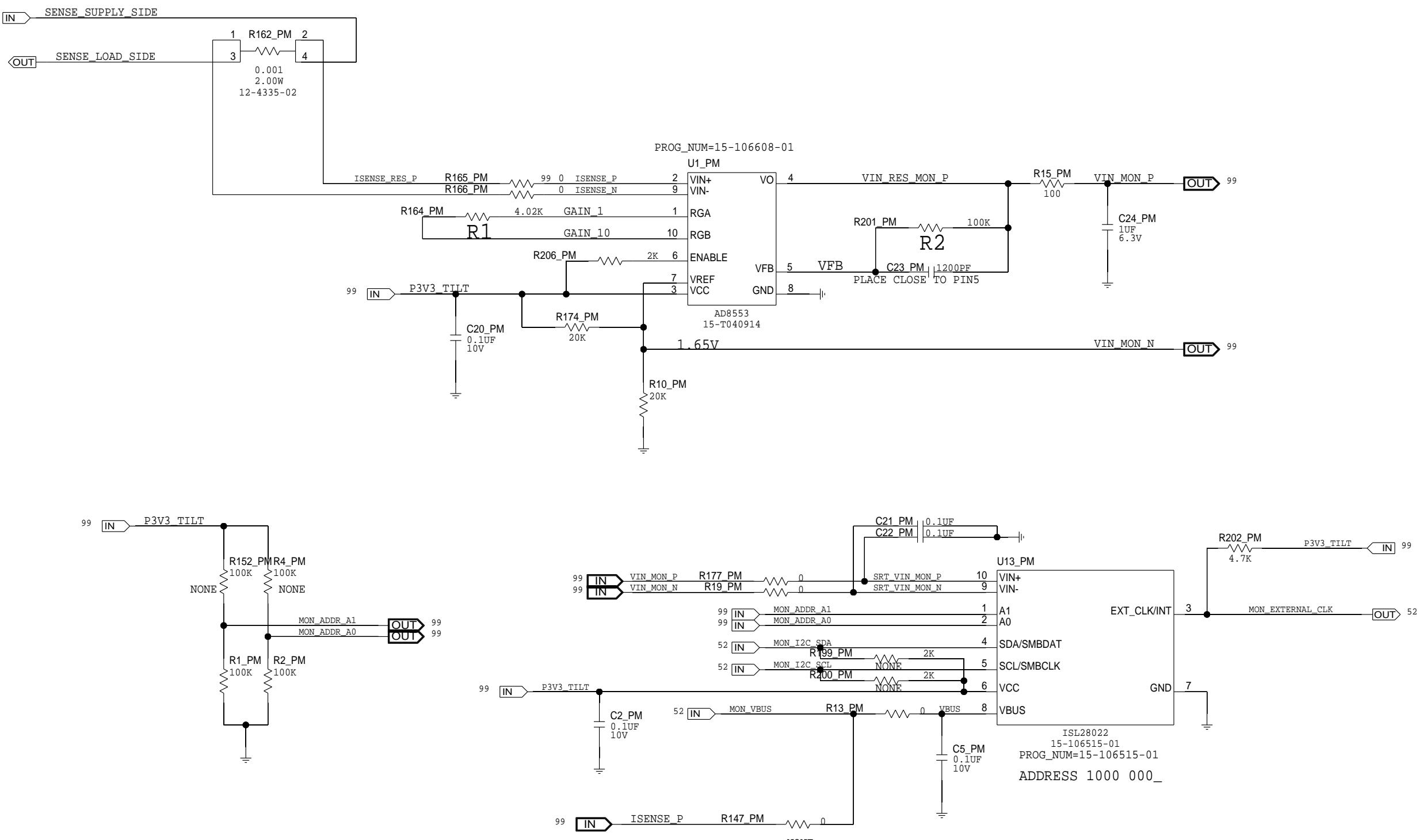
### QSFP PORT 1-2



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Fri Nov 5 15:07:38 2021	REV A0
98 OF 138		

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

REVISION					
REV	ECO	DESCRIPTION	APPROVALS		
			DFTG	CHK	APVD



OTY REQD		PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION	
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION    DECIM    ANGLES			APPROVALS	DATE			
± .xx +.01      ±1 ° ± .xxx+.005			DRAWN BY ? CAD ?				
		MATERIAL	MECH ? ?	TITLE:			
			ENGR ? ?				
NEXT ASSY	USED ON	FINISH	MFG ? ?	SIZE <b>B</b>	CLASS CODE _____	DWG. NO.	REV A0
			TEST ? ?	SCALE	DATE:		
APPLICATION		DO NOT SCALE DWG					99 OF 138

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

DWG NO 92-105229-01	SHT 138	REV A0	1
REVISION			
REV	ECO	DESCRIPTION	APPROVALS
			DFTG      CHK      APVD

# CYCLONE 5 FPGA AUX VOLTAGE RAILS REV 01

3.3V: 15A (TPS53915)  
2.5V: 3A (1 PHASE TPS54394  
1.1V: 3A (1 PHASE TPS54394

## CHANGE HISTORY

REV01: COPY FROM CY5\_9A 3A\_3A REV 03 SUBDESIGN. NOT FOOTPRINT COMPATIBLE

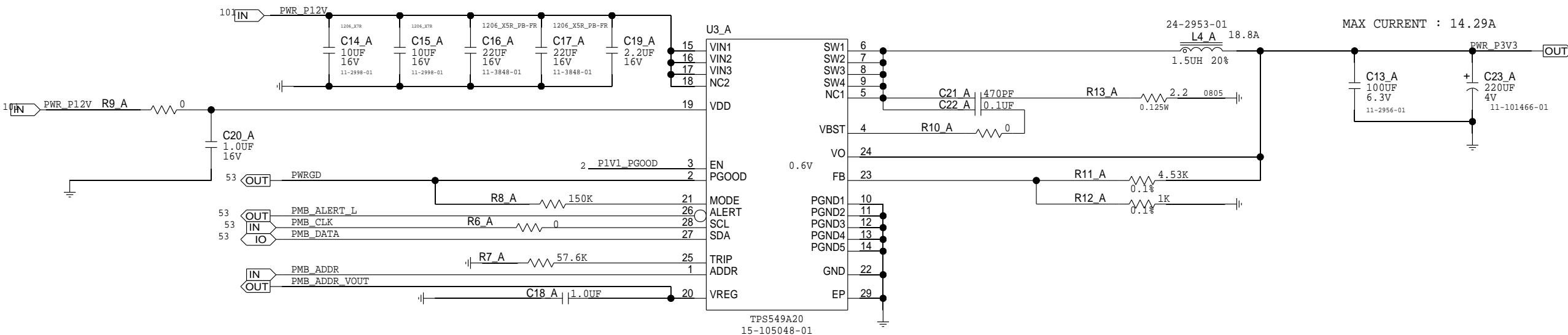


QTY REQD	PART OR IDENTIFYING NO.			NOMENCLATURE OR DESCRIPTION			MATERIAL SPECIFICATION	
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION      DECIM      ANGLES $\pm$ .xx +.01 - $\pm 1^\circ$ $\pm$ .xxx+.005			APPROVALS	DATE	 <b>CISCO</b>			
			DRAWN BY ?	CAD ?				
MATERIAL		MECH	TITLE:					
		?						
FINISH		ENGR						
		?						
DO NOT SCALE DWG		MFG	SIZE	CLASS CODE	DWG. NO.			REV
		?	B	_____				A0
		TEST	SCALE		DATE:		100 OF 138	
		?						

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

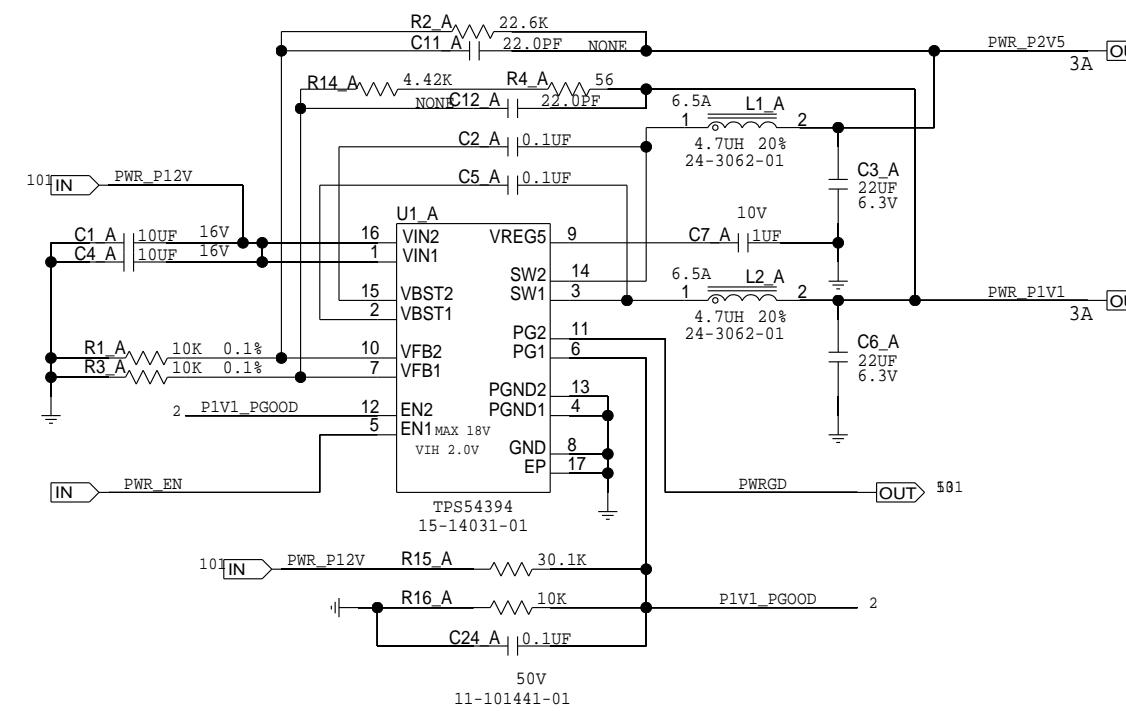
D

D



C

C



B

B

CONTROLLER



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Thu Nov 4 15:26:21 2021	101 OF 138

101

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

1

THIS DOCUMENT CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF CISCO SYSTEMS. NO PART OF THIS DOCUMENT MAY BE DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF CISCO SYSTEMS.

REVISION			APPROVALS		
REV	ECO	DESCRIPTION	DFTG	CHK	APVD

# SUNDOWN1 MIN FW1201 SUBDESIGN REV01

D

D

C

C

B

B

A

A

01:BASED ON SUNDOWN1 SUBDESIGN REV06, WITH NEW CPN MIN FW1201.

TITLE PAGE			
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION    DECIM		APPROVALS	DATE
.xx x .01 .xxx x .005		DRAWN BY BEYENE LULSEGED	
?		CAD	
MATERIAL		MECH ?	
FINISH		ENGR BEYENE LULSEGED	
NEXT ASSY	USED ON	MFG ?	
APPLICATION		TEST ?	
		SCALE	REV A0
		DATE:	102 OF 138



**TABLE OF CONTENTS**

1	TITLE PAGE
3	SNDN_HS0_TO_HS8_N_S0
4	SNDN_HS9_TO_HS17_N_S0
5	SNDN_PCIE_CLK_JTAG_MISC
6	SNDN STRAP OPTIONS
7	SNDN_VDDA / VDDHA
8	SNDN_VDD / VDDIO
9	SNDN_GND
10	SNDN_DECAP_1
11	SNDN_DECAP_2

D

D

C

C

B

B

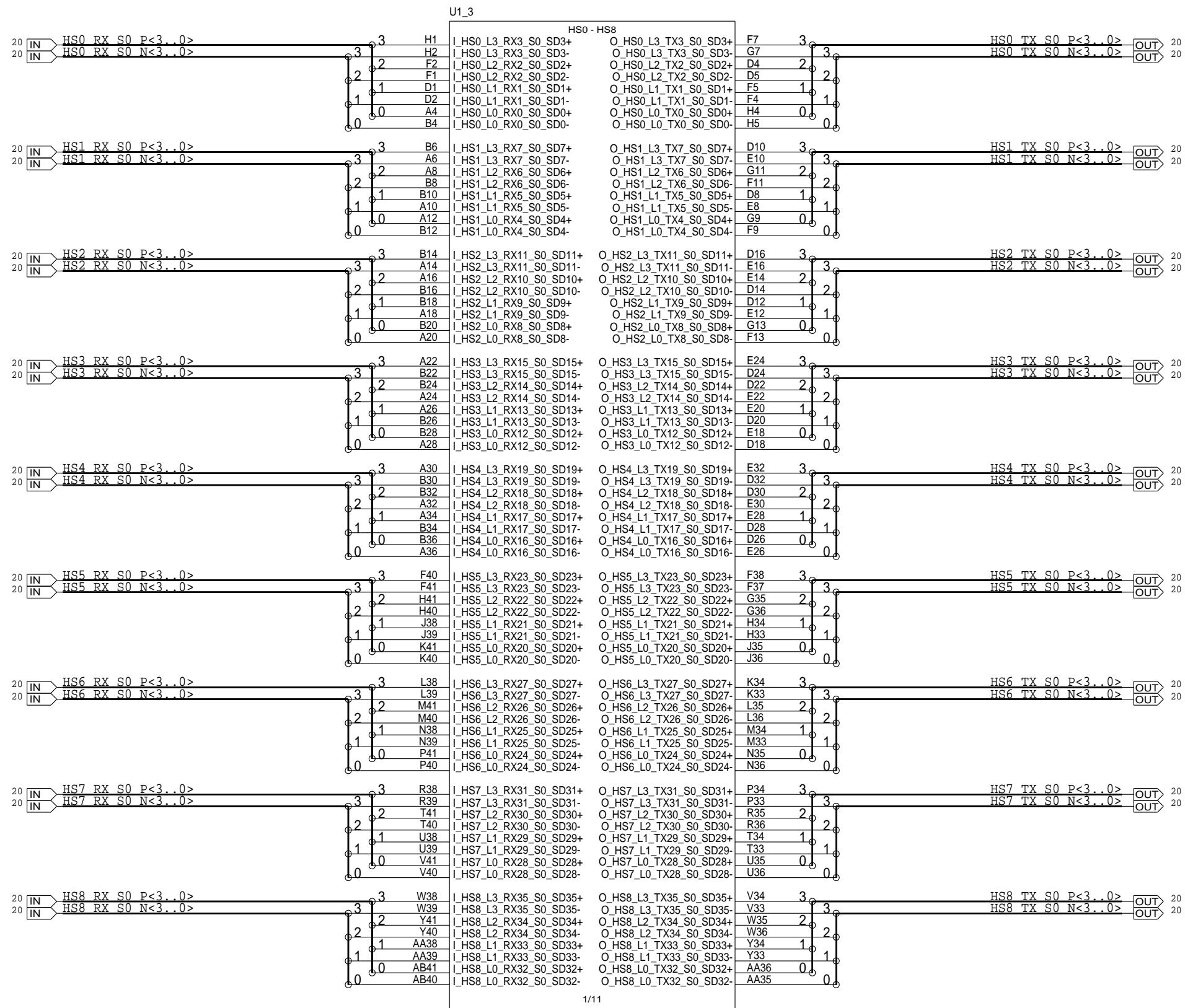
A

A



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Tue Mar 26 21:44:36 2019		103 OF 138

PROG\_NUM=08-1199-01 MIN FW 1201  
ADDCOMP=700-105818-01; 700-104727-01



SNDN\_HS0\_TO\_HS8 \_N S0



SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Wed Feb 23 12:58:35 2022	104 OF 138

D

D

C

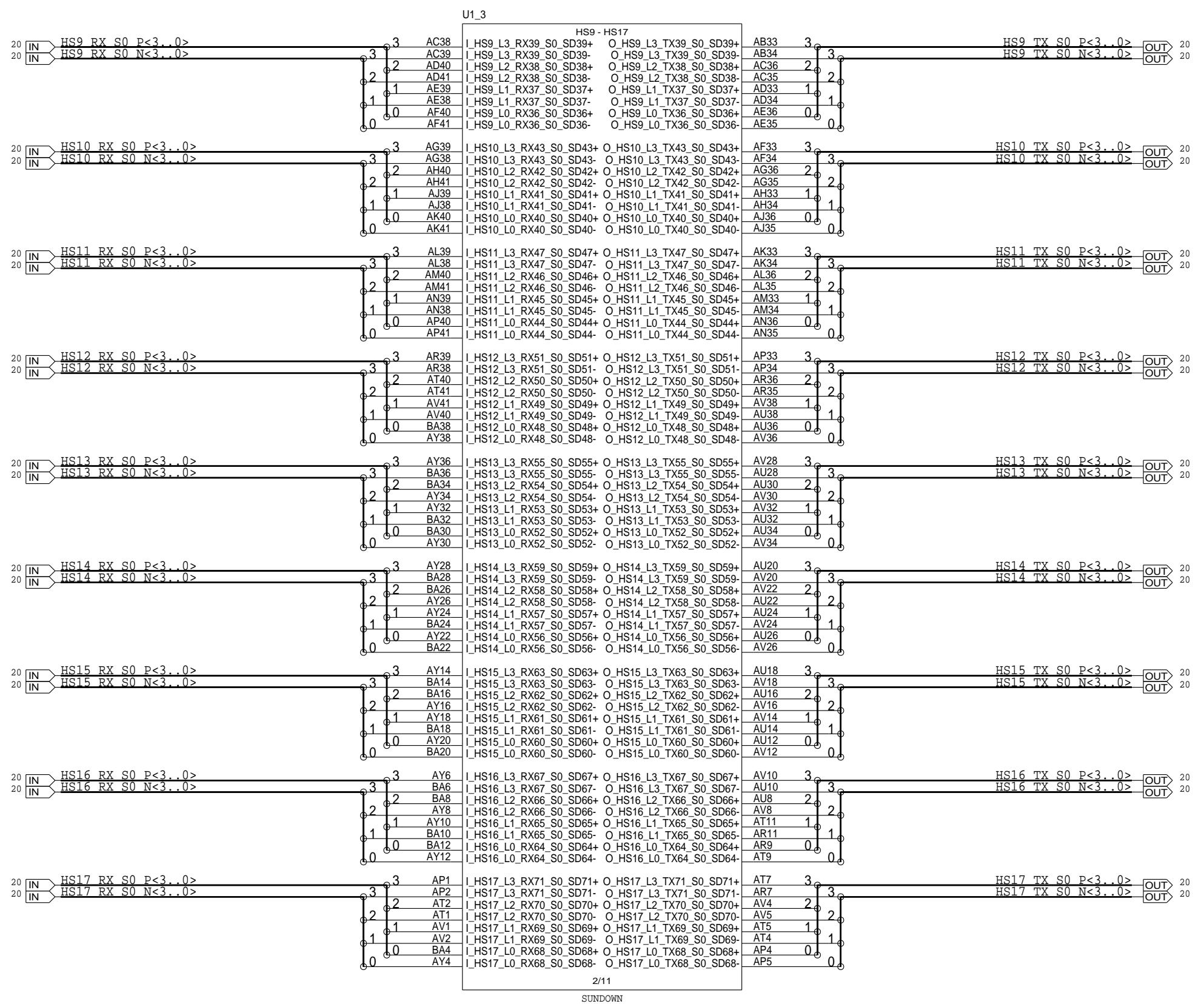
C

B

B

A

A



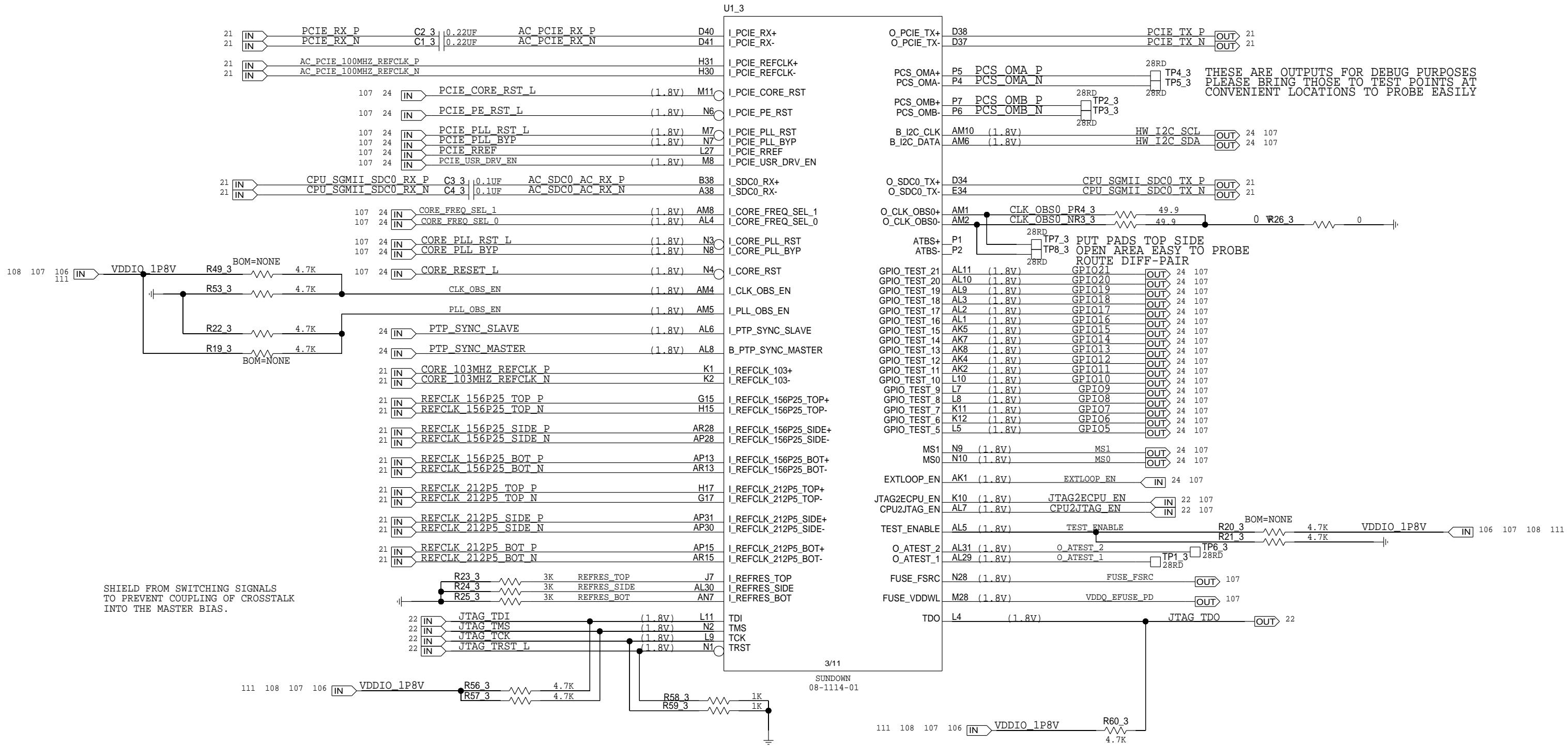
SNDN\_HS9\_TO\_HS17\_N\_S0



SIZE	CLASS CODE	DWG. NO.
B	—	92-105229-01
SCALE	DATE: Wed Feb 23 12:58:35 2022	105 OF 138

D

D



SNDN PCIE\_CLK\_JTAG\_MISC

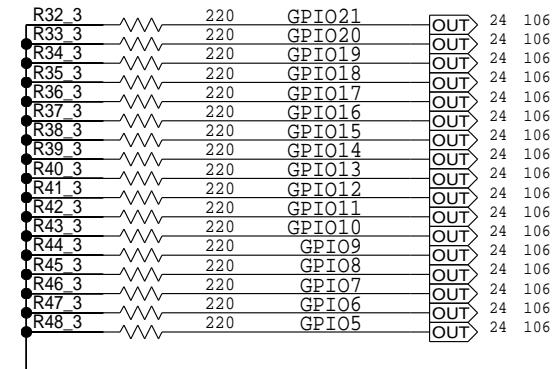


SIZE	CLASS CODE	DWG. NO.
B	_____	92-105229-01
SCALE	DATE: Wed Feb 23 12:58:35 2022	REV A0

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

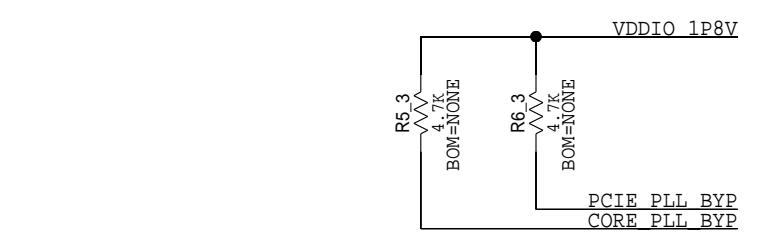
D

D



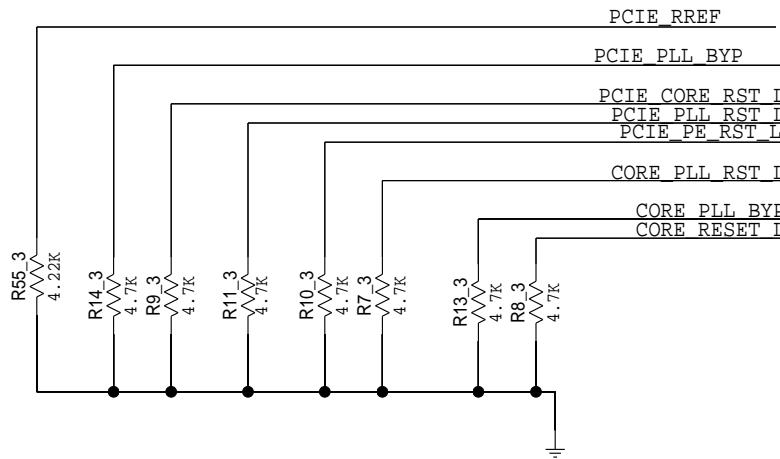
C

C



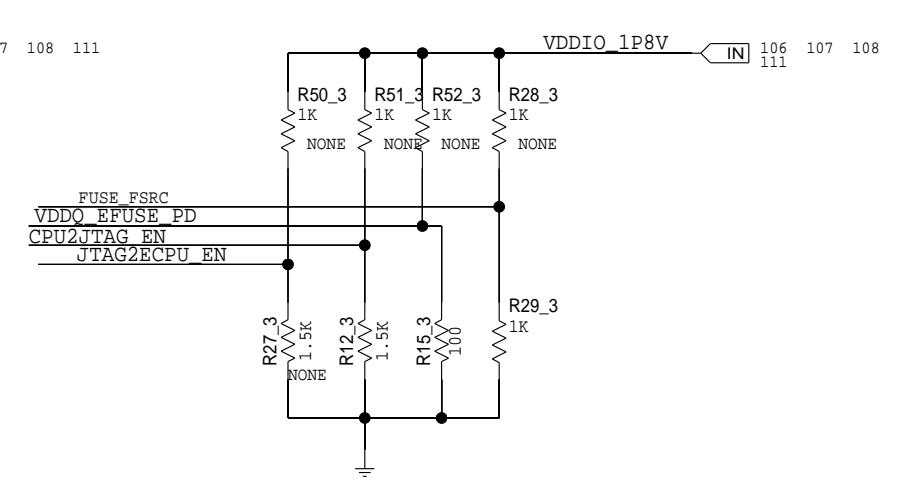
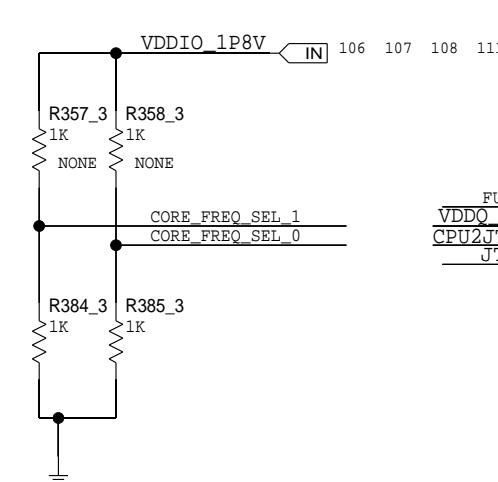
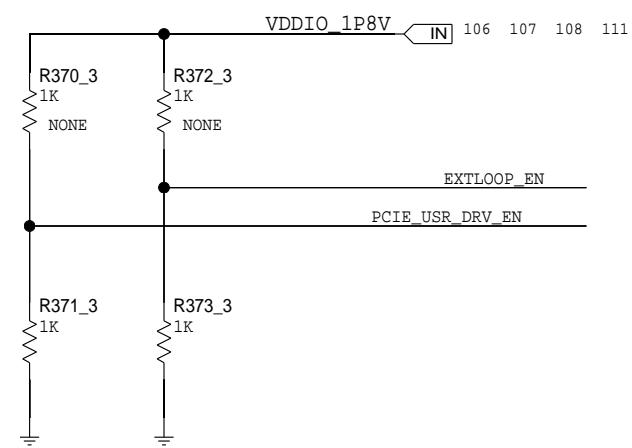
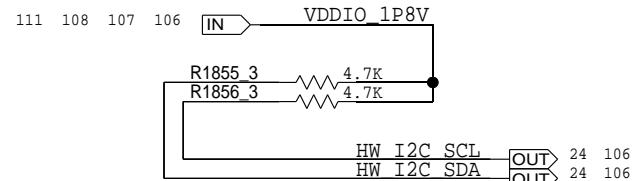
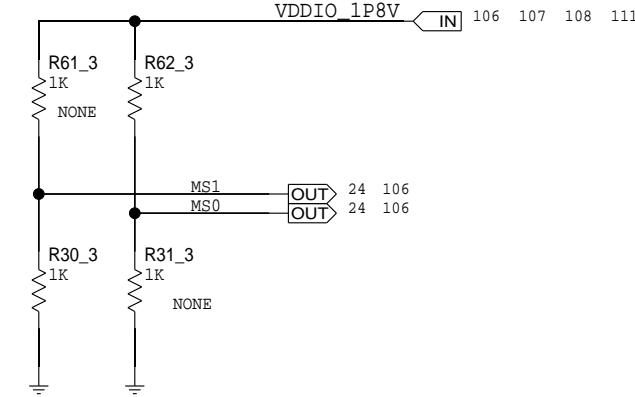
B

B



A

A



#### SNDN STRAP OPTIONS



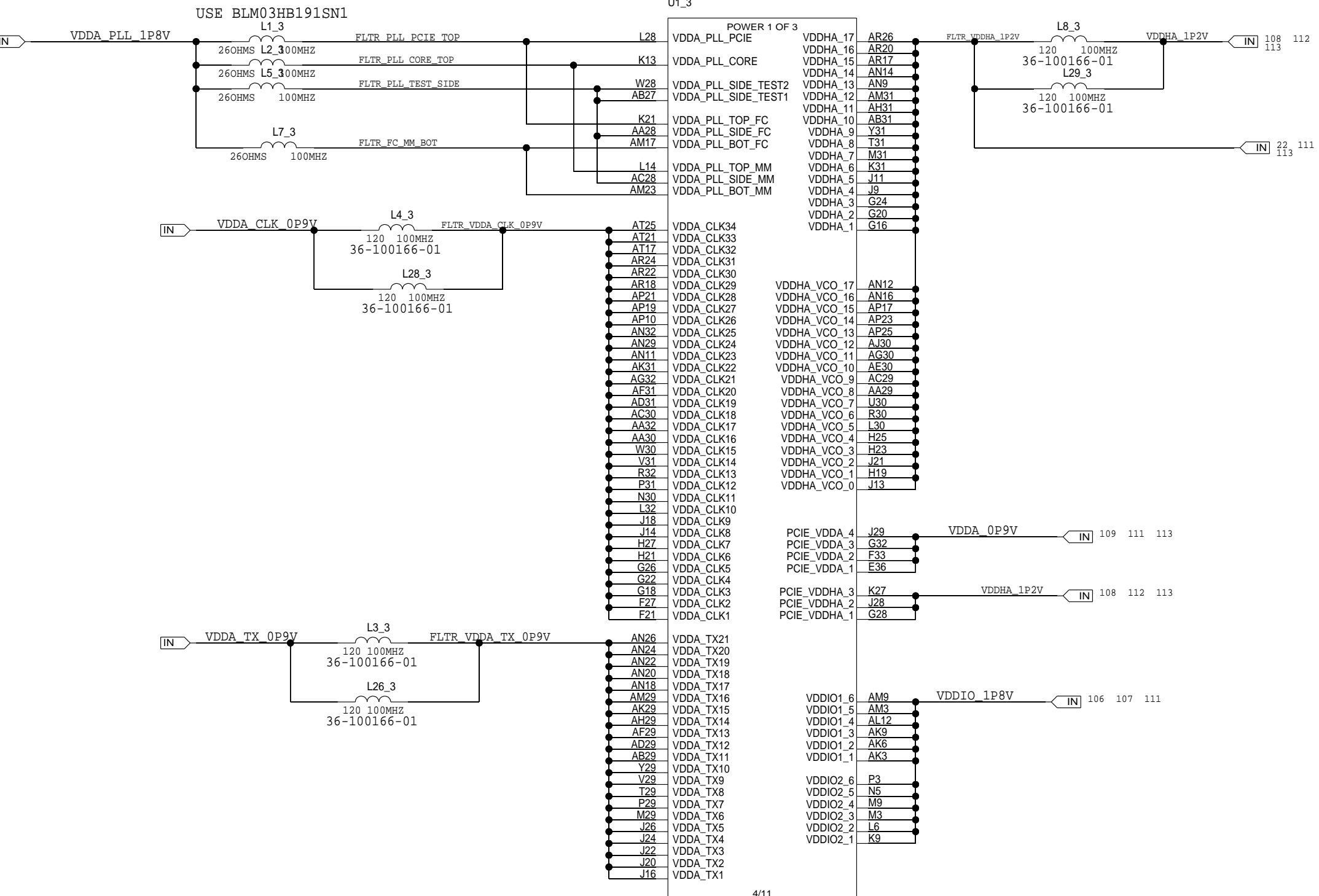
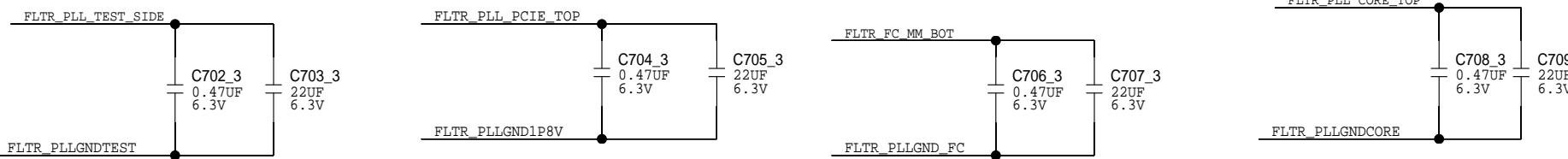
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Wed Feb 23 12:58:36 2022	107 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

1

8 7 6 5 4 3 2 1

## FILTER GROUPING PER BGA PIN LOCATION

SUNDOWN  
08-1114-01

SNDN VDDA / VDDHA



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Wed Feb 23 12:58:36 2022	REV A0

8 7 6 5 4 3 2 1

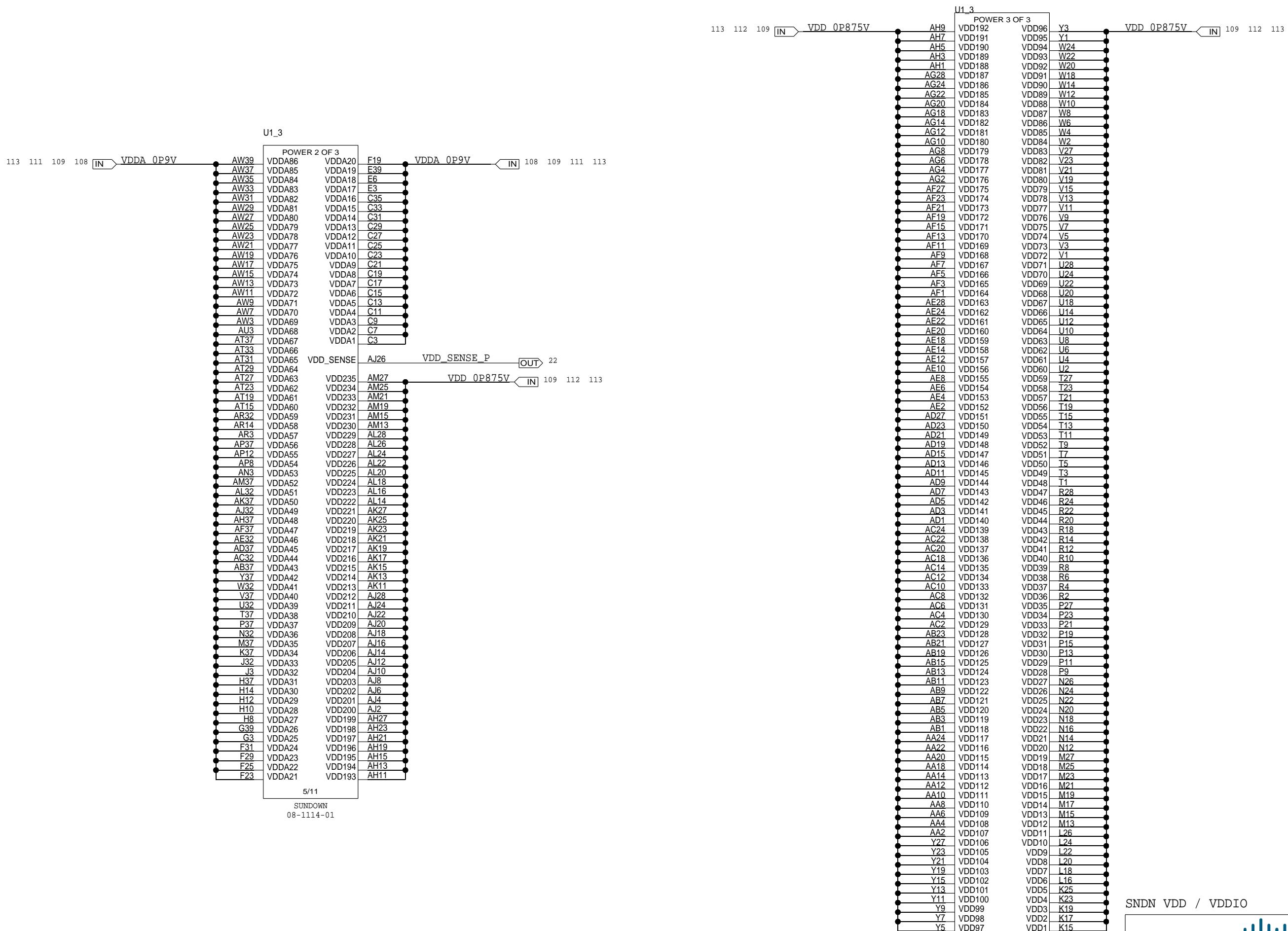
8

7

6

4

1



SNDN VDD / VDDIO



SUNDOWN  
08-1114-0

SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Fri Nov 5 16:08:51 2021		109 OF 138

D

D

C

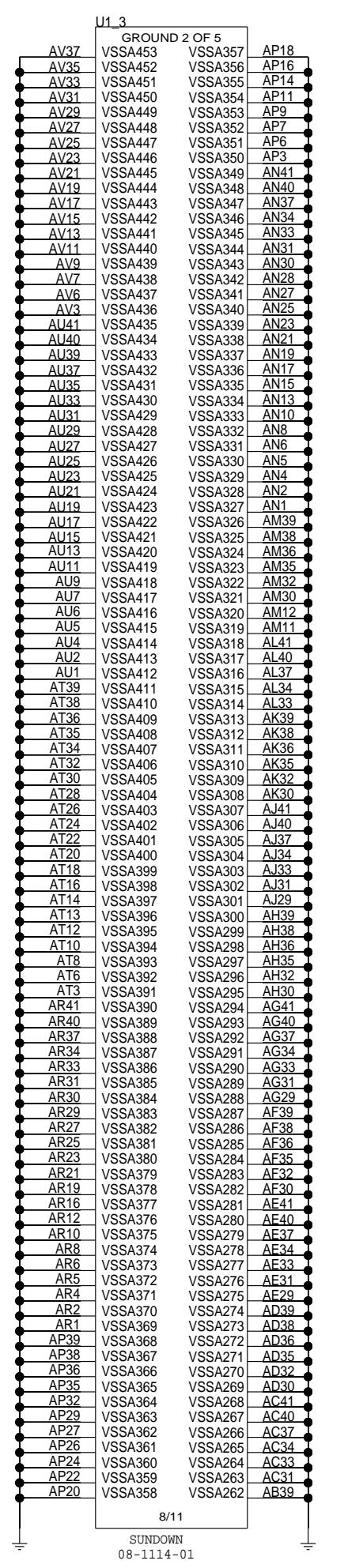
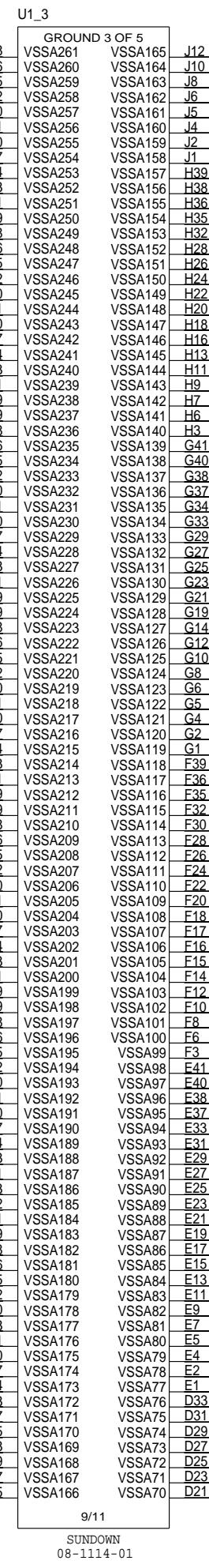
C

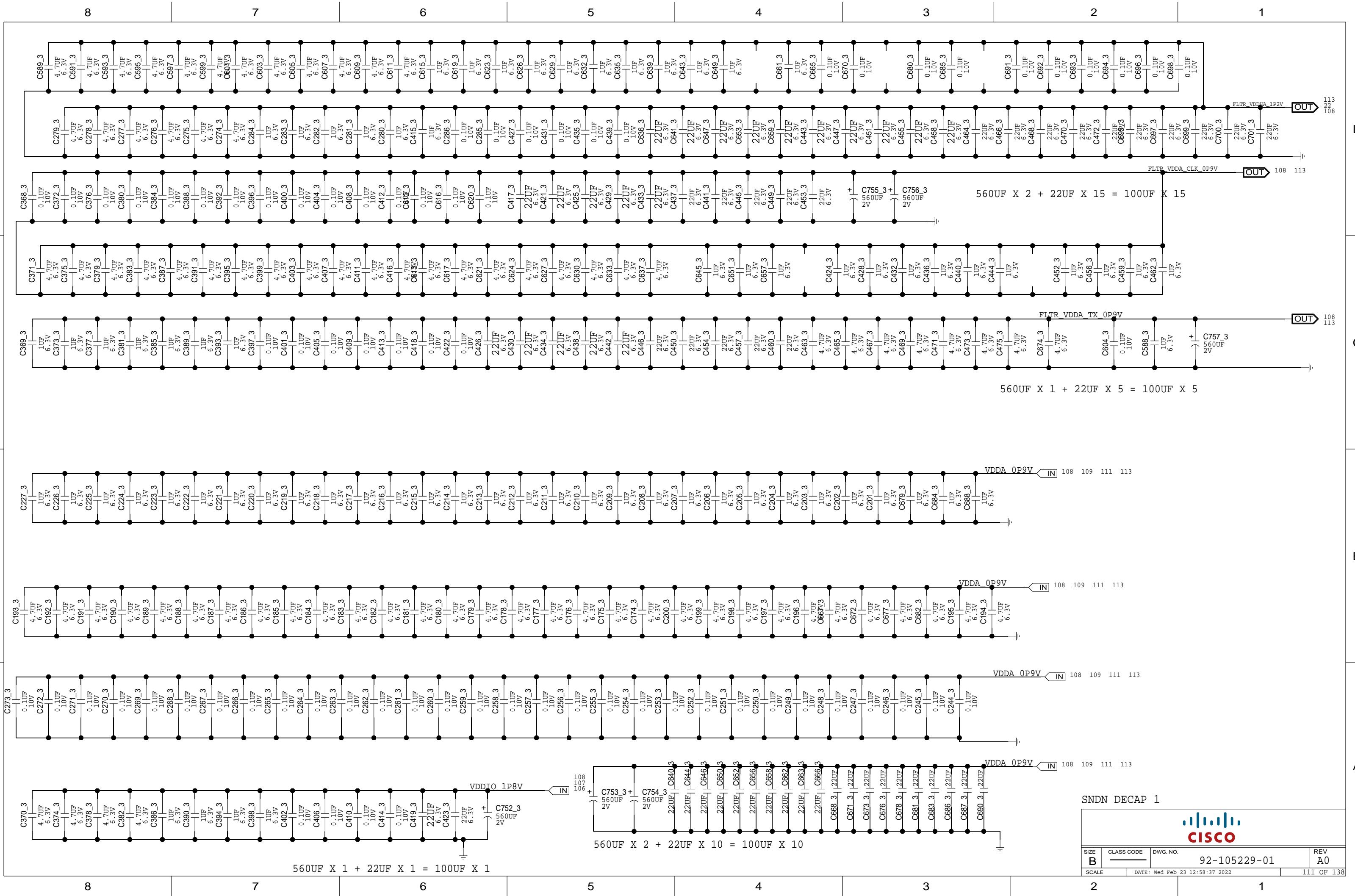
B

B

A

A





8

7

6

5

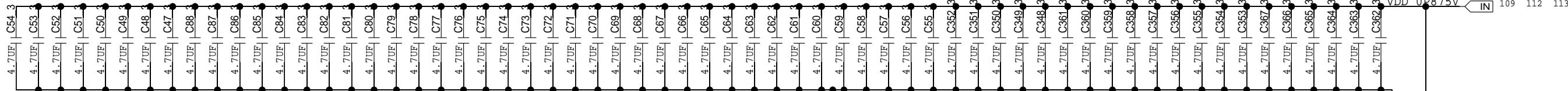
4

3

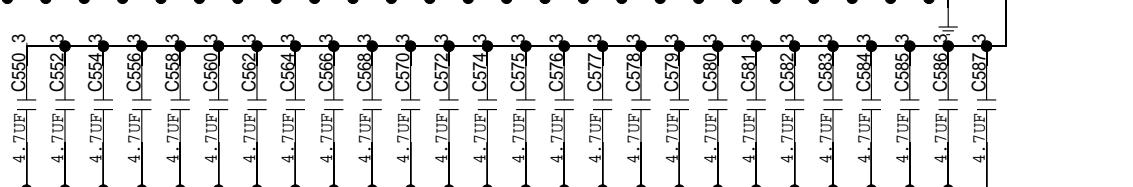
2

1

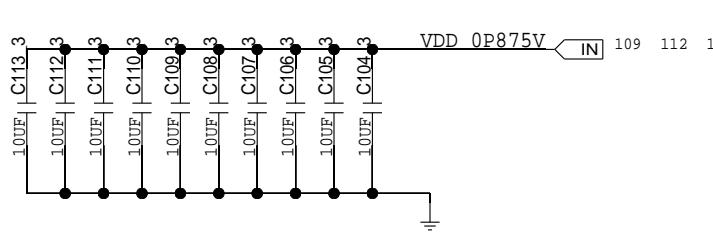
## 88 4.7UF CAPS



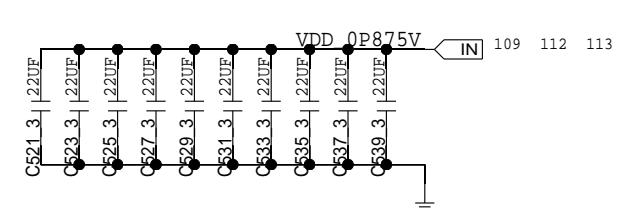
## 88 1UF CAPS



## 10 &gt;&gt; 11-3844-01 10UF CAPS

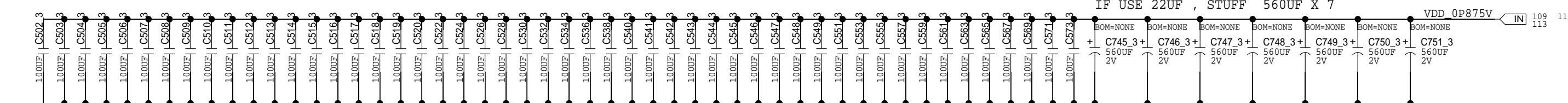


## 10 &gt;&gt; 11-2686-01 22UF CAPS



$$560\text{UF X 1} + 22\text{UF X 3} = 100\text{UF X 3}$$

## 50 &gt;&gt; 11-101311-01 100UF CAPS



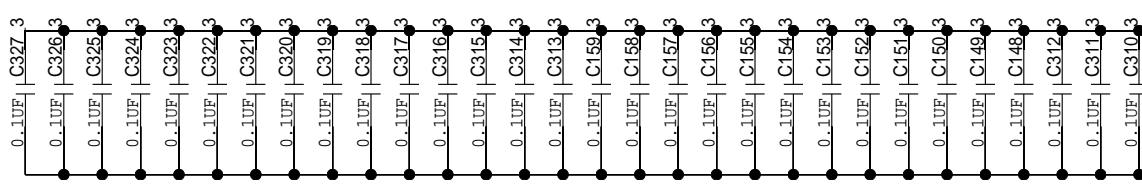
$$560\text{UF X 7} + 22\text{UF X 50} = 100\text{UF X 50}$$

IF USE 22UF , STUFF 560UF X 7

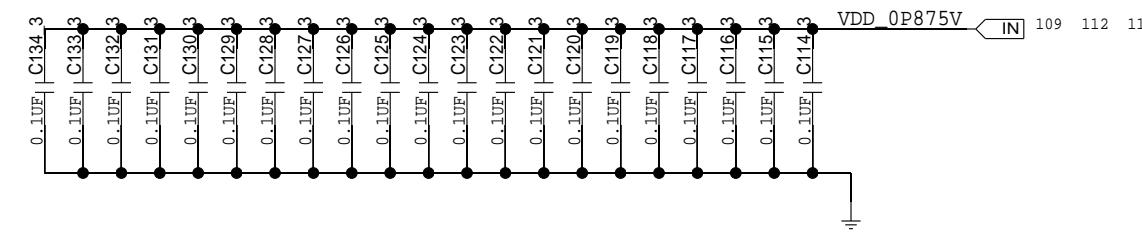
$$560\text{UF X 7} + 22\text{UF X 50} = 100\text{UF X 50}$$

BOM=NONE BOM=NONE BOM=NONE BOM=NONE BOM=NONE BOM=NONE BOM=NONE

$$C745_{3+} 560\text{UF 2V} C746_{3+} 560\text{UF 2V} C747_{3+} 560\text{UF 2V} C748_{3+} 560\text{UF 2V} C749_{3+} 560\text{UF 2V} C750_{3+} 560\text{UF 2V} C751_{3+} 560\text{UF 2V}$$



## 88 &gt;&gt; 11-2330-02 0.1UF CAPS



## SNDN DECAP 2



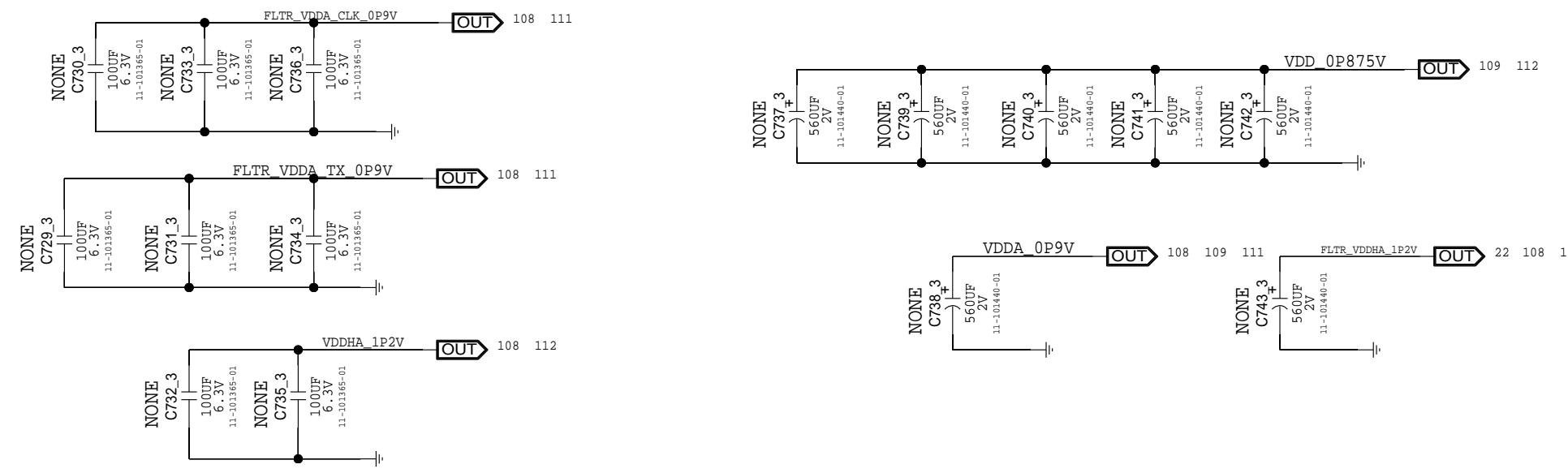
SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Wed Feb 23 12:58:38 2022	REV A0
		112 OF 138

8 7 6 5 4 3 2 1

D

D

# 0805 100UF CAP MIDIGATION ADDITIONS



C

C

B

B

A

A

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:38 2022		113 OF 138

8 7 6 5 4 3 2 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

C

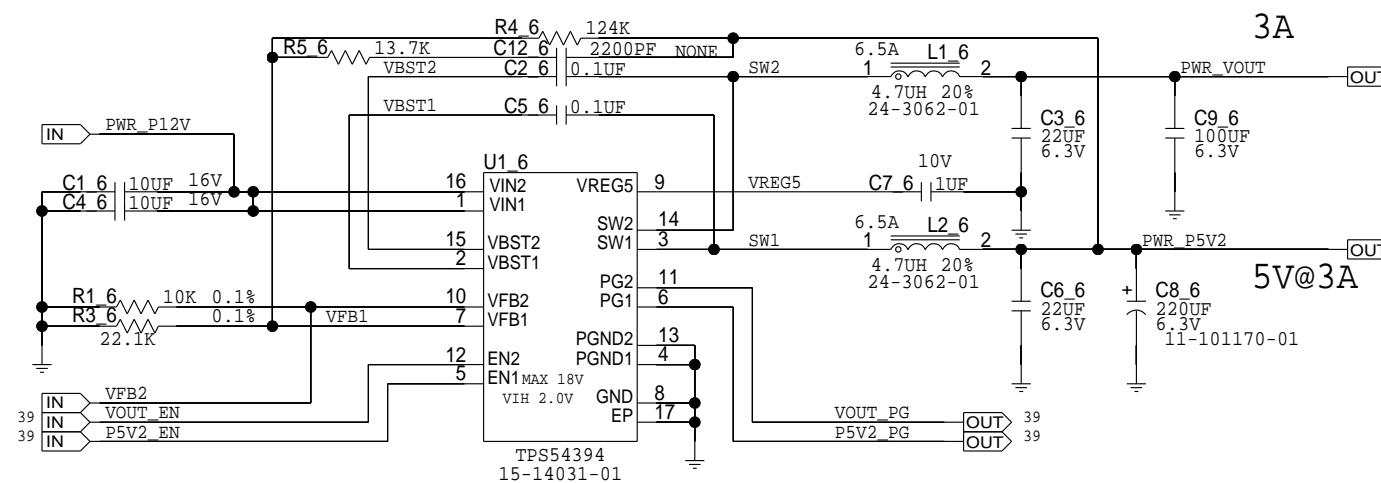
B

B

A

A

## 5.2V & VARIABLE VOLTAGE REGULATORS



CONTROLLER

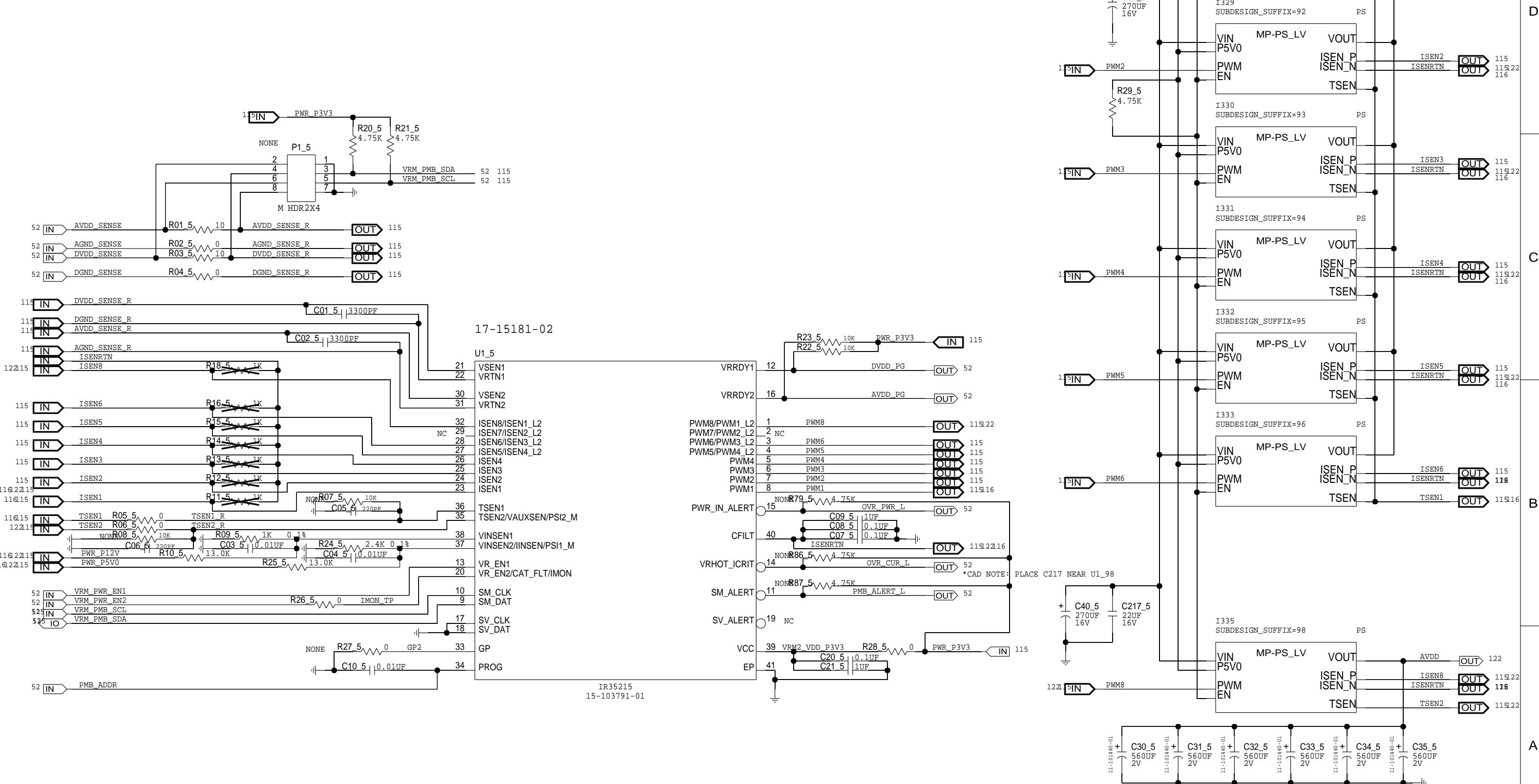


SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:43 2022		114 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# ACADIA MULTI-PHASE 6+1 POWER STAGE MACRO

NOTE: SELECT INFINEON, FAIRCHILD OR TI IN THE VARIANT



CISCO

SIZE	CLASS CODE	DWG. NO.
B		92-105229-01

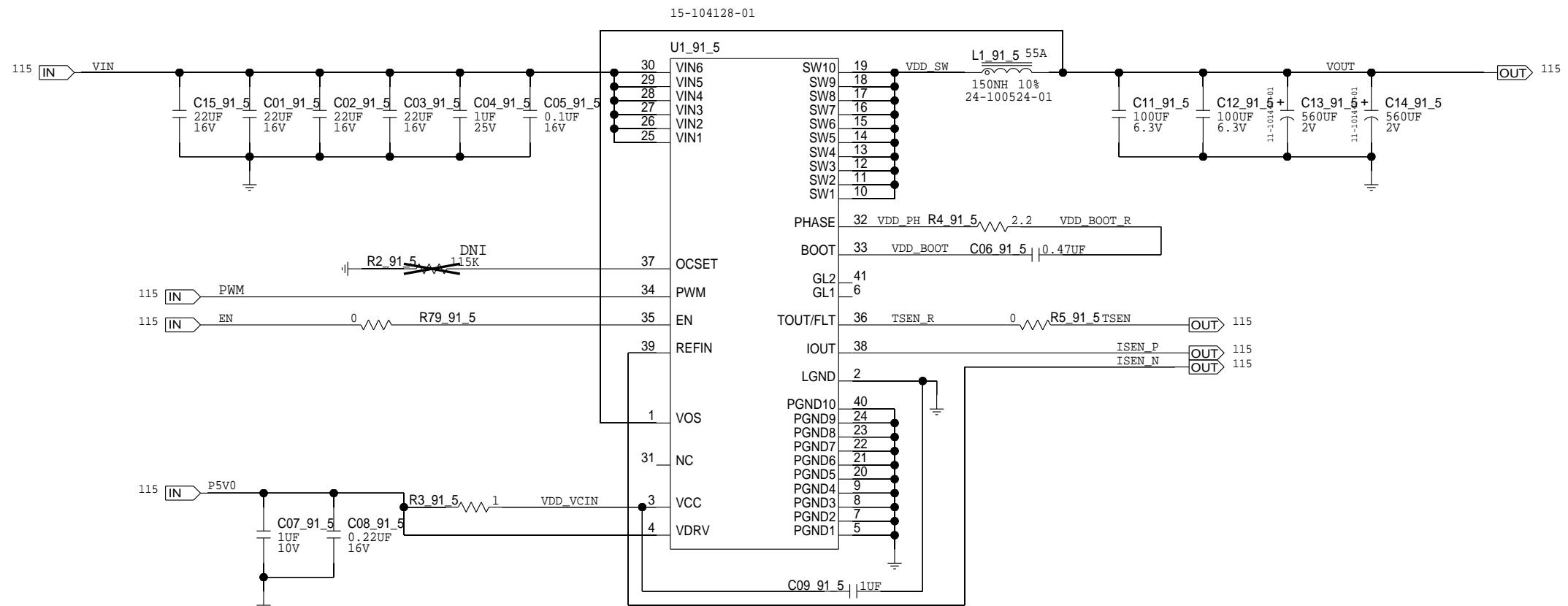
REV A0

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE:	Wed Feb 23 12:58:34 2022	116 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

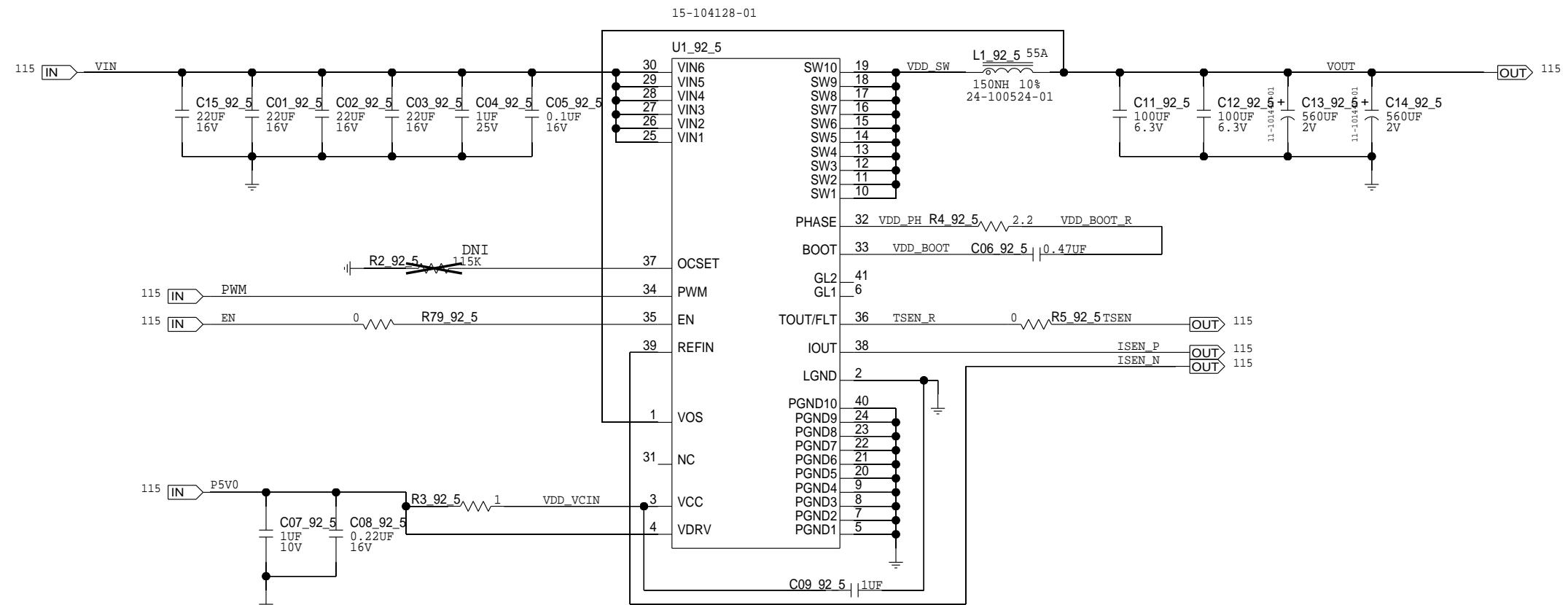
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE:	Wed Feb 23 12:58:34 2022	117 OF 138

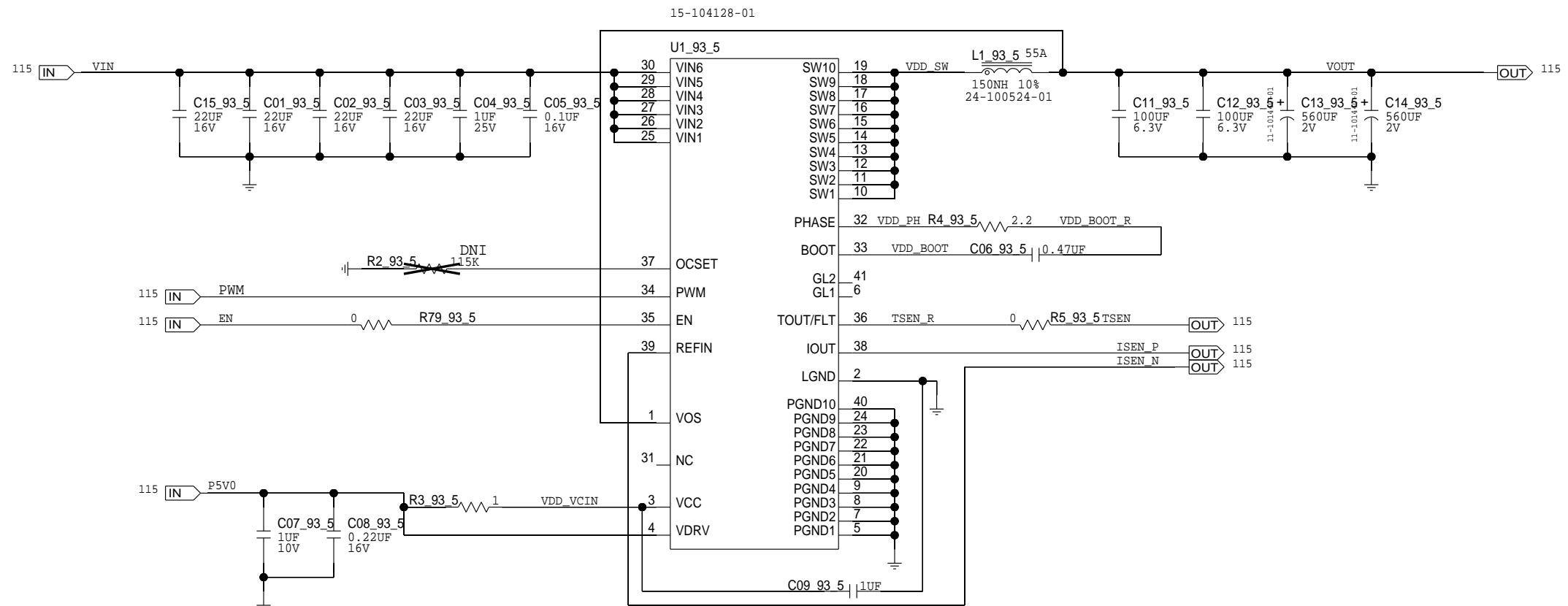
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022		118 OF 138

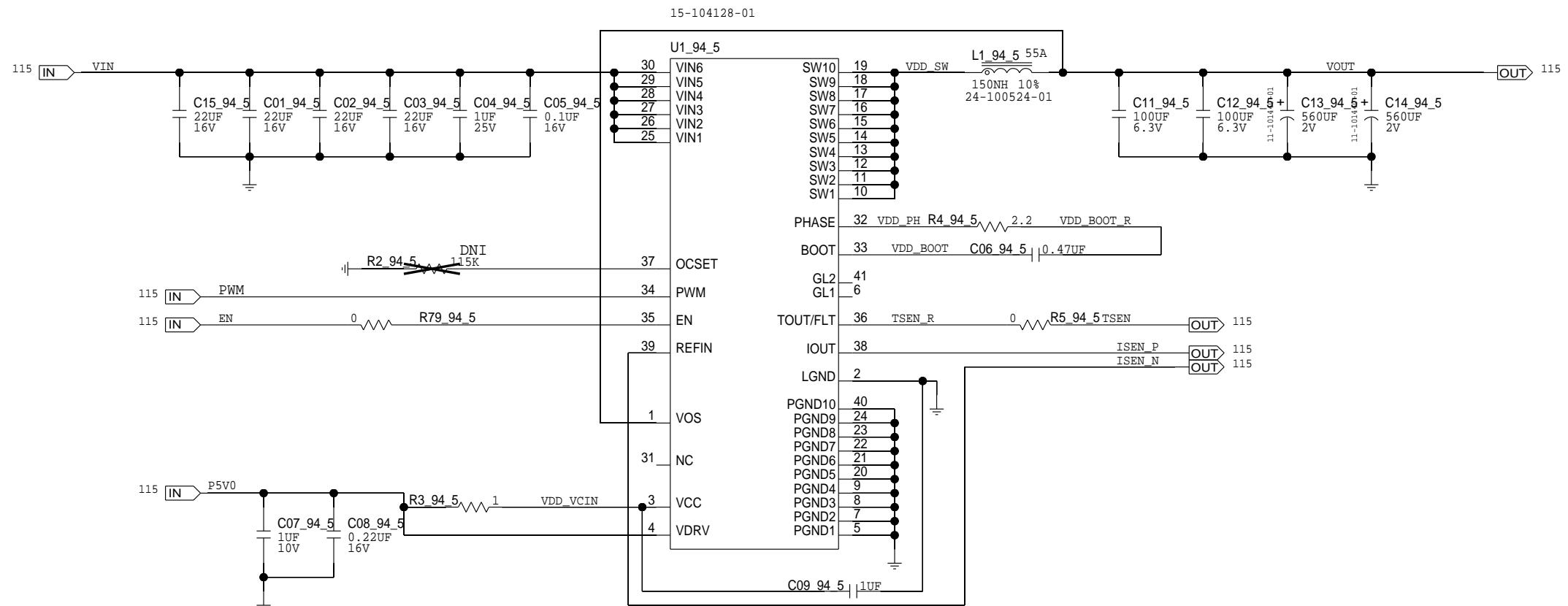
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE:	Wed Feb 23 12:58:34 2022	119 OF 138

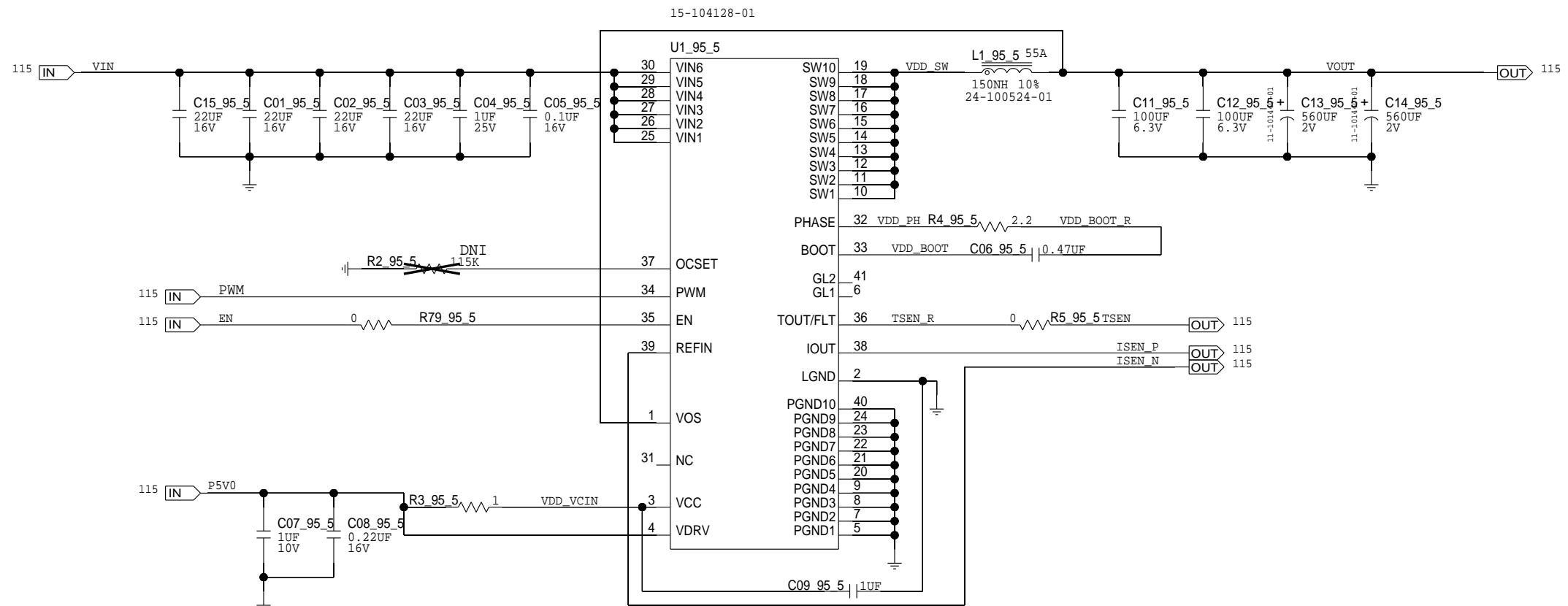
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



C

C

B

B

A

A

MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE:	Wed Feb 23 12:58:34 2022	120 OF 138

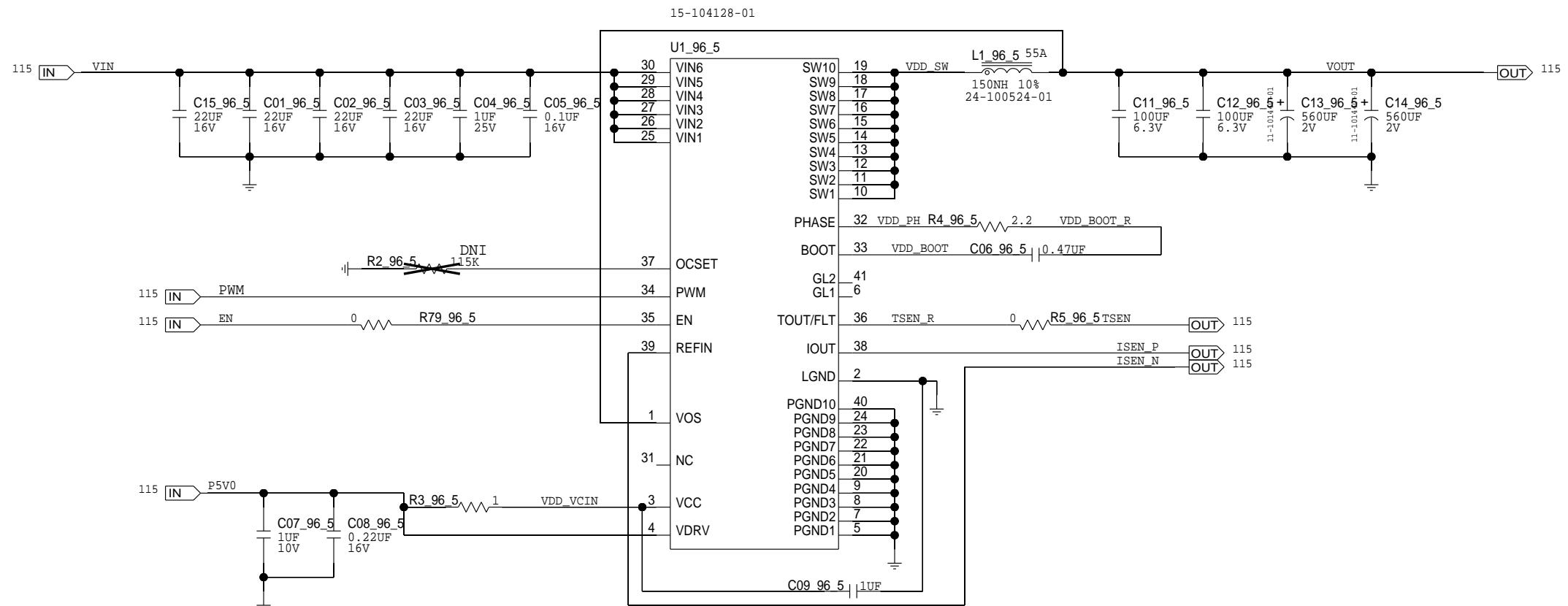
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



C

C

B

B

A

A

MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022		121 OF 138

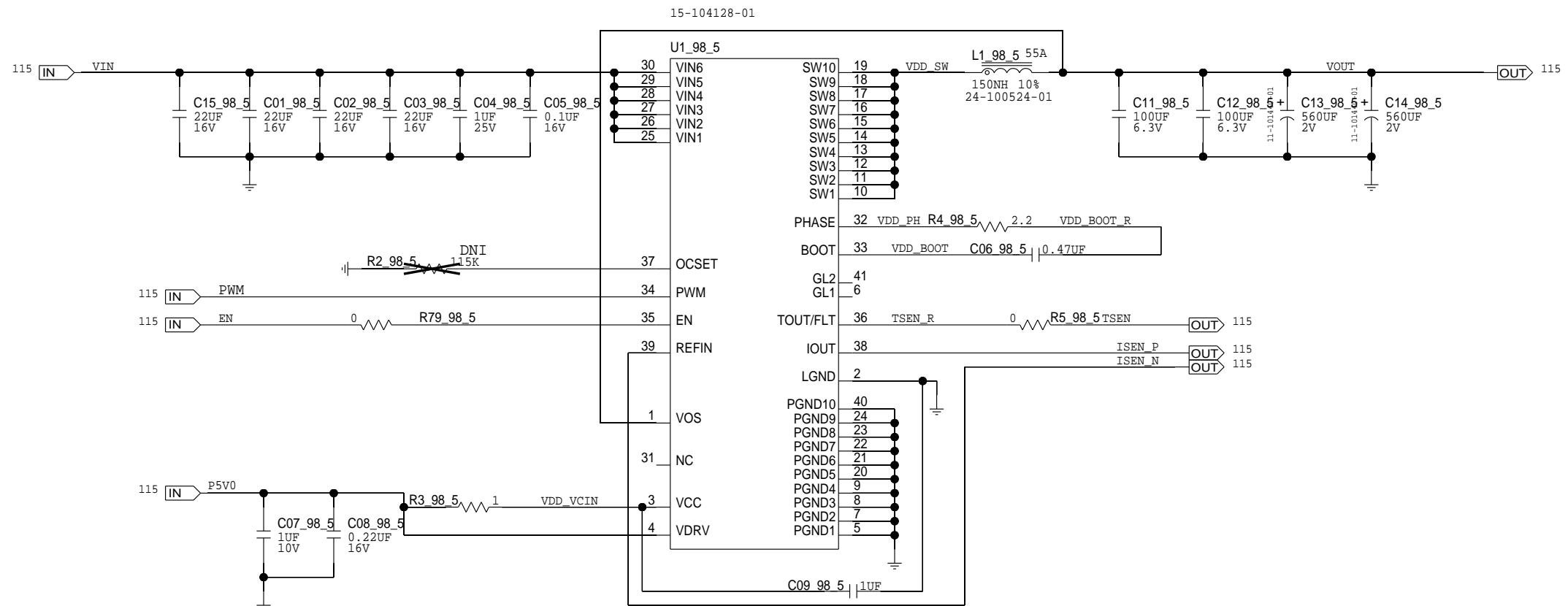
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



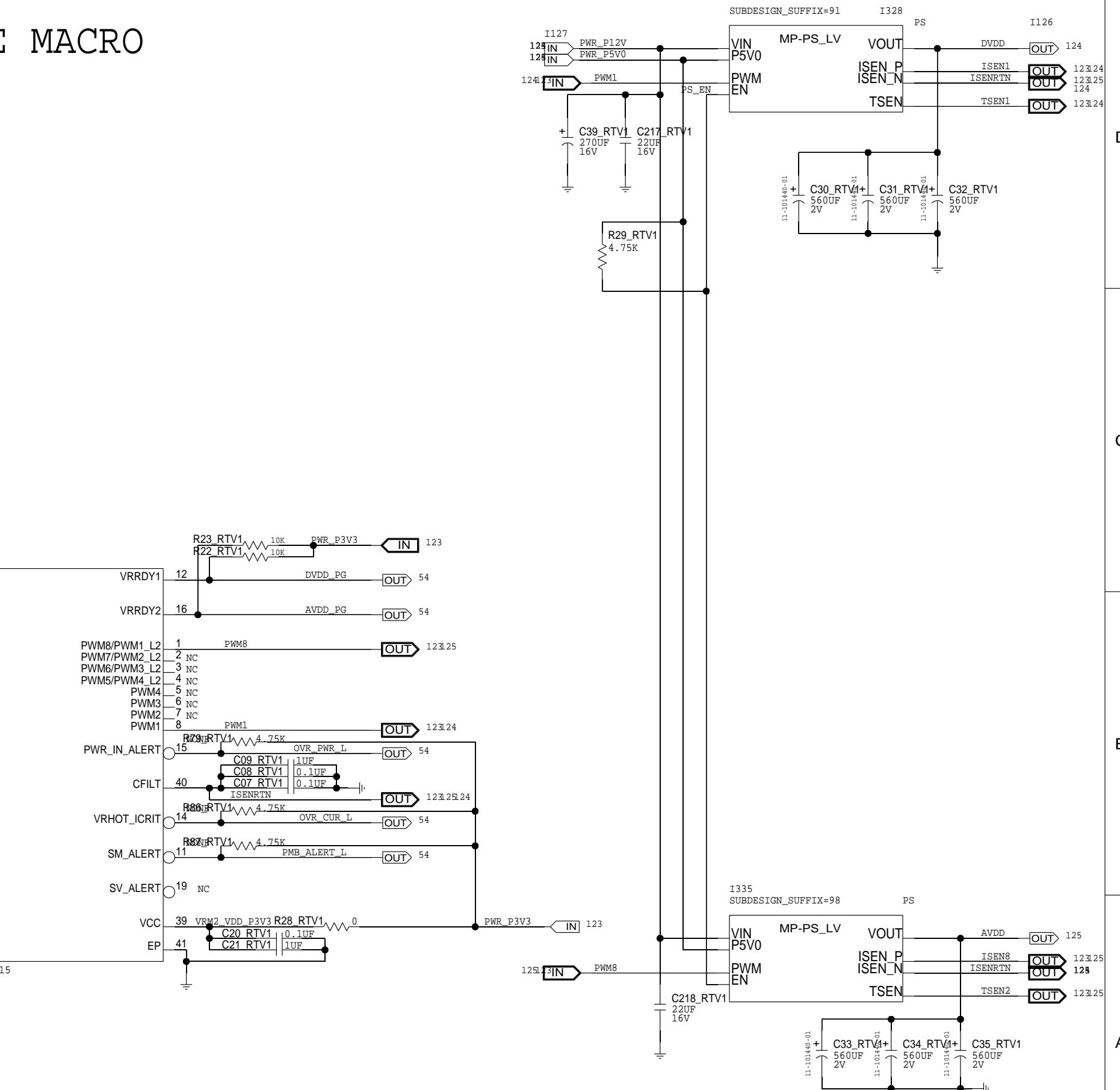
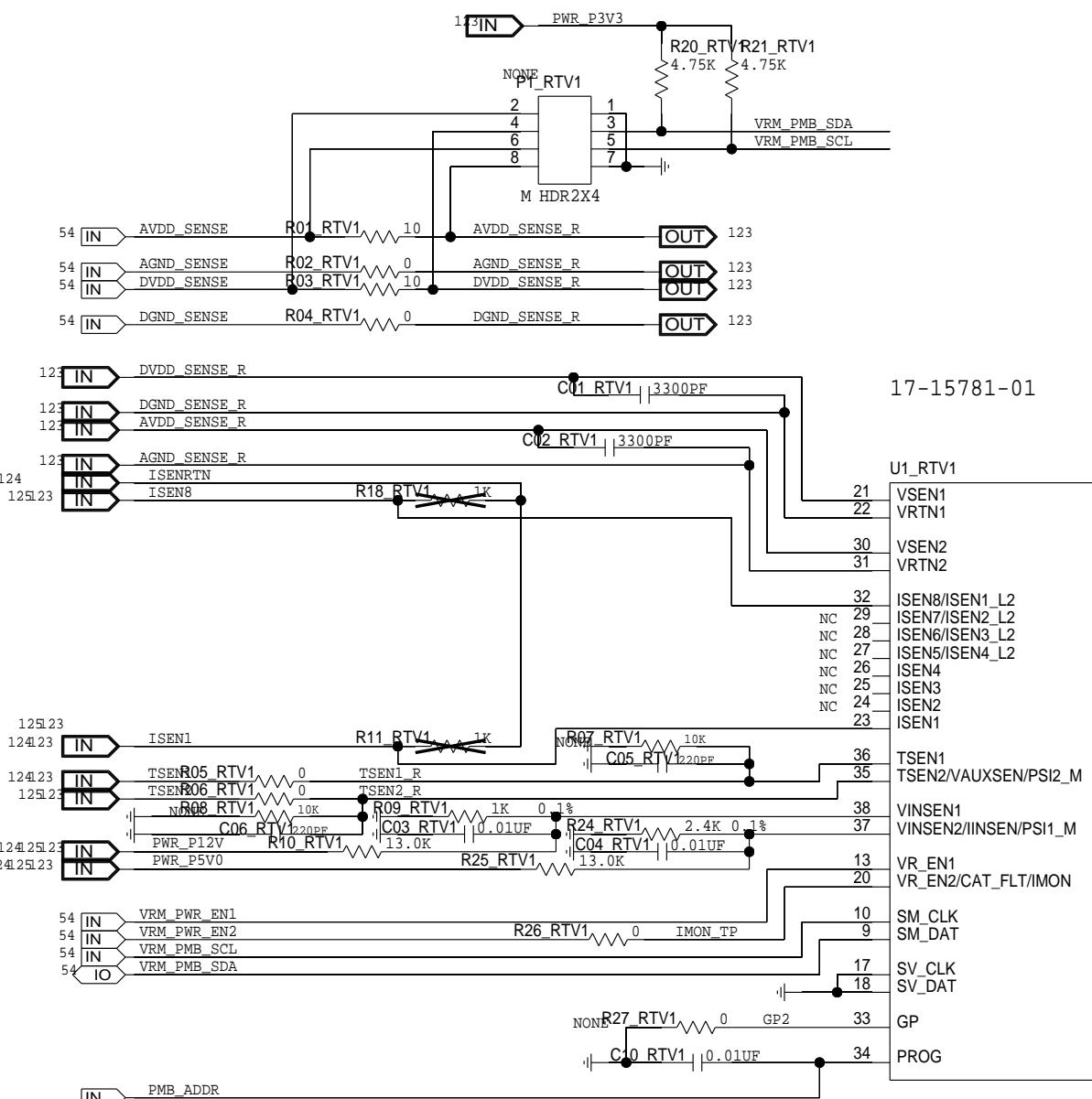
SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022		122 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# ACADIA MULTI-PHASE 1+1 POWER STAGE MACRO

NOTE:SELECT INFINEON,FAIRCHILD OR TI IN THE VARIANT

PLACE C217,C218 CLOSE TO EACH POWER STAGE

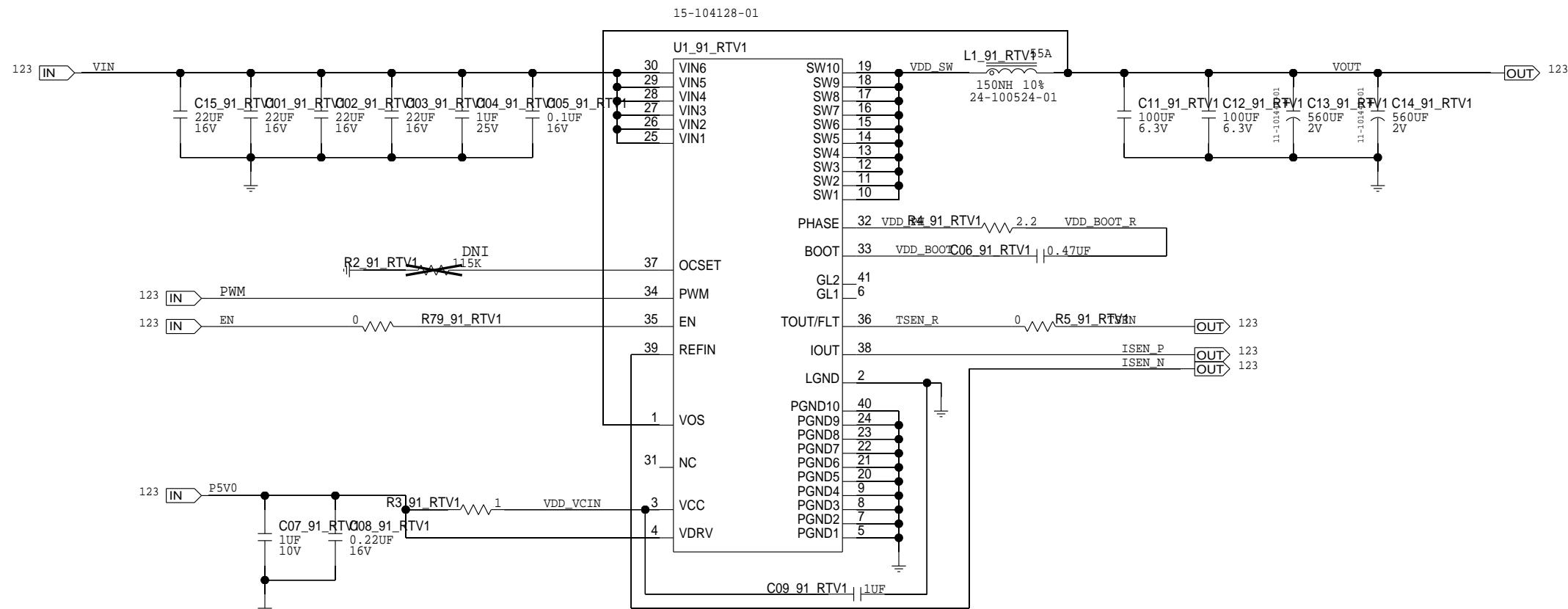


8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



A

A

MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022	124 OF 138	

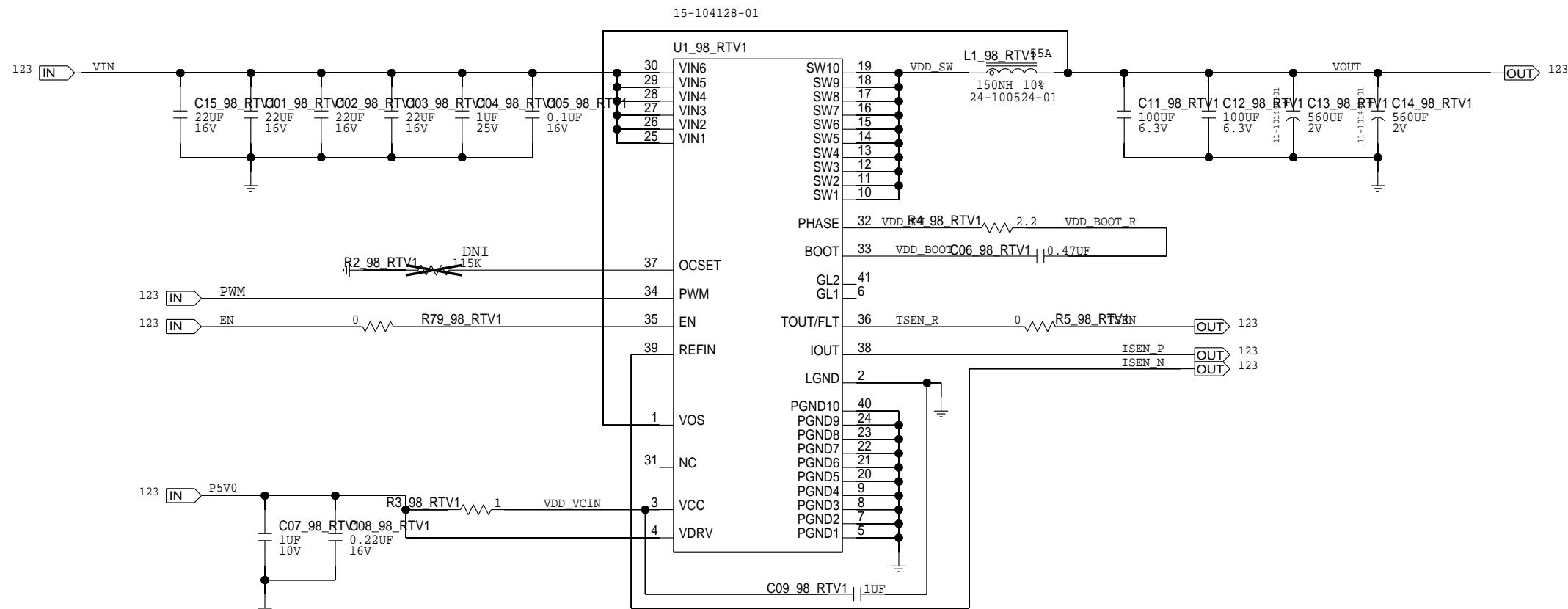
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022		125 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

8

7

6

5

4

3

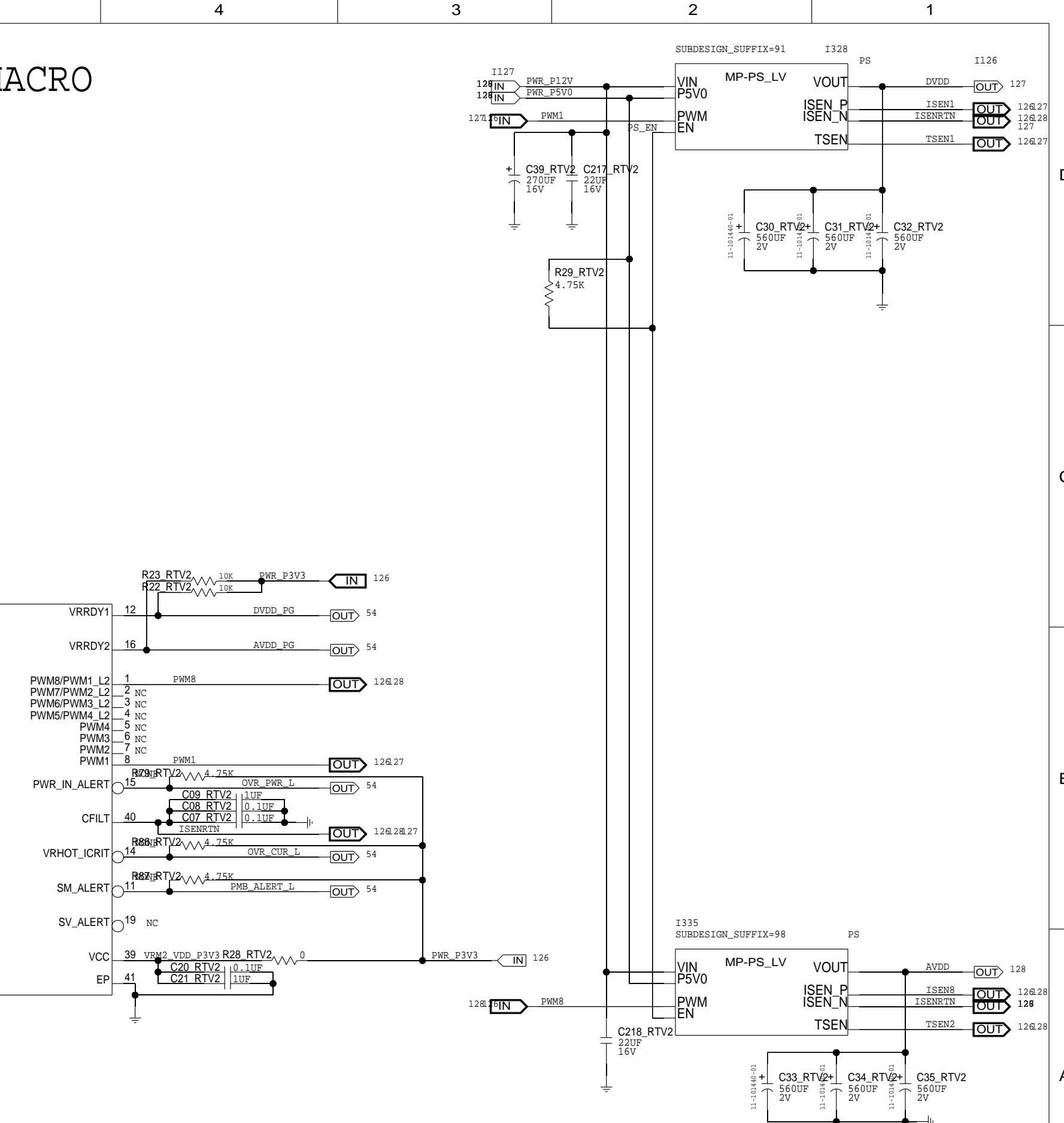
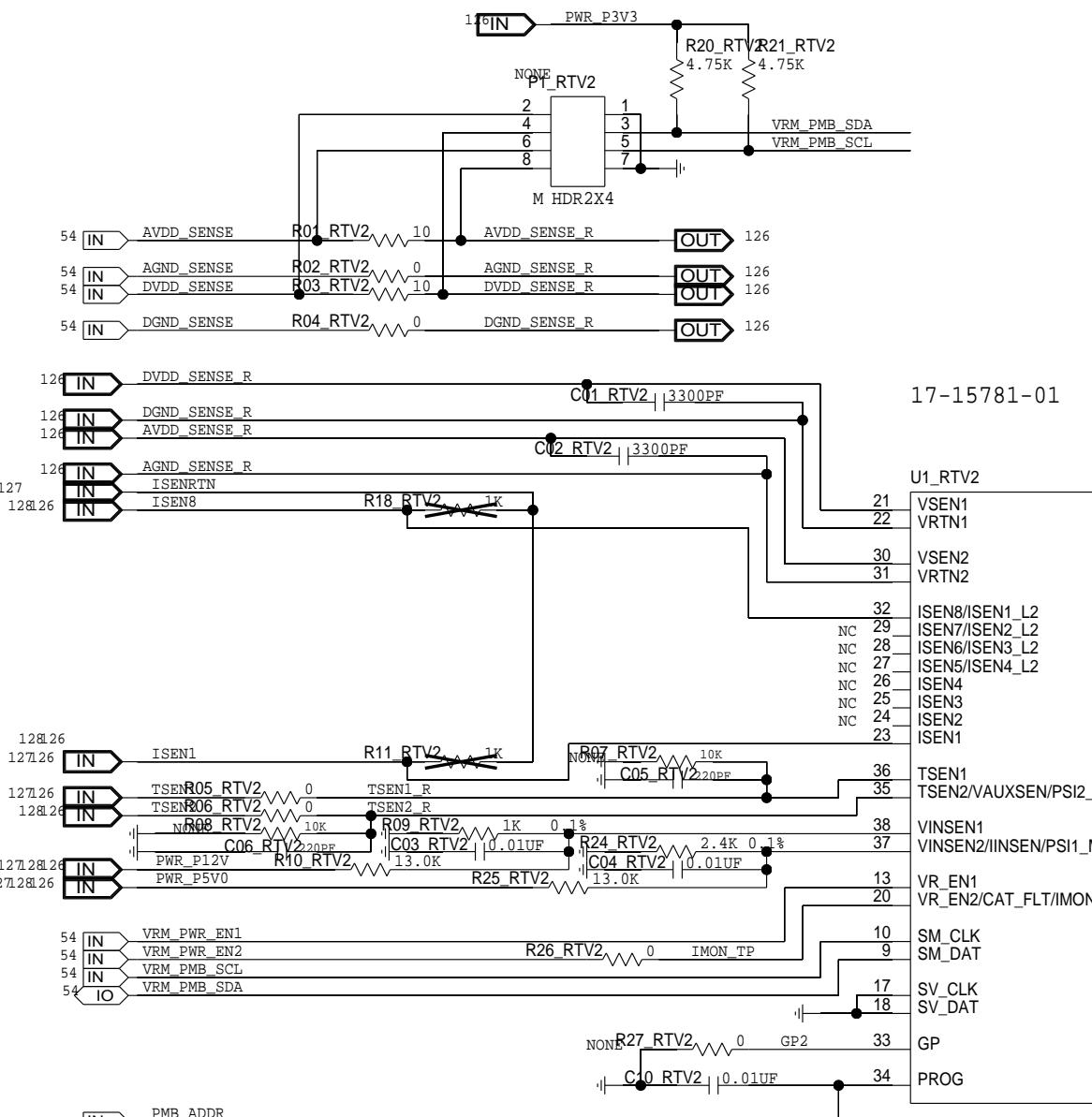
2

1

# ACADIA MULTI-PHASE 1+1 POWER STAGE MACRO

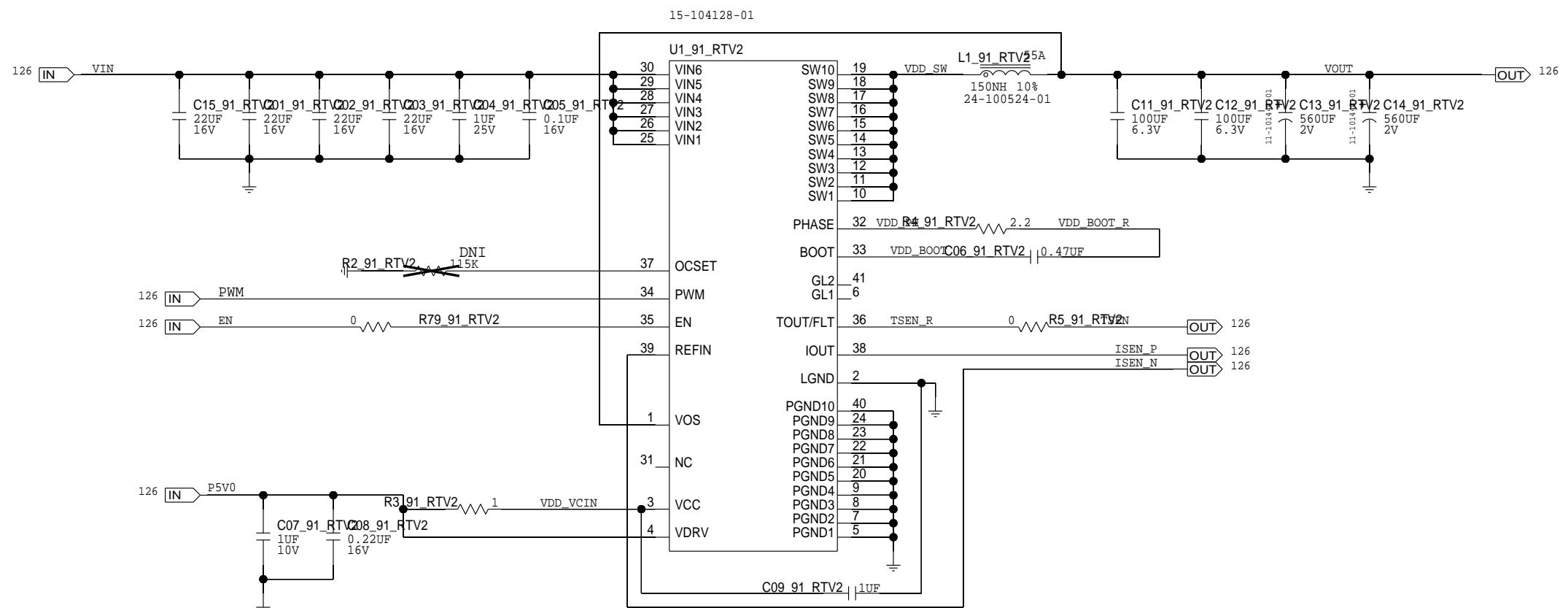
NOTE: SELECT INFINEON, FAIRCHILD OR TI IN THE VARIANT

PLACE C217, C218 CLOSE TO EACH POWER STAGE



8                    7                    6                    5                    4                    3                    2                    1

# INFINEON POWER STAGE\_LV



## MULTI-PHASE POWER STAGE



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Wed Feb 23 12:58:34 2022	127	OF 138

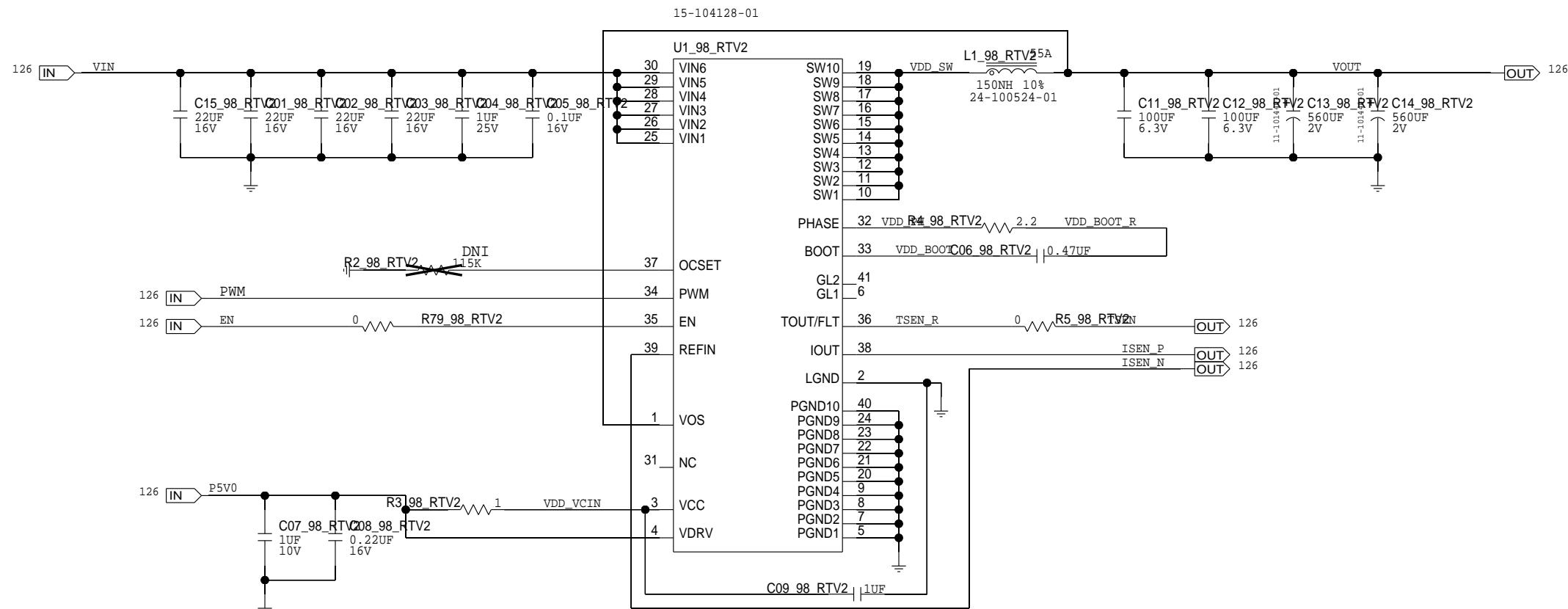
8                    7                    6                    5                    4                    3                    2                    1

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

# INFINEON POWER STAGE\_LV



C

C

B

B

A

A

MULTI-PHASE POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B	_____	92-105229-01	A0
SCALE	DATE: Wed Feb 23 12:58:34 2022		128 OF 138

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

## VISHAY SIC450 AND ONSEMI FAN251030 2.5V-3.3V/30A DUAL BOM VR



## VOUT SET RESISTOR

ONSEMI	VSET Resistor Value (kΩ)	V <sub>out</sub> preset value (V)
	Short	0.6
0.845		0.6
1.3		0.9
1.78		0.95
2.32		1.00
2.87		1.05
3.48		1.2
4.12		1.25
4.75		1.5
5.49		1.8
6.19		2.1
6.98		2.5
7.87		3.3
8.87		5
10 & greater value		0.8

OUTPUT VOLTAGE SETTINGS	
V <sub>SET</sub> RESISTOR (kΩ)	V <sub>out</sub> (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

## BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H) Table 1. PMBUS™ ADDRESS SETTING		
ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10K	0D	Base+0D

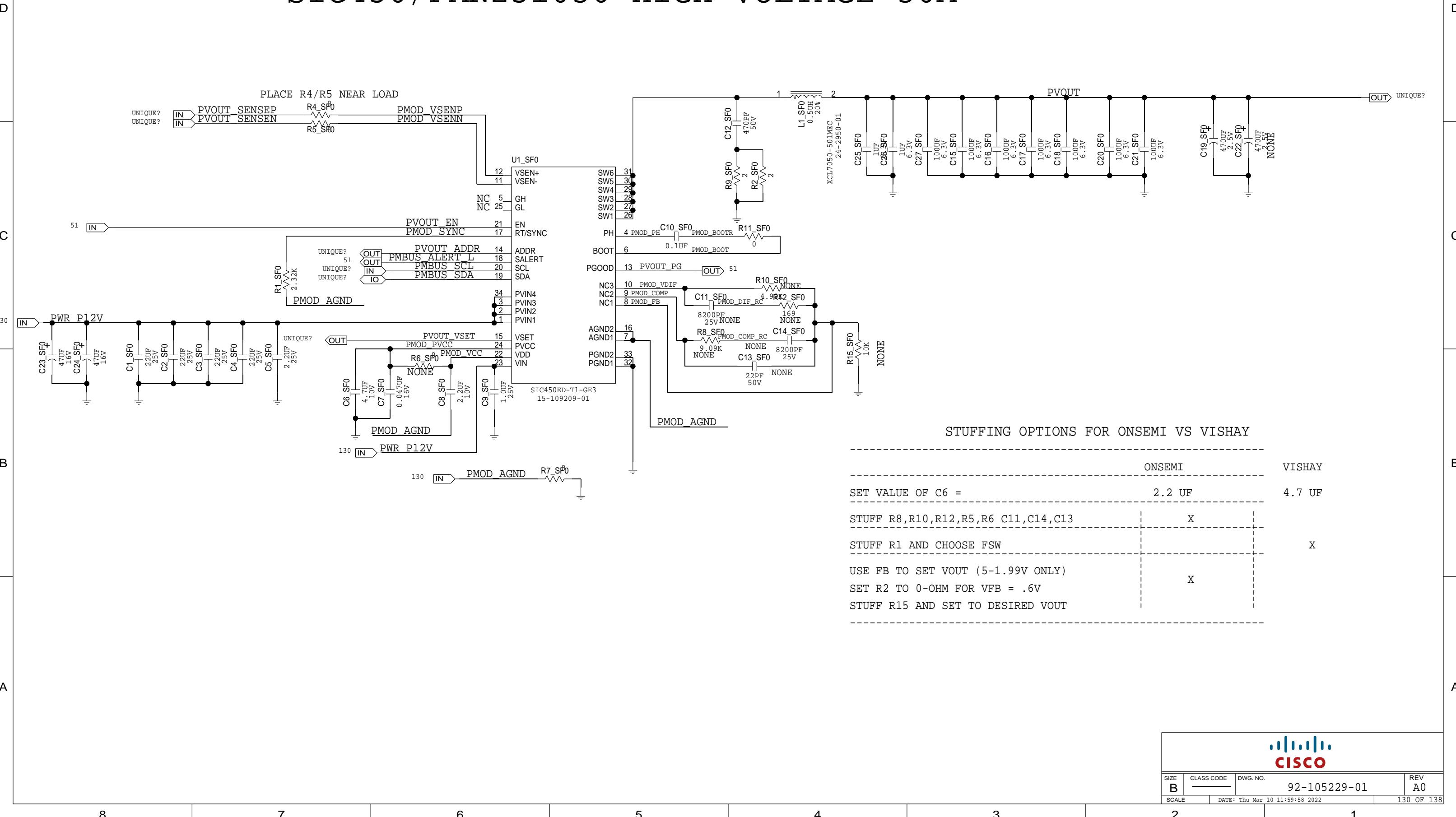
VISHAY (REGISTER D7H, DEFAULT 10H) MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H) MFR_BASE_ADDRESS 2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845	1	0	101b	1010 000b
1.30	2	1	101b	1010 001b
1.78	3	2	101b	1010 010b
2.32	4	3	101b	1010 011b
2.87	5	4	101b	1010 100b
3.48	6	5	101b	1010 101b
4.12	7	6	101b	1010 110b
4.75	8	7	101b	1010 111b
5.49	9	8	101b	1011 000b
6.19	10	9	101b	1011 001b
6.98	11	A	101b	1011 010b
7.87	12	B	101b	1011 011b
8.87	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

FREQ SET RESISTOR(VISHAY ONLY)		
FREQUENCY SETTINGS	RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845		300
1.30		400
1.78		500
2.32		550
2.87		600
3.48		650
4.12		700
4.75		750
5.49		800
6.19		850
6.98		900
7.87		950
8.87		1000
10K		1250
11K		1500

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# SIC450/FAN251030 HIGH VOLTAGE 30A



SIZE	CLASS CODE	DWG. NO.
B		92-105229-01
SCALE	DATE: Thu Mar 10 11:59:58 2022	REV A0

130 OF 138

## VISHAY SIC450 AND ONSEMI FAN251030 2.5V-3.3V/30A DUAL BOM VR



## VOUT SET RESISTOR

ONSEMI	VSET Resistor Value (kΩ)	V <sub>out</sub> preset value (V)
	Short	0.6
0.845		0.6
1.3		0.9
1.78		0.95
2.32		1.00
2.87		1.05
3.48		1.2
4.12		1.25
4.75		1.5
5.49		1.8
6.19		2.1
6.98		2.5
7.87		3.3
8.87		5
10 & greater value		0.8

## VISHAY

OUTPUT VOLTAGE SETTINGS	
V <sub>SET</sub> RESISTOR (kΩ)	V <sub>out</sub> (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

## BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)  
Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10K	0D	Base+0D
11K	0E	Base+0E

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS 2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

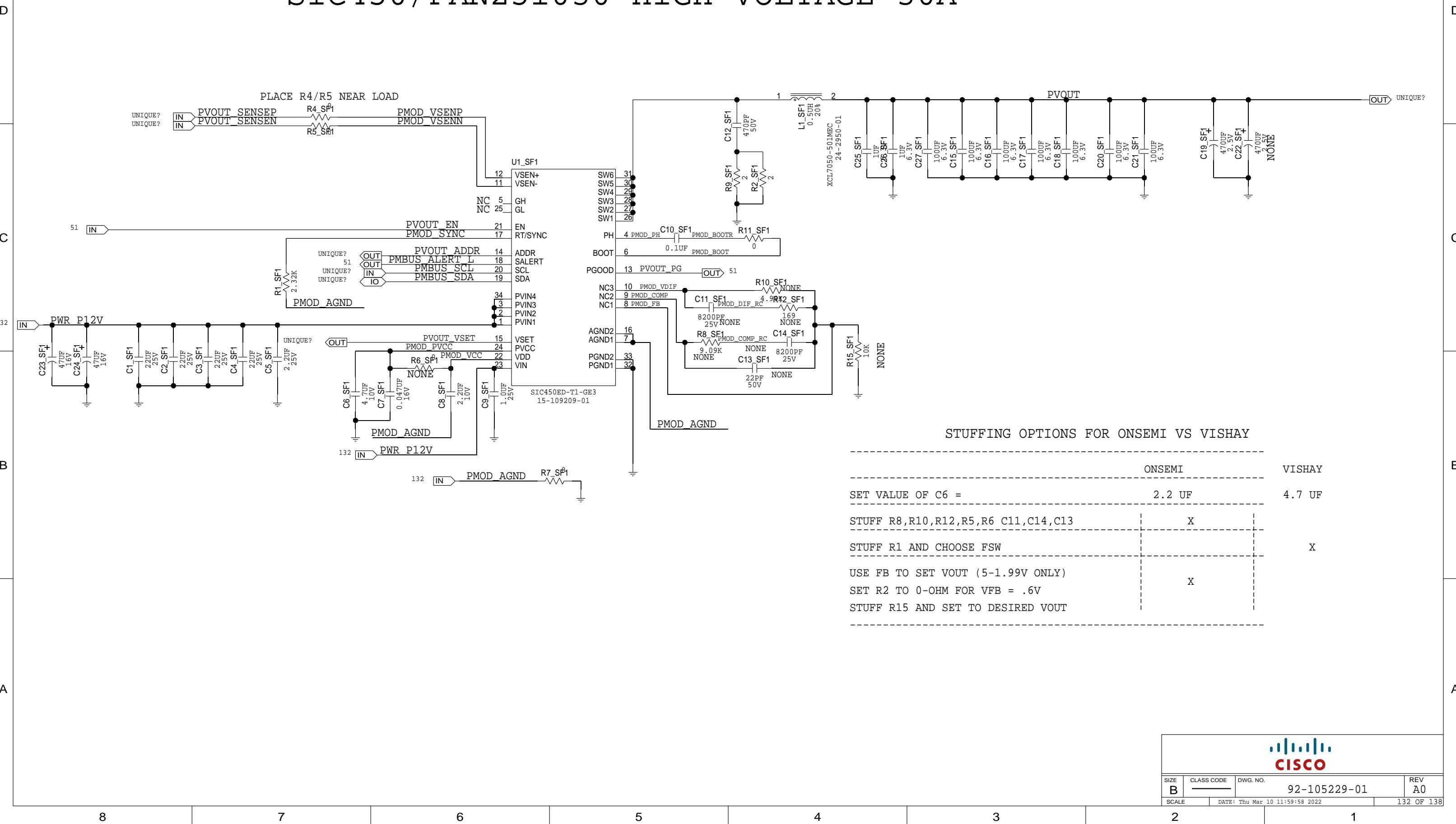
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10K	1250
11K	1500

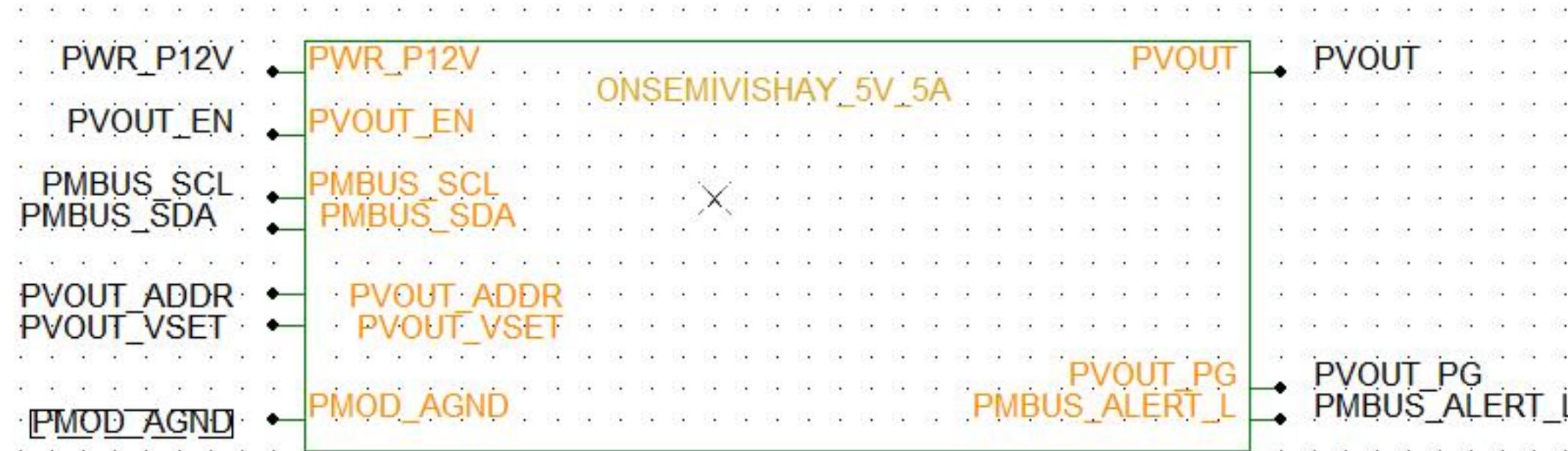


8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# SIC450/FAN251030 HIGH VOLTAGE 30A



# ONSEMI FAN25015 AND VISHAY SIC453 5V, 5A DUAL BOM VR



## VOUT SET RESISTOR

ONSEMI	
VSET Resistor Value (kΩ)	V <sub>out</sub> preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY	
OUTPUT VOLTAGE SETTINGS	
V <sub>SET</sub> RESISTOR (kΩ)	V <sub>out</sub> (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

## BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)  
Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10K	0D	Base+0D
11K	0E	Base+0E

VISHAY(REGISTER D7H, DEFAULT 10H)

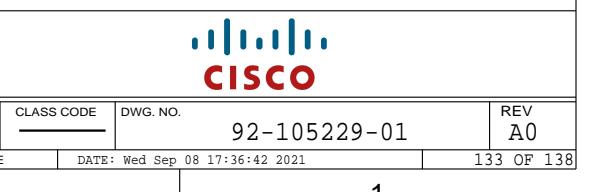
MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

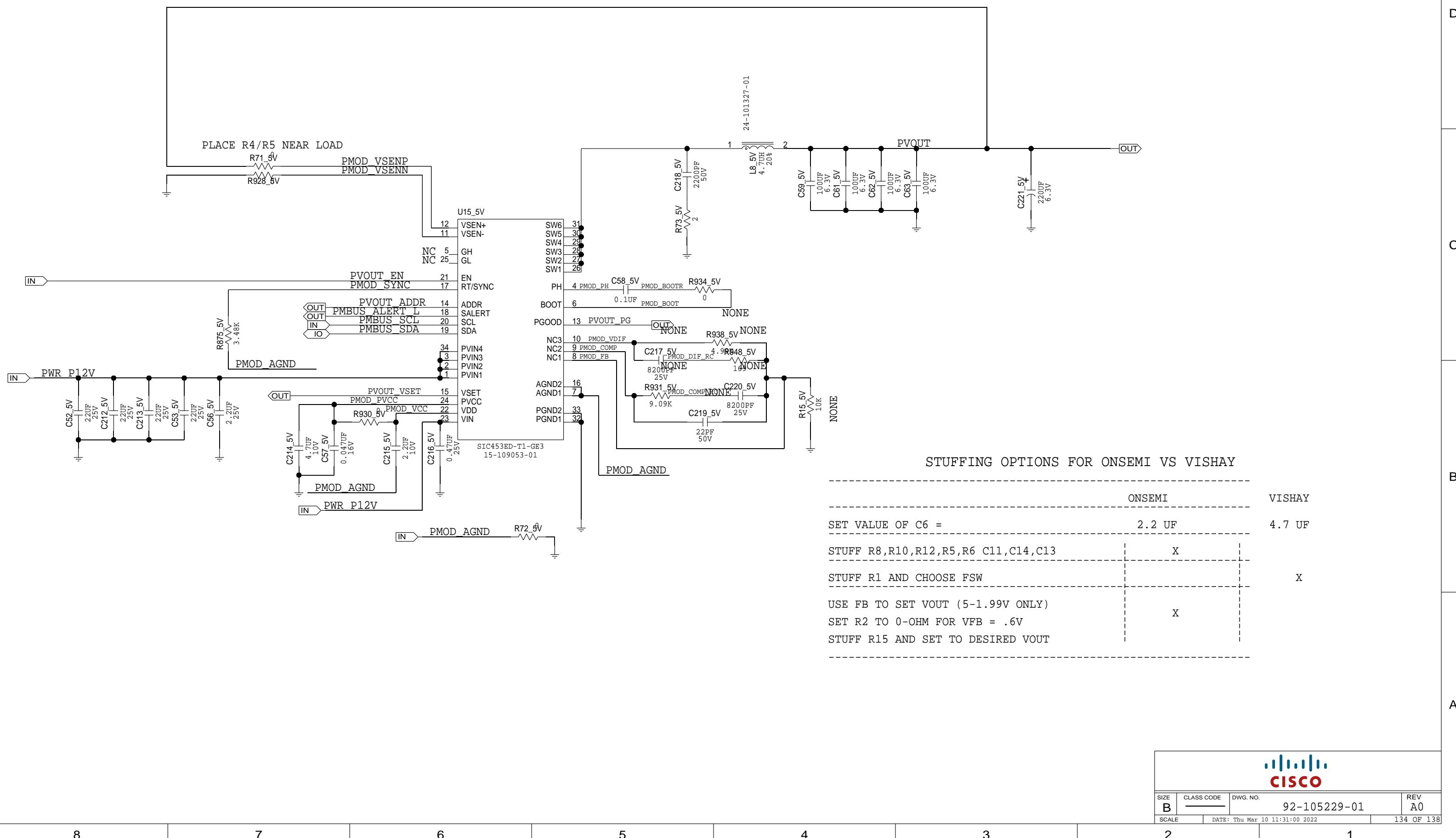
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10K	1250
11K	1500



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# FAN251015/SIC453 5V, 5A



8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

## ONSEMI FAN25015 AND VISHAY SIC453 2.5-3.3V/9A DUAL BOM VR



## VOUT SET RESISTOR

ONSEMI	
VSET Resistor Value (kΩ)	V <sub>out</sub> preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY	
OUTPUT VOLTAGE SETTINGS	
V <sub>SET</sub> RESISTOR (kΩ)	V <sub>out</sub> (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

ONSEMI (REGISTER C9H, DEFAULT 40H)  
Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10K	0D	Base+0D
11K	0E	Base+0E

## BASE ADDRESS OFFSET RESISTOR

VISHAY(REGISTER D7H, DEFAULT 10H)

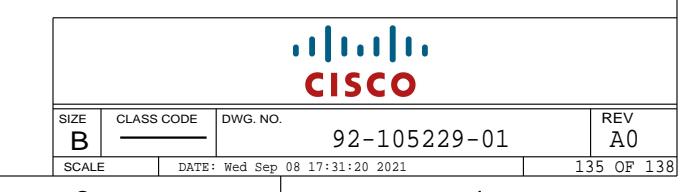
MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

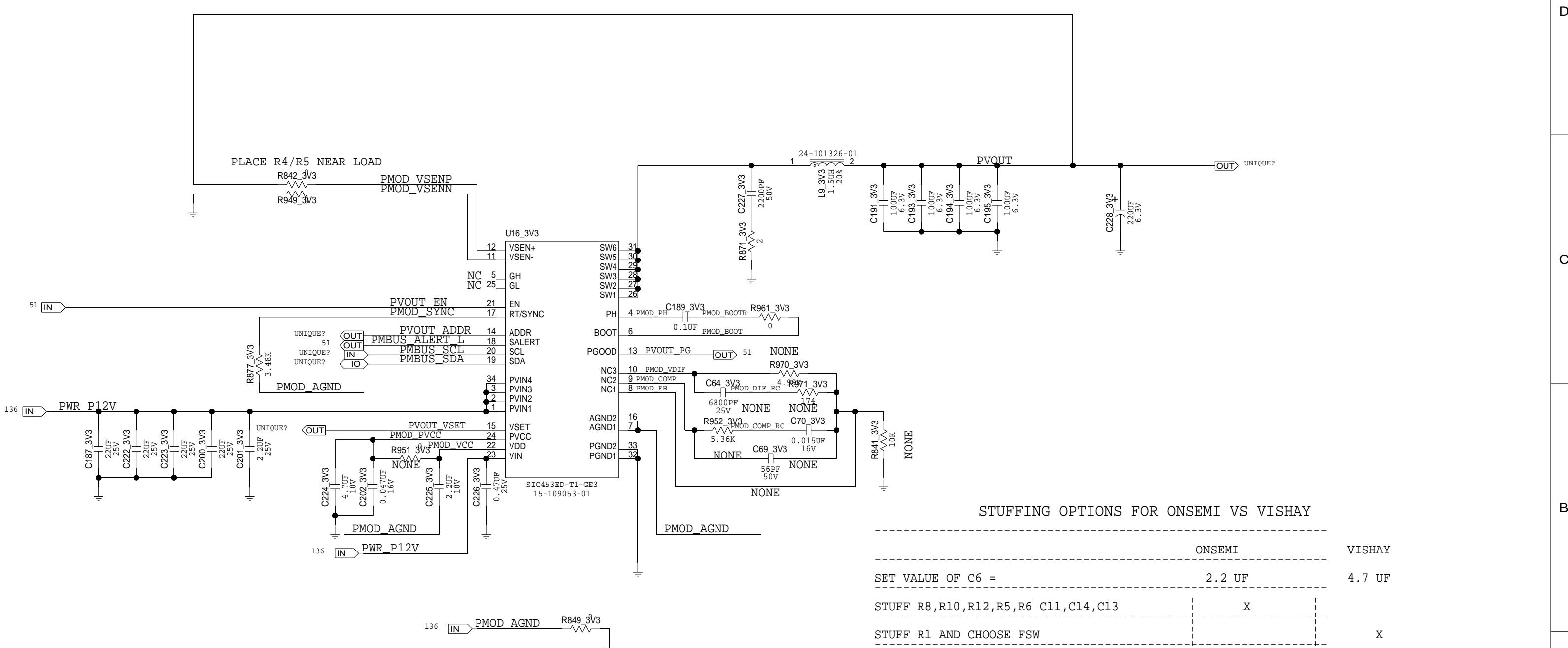
## FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10K	1250
11K	1500



8                    7                    6                    5                    4                    3                    2                    1

FAN251015/SIC453 HIGH VOLTAGE 9A



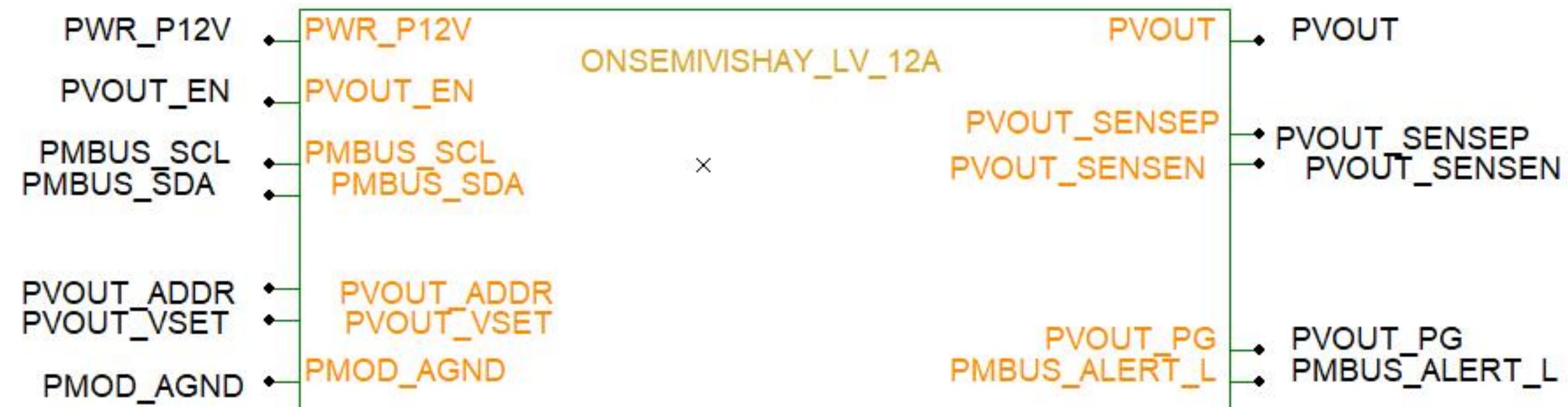
## STUFFING OPTIONS FOR ONSEM1 VS VTSHAY

SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY)		
SET R2 TO 0-OHM FOR VFB = .6V	X	
STUFF R15 AND SET TO DESIRED VOUT		



SIZE <b>B</b>	CLASS CODE _____	DWG. NO. <b>92-105229-01</b>	REV <b>A0</b>
SCALE	DATE: Thu Mar 10 11:24:36 2022		136 OF 138

## ONSEMI FAN25015 AND VISHAY SIC453 .8V-1.8V/12A DUAL BOM VR



## VOUT SET RESISTOR

ONSEMI	VSET Resistor Value (kΩ)	V <sub>out</sub> preset value (V)
	Short	0.6
0.845	0.6	0.845
1.3	0.9	1.30
1.78	0.95	1.78
2.32	1.00	2.32
2.87	1.05	2.87
3.48	1.2	3.48
4.12	1.25	4.12
4.75	1.5	4.75
5.49	1.8	5.49
6.19	2.1	6.19
6.98	2.5	6.98
7.87	3.3	7.87
8.87	5	8.87
10 & greater value	0.8	11.0

OUTPUT VOLTAGE SETTINGS	
V <sub>SET</sub> Resistor Value (kΩ)	V <sub>out</sub> (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

## BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H) Table 1. PMBUS™ ADDRESS SETTING		
ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10K	0D	Base+0D
11K	0E	Base+0E

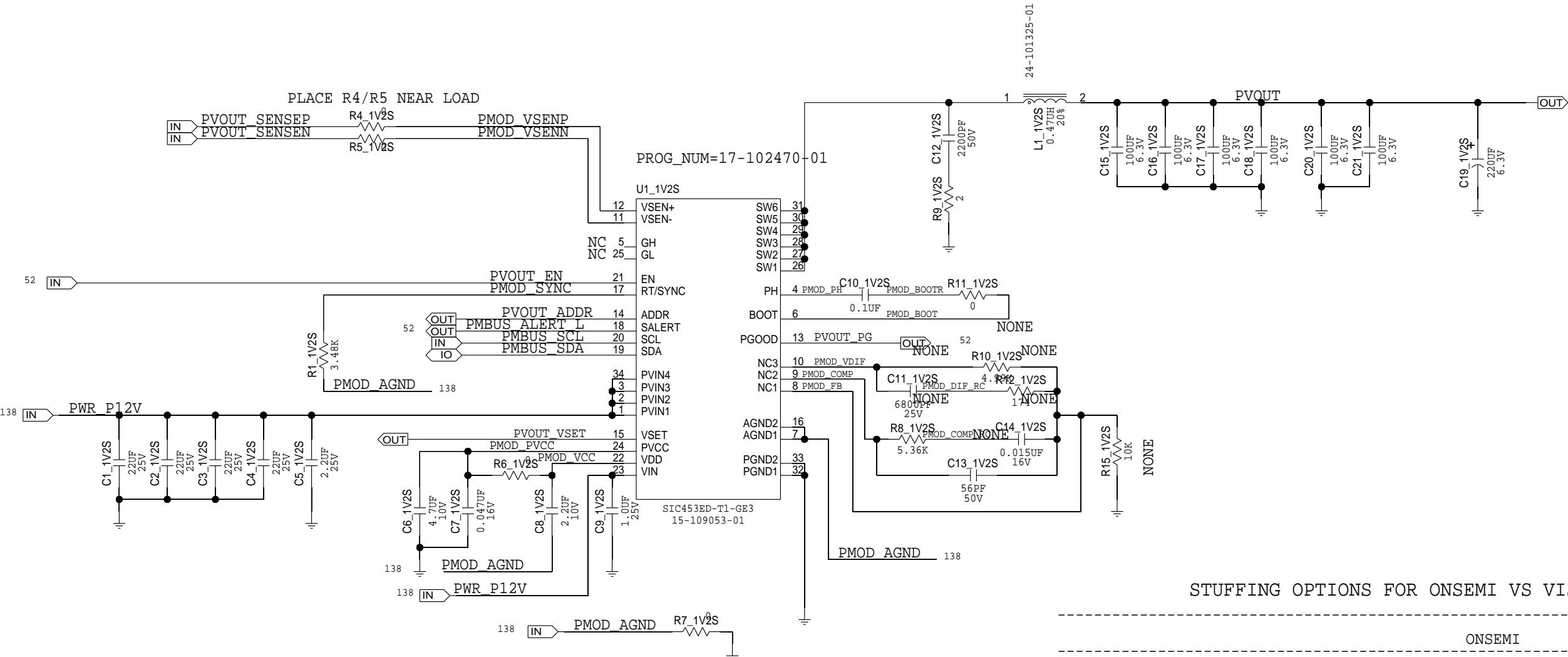
VISHAY(REGISTER D7H, DEFAULT 10H)				
MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)				
MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845	1	0	101b	1010 000b
1.3	2	1	101b	1010 001b
1.78	3	2	101b	1010 010b
2.32	4	3	101b	1010 011b
2.87	5	4	101b	1010 100b
3.48	6	5	101b	1010 101b
4.12	7	6	101b	1010 110b
4.75	8	7	101b	1010 111b
5.49	9	8	101b	1011 000b
6.19	10	9	101b	1011 001b
6.98	11	A	101b	1011 010b
7.87	12	B	101b	1011 011b
8.87	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

FREQ SET RESISTOR(VISHAY ONLY)	
FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10K	1250
11K	1500

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

# FAN251015/SIC453 LOW VOLTAGE 12A



## STUFFING OPTIONS FOR ONSEMI VS VISHAY

ONSEMI

SET VALUE OF C6 = 2.2 UF

STUFF R8,R10,R12,R5,R6 C11,C14,C13 X

STUFF R1 AND CHOOSE FSW

USE FB TO SET VOUT (5-1.99V ONLY)

SET R2 TO 0-OHM FOR VFB = .6V

STUFF R15 AND SET TO DESIRED VOUT



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Mon Mar 14 10:57:10 2022		138 OF 138