Table 1 PCAMAP History

PCA-MAP REV	PCA NUMBER AND REVISION (73-BBBB-VV_RR)	ECO/CUP	DATE	HW VER.	ENGINEER	REASON/PURPOSE OF CHANGE
-A0	73-102931-01_A0	EA597057	05/03/2022	1.0	Kuouyang	Production Release
-B0	73-102931-01_B0	EA598210	06/23/2022	1.0	Kuouyang	PCAMAP VID update and BOM update

1.0 Purpose

1.1 This document is to be used to assemble Superfuzz 73-102931-01.

1.2 This document provides electronic identification and programming instructions.

1.3 This document defines the instructions required to rework from a previous version or revision, if any.

2.0 Manufacturing Assembly Instructions

2.1 Parts required:

2.1.1 General

2.1.1.1 Unless otherwise noted below, install all parts per the current revision of assembly drawing **60-105172-01** and bill of materials **73-102931-01**.

2.1.1.2 Verify that the fab number of the bare PCB is **28-102746-01**. This information is normally located on the solder (bottom) side of the PCB. If this information is not correct, either you have the wrong PCB or this is not the correct assembly procedure. Do not proceed until you have the correct material and documentation. Unless otherwise instructed by Cisco, do not begin the assembly processing of this board unless all the components, called out on the BOM above, are present.

2.1.2 **Part Changes Not in Schematic**

2.1.2.1 NONE

2.1.3 Part Changes Not in BOM but on POI list

2.1.3.1 NONE

2.2 Assembly Steps and Procedures:

2.2.1 General

2.2.1.1 PWB flatness: Flatness should be verified on BGA package sites of 47.5mm and above per the requirements on the fabrication drawing. 10% of the boards per PCB lot should be tested. Any out of specification measurement would require a 100% sampling response prior to assembly (This measurement may be performed by the PWB supplier at the Contract Manufacturer).

2.2.1.2 Minimum soldermask features: BGA package sites with 0.8 mm pitch and below need to be inspected for adequate soldermask dam (measured soldermask web width should be 3 mils minimum). The sampling plan should be per the Mil-STD-10 5D,AQL of 1% for normal inspection (Typi al PCB Lot sizes are 26-50).

2.2.1.3 **LCCC's:** Component stand-off height is critical. Stand-off height is a function of pad paste volume. The minimum stand-off height is >= 0.0015". Optimal stand-off height is 0.0025". Stencil apertures should be 1:1 to the PCB pad soldermask opening. Use a stencil thickness of 0.006". All LCCC solder paste deposits must be measured (AOI/SVS) to insure that they are the same (within 10% of each other) to prevent significant component tilt after assembly.

2.2.1.4 Post Soldering Heat Sink Installation

2.2.1.4.1 With PCB backplane connectors facing away, and the front panel I/O connectors facing toward you, the air-flow direction is from FRONT TO BACK OR BACK TO FRONT.

2.2.1.4.2 When installing adhesive-backed heat sinks, verify the fins are parallel to this airflow direction and the component surface is free of any contamination or solvents.

2.2.1.4.3 For cross-cut fin heat sinks, make sure the wider gap is parallel to the air-flow direction.

2.2.1.5 Ensure that all LEDs and connectors are installed flush with PCB surface and aligned straight with respect to their silkscreens. Pay particular attention to board edge connectors.

2.2.2 Label Placement

2.2.2.1 Refer to the Cisco specifications for labels and printing requirements found on the BOM for each label part number. DO NOT use the part number and revision from the drawing itself or from this assembly procedure. Label the bill of materials assembly number and revision in the PCA area provided per the assembly drawing. Note: CAD artwork specified label locations supersede locations specified in label specification documents. Contact the Cisco EPE if clarification is required for label placement.

2.2.3 Mechanical Assembly

2.2.3.1 Press in connectors should be mounted flush with the board surface and end caps used to protect exposed pins

2.2.3.2 Connectors are press-fit please process after SMT reflow.

2.2.3.3 For location SFP_S0, SFP_S1 AND SFP_S2 MUST USE SAME VENDORS. NO MIXED IN VENDORS.

2.2.3.4 For location QSFP_Q0, QSFP_Q1 AND QSFP_Q2 MUST USE SAME VENDORS. NO MIXED IN VENDORS.

2.2.3.5 It may be necessary to mask the screw mounting holes on the bottom side of the board. The holes are designed in order to minimize solder pickup. No solder is allowed on the screw mounting holes.

2.2.3.6 All screws and standoffs should be tightened to required torque outlined in 95-5874-01

2.2.3.7 Follow assembly instructions outlined in 62-XXXX-01.

2.2.4 PCB and Assembly Defect Repair:

2.2.4.1 Unless otherwise noted, all jumpers (30 ga wire min) are to be installed on the component side of the board.

2.2.4.2 Jumper connections are to be used as a reference for jumper wire end points only and do not define routing paths.

2.2.4.3 All wires should be routed around ICs and tacked to the PCB using glue or tape at intervals of 1.5" or less. Wires should not touch IC legs or other component pins except at end points.

2.2.4.4 All rework must meet or exceed latest revision of IPC-R-700 Class 2.

2.2.4.5 If the Leffe board (CPN 73-101845-0X) in the system is replaced with a different board, follow 2.3.2 to reprogram the MAC's for the management ports.

2.3 Test Requirements

2.3.1 X-ray shall be used (as a minimum requirement) to verify solder joints on all of the BGA packages present on the board. Additionally, In Circuit testing (ICT) (if Available) shall be performed on the board to ensure solder joint quality and bad component identification. For defects found using both tests, the board shall be fixed and the rework recorded by serial number and archived for future reference.

2.3.2 Instruction for programming the MAC for the management ports on Leffe. *Leffe needs two MAC's (1 for SFP, and 1 for RJ45 copper). Assign the first 2 MAC's to Leffe. For service, rework and repair, to check and reprogram if the MAC's on Leffe does not match with the first two MAC's on Sumpin.*

3.0 Programming Instructions

3.1 Programmable Devices Data

3.1.1 See Table 1 for the programmable data information. If the pre-programmed image in the devices is not the same as those listed in the table, then the images are to be updated to match those listed in the table.

3.1.2 The files for the 17-level images can be found in Agile.

Table 1 - Programmable Data

Image Desc	Ref Des	Part Number	Filename
MI_FPGA	MIROM1	17-15887-04 16-1011779-07	mi_elysian_v16_auto.rpd
CPLD	CPLD1-CPLD3	17-13886-01 16-4342-01	salt_lake_city_imp_0_v2
CPLD	CPLD4	17-14336-01 16-4342-01	sumpin_imp_0_v2
PWR CONTROLLER	U1_5	17-15181-02 15-103791-01	17-15181-02-00_SD1_6P1_0P875.mic
POWER CONTROLLER	U1_RTV1, U1_TRV2	17-15781-01 15-103791-01	17-15781-01-00-pmbaddr-0x60-BV1+1.mic

4.0 SPROM Programming Instruction

4.1 Reference the XXX-PROM Programming Document used to program XXX-PROM.

Block #	Offset	Range	Block Size (Bytes)
1	0x0	0x0 – 0x9F	160
2	0xA0	0xA0 – 0x106	103
3	0x107	0x107 – 0x14D	71

Block # 1 -
Common Block

Byte address		item	Value (decimal/hex)	comment
(hex)	(dec)			
0-1	0-1	block signature	0xabab	0xabab
2	2	block version	3	3
3	3	block length	160	160
4-5	4-5	block checksum		see section on checksum
6-7	6-7	SPROM size	65535	65535 (64k Bytes)
8-9	8-9	block count	3	
0A-0B	10-11	FRU major type	0x6002	See FRU section
0C-0D	12-13	FRU minor type	0	See FRU section
0E-21	14-33	OEM string	Cisco Systems, Inc.	Cisco Systems, Inc.

22-35	34-53	product number	N9K-C93180YC-FX3	
36-49	54-73	serial number		
4A-59	74-89	part number	73-102931-01	See PCA MAP
5A-5D	90-93	part revision	B0	See PCA MAP
5E-71	94-113	mfg deviation	0	used by manufacturing
72-73	114-115	hw rev major	1	
74-75	116-117	hw rev minor	0	
76-77	118-119	mfg bits	0	
78-79	120-121	eng bits	0x1	bits[1:0]= 00 > not defined bits[1:0]= 01 > Vishay bits[1:0]= 10 > Onsemi bits[1:0]= 11 > not defined
7A-89	122-137	snmp OID	0.0.0.0.0.0.0.0	Default = 0.0.0.0.0.0.0.0 (software will have its own table, no update plan)
8A-8B	138-139	power consumption	-5008	centiAmp, 601W (12V)
8C-8F	140-143	RMA failure code	0-0-0-0	0
90-9B	144-155	CLEI code	INMGF00CRC	Default = 12345678
9C-9F	156-159	VID	V03	Version ID Default = V01

Block #2 -

Byte offset		item	Value (decimal/hex)	comment
(hex)	(dec)			
0-1	0-1	block signature	0x6002	0x6002
2	2	block version	2	2
3	3	block length	103	103
4-5	4-5	block checksum		see section on checksum
6-D	6-13	feature bits	0	
E-15	14-21	hw changes bits	0x1114	Nibble 3 (new): 1 = new ASIC FW1201 Nibble2 (highlighted) 0= raw ZL30772 DPLL 1= preprogrammed ZL30772 DPLL Nibble 1 1 = Default Nibble 0 4 = Default
16-17	22-23	card index	21212	
18-1D	24-29	MAC base		Auto-generated

1E-1F	30-31	MAC length	100	48 front SFP ports + 6*4 (uplink breakout) + 12 (internal usage) + 16 (FC port channels and spares)= 100 MACs
20	32	EOBC connections	0	
21	33	EPLD num	0	
22-3F	34-63	EPLD versions	0	uint16*15 or uint8*30
40-4F	64-79	Port info	2-54;7-1	type-num; type-num;...
50-51	80-81	SRAM size	0	in kB
52-61	82-97	8 temp sensor info (major/minor)	70/42	1. Intake temp sensor (inlet)
			80/70	2. Exhaust temp sensor (outlet)
			90/80	3. Broadwell-DE CPU
			-128/-128	4. Unused
			110/100	5. CPU VRM
			110/90	6. Sugarbowl/Homewood
			120/110	7. Sugarbowl VRM
			-128/-128	N/A
62-63	98-99	max connector power	5416	centiAmp
64-65	100-101	cooling requirement	100	cfm, see Cooling Req Section
66	102	ambient temperature	55	degrees Celsius

Block #3 -
Sensor Block

Byte offset (hex)	Byte offset (dec)	item	Value (decimal/hex)	comment
0-1	0-1	block signature	0x6008	0x6008
2	2	block version	1	1
3	3	block length	71	71
4-5	4-5	block checksum		see section on checksum
6	6	number of valid sensors	0	# of valid sensors in his block
7 - 46	7 - 70	32 temp sensor info (major/minor)	-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	Sensor instances 15 - 39

5.0 PCA Rework

- No rework from EA597057 to EA598210, D576872 is issued to FDO

6.0 References

6.1 EDCS-643205 PCAMAP Standardization Document
6.2 EDCS-605019 PCA Assembly Best Practices and Guidelines
6.3 EDCS-7000160 ECO Process & Tools Procedure
6.4 EDCS-7003900 Revision Version Policy
6.5 EDCS-7003340 BOM Structure Policy
6.6 EDCS-231946 Cisco UDI Compliance Specification
6.7 EDCS-231945 Unique Device Identifier (UDI) Policy
6.8 EDCS-7024110 CLEI Code Process