REVISION					
REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD
A0	EA597057	RELEASE TO PRODUCTION	DD	DD	DD

1RU SUNDOWN1 MIN FW1201 ASIC
48-PORTS SFP+ AND 6-PORTS QSFP

AN1
SNPNLBL

MFG PART NUMBERS

VISHAY BOM

SUPERFUZZ
NEW SUNDOWN1 FW1201 AND NEW PID

BOM NUMBER	73-102931-01
SCHEMATIC NUMBER	92-105229-01
FAB NUMBER	28-102746-01
ASSY PROCEDUE	61-106157-01
ASSY NUMBER	60-105172-01

REV	DATE	DESCRIPTION
P2		VRM CHANGES + OSC DUAL FOOTPRINT DUE TO SUPPLY SHORTAGE
A0	05/26/2022	RELEASE TO PRODUCTION

QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± | DECIM .xx ±.01 .xxx ±.005 | ANGLES ±1°

MATERIAL

FINISH

DO NOT SCALE DWG

APPROVALS	DATE
DRAWN BY TUAN PHAM	05/26/22
CAD HAIYAN LIU	05/26/22
MECH HARVEY YANG	05/26/22
ENGR TUAN PHAM	05/26/22
MFG KUN	05/26/22
TEST	05/26/22

CISCO

TITLE:
1 RU TOR ELYSIAN/SUPERFUZZ
48 SFP28 AND 6 QSFP28 PORTS

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0

SCALE | DATE: Tue May 3 15:26:06 2022 | 1 OF 138

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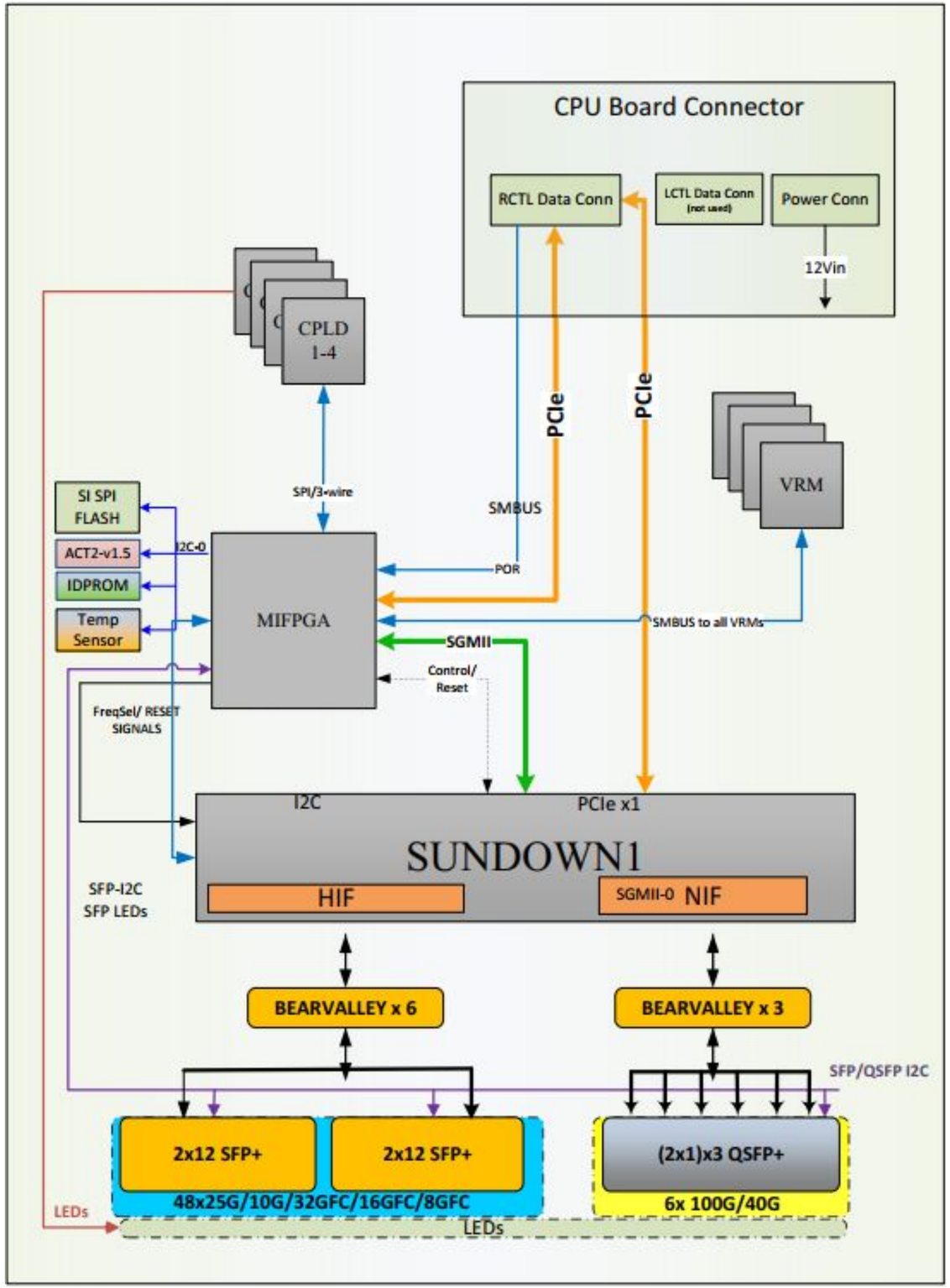

BLOCK DIAGRAM

SIZE	CLASS CODE	DWG. NO.	REV
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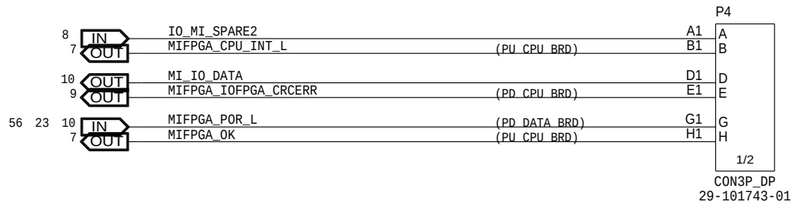

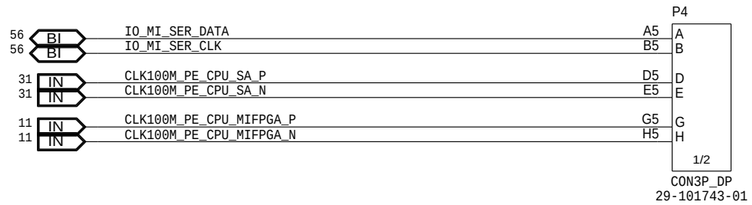

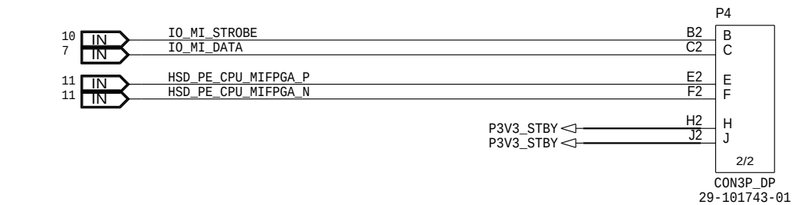

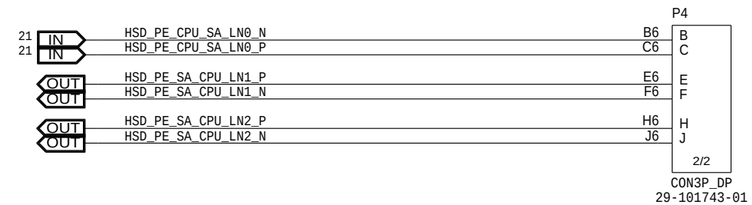

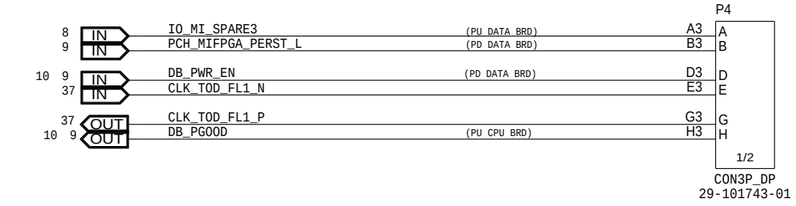

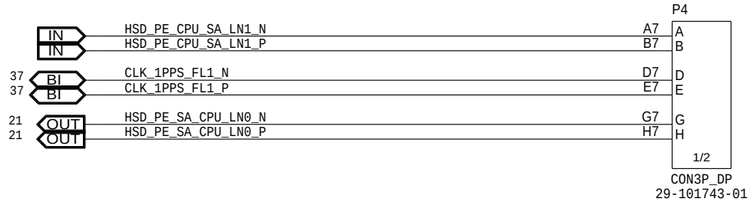

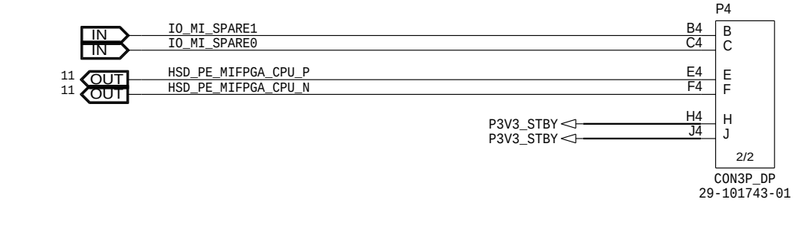

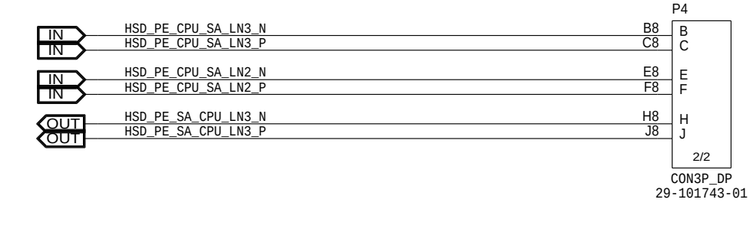

DATA CARD CONNECTOR

SIZE	CLASS CODE	DWG. NO.	REV
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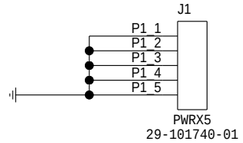
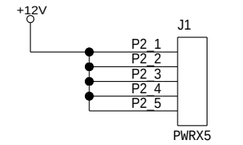
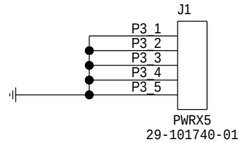
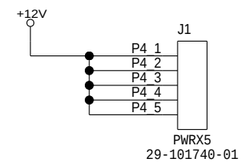
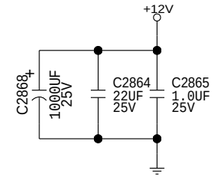
12V CAPACITANCE LOADING 2200UF TO 10000UF
12V STDBY CAPACITANCE LOADING 200UF TO 1000UF
NEED 5,000UF FOR 12MS HOLD UP TIME











SYSTEM POWER CONNECTOR

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
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BUFFER_6.6C
LED 2.5C
VF=2V
I=5MA

+3.3VA

220 R941 — CR16 RED
220 R945 — CR18 RED
220 R558 — CR13 RED
220 R559 — CR14 RED
220 R1053 — CR22 RED
220 R944 — CR19 RED
220 R940 — CR17 RED

ROOM=PWR_LEDS

U61

51 10 IN P3V3_PG 2 1A 18
52 10 IN VDDHA_P1V2_PG 4 16
52 10 IN VDDA_0P9V_PG 6 14
52 10 IN VDD_0P875V_PG 8 12
53 10 IN P1V8_PG 11 2A 9
13 7
51 10 IN SFP0_P3V3_PG 15 5
51 10 IN SFP1_P3V3_PG 17 3
1 AOE
R463 220 19 BOE V 20 +3.3VA
LVC2244

C18 0.1UF 10V

BUFFER_6.6C
LED 2.5C
VF=2V
I=5MA

+3.3VA

220 R704 — CR28 RED
220 R705 — CR29 RED
220 R706 — CR30 RED
220 R709 — CR31 RED

+2.5VA

220 R710 — CR32 RED
220 R711 — CR33 RED

ROOM=PWR_LEDS

U50

54 7 IN P1V0RT1_DVDD_PGOOD 1A
54 7 IN P1V0RT1_AVDD_PGOOD
54 7 IN P1V0RT2_DVDD_PGOOD
54 7 IN P1V0RT2_AVDD_PGOOD
2A
55 8 IN P2V5RT1_PGOOD
55 8 IN P2V5RT2_PGOOD
AOE
R712 220 BOE V +3.3VA
LVC2244

C584 0.1UF 10V

+5V
R8 866 P5V YEL_GRN

+12V
R1665 3K P12V YEL_GRN

P5

R738 10K
10 OUT TI_CABLE_PRSNT R731 1K
54 52 51 10 OUT MIFPGA_PMBUS_SCL
PMBUS_ALERT_L IN 7 51 52 54
MIFPGA_PMBUS_SDA BI 10 51 52 54
HDR2X5 M

POWER LEDS, HEADERS

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
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DUAL FOOTPRINT OPTIONAL FOR U44. PLACE U44_OPT NEXT TO U44

BOM=NONE

BOM=NONE

19-2220-01

19-2528-01

PROG_NUM=16-101568-01
MIFPGA CPN=16-101568-01

U49

BANK 3A & 3B

CV_5CGXFC4C_FG672
16-101437-01

1PPS FROM TOD

MIFPGA: BANK 3, MIROM1, JTAG HDR

MT25QL128ABA8ESF-0SIT
16-1011779-XX
PROG_NUM=17-15887-04

SIZE	CLASS CODE	DWG. NO.	REV
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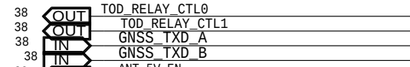
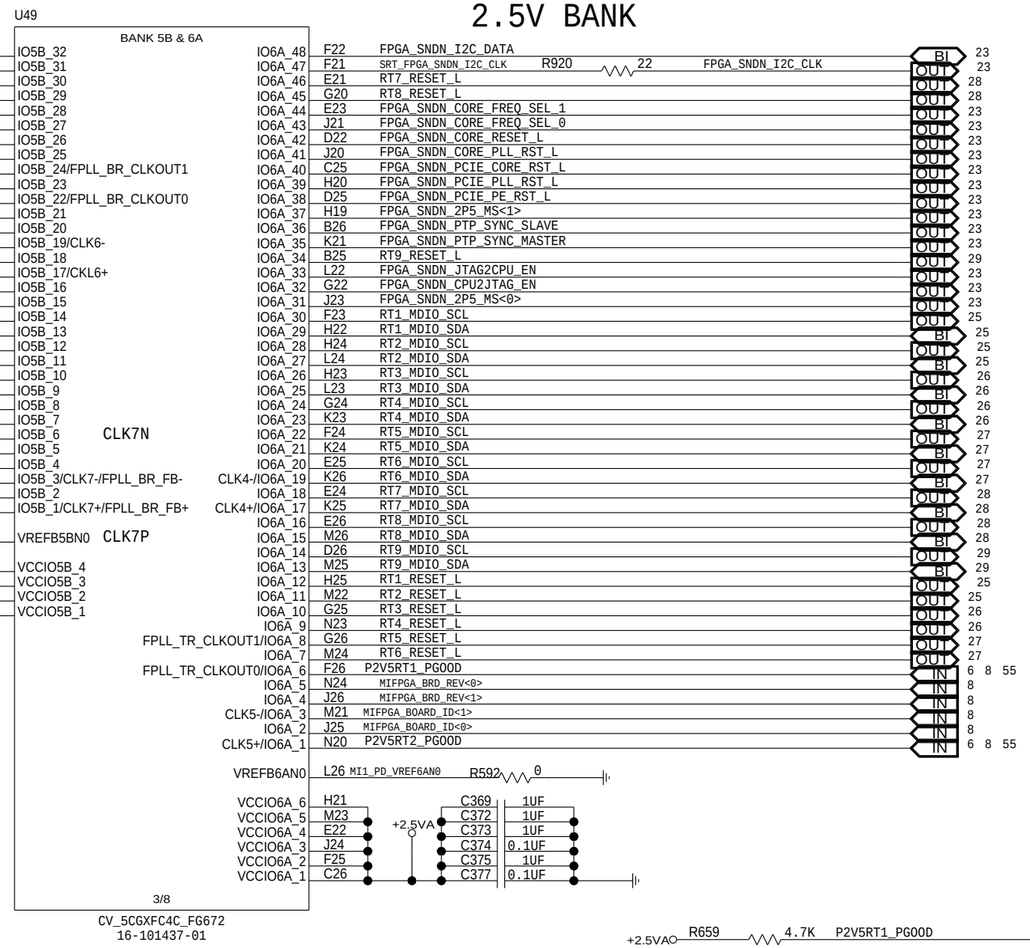
1PPS/10MHZ FROM GNSS ANTENNA

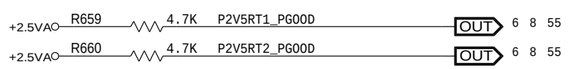
TOD CONSOLE INPUT

1PPS/10MHZ FROM SMA CONNECTOR

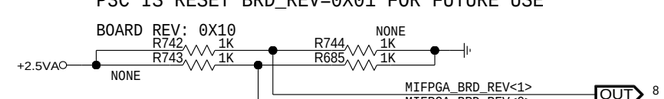


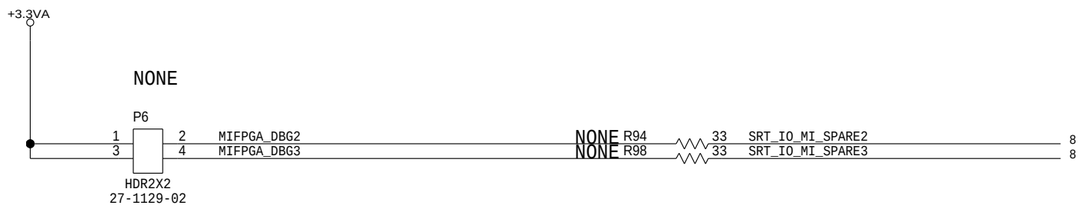


2.5V BANK



NOTE: P3A AND P3B HAVE BRD_REV=0X11 BY MISTAKE
P3C IS RESET BRD_REV=0X01 FOR FUTURE USE





MIFPGA: BANK 5B & 6A

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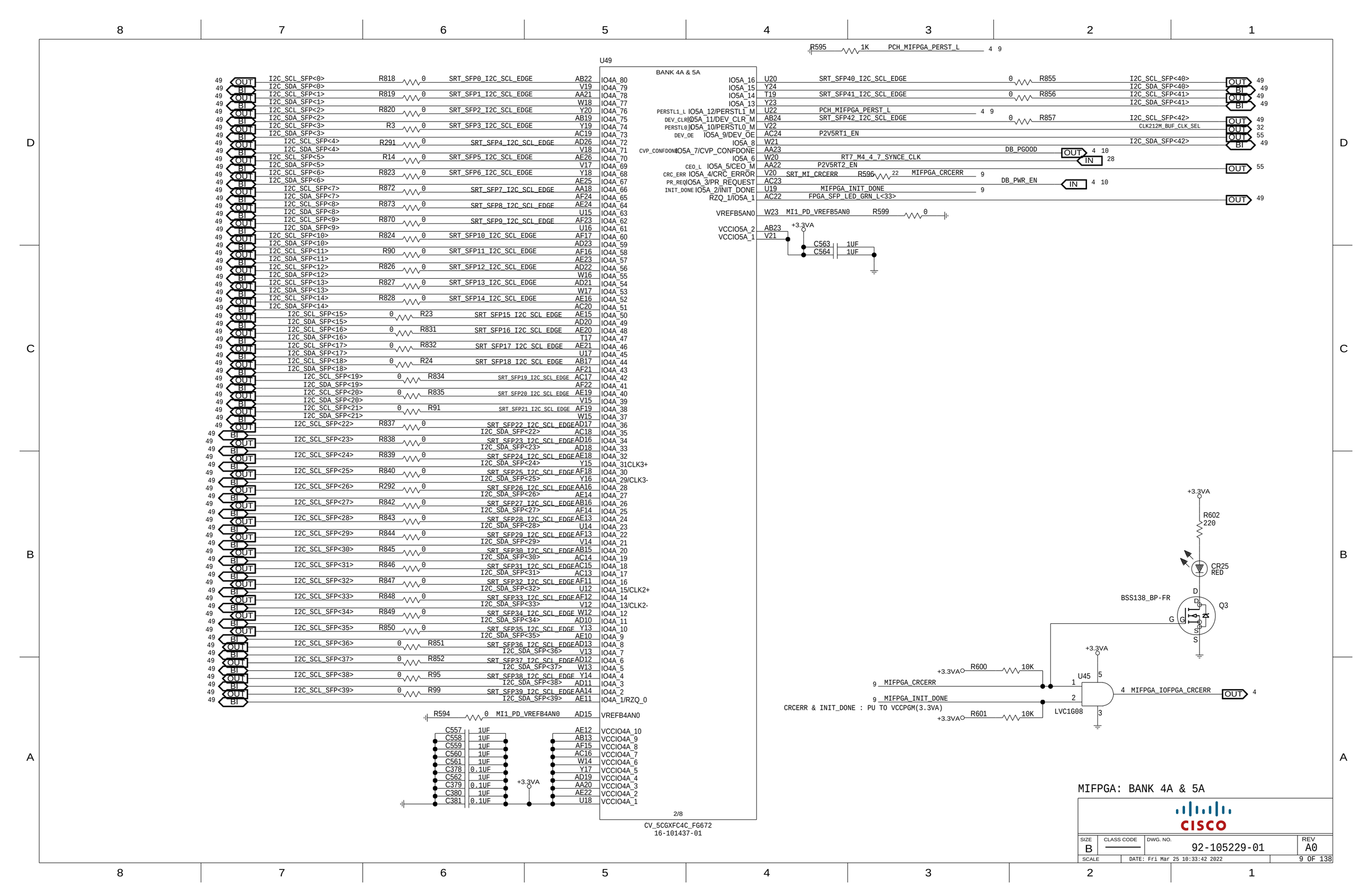
U49
BANK 4A & 5A
R595 1K PCH_MIFPGA_PERST_L 4 9
IO5A_16 U20 SRT_SFP40_I2C_SCL_EDGE 0 R855 I2C_SCL_SFP<40>
IO5A_15 Y24 I2C_SDA_SFP<40>
IO5A_14 T19 SRT_SFP41_I2C_SCL_EDGE 0 R856 I2C_SCL_SFP<41>
IO5A_13 Y23 I2C_SDA_SFP<41>
PERSTL1_L IO5A_12/PERSTL1_M U22 PCH_MIFPGA_PERST_L 4 9
DEV_CLR IO5A_11/DEV_CLR_M AB24 SRT_SFP42_I2C_SCL_EDGE 0 R857 I2C_SCL_SFP<42>
PERSTL0 IO5A_10/PERSTL0_M V22 CLK212M_BUF_CLK_SEL
DEV_OE IO5A_9/DEV_OE AC24 P2V5RT1_EN
IO5A_8 W21 I2C_SDA_SFP<42>
CVP_CONFDONE IO5A_7/CVP_CONFDONE AA23 DB_PGOOD OUT 4 10
IO5A_6 W20 RT7_M4_4_7_SYNCE_CLK IN 28
CEO_L IO5A_5/CEO_M AA22 P2V5RT2_EN
CRC_ERR IO5A_4/CRC_ERROR V20 SRT_MI_CRCERR R596 22 MIFPGA_CRCERR 9
PR_REQ IO5A_3/PR_REQUEST AC23 DB_PWR_EN IN 4 10
INIT_DONE IO5A_2/INIT_DONE U19 MIFPGA_INIT_DONE 9
RZQ_1/IO5A_1 AC22 FPGA_SFP_LED_GRN_L<33>
VREFB5AN0 W23 MI1_PD_VREFB5AN0 R599 0
VCCIO5A_2 AB23 +3.3VA
VCCIO5A_1 V21
C563 1UF
C564 1UF
I2C_SCL_SFP<0> R818 0 SRT_SFP0_I2C_SCL_EDGE AB22 IO4A_80
I2C_SDA_SFP<0> V19 IO4A_79
I2C_SCL_SFP<1> R819 0 SRT_SFP1_I2C_SCL_EDGE AA21 IO4A_78
I2C_SDA_SFP<1> W18 IO4A_77
I2C_SCL_SFP<2> R820 0 SRT_SFP2_I2C_SCL_EDGE Y20 IO4A_76
I2C_SDA_SFP<2> AB19 IO4A_75
I2C_SCL_SFP<3> R3 0 SRT_SFP3_I2C_SCL_EDGE Y19 IO4A_74
I2C_SDA_SFP<3> AC19 IO4A_73
I2C_SCL_SFP<4> R291 0 SRT_SFP4_I2C_SCL_EDGE AD26 IO4A_72
I2C_SDA_SFP<4> V18 IO4A_71
I2C_SCL_SFP<5> R14 0 SRT_SFP5_I2C_SCL_EDGE AE26 IO4A_70
I2C_SDA_SFP<5> V17 IO4A_69
I2C_SCL_SFP<6> R823 0 SRT_SFP6_I2C_SCL_EDGE Y18 IO4A_68
I2C_SDA_SFP<6> AE25 IO4A_67
I2C_SCL_SFP<7> R872 0 SRT_SFP7_I2C_SCL_EDGE AA18 IO4A_66
I2C_SDA_SFP<7> AF24 IO4A_65
I2C_SCL_SFP<8> R873 0 SRT_SFP8_I2C_SCL_EDGE AE24 IO4A_64
I2C_SDA_SFP<8> U15 IO4A_63
I2C_SCL_SFP<9> R870 0 SRT_SFP9_I2C_SCL_EDGE AF23 IO4A_62
I2C_SDA_SFP<9> U16 IO4A_61
I2C_SCL_SFP<10> R824 0 SRT_SFP10_I2C_SCL_EDGE AF17 IO4A_60
I2C_SDA_SFP<10> AD23 IO4A_59
I2C_SCL_SFP<11> R90 0 SRT_SFP11_I2C_SCL_EDGE AF16 IO4A_58
I2C_SDA_SFP<11> AE23 IO4A_57
I2C_SCL_SFP<12> R826 0 SRT_SFP12_I2C_SCL_EDGE AD22 IO4A_56
I2C_SDA_SFP<12> W16 IO4A_55
I2C_SCL_SFP<13> R827 0 SRT_SFP13_I2C_SCL_EDGE AD21 IO4A_54
I2C_SDA_SFP<13> W17 IO4A_53
I2C_SCL_SFP<14> R828 0 SRT_SFP14_I2C_SCL_EDGE AE16 IO4A_52
I2C_SDA_SFP<14> AC20 IO4A_51
I2C_SCL_SFP<15> 0 R23 SRT_SFP15_I2C_SCL_EDGE AE15 IO4A_50
I2C_SDA_SFP<15> AD20 IO4A_49
I2C_SCL_SFP<16> 0 R831 SRT_SFP16_I2C_SCL_EDGE AE20 IO4A_48
I2C_SDA_SFP<16> T17 IO4A_47
I2C_SCL_SFP<17> 0 R832 SRT_SFP17_I2C_SCL_EDGE AE21 IO4A_46
I2C_SDA_SFP<17> U17 IO4A_45
I2C_SCL_SFP<18> 0 R24 SRT_SFP18_I2C_SCL_EDGE AB17 IO4A_44
I2C_SDA_SFP<18> AF21 IO4A_43
I2C_SCL_SFP<19> 0 R834 SRT_SFP19_I2C_SCL_EDGE AC17 IO4A_42
I2C_SDA_SFP<19> AF22 IO4A_41
I2C_SCL_SFP<20> 0 R835 SRT_SFP20_I2C_SCL_EDGE AE19 IO4A_40
I2C_SDA_SFP<20> V15 IO4A_39
I2C_SCL_SFP<21> 0 R91 SRT_SFP21_I2C_SCL_EDGE AF19 IO4A_38
I2C_SDA_SFP<21> W15 IO4A_37
I2C_SCL_SFP<22> R837 0 SRT_SFP22_I2C_SCL_EDGE AD17 IO4A_36
I2C_SDA_SFP<22> AC18 IO4A_35
I2C_SCL_SFP<23> R838 0 SRT_SFP23_I2C_SCL_EDGE AD16 IO4A_34
I2C_SDA_SFP<23> AD18 IO4A_33
I2C_SCL_SFP<24> R839 0 SRT_SFP24_I2C_SCL_EDGE AE18 IO4A_32
I2C_SDA_SFP<24> Y15 IO4A_31/CLK3+
I2C_SCL_SFP<25> R840 0 SRT_SFP25_I2C_SCL_EDGE AF18 IO4A_30
I2C_SDA_SFP<25> Y16 IO4A_29/CLK3-
I2C_SCL_SFP<26> R292 0 SRT_SFP26_I2C_SCL_EDGE AA16 IO4A_28
I2C_SDA_SFP<26> AE14 IO4A_27
I2C_SCL_SFP<27> R842 0 SRT_SFP27_I2C_SCL_EDGE AB16 IO4A_26
I2C_SDA_SFP<27> AF14 IO4A_25
I2C_SCL_SFP<28> R843 0 SRT_SFP28_I2C_SCL_EDGE AE13 IO4A_24
I2C_SDA_SFP<28> U14 IO4A_23
I2C_SCL_SFP<29> R844 0 SRT_SFP29_I2C_SCL_EDGE AF13 IO4A_22
I2C_SDA_SFP<29> V14 IO4A_21
I2C_SCL_SFP<30> R845 0 SRT_SFP30_I2C_SCL_EDGE AB15 IO4A_20
I2C_SDA_SFP<30> AC14 IO4A_19
I2C_SCL_SFP<31> R846 0 SRT_SFP31_I2C_SCL_EDGE AC15 IO4A_18
I2C_SDA_SFP<31> AC13 IO4A_17
I2C_SCL_SFP<32> R847 0 SRT_SFP32_I2C_SCL_EDGE AF11 IO4A_16
I2C_SDA_SFP<32> U12 IO4A_15/CLK2+
I2C_SCL_SFP<33> R848 0 SRT_SFP33_I2C_SCL_EDGE AF12 IO4A_14
I2C_SDA_SFP<33> V12 IO4A_13/CLK2-
I2C_SCL_SFP<34> R849 0 SRT_SFP34_I2C_SCL_EDGE W12 IO4A_12
I2C_SDA_SFP<34> AD10 IO4A_11
I2C_SCL_SFP<35> R850 0 SRT_SFP35_I2C_SCL_EDGE Y13 IO4A_10
I2C_SDA_SFP<35> AE10 IO4A_9
I2C_SCL_SFP<36> 0 R851 SRT_SFP36_I2C_SCL_EDGE AD13 IO4A_8
I2C_SDA_SFP<36> V13 IO4A_7
I2C_SCL_SFP<37> 0 R852 SRT_SFP37_I2C_SCL_EDGE AD12 IO4A_6
I2C_SDA_SFP<37> W13 IO4A_5
I2C_SCL_SFP<38> 0 R95 SRT_SFP38_I2C_SCL_EDGE Y14 IO4A_4
I2C_SDA_SFP<38> AD11 IO4A_3
I2C_SCL_SFP<39> 0 R99 SRT_SFP39_I2C_SCL_EDGE AA14 IO4A_2
I2C_SDA_SFP<39> AE11 IO4A_1/RZQ_0
R594 0 MI1_PD_VREFB4AN0 AD15 VREFB4AN0
C557 1UF AE12 VCCIO4A_10
C558 1UF AB13 VCCIO4A_9
C559 1UF AF15 VCCIO4A_8
C560 1UF AC16 VCCIO4A_7
C561 1UF W14 VCCIO4A_6
C378 0.1UF Y17 VCCIO4A_5
C562 1UF AD19 VCCIO4A_4
C379 0.1UF AA20 VCCIO4A_3
C380 1UF AE22 VCCIO4A_2
C381 0.1UF U18 VCCIO4A_1
+3.3VA
2/8
CV_5CGXFC4C_FG672
16-101437-01
+3.3VA
R602 220
CR25 RED
BSS138_BP-FR
Q3
+3.3VA
R600 10K
MIFPGA_CRCERR
MIFPGA_INIT_DONE
CRCERR & INIT_DONE : PU TO VCCPGM(3.3VA)
R601 10K
U45
LVC1G08
MIFPGA_IOFPGA_CRCERR
MIFPGA: BANK 4A & 5A
CISCO
SIZE B
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U49

BANK 7A & 8A

I2C_SCL_SFP<43>	R858	0	SRT_SFP43_I2C_SCL_EDGE	D12	IO7A_80/RZQ_2	IO8A_32	E9
I2C_SDA_SFP<43>				D13	IO7A_79	IO8A_31	K6
I2C_SCL_SFP<44>	R859	0	SRT_SFP44_I2C_SCL_EDGE	D11	IO7A_78	IO8A_30	D8
I2C_SDA_SFP<44>				E13	IO7A_77	IO8A_29	L7
I2C_SCL_SFP<45>	R860	0	SRT_SFP45_I2C_SCL_EDGE	C12	IO7A_76	IO8A_28	J7
I2C_SDA_SFP<45>				L11	IO7A_75	IO8A_27	J10
I2C_SCL_SFP<46>	R861	0	SRT_SFP46_I2C_SCL_EDGE	C13	IO7A_74	IO8A_26	H7
I2C_SDA_SFP<46>				M11	IO7A_73	IO8A_25	K10
I2C_SCL_SFP<47>	R862	0	SRT_SFP47_I2C_SCL_EDGE	B11	IO7A_72	IO8A_24	F7
I2C_SDA_SFP<47>				F12	IO7A_71	IO8A_23	J8
QSFP_SCL<0>	R878	0	SRT_QSFP_SCL<0>	A12	IO7A_70	IO8A_22	G7
QSFP_SDA<0>				G12	IO7A_69	IO8A_21	K8
QSFP_SCL<1>	R888	0	SRT_QSFP_SCL<1>	A13	IO7A_68	IO8A_20	G6
QSFP_SDA<1>				G11	IO7A_67/CLK10-	CLK8-/IO8A_19	K9
QSFP_SCL<2>	R879	0	SRT_QSFP_SCL<2>	B12	IO7A_66	IO8A_18	F6
QSFP_SDA<2>				H12	IO7A_65/CLK10+	CLK8+/IO8A_17	L8
QSFP_SCL<3>	R880	0	SRT_QSFP_SCL<3>	E11	IO7A_64	IO8A_16	C7
QSFP_SDA<3>				E15	IO7A_63	IO8A_15	G10
QSFP_SCL<4>	R881	0	SRT_QSFP_SCL<4>	E10	IO7A_62	IO8A_14	D7
QSFP_SDA<4>				F16	IO7A_61	IO8A_13	H10
QSFP_SCL<5>	R882	0	SRT_QSFP_SCL<5>	A11	IO7A_60	IO8A_12	E6
QSFP_SDA<5>				M12	IO7A_59	IO8A_11	L9
SFP_MOD_ABS_FPGA<33>				B10	IO7A_58	IO8A_10	D6
SFP_RX_LOS_FPGA<33>				N12	IO7A_57	IO8A_9	M9
SFP_TX_FAULT_FPGA<33>				C10	IO7A_56	FPLL_TL_CLKOUT1/IO8A_8	B7
SFP_MOD_ABS_FPGA<34>				D16	IO7A_55	IO8A_7	H9
SFP_RX_LOS_FPGA<34>				D10	IO7A_54	FPLL_TL_CLKOUT0/IO8A_6	A7
SFP_TX_FAULT_FPGA<34>				E16	IO7A_53	IO8A_5	H8
FPGA_SFP_TX_DISABLE<33>				B9	IO7A_52	IO8A_4	B6
AC_CLK25M_MI0_SYNC_E_REFCLK_N				G14	IO7A_51/CLK11-	CLK9-/IO8A_3	M10
FPGA_SFP_LED_YEL_L<33>				C9	IO7A_50	IO8A_2	A5
AC_CLK25M_MI0_SYNC_E_REFCLK_P				G15	IO7A_49/CLK11+	CLK9+/IO8A_1	N9
FPGA_SFP_LED_GRN_L<34>				A9	IO7A_48		
FPGA_SFP_LED_YEL_L<34>				D15	IO7A_47		
TI_CABLE_PRSNT				A8	IO7A_46		
JTAG_CABLE_PRSNT_L				C14	IO7A_45		
JTAG_CABLE_PRSNT_L_DAV_HDR				C15	IO7A_44		
CLK100M_SNDN1_BUF_CLK_SEL				K11	IO7A_43		
			FPGA_MONI_INT	B15	IO7A_42		
			SNDN_VDDHA_1P2V_EN	L12	IO7A_41		
			SNDN_P0V9_EN	B14	IO7A_40		
			SNDN_CORE_EN	F18	IO7A_39		
		RT8_M4_0_3_SYNCE_CLK		A14	IO7A_38		
			P1V8_EN	E18	IO7A_37		
			P3V3_SFP_EN	B17	IO7A_36		
			P3V3_EN	H13	IO7A_35		
			P5V_EN	C17	IO7A_34		
		RT8_M4_4_7_SYNCE_CLK		H14	IO7A_33		
			VDDHA_P1V2_PG	A16	IO7A_32		
			VDDA_0P9V_PG	D17	IO7A_31		
			VDD_0P875V_PG	A17	IO7A_30		
			DPLL_SYNCE_RESET_L	D18	IO7A_29		
			P1V8_PG	A18	IO7A_28		
			SFP1_P3V3_PG	J11	IO7A_27		
			SFP0_P3V3_PG	A19	IO7A_26		
			P3V3_PG	J12	IO7A_25		
			P5V_PG	C18	IO7A_24		
			FPGA_CPLD2_DATA	E19	IO7A_23		
			FPGA_CPLD2_SPI_MOSI	C19	IO7A_22		
			MIFPGA_LED_CTRL	E20	IO7A_21		
			FPGA_CPLD2_SPI_CS_L	B19	IO7A_20		
			CPLD2_FPGA_DATA	G17	IO7A_19		
			CPLD2_FPGA_SPI_MISO	C20	IO7A_18		
FPGA_CPLD2_CLK	R324	33	SRT_FPGA_CPLD2_CLK	G16	IO7A_17		
FPGA_CPLD2_SPI_SCK	R325	33	SRT_FPGA_CPLD2_SPI_SCK	B20	IO7A_16		
			FPGA_CPLD1_DATA	D20	IO7A_15		
			FPGA_CPLD1_SPI_MOSI	B21	IO7A_14		
			FPGA_CPLD_RST_L	D21	IO7A_13		
			FPGA_CPLD1_SPI_CS_L	A21	IO7A_12		
			CPLD1_FPGA_DATA	H17	IO7A_11		
			CPLD1_FPGA_SPI_MISO	B22	IO7A_10		
FPGA_CPLD1_CLK	R16	33	SRT_FPGA_CPLD1_CLK	H18	IO7A_9		
FPGA_CPLD1_SPI_SCK	R326	33	SRT_FPGA_CPLD1_SPI_SCK	A22	IO7A_8		
MIFPGA_PMBUS_SCL	R60	22	SRT_MIFPGA_PMBUS_SCL	A24	IO7A_7		
			MIFPGA_PMBUS_SDA	A23	IO7A_6		
			MIFPGA_POR_L	B24	IO7A_5		
		RT9_M4_0_3_SYNCE_CLK		C22	IO7A_4		
		RT9_M4_4_7_SYNCE_CLK		J16	IO7A_3		
RT_DOWNLINK_M4_4_7_SYNCE_CLK	R125	33	SRT_RT_DOWNLINK_M4_4_7_SYNCE_CLK	C23	IO7A_2		
RT_DOWNLINK_M4_0_3_SYNCE_CLK	R135	33	SRT_RT_DOWNLINK_M4_0_3_SYNCE_CLK	H15	IO7A_1		
R603	0	MI1_PD_VREFB7AN0		B16	VREFB7AN0	VREFB8AN0	C8
MIFPGA_POR_L	1K	R321		H11	VCCIO7A_10	VCCIO8A_4	K7
DB_PWR_EN	1K	R51		E12	VCCIO7A_9	VCCIO8A_3	G8
C565 1UF, C566 1UF, C382 0.1UF, C567 1UF, C383 0.1UF, C568 1UF, C384 0.1UF, C569 1UF, C385 0.1UF, C386 1UF				B13	VCCIO7A_8	VCCIO8A_2	D9
				F15	VCCIO7A_7	VCCIO8A_1	C6
				C16	VCCIO7A_6		
				G18	VCCIO7A_5		
				D19	VCCIO7A_4		
				A20	VCCIO7A_3		
				B23	VCCIO7A_2		
				A10	VCCIO7A_1		
				D23	GND_7A		

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CV_5CGXFC4C_FG672
16-101437-01

+3.3VA

C387 1UF, C388 0.1UF, C390 1UF, C391 0.1UF

R47 2K FPGA_OSC_SDA
R48 2K FPGA_OSC_SCL
R126 4.75K MIFPGA_PMBUS_SCL
R131 4.75K MIFPGA_PMBUS_SDA

R38 10K FPGA_CPLD_RST_L

NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTORS AS SHORT AS POSSIBLE

BOM=NONE
R138 200
C231 0.1UF
C230 0.1UF
BOM=NONE

R19 75
R20 82
NONE
R21 150
R22 130
NONE

NOTES: CLK25M_MI0_SYNCE_E_REFCLK IS CHANGED TO LVCMOS
TERMINATION PER SI TO SMOOTH THE CLK KINKS AND SET PROPER DC BIAS

CR2 GRN
+12V
487
R52
Q1 BSS138_BP-FR
PWR_ADOMAIN_PGOOD

CR108 GRN
+12V
R1422 487
Q24 BSS138_BP-FR
DB_PGOOD
R412 1K

IO_MI_STROBE
1UF C60 NONE

MIFPGA: BANK 7 & 8, DBG HDR/LEDS

CISCO

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MSEL=10010, ACTIVE SERIAL, FAST POR

U49

BANK 9A

+3.3VA
R532 10K NONE
R606 100 J5 MSEL4
R607 100 K5 MSEL3
R608 100 A2 MSEL2
R609 100 L6 MSEL1
R534 100 NONE M7 MSEL0
R612 100

53 10 IN PWR_ADOMAIN_PGOOD
R605 0
R549 10K
MIFPGA_CONFIG_L F5 CONFIG
MIFPGA_CE_L D5 CE

R550 2K 1% MIFPGA_RREF0 B1 RREF_TL

CONF_DONE A6
STATUS B5 MIFPGA_STATUS_L
GND_9A H5

+3.3VA
R551 10K
+3.3VA
R556 220
1 25-1282-01 2
CR4 RED
+3.3VA
R553 10K
MIFPGA_CONFIG_DONE

GXB-L0 & GXB-L1

R615 100 M2 GXB_RX_L5P_GXB_REFCLK_L5+
R616 100 M1 GXB_RX_L5N_GXB_REFCLK_L5-
R617 100 T2 GXB_RX_L4P_GXB_REFCLK_L4+
R618 100 T1 GXB_RX_L4N_GXB_REFCLK_L4-
R619 100 V2 GXB_RX_L3P_GXB_REFCLK_L3+
R620 100 V1 GXB_RX_L3N_GXB_REFCLK_L3-

GXB_TX_L5+ K2
GXB_TX_L5- K1
GXB_TX_L4+ P2
GXB_TX_L4- P1
GXB_TX_L3+ W4
GXB_TX_L3- W3

N7 REFCLK1L+
P6 REFCLK1L-

R624 100 Y2 GXB_RX_L2P_GXB_REFCLK_L2+
R626 100 Y1 GXB_RX_L2N_GXB_REFCLK_L2-

GXB_TX_L2+ AA4
GXB_TX_L2- AA3

21 IN LAN1_PORT0_CPU_RX_P NONE C576 0.1UF LAN1_PORT0_CPU_RX_AC_P AB2 GXB_RX_L1P_GXB_REFCLK_L1+
21 IN LAN1_PORT0_CPU_RX_N NONE C577 0.1UF LAN1_PORT0_CPU_RX_AC_N AB1 GXB_RX_L1N_GXB_REFCLK_L1-
4 IN HSD_PE_CPU_MIFPGA_P C570 0.1UF HSD_PE_CPU_MIFPGA_AC_P AD2 GXB_RX_L0P_GXB_REFCLK_L0+
4 IN HSD_PE_CPU_MIFPGA_N C571 0.1UF HSD_PE_CPU_MIFPGA_AC_N AD1 GXB_RX_L0N_GXB_REFCLK_L0-

GXB_TX_L1+ AC4 LAN1_PORT0_CPU_TX_P OUT 21
GXB_TX_L1- AC3 LAN1_PORT0_CPU_TX_N OUT 21
GXB_TX_L0+ AE4 HSD_PE_MIFPGA_CPU_P OUT 4
GXB_TX_L0- AE3 HSD_PE_MIFPGA_CPU_N OUT 4

4 IN CLK100M_PE_CPU_MIFPGA_P
4 IN CLK100M_PE_CPU_MIFPGA_N
R737 0 CLK100M_PE_CPU_MIFPGA_AC_P V6 REFCLK0L+
R739 0 CLK100M_PE_CPU_MIFPGA_AC_N W6 REFCLK0L-

BOM=NONE R707 150
BOM=NONE R708 150

+3.3VA
+3.3VA
BOM=NONE R715 150
BOM=NONE R716 150
BOM=NONE R720 84.5
BOM=NONE R721 84.5

NC

G3 NC_16
H1 NC_15
H2 NC_14
D1 NC_13
D2 NC_12
E3 NC_11
F1 NC_10
F2 NC_9
C3 NC_8
L5 NC_7
G4 NC_6
E4 NC_5
C4 NC_4
AB7 NC_3
M6 NC_2
AA12 NC_1

DNU_4 F14
DNU_3 C24
DNU_2 A3
DNU_1 A4

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CV_5CGXFC4C_FG672
16-101437-01

WE CAN BOM NONE THIS
USE THE 125MHZ FOR FPGA LOGIC

PROG_NUM=19-100573-01

+3.3VA
R88 1K
U9
+3.3VA
R1109 220 BOM=NONE
L60 600 100MHZ
FLTR_CLK25M_OSC
1 VCON
/GND
6 VCC
OUT 4 SRT_CLK25M_OSC
GND 3
R89 33 CLK25M_MIFPGA
OUT 7
TCXO_6P
19-2479-01
25.000MHZ
2.5PM
C1185 22UF
C1184 0.1UF

MIFPGA: CONFIG, REFCLK, SERDES

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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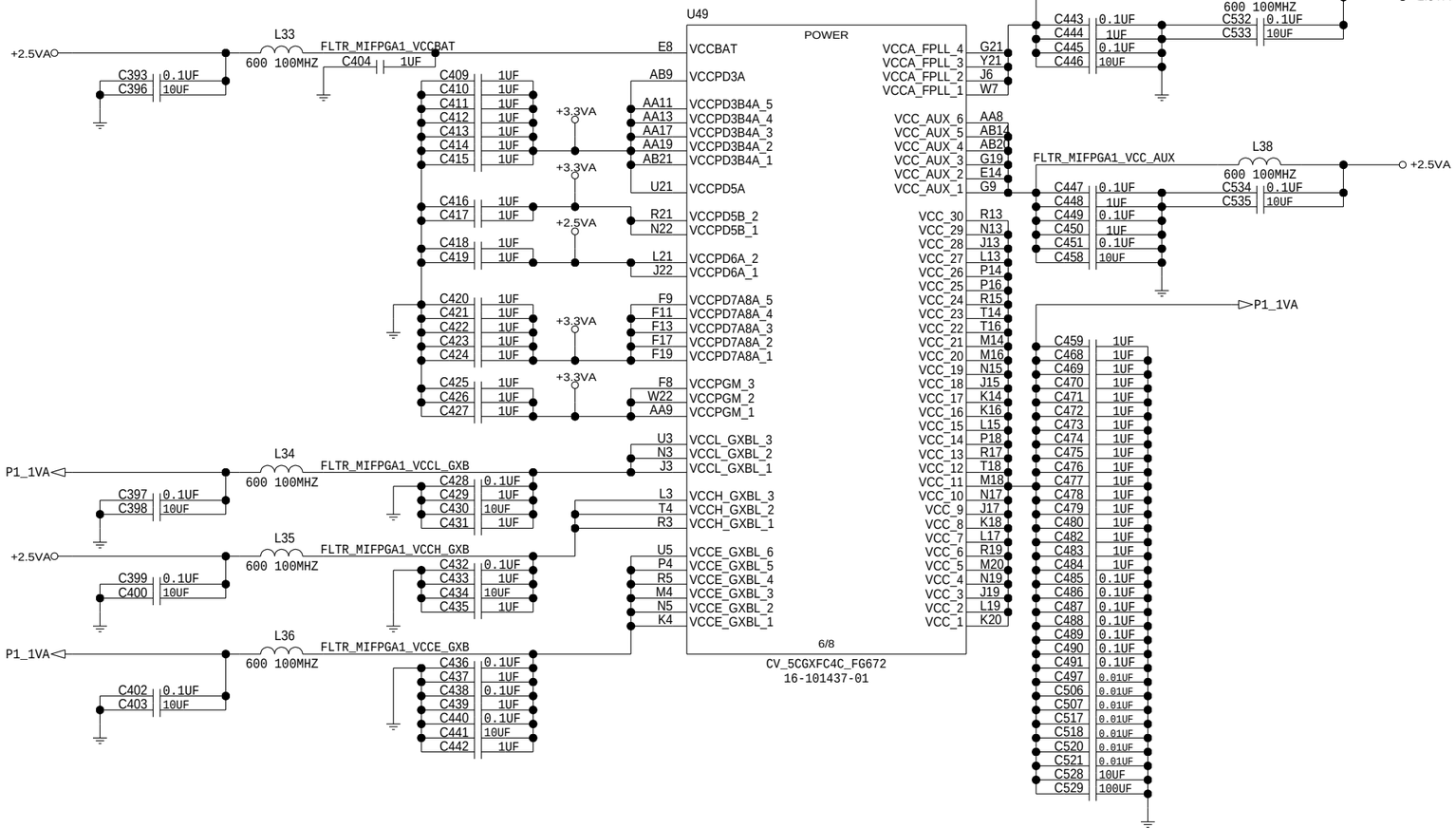

MIFPGA: POWER & GROUND

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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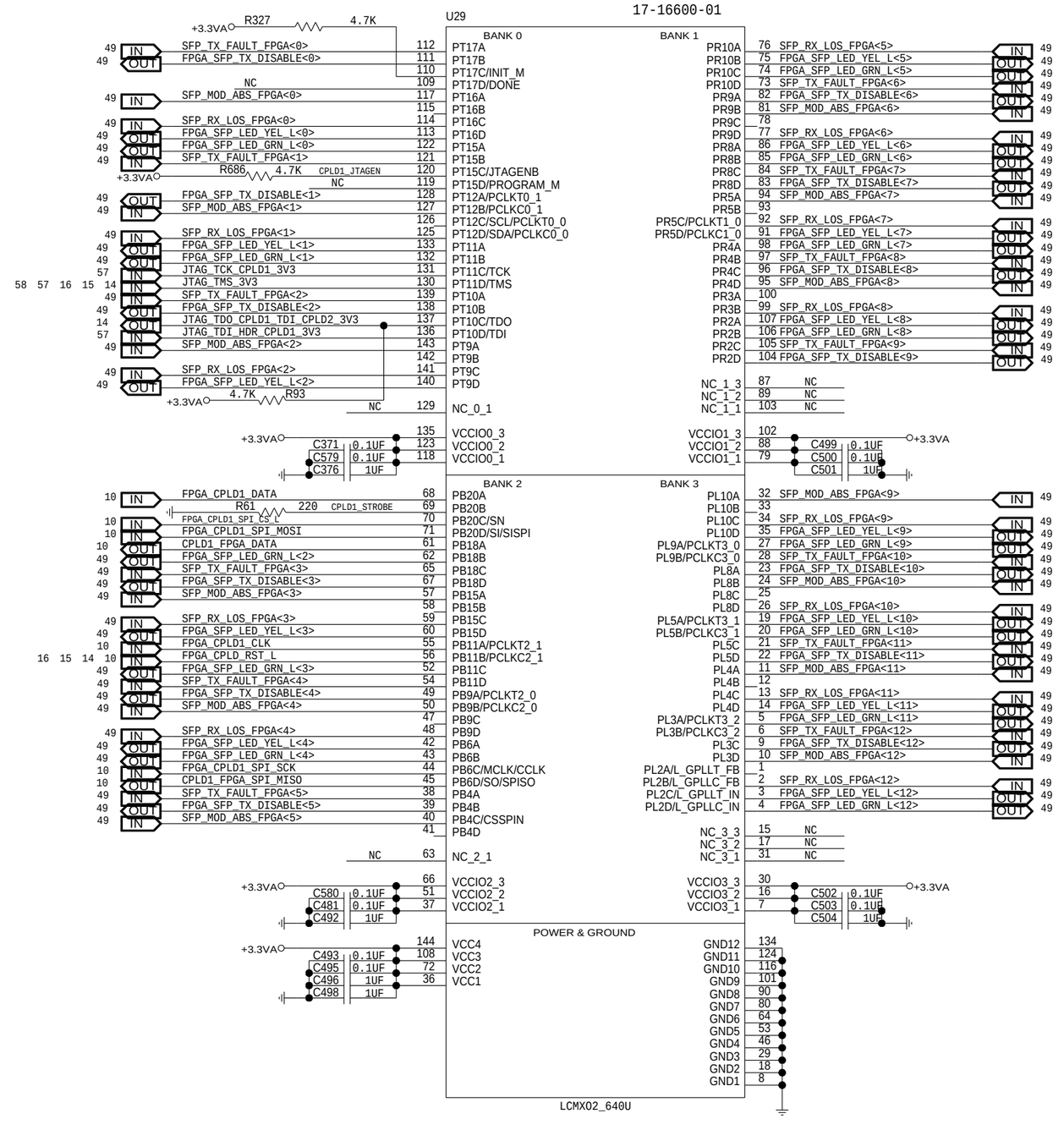
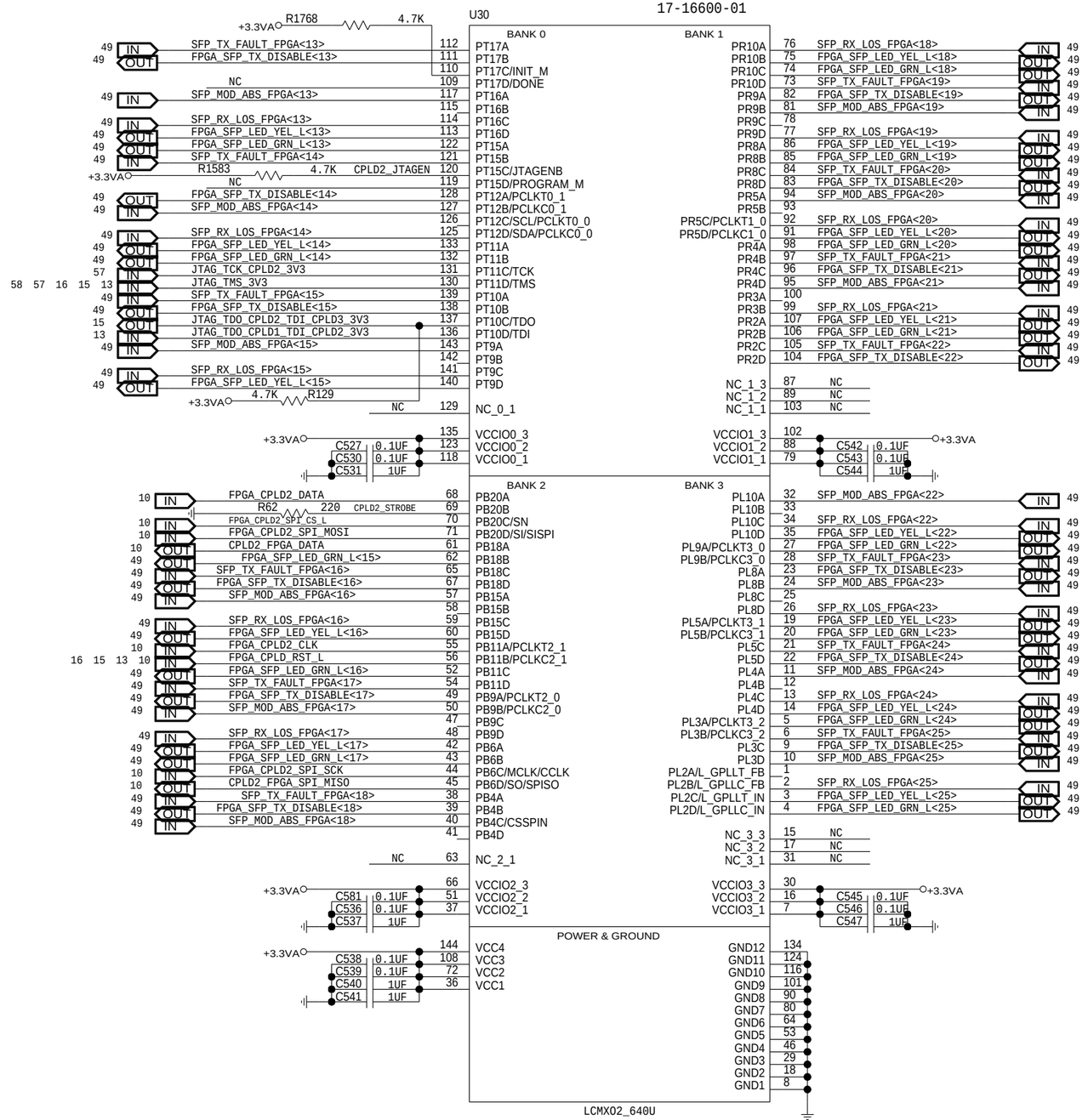


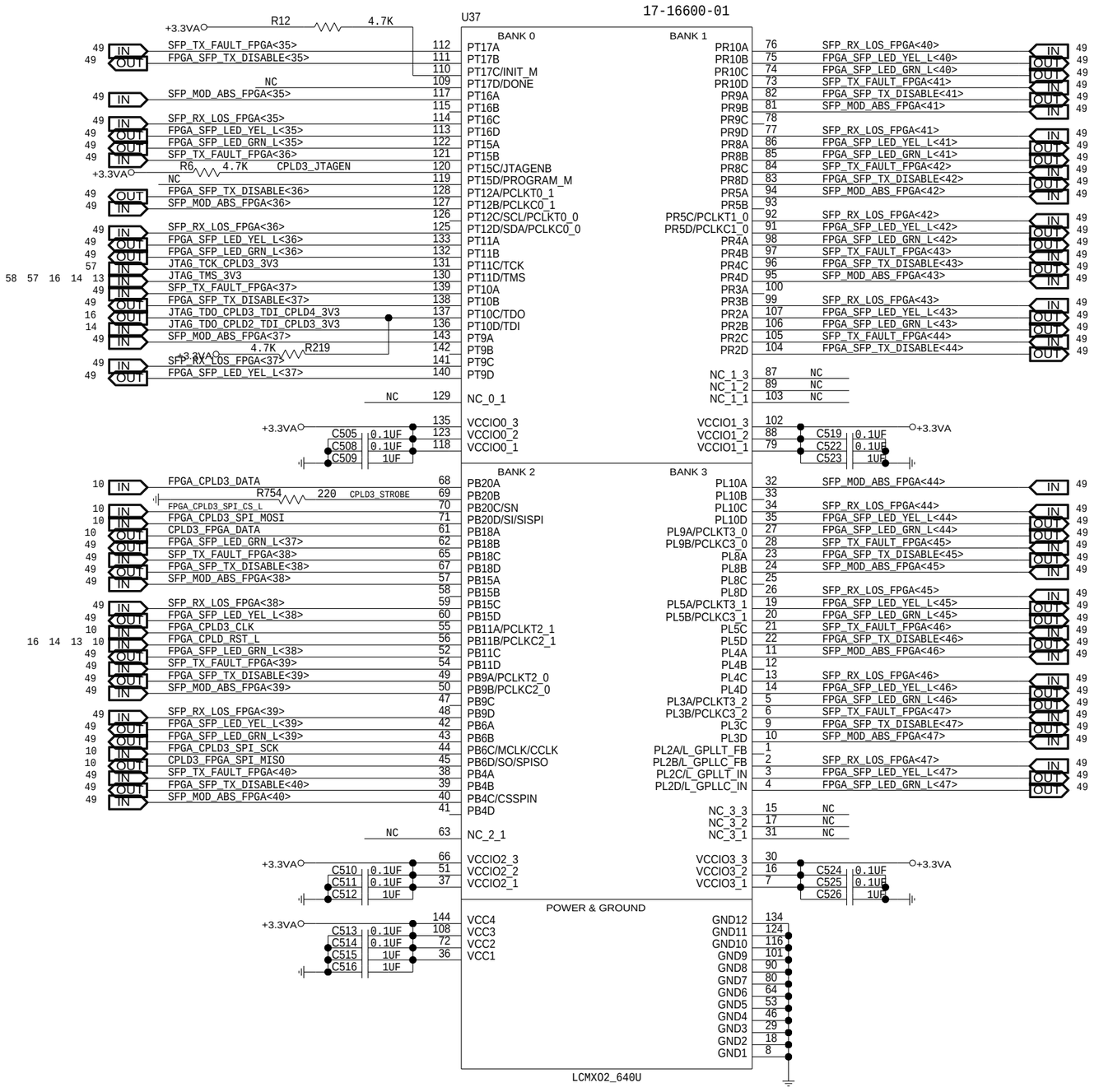
IO EXPANDER CPLD 1

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:46 2022		13 OF 138



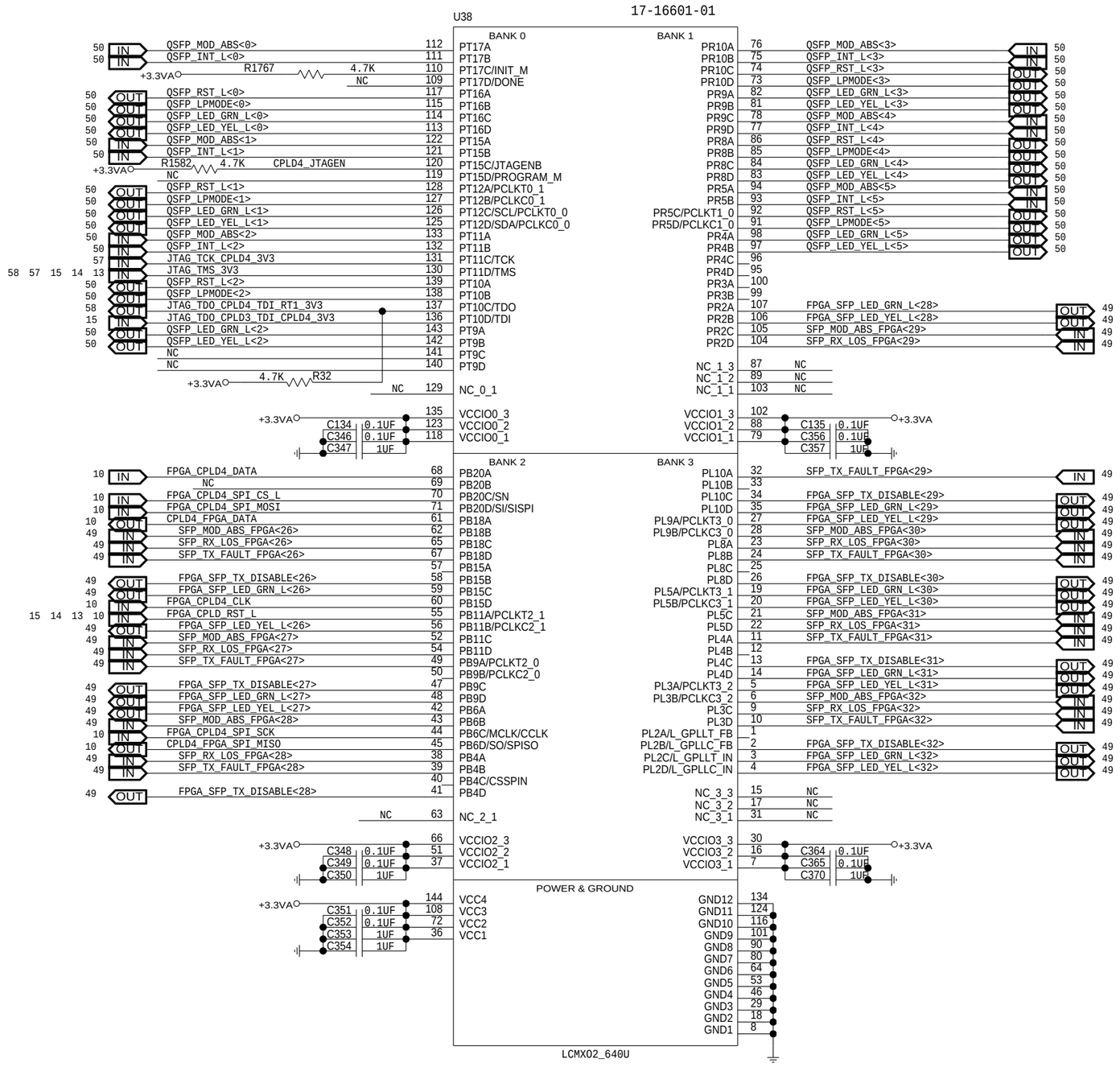
IO EXPANDER CPLD 2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:46 2022		14 OF 138



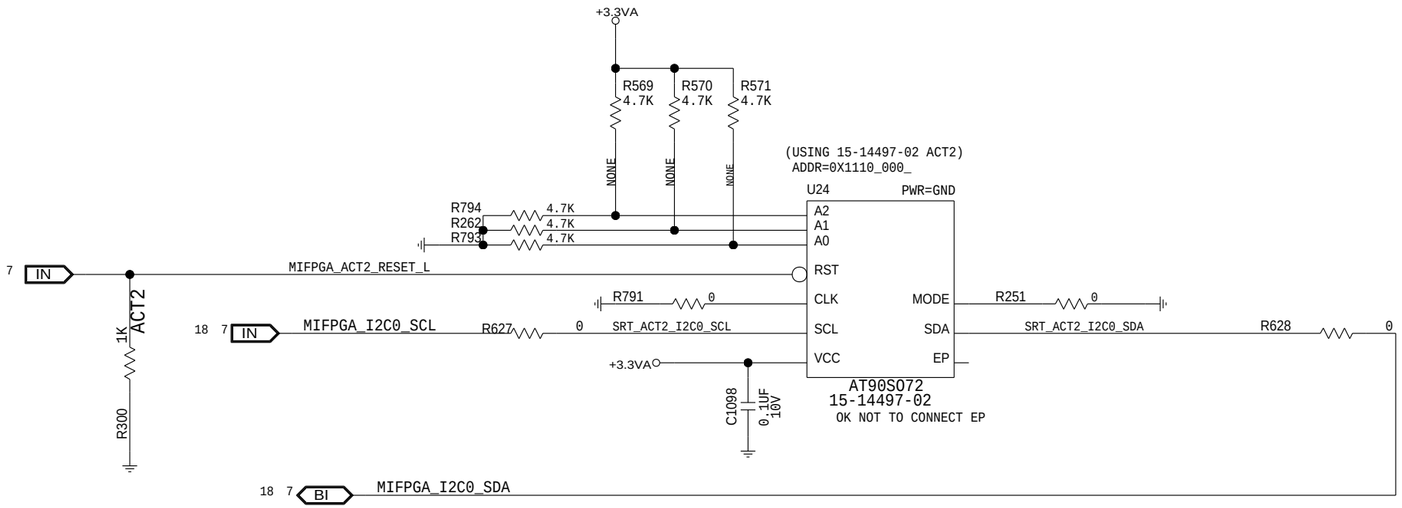
IO EXPANDER CPLD 3

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:47 2022		15 OF 138



IO EXPANDER CPLD 4

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:45 2022		16 OF 138



ACT2

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
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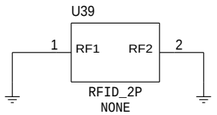
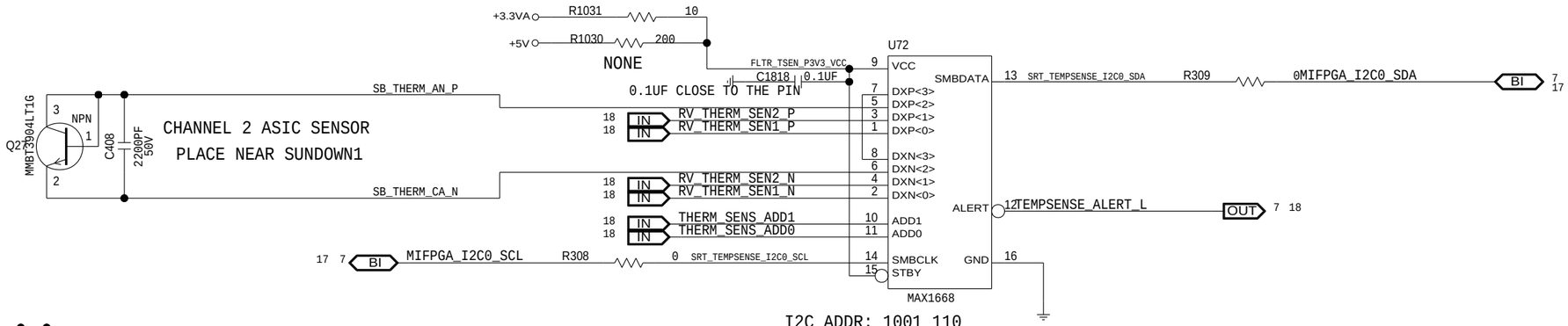
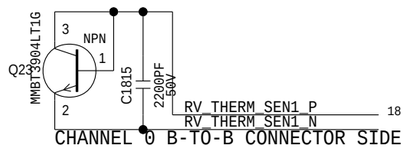
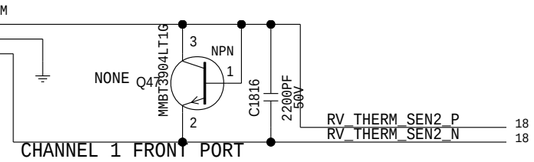
RFID

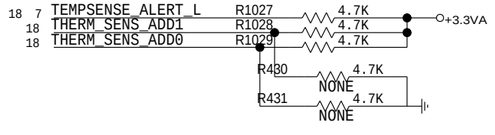






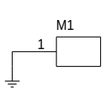
18

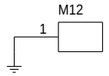


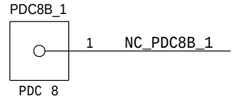


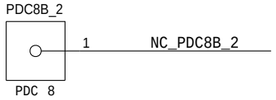
RFID, SIROM, TEMP SENSOR

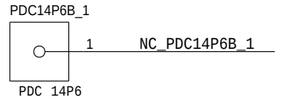
SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:41 2022		18 OF 138

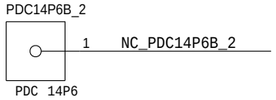


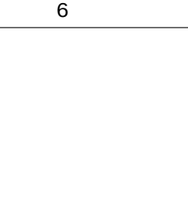


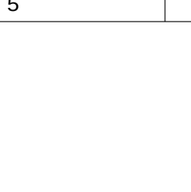


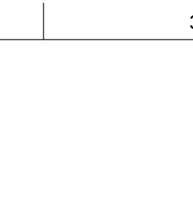


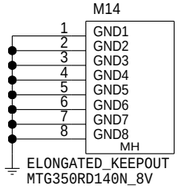


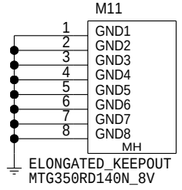












MTG HOLES

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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I1
SUBDESIGN_SUFFIX=3

SUNDOWN1_MINFW1201_CDS_491059270

sundown1_minfw1201

104	45	SNDN_HS0_RX_S0_P<3..0>	HS0_RX_S0_P<3..0>	HS0_TX_S0_P<3..0>	SNDN_HS0_TX_S0_P<3..0>	45	104
104	45	SNDN_HS0_RX_S0_N<3..0>	HS0_RX_S0_N<3..0>	HS0_TX_S0_N<3..0>	SNDN_HS0_TX_S0_N<3..0>	45	104
104	45	SNDN_HS1_RX_S0_P<3..0>	HS1_RX_S0_P<3..0>	HS1_TX_S0_P<3..0>	SNDN_HS1_TX_S0_P<3..0>	45	104
104	45	SNDN_HS1_RX_S0_N<3..0>	HS1_RX_S0_N<3..0>	HS1_TX_S0_N<3..0>	SNDN_HS1_TX_S0_N<3..0>	45	104
104	44	SNDN_HS2_RX_S0_P<3..0>	HS2_RX_S0_P<3..0>	HS2_TX_S0_P<3..0>	SNDN_HS2_TX_S0_P<3..0>	44	104
104	44	SNDN_HS2_RX_S0_N<3..0>	HS2_RX_S0_N<3..0>	HS2_TX_S0_N<3..0>	SNDN_HS2_TX_S0_N<3..0>	44	104
104	44	SNDN_HS3_RX_S0_P<3..0>	HS3_RX_S0_P<3..0>	HS3_TX_S0_P<3..0>	SNDN_HS3_TX_S0_P<3..0>	44	104
104	44	SNDN_HS3_RX_S0_N<3..0>	HS3_RX_S0_N<3..0>	HS3_TX_S0_N<3..0>	SNDN_HS3_TX_S0_N<3..0>	44	104
104	44	SNDN_HS4_RX_S0_P<3..0>	HS4_RX_S0_P<3..0>	HS4_TX_S0_P<3..0>	SNDN_HS4_TX_S0_P<3..0>	44	104
104	44	SNDN_HS4_RX_S0_N<3..0>	HS4_RX_S0_N<3..0>	HS4_TX_S0_N<3..0>	SNDN_HS4_TX_S0_N<3..0>	44	104
104	44	SNDN_HS5_RX_S0_P<3..0>	HS5_RX_S0_P<3..0>	HS5_TX_S0_P<3..0>	SNDN_HS5_TX_S0_P<3..0>	44	104
104	44	SNDN_HS5_RX_S0_N<3..0>	HS5_RX_S0_N<3..0>	HS5_TX_S0_N<3..0>	SNDN_HS5_TX_S0_N<3..0>	44	104
104	43	SNDN_HS6_RX_S0_P<3..0>	HS6_RX_S0_P<3..0>	HS6_TX_S0_P<3..0>	SNDN_HS6_TX_S0_P<3..0>	43	104
104	43	SNDN_HS6_RX_S0_N<3..0>	HS6_RX_S0_N<3..0>	HS6_TX_S0_N<3..0>	SNDN_HS6_TX_S0_N<3..0>	43	104
104	43	SNDN_HS7_RX_S0_P<3..0>	HS7_RX_S0_P<3..0>	HS7_TX_S0_P<3..0>	SNDN_HS7_TX_S0_P<3..0>	43	104
104	43	SNDN_HS7_RX_S0_N<3..0>	HS7_RX_S0_N<3..0>	HS7_TX_S0_N<3..0>	SNDN_HS7_TX_S0_N<3..0>	43	104
104	43	SNDN_HS8_RX_S0_P<3..0>	HS8_RX_S0_P<3..0>	HS8_TX_S0_P<3..0>	SNDN_HS8_TX_S0_P<3..0>	43	104
104	43	SNDN_HS8_RX_S0_N<3..0>	HS8_RX_S0_N<3..0>	HS8_TX_S0_N<3..0>	SNDN_HS8_TX_S0_N<3..0>	43	104
105	43	SNDN_HS9_RX_S0_P<3..0>	HS9_RX_S0_P<3..0>	HS9_TX_S0_P<3..0>	SNDN_HS9_TX_S0_P<3..0>	43	105
105	43	SNDN_HS9_RX_S0_N<3..0>	HS9_RX_S0_N<3..0>	HS9_TX_S0_N<3..0>	SNDN_HS9_TX_S0_N<3..0>	43	105
105	42	SNDN_HS10_RX_S0_P<3..0>	HS10_RX_S0_P<3..0>	HS10_TX_S0_P<3..0>	SNDN_HS10_TX_S0_P<3..0>	42	105
105	42	SNDN_HS10_RX_S0_N<3..0>	HS10_RX_S0_N<3..0>	HS10_TX_S0_N<3..0>	SNDN_HS10_TX_S0_N<3..0>	42	105
105	42	SNDN_HS11_RX_S0_P<3..0>	HS11_RX_S0_P<3..0>	HS11_TX_S0_P<3..0>	SNDN_HS11_TX_S0_P<3..0>	42	105
105	42	SNDN_HS11_RX_S0_N<3..0>	HS11_RX_S0_N<3..0>	HS11_TX_S0_N<3..0>	SNDN_HS11_TX_S0_N<3..0>	42	105
105	42	SNDN_HS12_RX_S0_P<3..0>	HS12_RX_S0_P<3..0>	HS12_TX_S0_P<3..0>	SNDN_HS12_TX_S0_P<3..0>	42	105
105	42	SNDN_HS12_RX_S0_N<3..0>	HS12_RX_S0_N<3..0>	HS12_TX_S0_N<3..0>	SNDN_HS12_TX_S0_N<3..0>	42	105
105	42	SNDN_HS13_RX_S0_P<3..0>	HS13_RX_S0_P<3..0>	HS13_TX_S0_P<3..0>	SNDN_HS13_TX_S0_P<3..0>	42	105
105	42	SNDN_HS13_RX_S0_N<3..0>	HS13_RX_S0_N<3..0>	HS13_TX_S0_N<3..0>	SNDN_HS13_TX_S0_N<3..0>	42	105
105	41	SNDN_HS14_RX_S0_P<3..0>	HS14_RX_S0_P<3..0>	HS14_TX_S0_P<3..0>	SNDN_HS14_TX_S0_P<3..0>	41	105
105	41	SNDN_HS14_RX_S0_N<3..0>	HS14_RX_S0_N<3..0>	HS14_TX_S0_N<3..0>	SNDN_HS14_TX_S0_N<3..0>	41	105
105	41	SNDN_HS15_RX_S0_P<3..0>	HS15_RX_S0_P<3..0>	HS15_TX_S0_P<3..0>	SNDN_HS15_TX_S0_P<3..0>	41	105
105	41	SNDN_HS15_RX_S0_N<3..0>	HS15_RX_S0_N<3..0>	HS15_TX_S0_N<3..0>	SNDN_HS15_TX_S0_N<3..0>	41	105
105	41	SNDN_HS16_RX_S0_P<3..0>	HS16_RX_S0_P<3..0>	HS16_TX_S0_P<3..0>	SNDN_HS16_TX_S0_P<3..0>	41	105
105	41	SNDN_HS16_RX_S0_N<3..0>	HS16_RX_S0_N<3..0>	HS16_TX_S0_N<3..0>	SNDN_HS16_TX_S0_N<3..0>	41	105
105	41	SNDN_HS17_RX_S0_P<3..0>	HS17_RX_S0_P<3..0>	HS17_TX_S0_P<3..0>	SNDN_HS17_TX_S0_P<3..0>	41	105
105	41	SNDN_HS17_RX_S0_N<3..0>	HS17_RX_S0_N<3..0>	HS17_TX_S0_N<3..0>	SNDN_HS17_TX_S0_N<3..0>	41	105

SUNDOWN PORTS

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B		92-105229-01	A0
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PCIE BUS CONNECTOR NETNAME ALIAS "CPU<<>>SNDN1"

4 IN HSD_PE_CPU_SA_LN0_P — ALIAS — HSD_PE_CPU_DAV_P\BASE — OUT 21 106
4 IN HSD_PE_CPU_SA_LN0_N — ALIAS — HSD_PE_CPU_DAV_N\BASE — OUT 21 106

4 OUT HSD_PE_SA_CPU_LN0_P — ALIAS — HSD_PE_DAV_CPU_P\BASE — IN 21 106
4 OUT HSD_PE_SA_CPU_LN0_N — ALIAS — HSD_PE_DAV_CPU_N\BASE — IN 21 106

I74

SUBDESIGN_SUFFIX=3

SUNDOWN1_MINFW1201_CDS_491059270

106 21 IN HSD_PE_CPU_DAV_P → PCIE_RX_P
106 21 IN HSD_PE_CPU_DAV_N → PCIE_RX_N

PCIE_TX_P → HSD_PE_DAV_CPU_P → OUT 21 106
PCIE_TX_N → HSD_PE_DAV_CPU_N → OUT 21 106

+3.3V — NONE — R1011 130 — R1010 82.5 NONE
NONE — R1012 130 — R1009 82.5 NONE

31 IN SNDN_PCIE_100MHZ_REFCLK_P — C727 0.1UF — 106 AC_PCIE_100MHZ_REFCLK_P → AC_PCIE_100MHZ_REFCLK_P
31 IN SNDN_PCIE_100MHZ_REFCLK_N — C728 0.1UF — 106 AC_PCIE_100MHZ_REFCLK_N → AC_PCIE_100MHZ_REFCLK_N

106 40 IN CLK103M_DAV_SNDN1_CORE_REFCLK_P → CORE_103MHZ_REFCLK_P
106 40 IN CLK103M_DAV_SNDN1_CORE_REFCLK_N → CORE_103MHZ_REFCLK_N

106 32 IN CLK156M25_BUF_MM_BOT_REFCLK_P → REFCLK_156P25_BOT_P
106 32 IN CLK156M25_BUF_MM_BOT_REFCLK_N → REFCLK_156P25_BOT_N

106 32 IN CLK156M25_BUF_MM_SIDE_REFCLK_P → REFCLK_156P25_SIDE_P
106 32 IN CLK156M25_BUF_MM_SIDE_REFCLK_N → REFCLK_156P25_SIDE_N

sundown1_minfw1201

106 32 IN CLK156M25_BUF_MM_TOP_REFCLK_P → REFCLK_156P25_TOP_P
106 32 IN CLK156M25_BUF_MM_TOP_REFCLK_N → REFCLK_156P25_TOP_N

106 32 IN CLK212M_BUF_FC_BOT_REFCLK_P → REFCLK_212P5_BOT_P
106 32 IN CLK212M_BUF_FC_BOT_REFCLK_N → REFCLK_212P5_BOT_N

106 32 IN CLK212M_BUF_FC_SIDE_REFCLK_P → REFCLK_212P5_SIDE_P
106 32 IN CLK212M_BUF_FC_SIDE_REFCLK_N → REFCLK_212P5_SIDE_N

106 32 IN CLK212M_BUF_FC_TOP_REFCLK_P → REFCLK_212P5_TOP_P
106 32 IN CLK212M_BUF_FC_TOP_REFCLK_N → REFCLK_212P5_TOP_N

106 11 IN LAN1_PORT0_CPU_TX_P → CPU_SGMII_SDC0_RX_P
106 11 IN LAN1_PORT0_CPU_TX_N → CPU_SGMII_SDC0_RX_N

CPU_SGMII_SDC0_TX_P → LAN1_PORT0_CPU_RX_P → OUT 11 106
CPU_SGMII_SDC0_TX_N → LAN1_PORT0_CPU_RX_N → OUT 11 106

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
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I17

SUBDESIGN_SUFFIX=3

SUNDOWN1_MINFW1201_CDS_491059270

VDD_P0V875

VDD_0P875V

+0.8V

VDDA_0P9V

VDDA_CLK_0P9V

VDDA_TX_0P9V

VDDHA_1P2V

VDDHA_1P2V

52 OUT VDDHA_FLTR_SENSE — R218 0 — 108 FLTR_VDDHA_1P2V

FLTR_VDDHA_1P2V

FOR MONITRING ONLY
DO NOT CONNECT TO POWER

PLACE CLOSE TO SUNDN

P1V8

VDDIO_1P8V

VDDA_PLL_1P8V

sundown1_minfw1201

VDD_SENSE_P — SNDN_VDD_SENSE_P — OUT 52 109

VSS_SENSE_N — SNDN_VSS_SENSE_N — OUT 52 110

VDDQ_EFUSE_PD NC

106 23 IN SNDN_CPU2JTAG_EN — CPU2JTAG_EN

106 23 IN SNDN_JTAG2CPU_EN — JTAG2ECPU_EN

106 57 IN JTAG_SNDN_TDI — JTAG_TDI

106 57 IN JTAG_SNDN_TCK — JTAG_TCK

106 57 IN JTAG_SNDN_TMS — JTAG_TMS

106 57 IN JTAG_SNDN_TRST_L — JTAG_TRST_L

JTAG_TDO — JTAG_SNDN_TDO — OUT 57 106

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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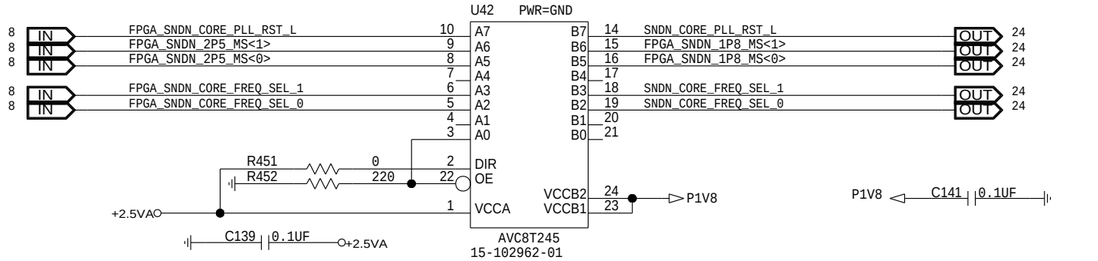
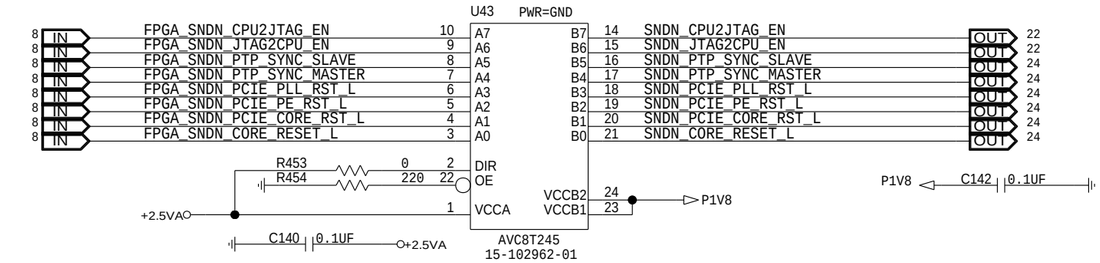
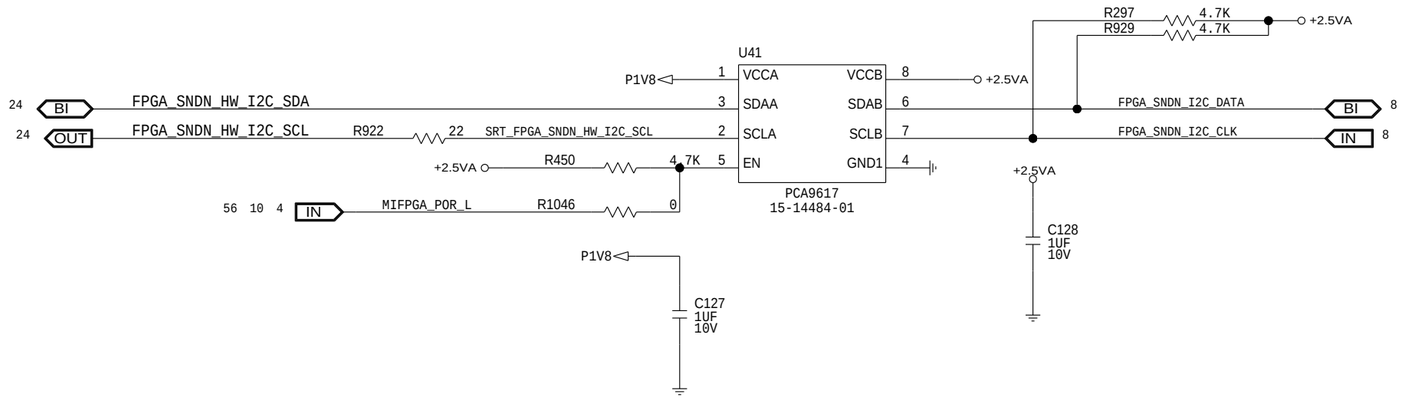




CHANGE RAIL LEVEL TO 2.5



SNDN IO LEVEL SHIFTER

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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PCIE_RREF TERMINATED IN SUBDESIGN

I75
SUBDESIGN_SUFFIX=3

SUNDOWN1_MINFW1201_CDS_491059270

sundown1_minfw1201

106	23	IN	SNDN_PTP_SYNC_SLAVE	PTP_SYNC_SLAVE	MS1	FPGA_SNDN_1P8_MS<1>	IN	23	106
106	23	IN	SNDN_PTP_SYNC_MASTER	PTP_SYNC_MASTER	MS0	FPGA_SNDN_1P8_MS<0>	IN	23	106
106		IN	SNDN_PCIE_RREF	PCIE_RREF	HW_I2C_SDA	FPGA_SNDN_HW_I2C_SDA	BI	23	106
106		IN	SNDN_USR_DRV_EN	PCIE_USR_DRV_EN	HW_I2C_SCL	FPGA_SNDN_HW_I2C_SCL	IN	23	106
106	23	IN	SNDN_PCIE_PLL_RST_L	PCIE_PLL_RST_L	GPIO21	FPGA_SNDN_GPIO21	BI	106	
106		IN	SNDN_PCIE_PLL_BYP	PCIE_PLL_BYP	GPIO20	FPGA_SNDN_GPIO20	BI	106	
106	23	IN	SNDN_PCIE_PE_RST_L	PCIE_PE_RST_L	GPIO19	FPGA_SNDN_GPIO19	BI	106	
106	23	IN	SNDN_PCIE_CORE_RST_L	PCIE_CORE_RST_L	GPIO18	FPGA_SNDN_GPIO18	BI	106	
106		IN	SNDN_EXTLOOP_EN	EXTLOOP_EN	GPIO17	FPGA_SNDN_GPIO17	BI	106	
106	23	IN	SNDN_CORE_PLL_RST_L	CORE_PLL_RST_L	GPIO16	FPGA_SNDN_GPIO16	BI	106	
106		IN	SNDN_CORE_PLL_BYP	CORE_PLL_BYP	GPIO15	FPGA_SNDN_GPIO15	BI	106	
106	23	IN	SNDN_CORE_RESET_L	CORE_RESET_L	GPIO14	FPGA_SNDN_GPIO14	BI	106	
106	23	IN	SNDN_CORE_FREQ_SEL_1	CORE_FREQ_SEL_1	GPIO13	FPGA_SNDN_GPIO13	BI	106	
106	23	IN	SNDN_CORE_FREQ_SEL_0	CORE_FREQ_SEL_0	GPIO12	FPGA_SNDN_GPIO12	BI	106	
					GPIO11	FPGA_SNDN_GPIO11	BI	106	
					GPIO10	FPGA_SNDN_GPIO10	BI	106	
					GPIO9	FPGA_SNDN_GPIO9	BI	106	
					GPIO8	FPGA_SNDN_GPIO8	BI	106	
					GPIO7	FPGA_SNDN_GPIO7	BI	106	
					GPIO6	FPGA_SNDN_GPIO6	BI	106	
					GPIO5	FPGA_SNDN_GPIO5	BI	106	
					FUSE_FSRC				

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
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SUBDESIGN_SUFFIX=RT1_2 I1

BEARVALLEYX2_SUB
REV01

FROM ASIC / TO ASIC

74 41 IN HSD_RT_HOST_HS17_TX_S0_P<3..0> → BV0P0_HOST_IN_P<3..0>
74 41 IN HSD_RT_HOST_HS17_TX_S0_N<3..0> → BV0P0_HOST_IN_N<3..0>
BV0P0_HOST_OUT_P<3..0> → HSD_RT_HOST_HS17_RX_S0_P<3..0> OUT 41 74
BV0P0_HOST_OUT_N<3..0> → HSD_RT_HOST_HS17_RX_S0_N<3..0> OUT 41 74

74 41 IN HSD_RT_HOST_HS16_TX_S0_P<3..0> → BV0P1_HOST_IN_P<3..0>
74 41 IN HSD_RT_HOST_HS16_TX_S0_N<3..0> → BV0P1_HOST_IN_N<3..0>
BV0P1_HOST_OUT_P<3..0> → HSD_RT_HOST_HS16_RX_S0_P<3..0> OUT 41 74
BV0P1_HOST_OUT_N<3..0> → HSD_RT_HOST_HS16_RX_S0_N<3..0> OUT 41 74

76 41 IN HSD_RT_HOST_HS15_TX_S0_P<3..0> → BV1P0_HOST_IN_P<3..0>
76 41 IN HSD_RT_HOST_HS15_TX_S0_N<3..0> → BV1P0_HOST_IN_N<3..0>
BV1P0_HOST_OUT_P<3..0> → HSD_RT_HOST_HS15_RX_S0_P<3..0> OUT 41 76
BV1P0_HOST_OUT_N<3..0> → HSD_RT_HOST_HS15_RX_S0_N<3..0> OUT 41 76

76 41 IN HSD_RT_HOST_HS14_TX_S0_P<3..0> → BV1P1_HOST_IN_P<3..0>
76 41 IN HSD_RT_HOST_HS14_TX_S0_N<3..0> → BV1P1_HOST_IN_N<3..0>
BV1P1_HOST_OUT_P<3..0> → HSD_RT_HOST_HS14_RX_S0_P<3..0> OUT 41 76
BV1P1_HOST_OUT_N<3..0> → HSD_RT_HOST_HS14_RX_S0_N<3..0> OUT 41 76

FROM SFP / TO SFP

74 41 IN HSD_RT_LINE_OUT_P<3..0> → BV0P0_LINE_IN_P<3..0>
74 41 IN HSD_RT_LINE_OUT_N<3..0> → BV0P0_LINE_IN_N<3..0>
BV0P0_LINE_OUT_P<3..0> → HSD_RT_LINE_IN_P<3..0> OUT 41 74
BV0P0_LINE_OUT_N<3..0> → HSD_RT_LINE_IN_N<3..0> OUT 41 74

74 41 IN HSD_RT_LINE_OUT_P<7..4> → BV0P1_LINE_IN_P<3..0>
74 41 IN HSD_RT_LINE_OUT_N<7..4> → BV0P1_LINE_IN_N<3..0>
BV0P1_LINE_OUT_P<3..0> → HSD_RT_LINE_IN_P<7..4> OUT 41 74
BV0P1_LINE_OUT_N<3..0> → HSD_RT_LINE_IN_N<7..4> OUT 41 74

76 41 IN HSD_RT_LINE_OUT_P<11..8> → BV1P0_LINE_IN_P<3..0>
76 41 IN HSD_RT_LINE_OUT_N<11..8> → BV1P0_LINE_IN_N<3..0>
BV1P0_LINE_OUT_P<3..0> → HSD_RT_LINE_IN_P<11..8> OUT 41 76
BV1P0_LINE_OUT_N<3..0> → HSD_RT_LINE_IN_N<11..8> OUT 41 76

76 41 IN HSD_RT_LINE_OUT_P<15..12> → BV1P1_LINE_IN_P<3..0>
76 41 IN HSD_RT_LINE_OUT_N<15..12> → BV1P1_LINE_IN_N<3..0>
BV1P1_LINE_OUT_P<3..0> → HSD_RT_LINE_IN_P<15..12> OUT 41 76
BV1P1_LINE_OUT_N<3..0> → HSD_RT_LINE_IN_N<15..12> OUT 41 76

74 33 IN CLK156M_RT1_P → BV0_CLK_IN_P
74 33 IN CLK156M_RT1_N → BV0_CLK_IN_N
76 33 IN CLK156M_RT2_P → BV1_CLK_IN_P
76 33 IN CLK156M_RT2_N → BV1_CLK_IN_N

74 8 IN RT1_RESET_L → BV0_RESET_L
76 8 IN RT2_RESET_L → BV1_RESET_L

74 25 IN RT1_ADDR<4..1> IPD → BV0_ADDR<4..1>
76 25 IN RT2_ADDR<4..1> IPD → BV1_ADDR<4..1>

74 58 IN JTAG_TDO_ZL_TDI_RT1_2V5 → BV_TDI
74 58 26 IN JTAG_TMS_RT1_RT2_RT3_RT4_2V5 → BV_TMS
74 58 IN JTAG_TCK_RT1_2V5 → BV0_TCK
76 58 IN JTAG_TCK_RT2_2V5 → BV1_TCK
74 58 26 IN JTAG_TRST_L_RT1_RT2_RT3_RT4_2V5 → BV_TRST_L

BV0_INT_L → RT1_M2_0_7_SYNCE_CLK OUT 74
BV1_INT_L → RT2_M2_0_7_SYNCE_CLK OUT 76

BV0_SDC_MDC → RT1_MDIO_SCL OUT 8 74
BV0_SDC_MDIO → RT1_MDIO_SDA BI 8 74
BV1_SDC_MDC → RT2_MDIO_SCL OUT 8 76
BV1_SDC_MDIO → RT2_MDIO_SDA BI 8 76

BV0_SCL → 74 SRT_RT1_M4_0_3_SYNCE_CLK 33 R253 RT1_M4_0_3_SYNCE_CLK OUT 7
BV0_SDA → 74 SRT_RT1_M4_4_7_SYNCE_CLK 33 R255 RT1_M4_4_7_SYNCE_CLK OUT 7
BV1_SCL → 76 SRT_RT2_M4_0_3_SYNCE_CLK 33 R257 RT2_M4_0_3_SYNCE_CLK OUT 7
BV1_SDA → 76 SRT_RT2_M4_4_7_SYNCE_CLK 33 R259 RT2_M4_4_7_SYNCE_CLK OUT 7

BV_TDO → P2V5RT1 NONE R552 4.7K → JTAG_TDO_RT2_TDI_RT3_2V5 OUT 26 76

P2V5RT1 → VDDO_P2V5
P1V0RT1_DVDD → DVDD_P1V0
P1V0RT1_AVDD → AVDD_P1V0

R555 0 NONE

P2V5RT1 →
4.7K NONE R133 RT1_ADDR<4> OUT 25 74
4.7K NONE R147 RT1_ADDR<3> OUT 25 74
4.7K NONE R161 RT1_ADDR<2> OUT 25 74
4.7K R164 RT1_ADDR<1> OUT 25 74

4.7K NONE R174 RT2_ADDR<4> OUT 25 76
4.7K NONE R199 RT2_ADDR<3> OUT 25 76
4.7K NONE R201 RT2_ADDR<2> OUT 25 76
4.7K R203 RT2_ADDR<1> OUT 25 76

CISCO

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SUBDESIGN_SUFFIX=RT3_4

I1

BEARVALLEYX2_SUB

REV01

79 42	IN	HSD_RT_HOST_HS13_TX_S0_P<3..0>	BV0P0_HOST_IN_P<3..0>	BV0P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS13_RX_S0_P<3..0>	OUT	42 79
79 42	IN	HSD_RT_HOST_HS13_TX_S0_N<3..0>	BV0P0_HOST_IN_N<3..0>	BV0P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS13_RX_S0_N<3..0>	OUT	42 79
79 42	IN	HSD_RT_HOST_HS12_TX_S0_P<3..0>	BV0P1_HOST_IN_P<3..0>	BV0P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS12_RX_S0_P<3..0>	OUT	42 79
79 42	IN	HSD_RT_HOST_HS12_TX_S0_N<3..0>	BV0P1_HOST_IN_N<3..0>	BV0P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS12_RX_S0_N<3..0>	OUT	42 79
81 42	IN	HSD_RT_HOST_HS11_TX_S0_P<3..0>	BV1P0_HOST_IN_P<3..0>	BV1P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS11_RX_S0_P<3..0>	OUT	42 81
81 42	IN	HSD_RT_HOST_HS11_TX_S0_N<3..0>	BV1P0_HOST_IN_N<3..0>	BV1P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS11_RX_S0_N<3..0>	OUT	42 81
81 42	IN	HSD_RT_HOST_HS10_TX_S0_P<3..0>	BV1P1_HOST_IN_P<3..0>	BV1P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS10_RX_S0_P<3..0>	OUT	42 81
81 42	IN	HSD_RT_HOST_HS10_TX_S0_N<3..0>	BV1P1_HOST_IN_N<3..0>	BV1P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS10_RX_S0_N<3..0>	OUT	42 81
79 42	IN	HSD_RT_LINE_OUT_P<19..16>	BV0P0_LINE_IN_P<3..0>	BV0P0_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<19..16>	OUT	42 79
79 42	IN	HSD_RT_LINE_OUT_N<19..16>	BV0P0_LINE_IN_N<3..0>	BV0P0_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<19..16>	OUT	42 79
79 42	IN	HSD_RT_LINE_OUT_P<23..20>	BV0P1_LINE_IN_P<3..0>	BV0P1_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<23..20>	OUT	42 79
79 42	IN	HSD_RT_LINE_OUT_N<23..20>	BV0P1_LINE_IN_N<3..0>	BV0P1_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<23..20>	OUT	42 79
81 42	IN	HSD_RT_LINE_OUT_P<27..24>	BV1P0_LINE_IN_P<3..0>	BV1P0_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<27..24>	OUT	42 81
81 42	IN	HSD_RT_LINE_OUT_N<27..24>	BV1P0_LINE_IN_N<3..0>	BV1P0_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<27..24>	OUT	42 81
81 42	IN	HSD_RT_LINE_OUT_P<31..28>	BV1P1_LINE_IN_P<3..0>	BV1P1_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<31..28>	OUT	42 81
81 42	IN	HSD_RT_LINE_OUT_N<31..28>	BV1P1_LINE_IN_N<3..0>	BV1P1_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<31..28>	OUT	42 81
79 33	IN	CLK156M_RT3_P	BV0_CLK_IN_P	BV0_INT_L	RT3_M2_0_7_SYNCE_CLK	OUT	79
79 33	IN	CLK156M_RT3_N	BV0_CLK_IN_N	BV1_INT_L	RT4_M2_0_7_SYNCE_CLK	OUT	81
81 33	IN	CLK156M_RT4_P	BV1_CLK_IN_P	BV0_SDC_MDC	RT3_MDIO_SCL	OUT	8 79
81 33	IN	CLK156M_RT4_N	BV1_CLK_IN_N	BV0_SDC_MDIO	RT3_MDIO_SDA	BI	8 79
79 8	IN	RT3_RESET_L	BV0_RESET_L	BV1_SDC_MDC	RT4_MDIO_SCL	OUT	8 81
81 8	IN	RT4_RESET_L	BV1_RESET_L	BV1_SDC_MDIO	RT4_MDIO_SDA	BI	8 81
79 26	IN	RT3_ADDR<4..1>	BV0_ADDR<4..1>	BV0_SCL	79 SRT_RT3_M4_0_3_SYNCE_CLK 33 R261	RT3_M4_0_3_SYNCE_CLK	OUT 7
81 26	IN	RT4_ADDR<4..1>	BV1_ADDR<4..1>	BV0_SDA	79 SRT_RT3_M4_4_7_SYNCE_CLK 33 R264	RT3_M4_4_7_SYNCE_CLK	OUT 7
				BV1_SCL	81 SRT_RT4_M4_0_3_SYNCE_CLK 33 R265	RT4_M4_0_3_SYNCE_CLK	OUT 7
				BV1_SDA	81 SRT_RT4_M4_4_7_SYNCE_CLK 33 R267	RT4_M4_4_7_SYNCE_CLK	OUT 7

25 IN JTAG_TDO_RT2_TDI_RT3_2V5 — R286 0 — 79 JTAG_TDO_RT3_RT4_2V5RT

79 58 25	IN	JTAG_TMS_RT1_RT2_RT3_RT4_2V5	BV_TDI
79 58	IN	JTAG_TCK_RT3_2V5	BV_TMS
81 58	IN	JTAG_TCK_RT4_2V5	BV0_TCK
79 58 25	IN	JTAG_TRST_L_RT1_RT2_RT3_RT4_2V5	BV1_TCK
			BV_TRST_L
			BV_TDO

P2V5RT1

NONE

R108 4.7K

R121 0 NONE

JTAG_TDO_RT4_TDI_RT5_2V5 OUT 27 81

P2V5RT1	VDDO_P2V5				
P1V0RT1_DVDD	DVDD_P1V0				
P1V0RT1_AVDD	AVDD_P1V0				

P2V5RT1

4.7K NONE	R208	RT3_ADDR<4>	OUT	26	79
4.7K NONE	R210	RT3_ADDR<3>	OUT	26	79
4.7K NONE	R221	RT3_ADDR<2>	OUT	26	79
4.7K	R223	RT3_ADDR<1>	OUT	26	79
4.7K NONE	R226	RT4_ADDR<4>	OUT	26	81
4.7K NONE	R228	RT4_ADDR<3>	OUT	26	81
4.7K NONE	R230	RT4_ADDR<2>	OUT	26	81
4.7K	R232	RT4_ADDR<1>	OUT	26	81

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SUBDESIGN_SUFFIX=RT5_6

I1

BEARVALLEYX2_SUB

REV01

84	43	IN	HSD_RT_HOST_HS9_TX_S0_P<3..0>	BV0P0_HOST_IN_P<3..0>	BV0P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS9_RX_S0_P<3..0>	OUT	43	84
84	43	IN	HSD_RT_HOST_HS9_TX_S0_N<3..0>	BV0P0_HOST_IN_N<3..0>	BV0P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS9_RX_S0_N<3..0>	OUT	43	84
84	43	IN	HSD_RT_HOST_HS8_TX_S0_P<3..0>	BV0P1_HOST_IN_P<3..0>	BV0P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS8_RX_S0_P<3..0>	OUT	43	84
84	43	IN	HSD_RT_HOST_HS8_TX_S0_N<3..0>	BV0P1_HOST_IN_N<3..0>	BV0P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS8_RX_S0_N<3..0>	OUT	43	84
86	43	IN	HSD_RT_HOST_HS7_TX_S0_P<3..0>	BV1P0_HOST_IN_P<3..0>	BV1P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS7_RX_S0_P<3..0>	OUT	43	86
86	43	IN	HSD_RT_HOST_HS7_TX_S0_N<3..0>	BV1P0_HOST_IN_N<3..0>	BV1P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS7_RX_S0_N<3..0>	OUT	43	86
86	43	IN	HSD_RT_HOST_HS6_TX_S0_P<3..0>	BV1P1_HOST_IN_P<3..0>	BV1P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS6_RX_S0_P<3..0>	OUT	43	86
86	43	IN	HSD_RT_HOST_HS6_TX_S0_N<3..0>	BV1P1_HOST_IN_N<3..0>	BV1P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS6_RX_S0_N<3..0>	OUT	43	86
84	43	IN	HSD_RT_LINE_OUT_P<35..32>	BV0P0_LINE_IN_P<3..0>	BV0P0_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<35..32>	OUT	43	84
84	43	IN	HSD_RT_LINE_OUT_N<35..32>	BV0P0_LINE_IN_N<3..0>	BV0P0_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<35..32>	OUT	43	84
84	43	IN	HSD_RT_LINE_OUT_P<39..36>	BV0P1_LINE_IN_P<3..0>	BV0P1_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<39..36>	OUT	43	84
84	43	IN	HSD_RT_LINE_OUT_N<39..36>	BV0P1_LINE_IN_N<3..0>	BV0P1_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<39..36>	OUT	43	84
86	43	IN	HSD_RT_LINE_OUT_P<43..40>	BV1P0_LINE_IN_P<3..0>	BV1P0_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<43..40>	OUT	43	86
86	43	IN	HSD_RT_LINE_OUT_N<43..40>	BV1P0_LINE_IN_N<3..0>	BV1P0_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<43..40>	OUT	43	86
86	43	IN	HSD_RT_LINE_OUT_P<47..44>	BV1P1_LINE_IN_P<3..0>	BV1P1_LINE_OUT_P<3..0>	HSD_RT_LINE_IN_P<47..44>	OUT	43	86
86	43	IN	HSD_RT_LINE_OUT_N<47..44>	BV1P1_LINE_IN_N<3..0>	BV1P1_LINE_OUT_N<3..0>	HSD_RT_LINE_IN_N<47..44>	OUT	43	86

84	33	IN	CLK156M_RT5_P	BV0_CLK_IN_P	BV0_INT_L	RT5_M2_0_7_SYNCE_CLK	OUT	84	
84	33	IN	CLK156M_RT5_N	BV0_CLK_IN_N					
86	33	IN	CLK156M_RT6_P	BV1_CLK_IN_P	BV1_INT_L	RT6_M2_0_7_SYNCE_CLK	OUT	86	
86	33	IN	CLK156M_RT6_N	BV1_CLK_IN_N					
84	8	IN	RT5_RESET_L	BV0_RESET_L	BV0_SDC_MDC	RT5_MDIO_SCL	OUT	8	84
86	8	IN	RT6_RESET_L	BV1_RESET_L	BV0_SDC_MDIO	RT5_MDIO_SDA	BI	8	84
84	27	IN	RT5_ADDR<4..1>	IPD BV0_ADDR<4..1>	BV1_SDC_MDC	RT6_MDIO_SCL	OUT	8	86
86	27	IN	RT6_ADDR<4..1>	IPD BV1_ADDR<4..1>	BV1_SDC_MDIO	RT6_MDIO_SDA	BI	8	86

BV0_SCL	84	SRT_RT5_M4_0_3_SYNCE_CLK	33	R269	RT5_M4_0_3_SYNCE_CLK	OUT	7
BV0_SDA	84	SRT_RT5_M4_4_7_SYNCE_CLK	33	R271	RT5_M4_4_7_SYNCE_CLK	OUT	8
BV1_SCL	86	SRT_RT6_M4_0_3_SYNCE_CLK	33	R273	RT6_M4_0_3_SYNCE_CLK	OUT	8
BV1_SDA	86	SRT_RT6_M4_4_7_SYNCE_CLK	33	R275	RT6_M4_4_7_SYNCE_CLK	OUT	8

26 IN JTAG_TDO_RT4_TDI_RT5_2V5 — R287 84 0 JTAG_TDO_RT5_RT6_2V5RT

84	58 29 28	IN	JTAG_TMS_RT5_RT6_RT7_RT8_RT9_2V5	BV_TDI	
84	58	IN	JTAG_TCK_RT5_2V5	BV_TMS	
86	58	IN	JTAG_TCK_RT6_2V5	BV0_TCK	
84	58 29 28	IN	JTAG_TRST_L_RT5_RT6_RT7_RT8_RT9_2V5	BV1_TCK	
				BV_TRST_L	BV_TDO

P2V5RT2

NONE

R110

4.7K

P2V5RT2			VDDO_P2V5		
P1V0RT2_DVDD			DVDD_P1V0		
P1V0RT2_AVDD			AVDD_P1V0		

R122 0 NONE — JTAG_TDO_RT6_TDI_RT7_2V5 OUT 28 86

P2V5RT1

4.7K NONE	R237	RT5_ADDR<4>	OUT	27	84
4.7K NONE	R239	RT5_ADDR<3>	OUT	27	84
4.7K NONE	R241	RT5_ADDR<2>	OUT	27	84
4.7K	R243	RT5_ADDR<1>	OUT	27	84
4.7K NONE	R246	RT6_ADDR<4>	OUT	27	86
4.7K NONE	R248	RT6_ADDR<3>	OUT	27	86
4.7K NONE	R252	RT6_ADDR<2>	OUT	27	86
4.7K	R254	RT6_ADDR<1>	OUT	27	86

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SUBDESIGN_SUFFIX=RT7_8

I1

BEARVALLEYX2_SUB

REV01

89	44	IN	HSD_RT_HOST_HS4_TX_S0_P<3..0>	BV0P0_HOST_IN_P<3..0>	BV0P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS4_RX_S0_P<3..0>	OUT	44	89
89	44	IN	HSD_RT_HOST_HS4_TX_S0_N<3..0>	BV0P0_HOST_IN_N<3..0>	BV0P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS4_RX_S0_N<3..0>	OUT	44	89
89	44	IN	HSD_RT_HOST_HS5_TX_S0_P<3..0>	BV0P1_HOST_IN_P<3..0>	BV0P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS5_RX_S0_P<3..0>	OUT	44	89
89	44	IN	HSD_RT_HOST_HS5_TX_S0_N<3..0>	BV0P1_HOST_IN_N<3..0>	BV0P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS5_RX_S0_N<3..0>	OUT	44	89
91	44	IN	HSD_RT_HOST_HS2_TX_S0_P<3..0>	BV1P0_HOST_IN_P<3..0>	BV1P0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS2_RX_S0_P<3..0>	OUT	44	91
91	44	IN	HSD_RT_HOST_HS2_TX_S0_N<3..0>	BV1P0_HOST_IN_N<3..0>	BV1P0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS2_RX_S0_N<3..0>	OUT	44	91
91	44	IN	HSD_RT_HOST_HS3_TX_S0_P<3..0>	BV1P1_HOST_IN_P<3..0>	BV1P1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS3_RX_S0_P<3..0>	OUT	44	91
91	44	IN	HSD_RT_HOST_HS3_TX_S0_N<3..0>	BV1P1_HOST_IN_N<3..0>	BV1P1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS3_RX_S0_N<3..0>	OUT	44	91
89	44	IN	HSD_RT_LINE_QSFP0_OUT_P<3..0>	BV0P0_LINE_IN_P<3..0>	BV0P0_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP0_IN_P<3..0>	OUT	44	89
89	44	IN	HSD_RT_LINE_QSFP0_OUT_N<3..0>	BV0P0_LINE_IN_N<3..0>	BV0P0_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP0_IN_N<3..0>	OUT	44	89
89	44	IN	HSD_RT_LINE_QSFP1_OUT_P<3..0>	BV0P1_LINE_IN_P<3..0>	BV0P1_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP1_IN_P<3..0>	OUT	44	89
89	44	IN	HSD_RT_LINE_QSFP1_OUT_N<3..0>	BV0P1_LINE_IN_N<3..0>	BV0P1_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP1_IN_N<3..0>	OUT	44	89
91	44	IN	HSD_RT_LINE_QSFP2_OUT_P<3..0>	BV1P0_LINE_IN_P<3..0>	BV1P0_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP2_IN_P<3..0>	OUT	44	91
91	44	IN	HSD_RT_LINE_QSFP2_OUT_N<3..0>	BV1P0_LINE_IN_N<3..0>	BV1P0_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP2_IN_N<3..0>	OUT	44	91
91	44	IN	HSD_RT_LINE_QSFP3_OUT_P<3..0>	BV1P1_LINE_IN_P<3..0>	BV1P1_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP3_IN_P<3..0>	OUT	44	91
91	44	IN	HSD_RT_LINE_QSFP3_OUT_N<3..0>	BV1P1_LINE_IN_N<3..0>	BV1P1_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP3_IN_N<3..0>	OUT	44	91

89	33	IN	CLK156M_RT7_P	BV0_CLK_IN_P	BV0_INT_L	RT7_M2_0_7_SYNCE_CLK	OUT	89	
89	33	IN	CLK156M_RT7_N	BV0_CLK_IN_N					
91	33	IN	CLK156M_RT8_P	BV1_CLK_IN_P	BV1_INT_L	RT8_M2_0_7_SYNCE_CLK	OUT	91	
91	33	IN	CLK156M_RT8_N	BV1_CLK_IN_N					
89	8	IN	RT7_RESET_L	BV0_RESET_L	BV0_SDC_MDC	RT7_MDIO_SCL	OUT	8	89
91	8	IN	RT8_RESET_L	BV1_RESET_L	BV0_SDC_MDIO	RT7_MDIO_SDA	BI	8	89
89	28	IN	RT7_ADDR<4..1> IPD	BV0_ADDR<4..1>	BV1_SDC_MDC	RT8_MDIO_SCL	OUT	8	91
91	28	IN	RT8_ADDR<4..1> IPD	BV1_ADDR<4..1>	BV1_SDC_MDIO	RT8_MDIO_SDA	BI	8	91
					BV0_SCL	SRT_RT7_M4_0_3_SYNCE_CLK 33 R276 RT7_M4_0_3_SYNCE_CLK	OUT	8	
					BV0_SDA	SRT_RT7_M4_4_7_SYNCE_CLK 33 R278 RT7_M4_4_7_SYNCE_CLK	OUT	9	
27	IN	JTAG_TDO_RT6_TDI_RT7_2V5	R288 0 89 JTAG_TDO_RT7_RT8_2V5RT	BV_TDI	BV1_SCL	SRT_RT8_M4_0_3_SYNCE_CLK 33 R280 RT8_M4_0_3_SYNCE_CLK	OUT	10	
			89 58 29 27 IN JTAG_TMS_RT5_RT6_RT7_RT8_RT9_2V5	BV_TMS	BV1_SDA	SRT_RT8_M4_4_7_SYNCE_CLK 33 R282 RT8_M4_4_7_SYNCE_CLK	OUT	10	
			89 58 IN JTAG_TCK_RT7_2V5	BV0_TCK					
			91 58 IN JTAG_TCK_RT8_2V5	BV1_TCK					
			89 58 29 27 IN JTAG_TRST_L_RT5_RT6_RT7_RT8_RT9_2V5	BV_TRST_L	BV_TDO	P2V5RT2			
						NONE R111 4.7K			
P2V5RT2				VDDO_P2V5					
P1V0RT2_DVDD				DVDD_P1V0					
P1V0RT2_AVDD				AVDD_P1V0					

R123 0 NONE — JTAG_TDO_RT8_TDI_RT9_2V5 OUT 29 91

P2V5RT1	4.7K NONE	R258	RT7_ADDR<4>	OUT	28	89
	4.7K NONE	R260	RT7_ADDR<3>	OUT	28	89
	4.7K NONE	R263	RT7_ADDR<2>	OUT	28	89
	4.7K	R266	RT7_ADDR<1>	OUT	28	89
	4.7K NONE	R268	RT8_ADDR<4>	OUT	28	91
	4.7K NONE	R270	RT8_ADDR<3>	OUT	28	91
	4.7K NONE	R272	RT8_ADDR<2>	OUT	28	91
	4.7K	R274	RT8_ADDR<1>	OUT	28	91

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1XBEARVALLY_SUB

REV01

BVP0_HOST_IN_P<3..0>		BVP0_HOST_OUT_P<3..0>	HSD_RT_HOST_HS0_RX_S0_P<3..0> OUT 45 94
BVP0_HOST_IN_N<3..0>		BVP0_HOST_OUT_N<3..0>	HSD_RT_HOST_HS0_RX_S0_N<3..0> OUT 45 94
BVP1_HOST_IN_P<3..0>		BVP1_HOST_OUT_P<3..0>	HSD_RT_HOST_HS1_RX_S0_P<3..0> OUT 45 94
BVP1_HOST_IN_N<3..0>		BVP1_HOST_OUT_N<3..0>	HSD_RT_HOST_HS1_RX_S0_N<3..0> OUT 45 94
BVP0_LINE_IN_P<3..0>		BVP0_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP4_IN_P<3..0> OUT 45 94
BVP0_LINE_IN_N<3..0>		BVP0_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP4_IN_N<3..0> OUT 45 94
BVP1_LINE_IN_P<3..0>		BVP1_LINE_OUT_P<3..0>	HSD_RT_LINE_QSFP5_IN_P<3..0> OUT 45 94
BVP1_LINE_IN_N<3..0>		BVP1_LINE_OUT_N<3..0>	HSD_RT_LINE_QSFP5_IN_N<3..0> OUT 45 94
BV_CLK_IN_P		BV_INT_L	RT9_M2_0_7_SYNCE_CLK OUT 94
BV_CLK_IN_N			
BV_RESET_L		BV_SDC_MDC	RT9_MDIO_SCL OUT 8 94
BV_PHY_ADDR4		BV_SDC_MDIO	RT9_MDIO_SDA BI 8 94
BV_PHY_ADDR3		BV_SCL	SRT-RT9_M4_0_3_SYNCE_CLK 33 R284 RT9_M4_0_3_SYNCE_CLK OUT 10
BV_PHY_ADDR2		BV_SDA	SRT_RT9_M4_4_7_SYNCE_CLK 33 R285 RT9_M4_4_7_SYNCE_CLK OUT 10
BV_PHY_ADDR1			
BV_TDI		BV_TDO	
BV_TMS			
BV_TCK			
BV_TRST_L			
VDDO_P2V5			
DVDD_P1V0			
AVDD_P1V0			

94 45 IN HSD_RT_HOST_HS0_TX_S0_P<3..0>
94 45 IN HSD_RT_HOST_HS0_TX_S0_N<3..0>
94 45 IN HSD_RT_HOST_HS1_TX_S0_P<3..0>
94 45 IN HSD_RT_HOST_HS1_TX_S0_N<3..0>
94 45 IN HSD_RT_LINE_QSFP4_OUT_P<3..0>
94 45 IN HSD_RT_LINE_QSFP4_OUT_N<3..0>
94 45 IN HSD_RT_LINE_QSFP5_OUT_P<3..0>
94 45 IN HSD_RT_LINE_QSFP5_OUT_N<3..0>
94 33 IN CLK156M_RT9_P
94 33 IN CLK156M_RT9_N
94 8 IN RT9_RESET_L
94 29 IN RT9_ADDR<4..1> IPD 4 3 2 1
28 IN JTAG_TDO_RT8_TDI_RT9_2V5 R289 94 0 JTAG_TDO_RT8_RT9_2V5RT
94 58 28 27 IN JTAG_TMS_RT5_RT6_RT7_RT8_RT9_2V5
94 58 IN JTAG_TCK_RT9_2V5
94 58 28 27 IN JTAG_TRST_L_RT5_RT6_RT7_RT8_RT9_2V5
P2V5RT2
P1V0RT2_DVDD
P1V0RT2_AVDD

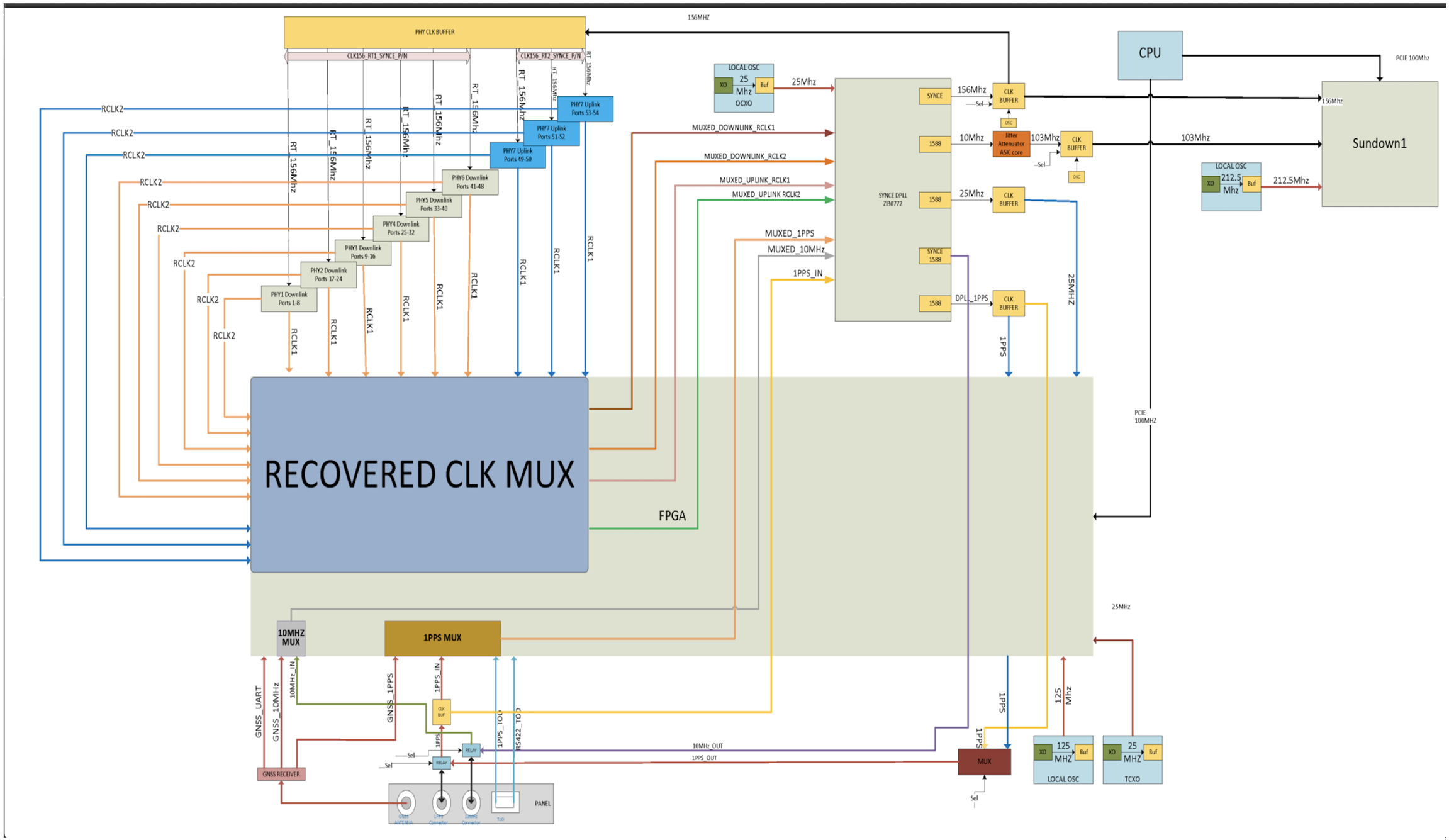
P2V5RT2
NONE
R120
4.7K

R124 0
NONE

JTAG_TDO_RT9_2V5RT OUT 58 94

P2V5RT1
4.7K NONE R277 RT9_ADDR<4> OUT 29 94
4.7K NONE R279 RT9_ADDR<3> OUT 29 94
4.7K NONE R281 RT9_ADDR<2> OUT 29 94
4.7K R283 RT9_ADDR<1> OUT 29 94

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:49 2022		29 OF 138



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Dec 5 17:45:43 2019		30 OF 138

PLACE BYPASS RESISTORS UNDER U63 PACKAGE

+3.3V
R1015 100
R1016 100
R1017 200
R1018 200
R1039 0 BOM=NONE
R1040 0 BOM=NONE

4 IN CLK100M_PE_CPU_SA_P ALIAS DC_CLK100M_SA_PCIE_REFCLK_P\BASE
4 IN CLK100M_PE_CPU_SA_N ALIAS DC_CLK100M_SA_PCIE_REFCLK_N\BASE
0.1UF R1023 SRT_CPU_PCIE_CLKOUT0_P
0.1UF R1024 SRT_CPU_PCIE_CLKOUT0_N

U63
PCLK 7
PCLK 6
VCC 8
VEE 5
Q1 3
Q1 4
Q0 1
Q0 2
ICS853S011BI
15-13454-01

SNDN_PCIE_100MHZ_REFCLK_P
SNDN_PCIE_100MHZ_REFCLK_N
OUT 21
OUT 21

+3.3V L25 600 100MHZ
C27 1UF
C406 22UF
C407 1UF

150 150 150 150
R1019 R1020 R1021 R1022

+3.3V R157 4.7K
R365 1K BOM=NONE
NC IN NC_MIFPGA_OSC_OE R204 0 CLK_OSC_OE

+3.3V 1 L3 2 1UH 20%
C132 22UF
C330 1UF
C133 0.1UF

C88 6.8PF
C87 6.8PF

PROG_NUM=19-100512-01
U51
(MAKE VERY SHORT)

31 10 BI IN FPGA_OSC_SDA
31 10 IN FPGA_OSC_SCL
SDA 7
SCL 8
OE 1
ADD 2
OUT+ 4 POSC_CLK212M5_P
OUT- 5 POSC_CLK212M5_N
VCC 6 FLTR_P3V3_OSC_212M5
GND 3
LMK61E2
19-100413-01
0B1011_010_

R610 33
R611 33
CLK212M_OSC_P
CLK212M_OSC_N
OUT 32
OUT 32

+3.3V R163 0 POSC_212M5_ADD
R593 0 NONE

NOTES: BOM NONE 103MHZ AND 156MHZ OSC, USE DPLL CLOCKS

BOM=NONE
+3.3V 1 L27 2 1UH 20%
C701 22UF
C702 1UF
C703 0.1UF
BOM=NONE
BOM=NONE
BOM=NONE

+3.3V
NONE
NONE
R565 130
R567 130
R575 82.5
R568 82.5
NONE
NONE

U52 BOM=NONE
31 10 BI IN FPGA_OSC_SDA
31 10 IN FPGA_OSC_SCL
SDA 7
SCL 8
OE 1
ADD 2
VCC 6 FLTR_P3V3_OSC_103M
OUT+ 4 AC_SNDN_CLK103M_P
OUT- 5 AC_SNDN_CLK103M_N
GND 3
LMK61E2
19-100411-01
0B1011_000_

BOM=NONE
+3.3V R597 0
R36 0 POSC_103M_ADD
BOM=NONE

BOM=NONE
C169 0.1UF
C170 0.1UF
BOM=NONE
(MAKE VERY SHORT)
CLK103M_DAV_CORE_REFCLK_P
CLK103M_DAV_CORE_REFCLK_N
OUT 40
OUT 40

150 150
R1085 R1086
BOM=NONE BOM=NONE

BOM=NONE
+3.3V 1 L4 2 1UH 20%
C45 22UF
C46 1UF
C47 0.1UF
BOM=NONE
BOM=NONE
BOM=NONE

PROG_NUM=19-100338-01
U53 BOM=NONE
31 10 BI IN FPGA_OSC_SDA
31 10 IN FPGA_OSC_SCL
SDA 7
SCL 8
OE 1
ADD 2
VCC 6 FLTR_P3V3_OSC_156M_RT
OUT+ 4 SRT_CLK156M_OSC_P
OUT- 5 SRT_CLK156M_OSC_N
GND 3
LMK61E2
19-100411-01
ULTRA-LO-JITTER_W-EEPROM
0B1011_001_

BOM=NONE
+3.3V R360 0 OSC_156M25_RT_ADD
R598 0
BOM=NONE

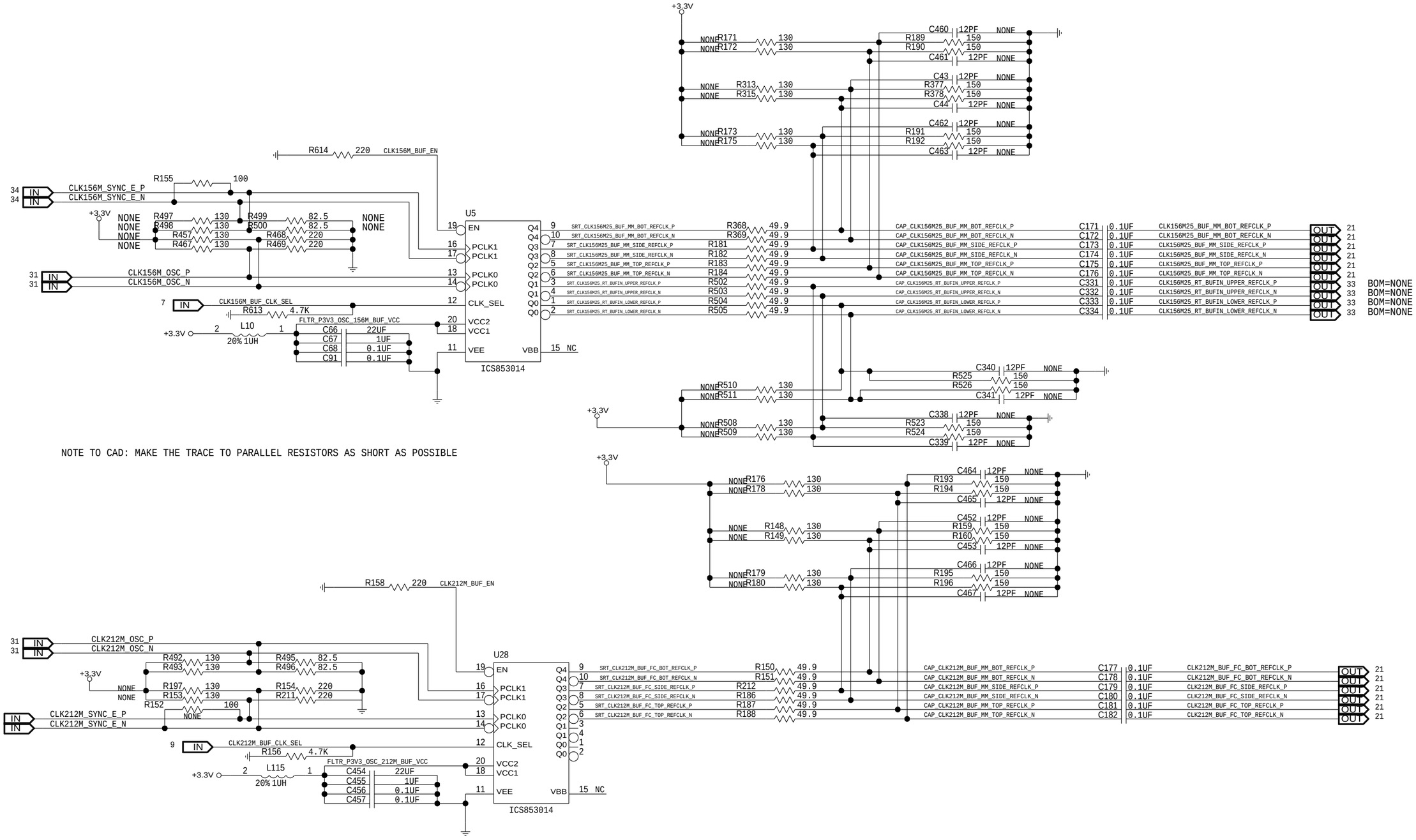
BOM=NONE
C48 6.8PF
C50 6.8PF
BOM=NONE

BOM=NONE
R366 33
R367 33
(MAKE VERY SHORT)
BOM=NONE
CLK156M_OSC_P
CLK156M_OSC_N
OUT 32
OUT 32

ASIC CLOCKS

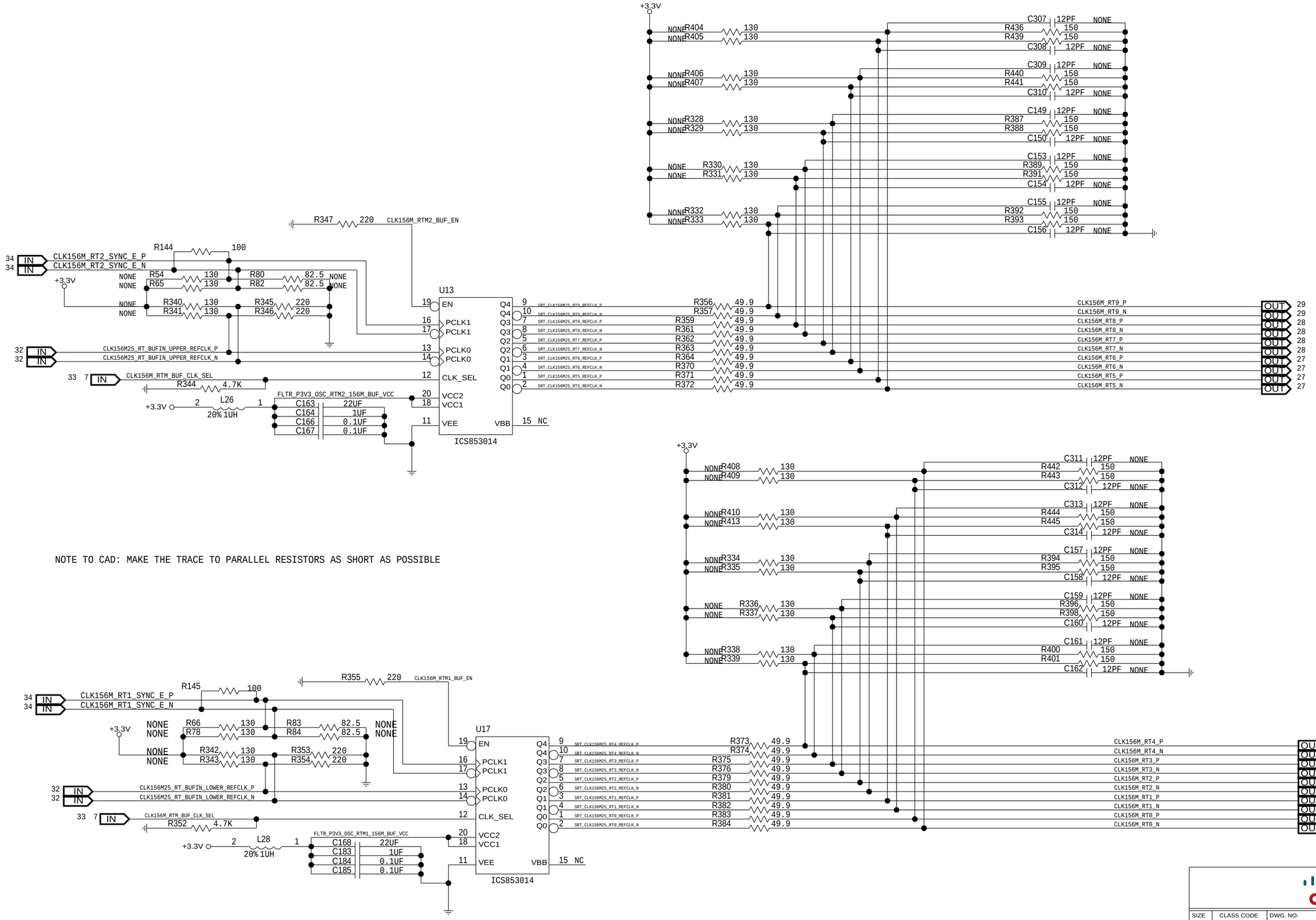
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:40 2022		31 OF 138

NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTORS AS SHORT AS POSSIBLE



CLK156M25 AND CLK212M ASIC

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:51 2022		32 OF 138


U13
ICS853014
EN
PCLK1
PCLK1
PCLK0
PCLK0
CLK_SEL
VCC2
VCC1
VEE
VBB
NC
CLK156M_RT2_SYNC_E_P
CLK156M_RT2_SYNC_E_N
CLK156M25_RT_BUFIN_UPPER_REFCLK_P
CLK156M25_RT_BUFIN_UPPER_REFCLK_N
CLK156M_RTM_BUF_CLK_SEL
CLK156M_RTM2_BUF_EN
FLTR_P3V3_OSC_RTM2_156M_BUF_VCC
U17
ICS853014
CLK156M_RT1_SYNC_E_P
CLK156M_RT1_SYNC_E_N
CLK156M25_RT_BUFIN_LOWER_REFCLK_P
CLK156M25_RT_BUFIN_LOWER_REFCLK_N
CLK156M_RTM_BUF_CLK_SEL
CLK156M_RTM1_BUF_EN
FLTR_P3V3_OSC_RTM1_156M_BUF_VCC
NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTORS AS SHORT AS POSSIBLE
SIZE B
CLASS CODE
DWG. NO. 92-105229-01
REV A0
SCALE
DATE: Fri Mar 25 10:33:49 2022
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+3.3VA
L14
600 100MHZ
FLT_P3V3_OSC114M_XO
R165 4.7K
C101
C102 10UF
0.1UF
U2
PWR
OE
OUT
GND
114.285MHZ
25PPM
19-100470-01
SRT_CLK114M_XO
R162 33
CLK114M_XO
OUT 34

NOTE TO CAD: ROUTE CLK114M_XO EQUAL TRACES TO U59 PIN 70 AND 77

PROG_NUM=15-107425-01
PREPROGRAMMED CPN

SYNCE/1588 INTERNAL LOOPBACK SUPPORTED

U59

INPUT REF/OUTPUT CLKS
REF4+/REFIN8 9
REF4-/REFIN9 10
REF3+/REFIN6 7
REF3-/REFIN7 8
REF2+/REFIN4 5
REF2-/REFIN5 6
REF1+/REFIN2 3
REF1-/REFIN3 4
REF0+/REFIN0 1
REF0-/REFIN1 2

34 IN CLK25M_OCXO
38 IN CLK_1_PPS_UTC_ZL_IN
10 IN RT_UPLINK_M4_4_7_SYNCE_CLK
10 IN RT_UPLINK_M4_0_3_SYNCE_CLK
10 IN RT_DOWNLINK_M4_4_7_SYNCE_CLK
10 IN RT_DOWNLINK_M4_0_3_SYNCE_CLK
8 IN CLK_10M_UTC_ZR_IN
7 IN CLK_MIFPGA_ZL_1PPS

HPOUT7+/HPOUT14 43
HPOUT7-/HPOUT15 42
HPOUT6+/HPOUT12 45
HPOUT6-/HPOUT13 46
HPOUT5+/HPOUT10 49
HPOUT5-/HPOUT11 48
HPOUT4+/HPOUT8 51
HPOUT4-/HPOUT9 52
HPOUT3+/HPOUT6 57
HPOUT3-/HPOUT7 56
HPOUT2+/HPOUT4 59
HPOUT2-/HPOUT5 60
HPOUT1+/HPOUT2 64
HPOUT1-/HPOUT3 63
HPOUT0+/HPOUT0 66
HPOUT0-/HPOUT1 67

R166 22 CLK_10M_ZR_OUT OUT 38
R177 22 CLK_10M_ZL_SI5326_OUT OUT 36
CLK25M_MI0_SYNC_E_REFCLK_P OUT 10
CLK25M_MI0_SYNC_E_REFCLK_N OUT
10

NOTES: CLK25M_MI0_SYNCE_E_REFCLK IS CHANGED TO LVCMOS

CLK156M_SYNC_E_P OUT 32
CLK156M_SYNC_E_N OUT 32
CLK156M_RT1_SYNC_E_P OUT 33
CLK156M_RT1_SYNC_E_N OUT 33
CLK156M_RT2_SYNC_E_P OUT 33
CLK156M_RT2_SYNC_E_N OUT 33

HOST IF
SCK/SCL
SI/SDA
SO/ASEL1
CS_M/ASEL0

36 34 7 IN DPLL_SCL_SYNCE_SPI_CLK 16
36 34 7 IN DPLL_SDA_SYNCE_SPI_MOSI 18
34 IN DPLL_SYNCE_ADDR_SEL1 17
34 IN DPLL_SYNCE_ADDR_SEL0 19

GPOUT1 78
GPOUT0 79

R46 22 CLK_ZL_1PPS_OUT OUT 38
R49 22
TP1 TPT35RD

CONTROL & STATUS
RST
SRST

THE PWR (F11) PIN SHOULD BE HELD LOW FOR 2 MS
AFTER ALL POWER SUPPLIES ARE STABILIZED.
THIS PIN IS INTERNALLY PULLED-UP TO VDD.

+3.3VA
R1101 4.7K DPLL_SYNCE_RESET_L OUT 10 34

34 10 IN DPLL_SYNCE_RESET_L 75
37

GPIO8 74
GPIO7 36
GPIO6/AC1 30
GPIO5/AC0 31
MC1 28
MC0 29
GPIO2 27
GPIO1 25
GPIO0/IF 20

DPLL_SYNCE_GPIO8 IN
DPLL_SYNCE_GPIO7 IN NOT USED 34
DPLL_SYNCE_GPIO6 IN 34
DPLL_SYNCE_GPIO5 IN 34
MC_FREQ_SEL[1] IN 34
MC_FREQ_SEL[0] IN 34
DPLL_SYNCE_GPIO2 IN 7
DPLL_SYNCE_GPIO1 IN 7
DPLL_SYNCE_GPIO0 IN 7 34

MSTR CLK/MISC
MCLKIN+
MCLKIN-
OSCI 70
OSCO 71 NC

34 IN CLK114M_XO 77
76
CLK114M_XO IN 34

+3.3VA
R33 1K R34 1K
R105 1K
R107 1K
R112 1K
R115 1K
NC 24 IC8
NC 26 IC7
NC 23 IC6
NC 33 IC5
NC 32 IC4
34 IC3
35 IC2
15 IC1
NC 11 IC0

1/2
ZL30772
PART_NUMBER=15-105653-01

NOTE TO CAD: PLACE THESE PD RESISTORS CLOSE TO DEVICE AND MINIMIZE STUB

+3.3VA
R30 1K DPLL_SCL_SYNCE_SPI_CLK OUT 7 34 36
R31 1K DPLL_SDA_SYNCE_SPI_MOSI OUT 7 34 36

PROG_NUM=19-100581-01
OCXO, 24.576MHZ, 4.6PPM
MPN=OX-221-9101-24M576

U1
RF_OUT 4 SRT_CLK25M_OCXO R1077 33.2 CLK25M_OCXO OUT 34
35 IN FLT_P3V3_OSC25M_OCXO 3 VCC GND 7
OCXO
19-2320-01

+3.3VA
R464 1K DPLL_SYNCE_ADDR_SEL0 OUT 34
R465 1K DPLL_SYNCE_ADDR_SEL1 OUT 34
R461 1K NONE
R462 1K NONE

CONFIGURED AS I2C
ADDR 7BIT = 0X27

+3.3VA
R1099 1K DPLL_SYNCE_GPIO0 OUT 34 7
R1098 NONE 1K DPLL_SYNCE_GPIO5 OUT 34
R1091 NONE 1K DPLL_SYNCE_GPIO6 OUT 34
NONE R25 1K
R26 1K
R27 1K
R1256 1K DPLL_SYNCE_GPIO8 OUT 34

GPIO0_IF = 1 : I2C MODE
GPIO[5_6] = 00: CONFIGURATION ZONE 0

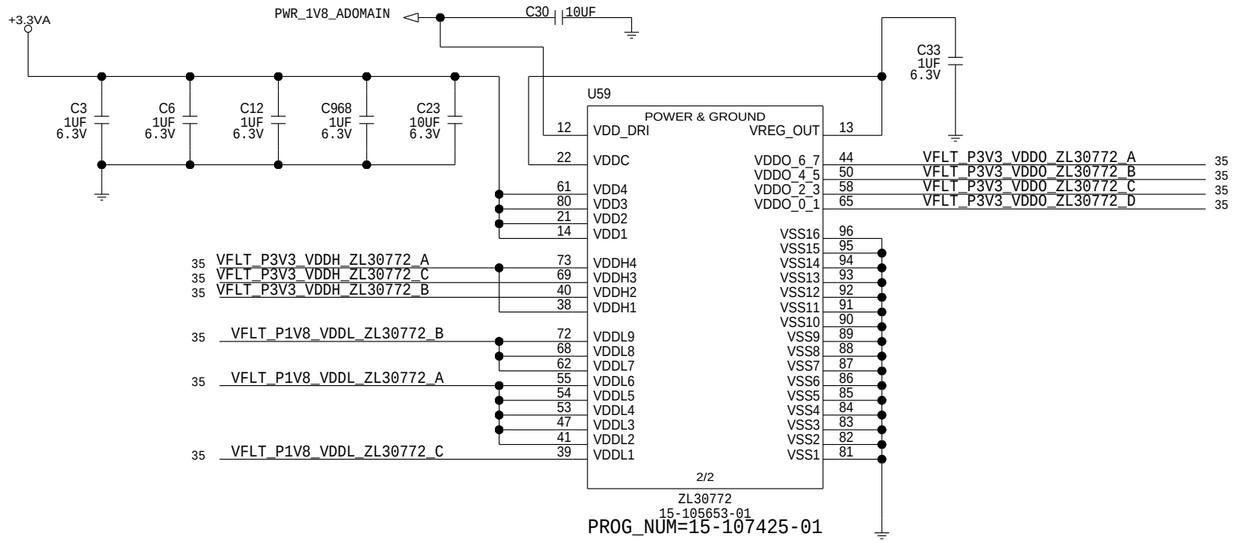
+3.3VA
R28 1K
R35 1K
NONE

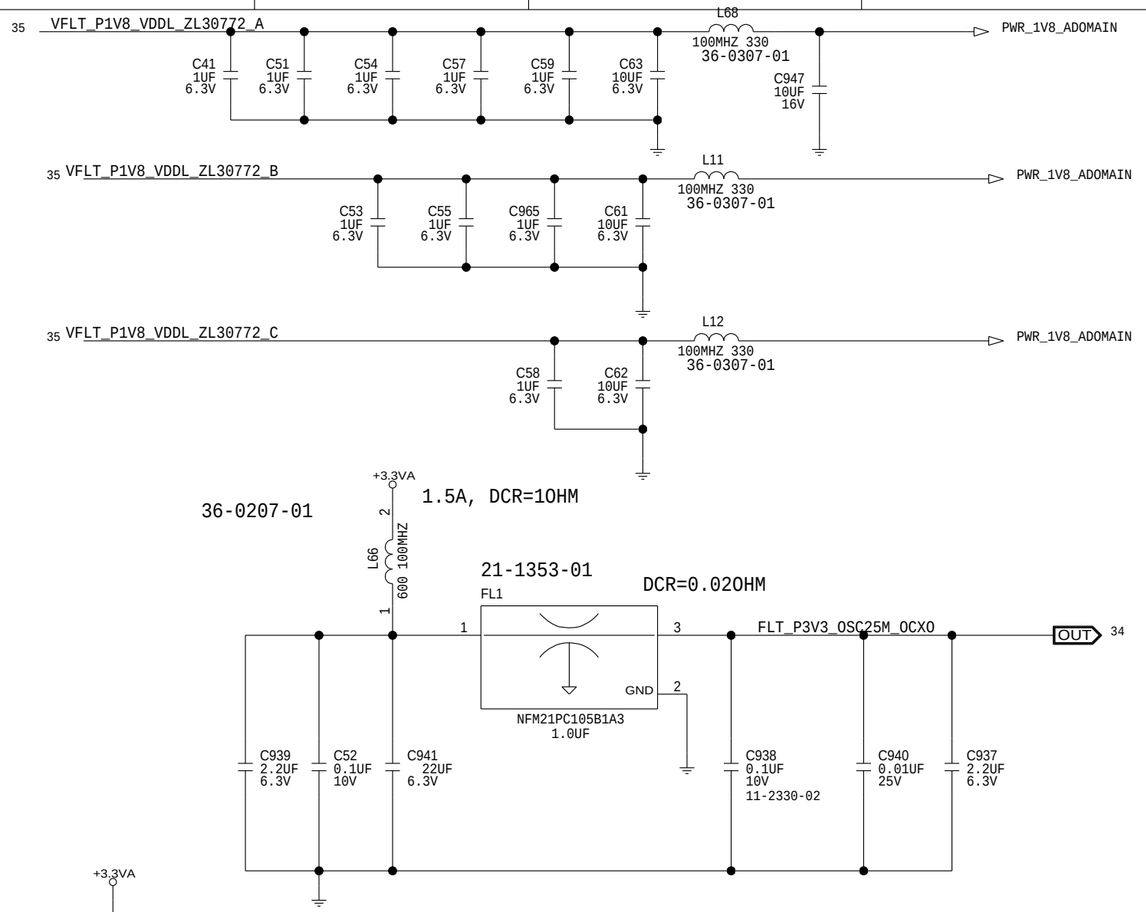
MC0/1 = 11 : 114.285M-125MHZ

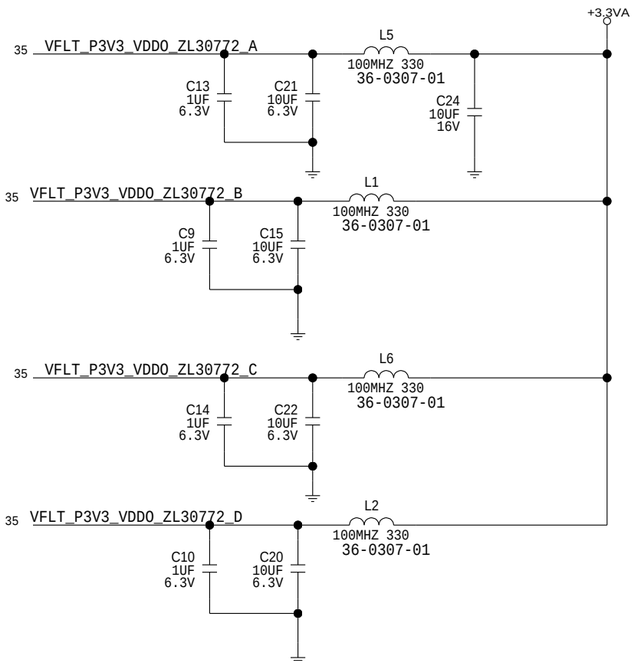
R44 1K
R29 1K
NONE
MC_FREQ_SEL[1] IN 34
MC_FREQ_SEL[0] IN 34

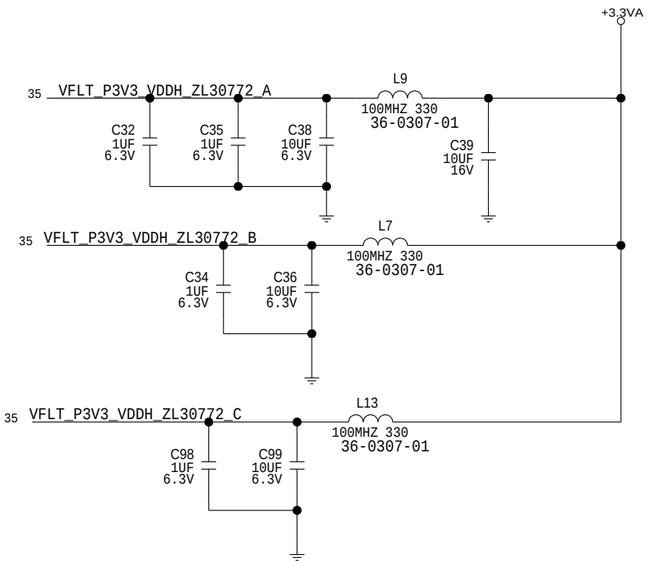
CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:44 2022		34 OF 138

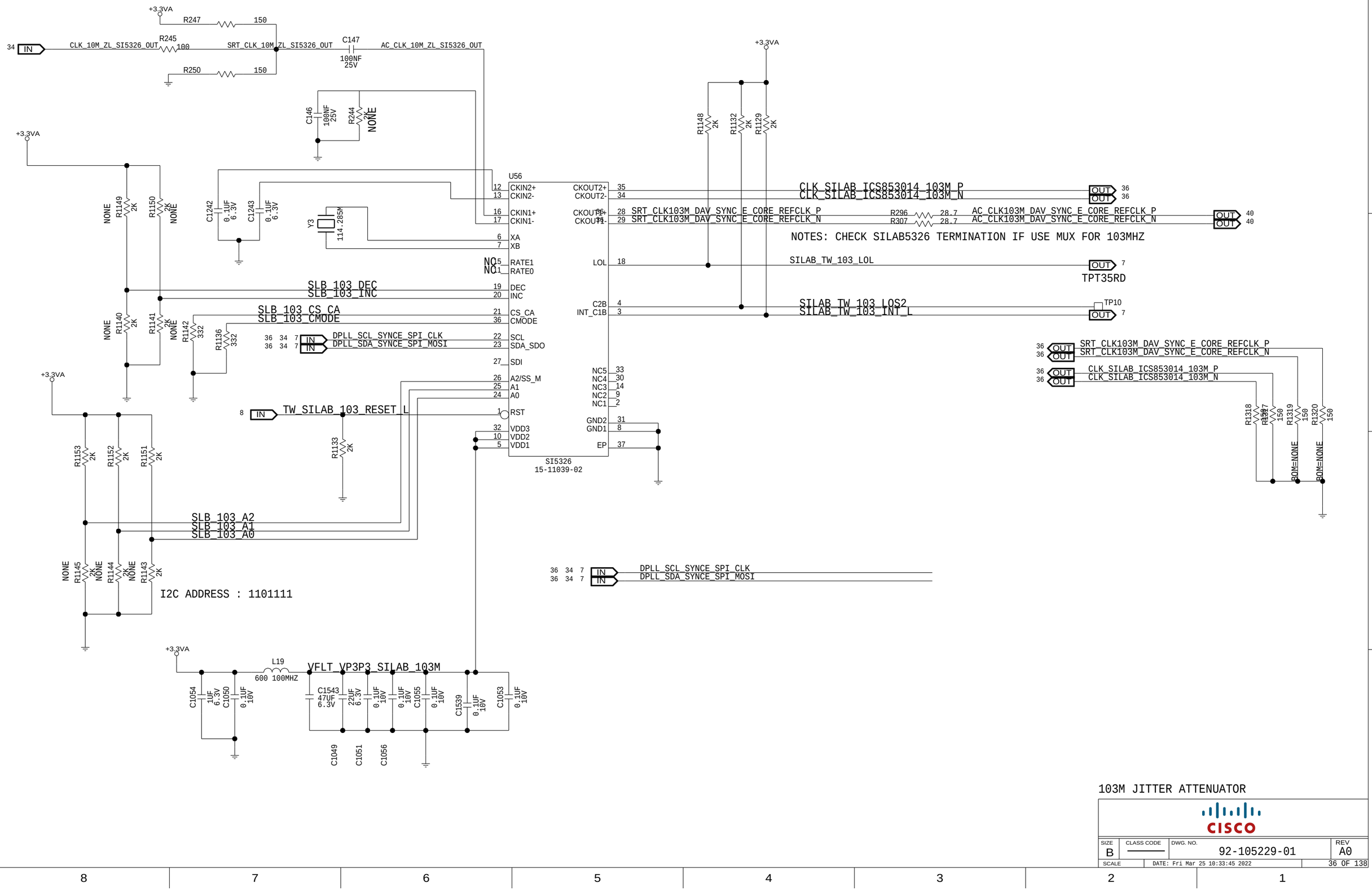








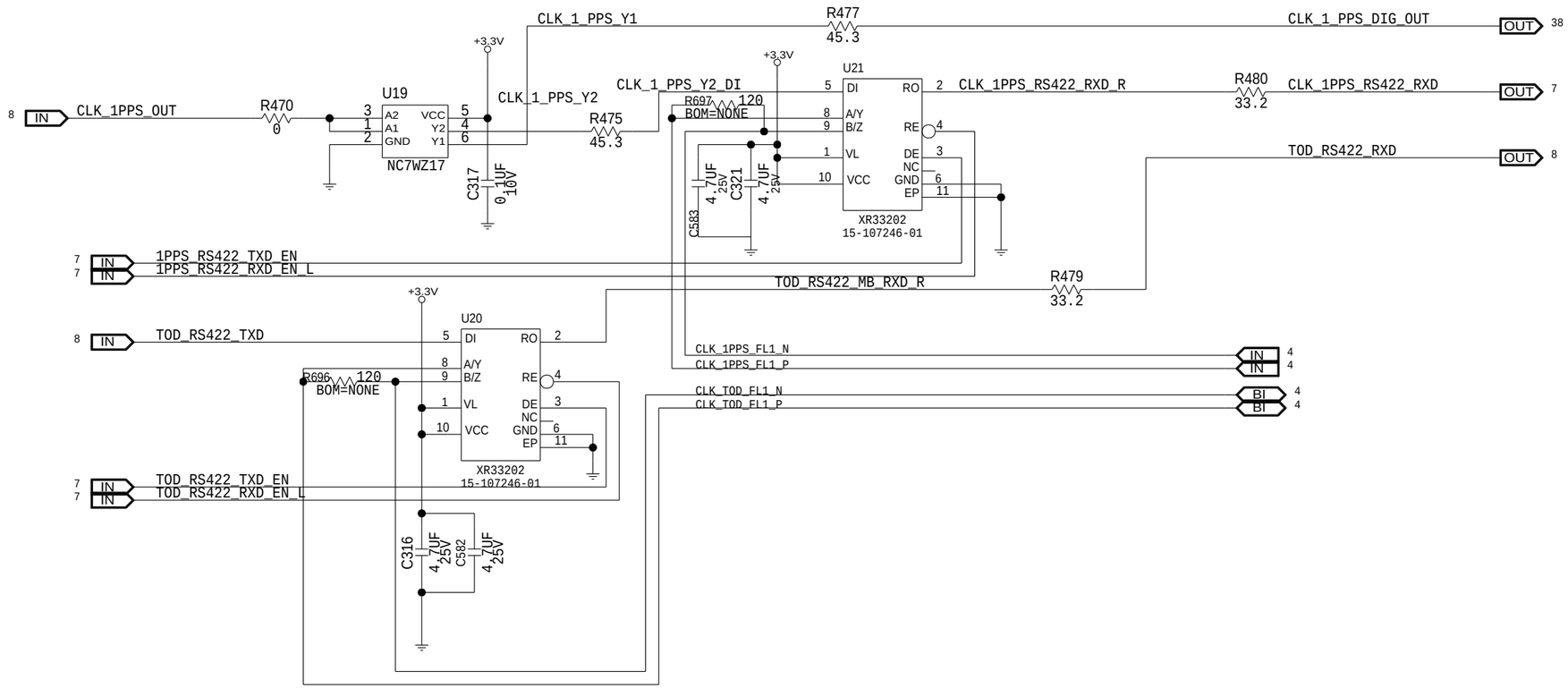
SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:38 2022		35 OF 138



103M JITTER ATTENUATOR

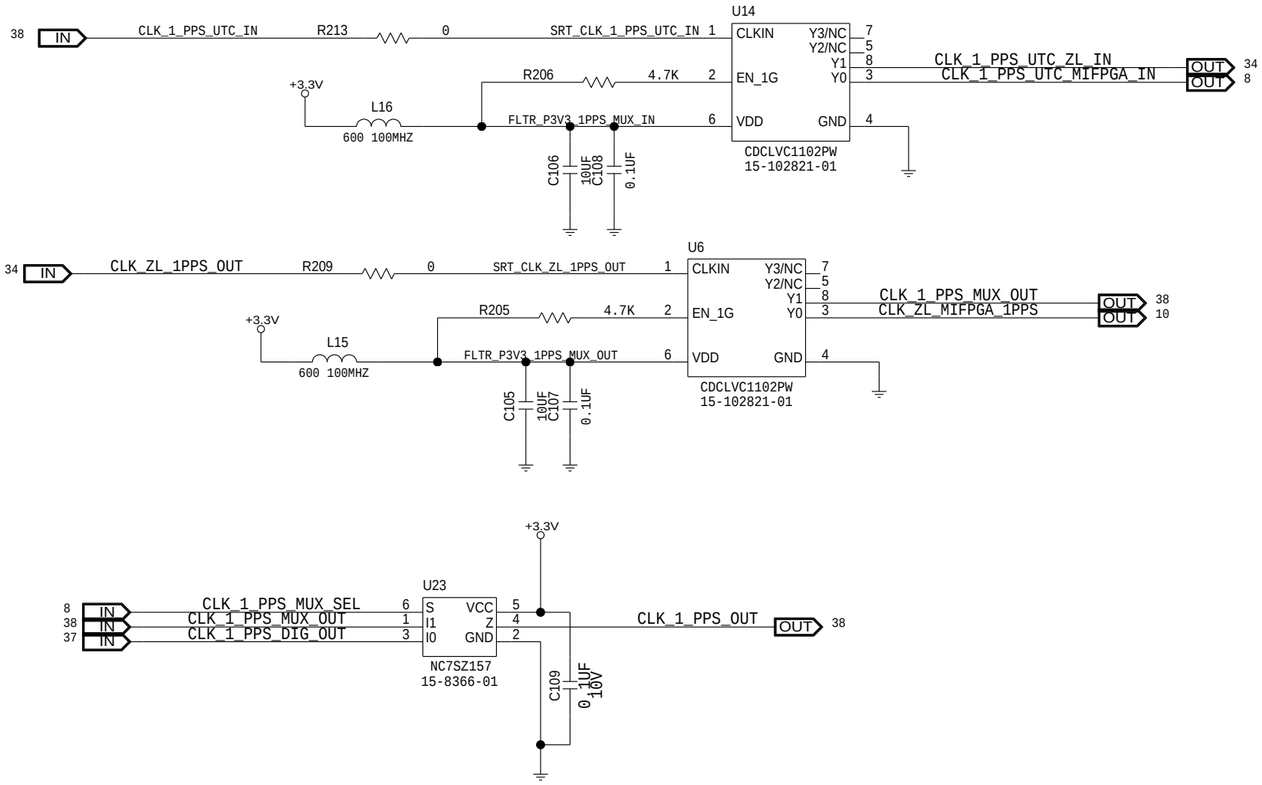
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:45 2022		36 OF 138

TOD
ONLY RS422 AND 1PPS / REMOVE RS232



ToD PORT

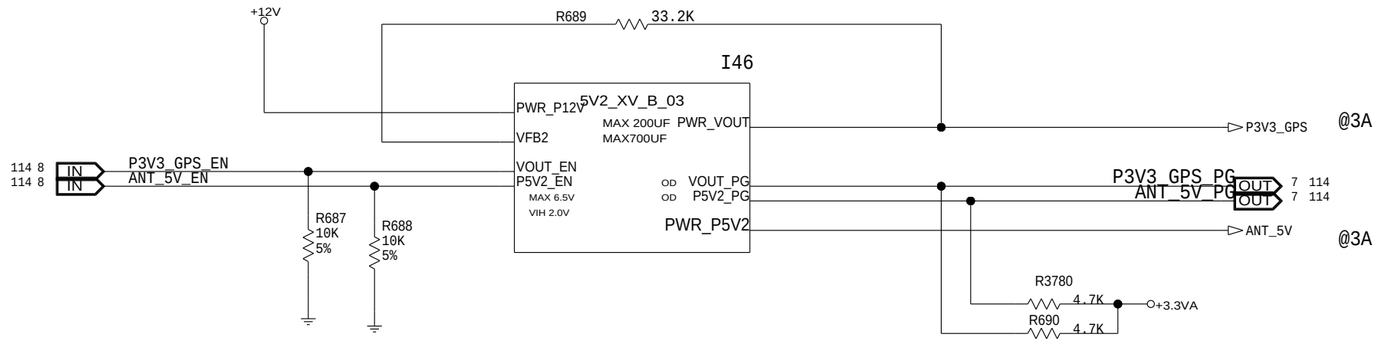
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:38 2022		37 OF 138



GNSS CONNECTOR

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:45 2022		38 OF 138

NOTE:ANT_5V NEEDS TO FOLLOW P3V3_GPS BOTH STARTUP AND POWER CYCLING

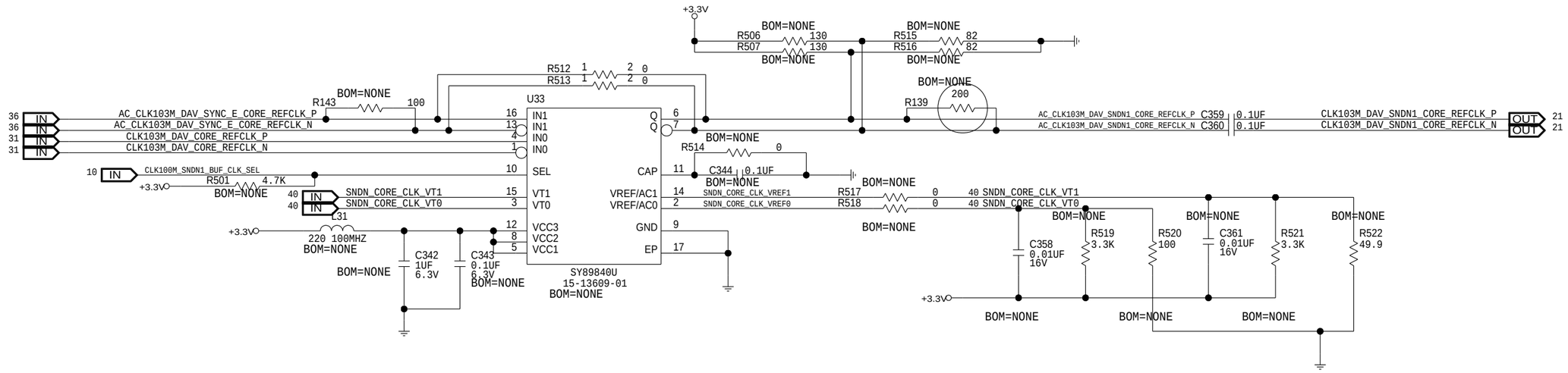


GNSS POWER

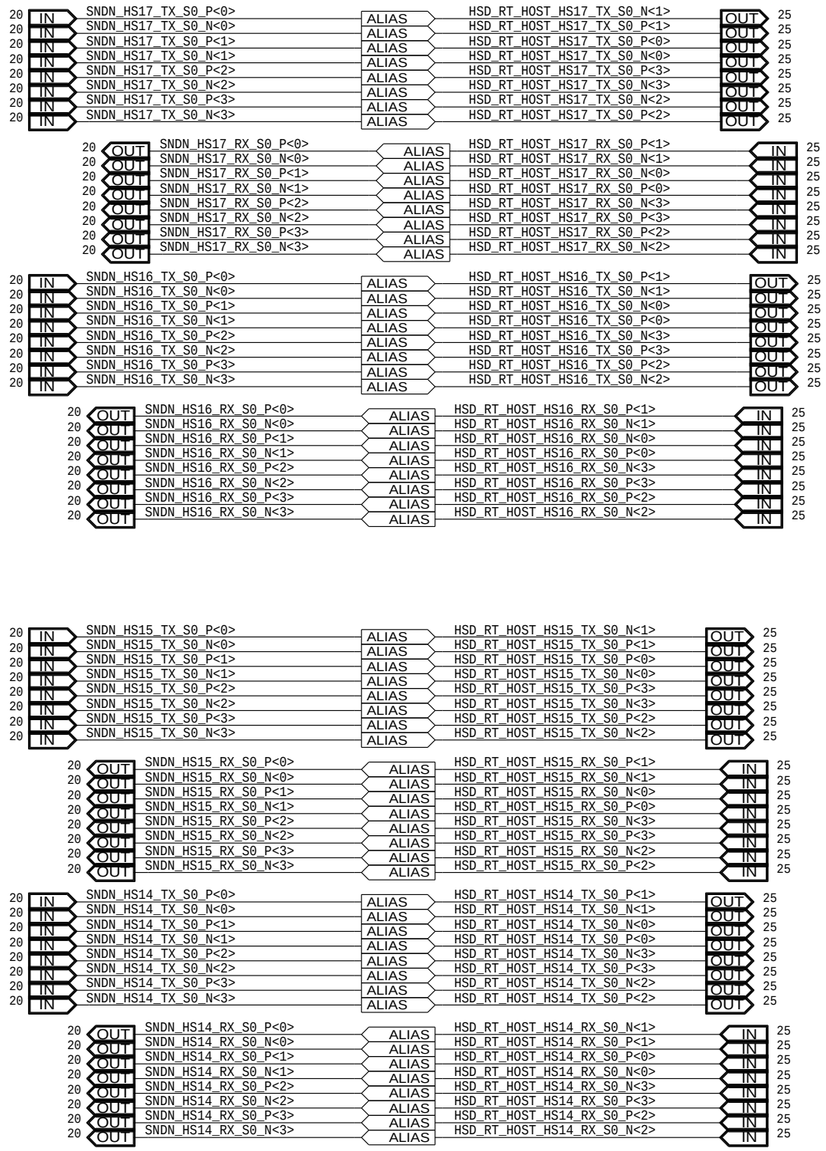
CISCO

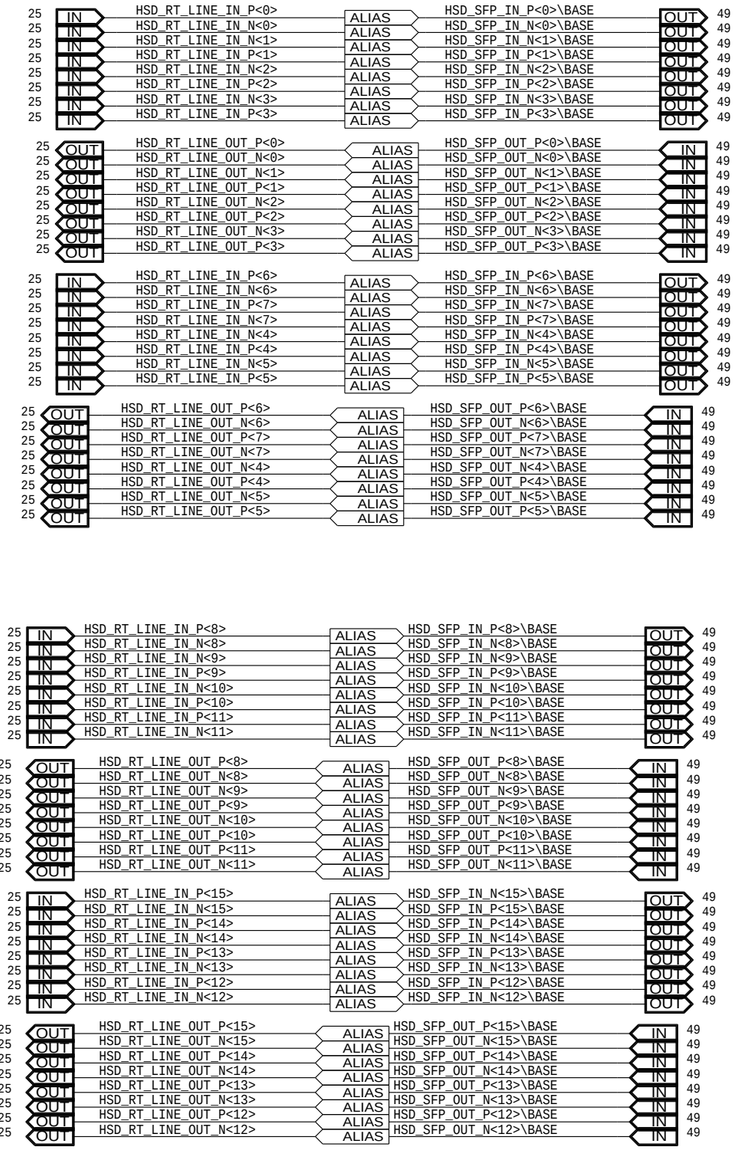
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:44 2022		39 OF 138

NOTE TO CAD: MAKE THE TRACE TO PARALLEL RESISTOR AS SHORT AS POSSIBLE
NOTE TO CAD: ROUTE NETS OF R512,513 UNDERNEATH U33 ON TOP LAYER
NOTES: BYPASS CLOCK MUX



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:38 2022		40 OF 138

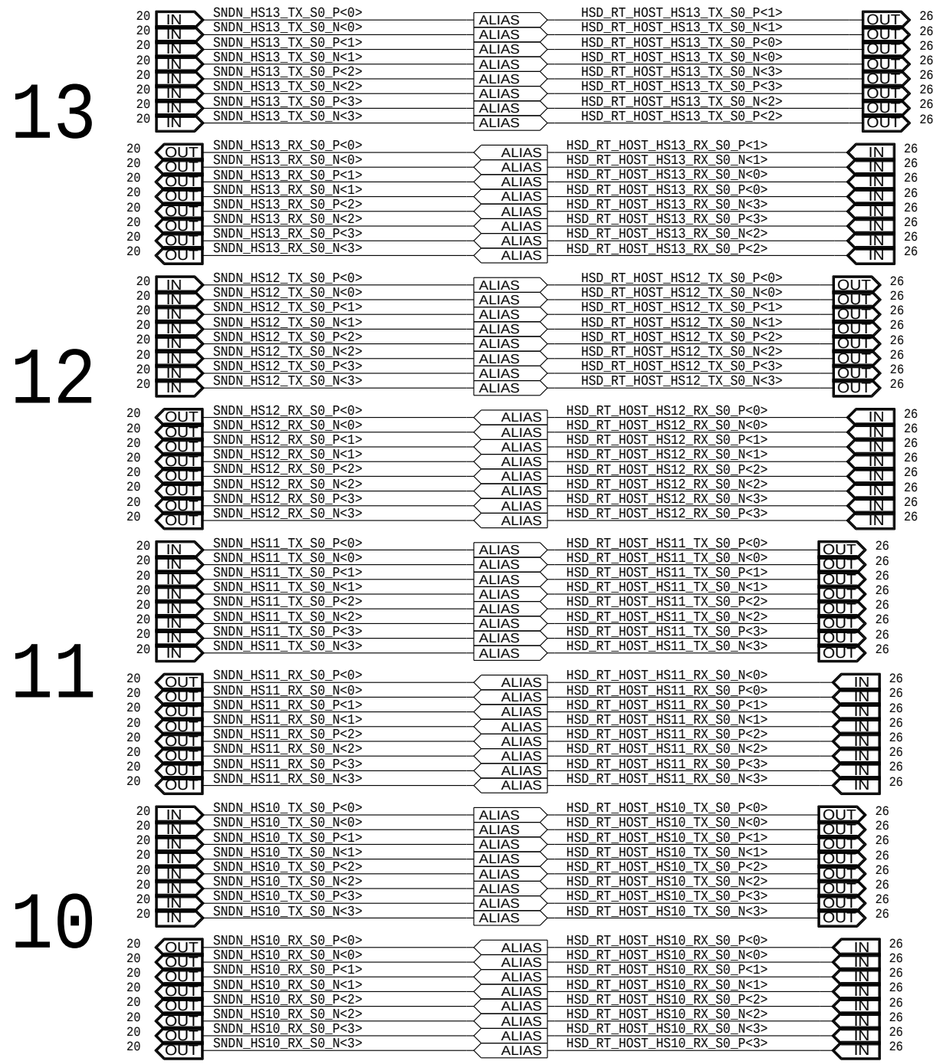


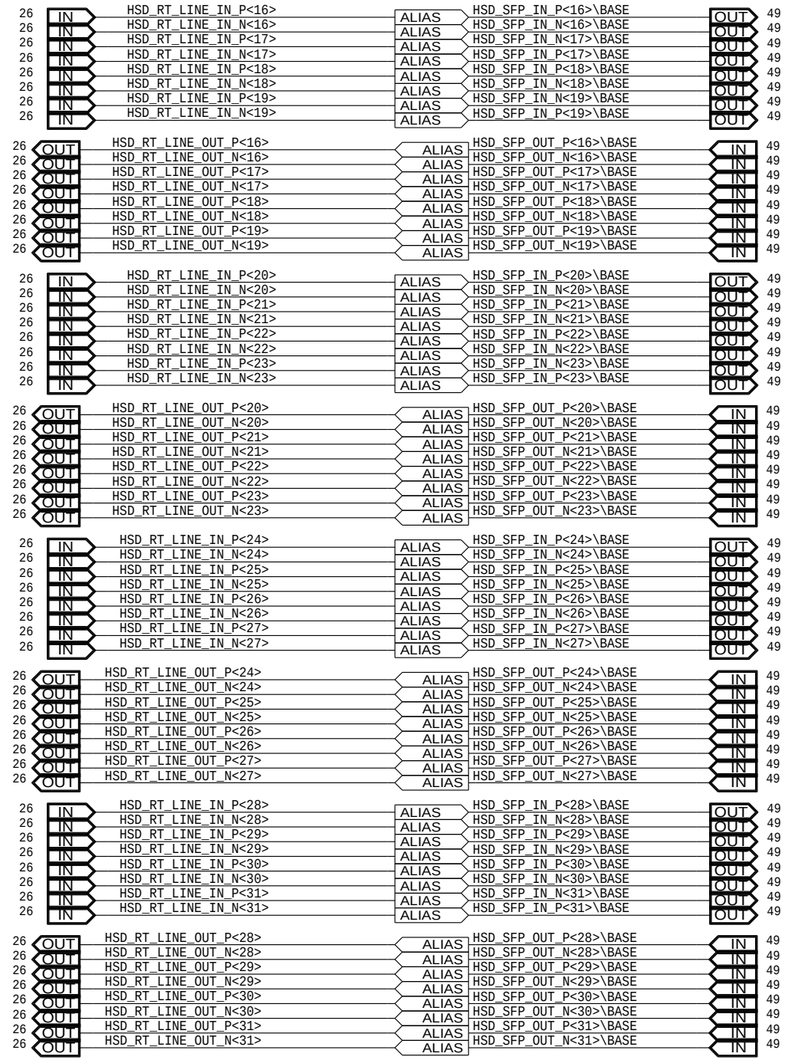


SFP SERDES MAPPING <15:0>

CISCO

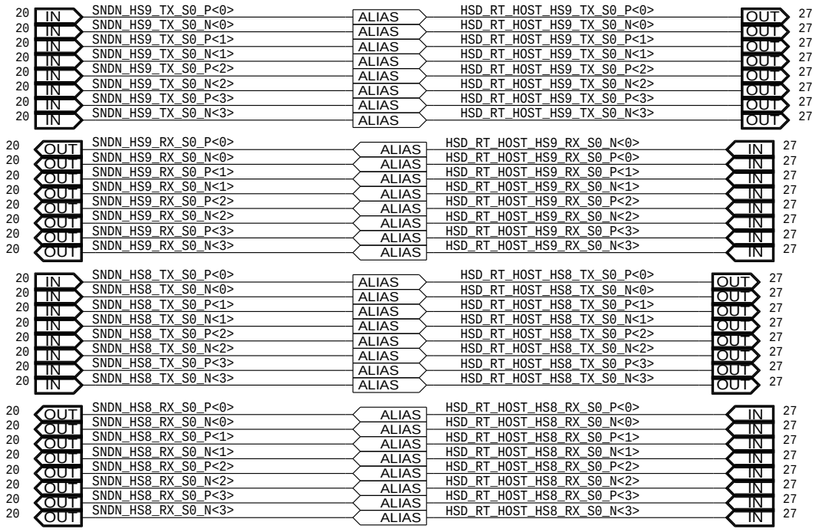
SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Wed Jun 5 13:37:46 2019		41 OF 138

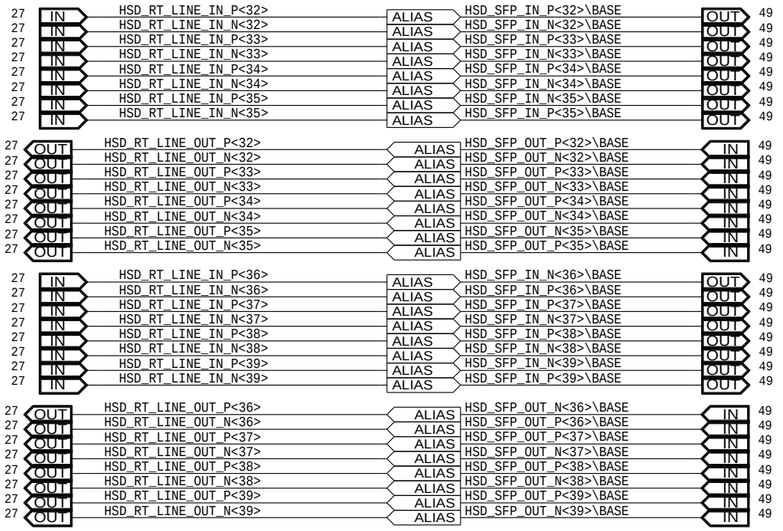




SFP SERDES MAPPING <31:16>

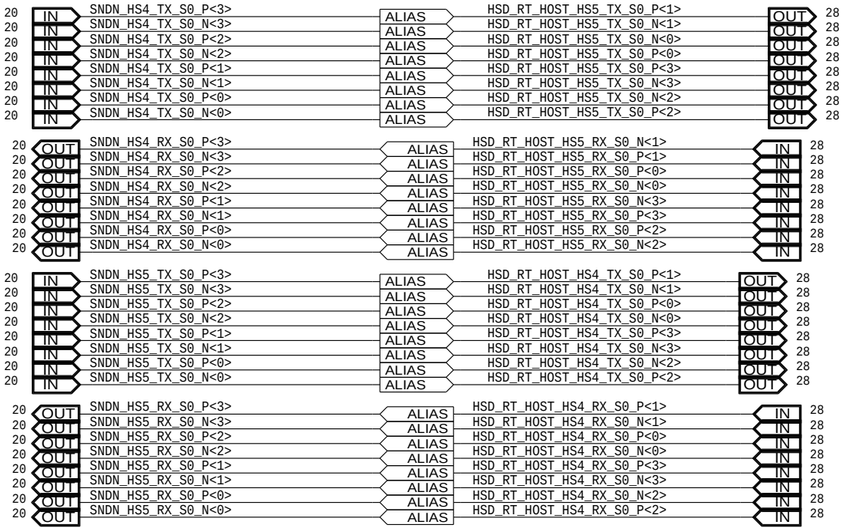
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Wed Jun 5 13:38:47 2019		42 OF 138

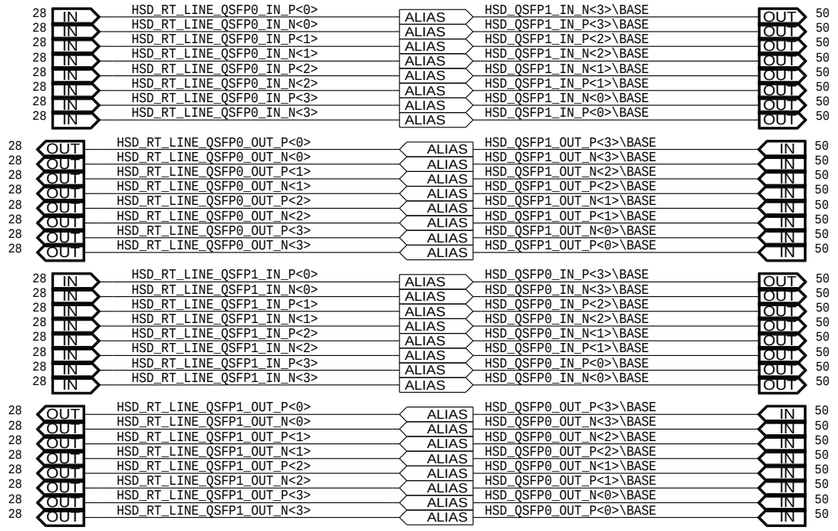


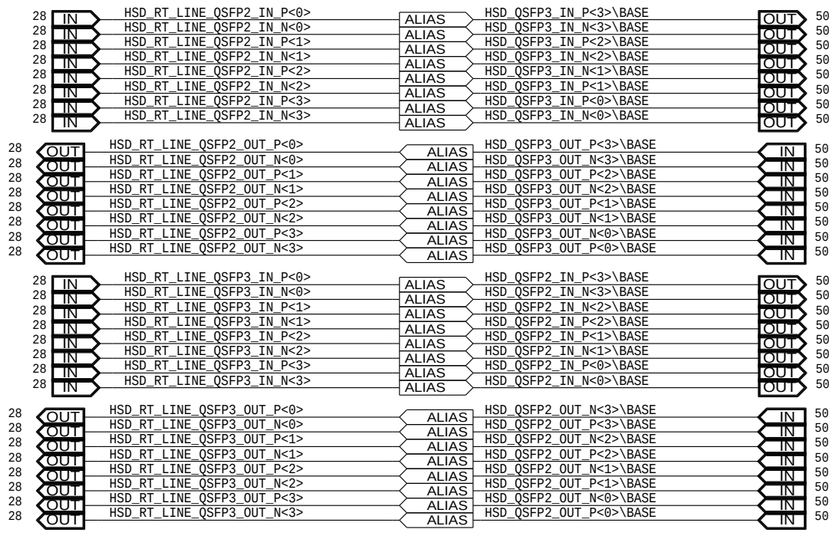


SFP SERDES MAPPING <47:32>

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Tue Apr 23 20:37:56 2019		43 OF 138

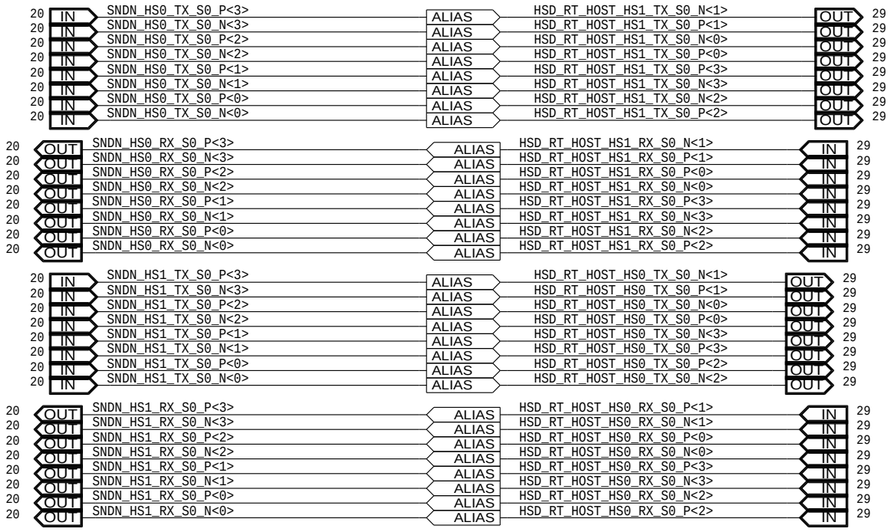


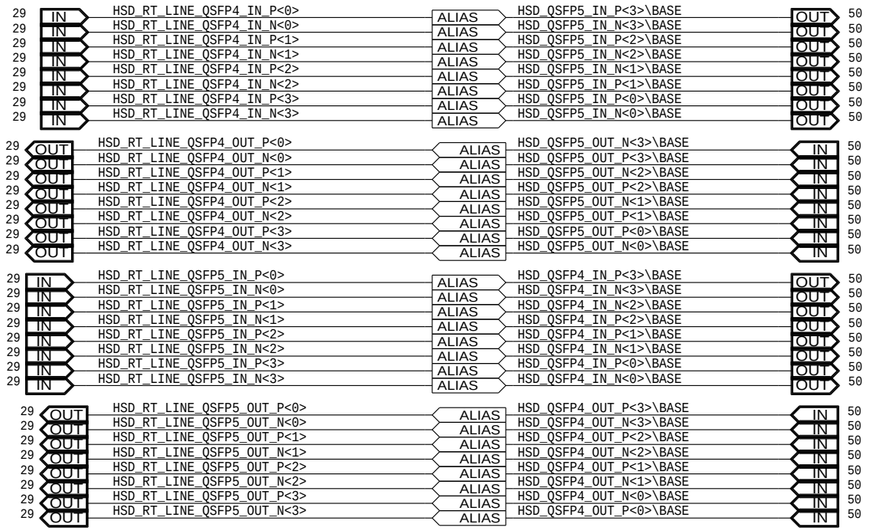




QSFP SERDES MAPPING <3:0>

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Tue Apr 23 20:37:57 2019		44 OF 138

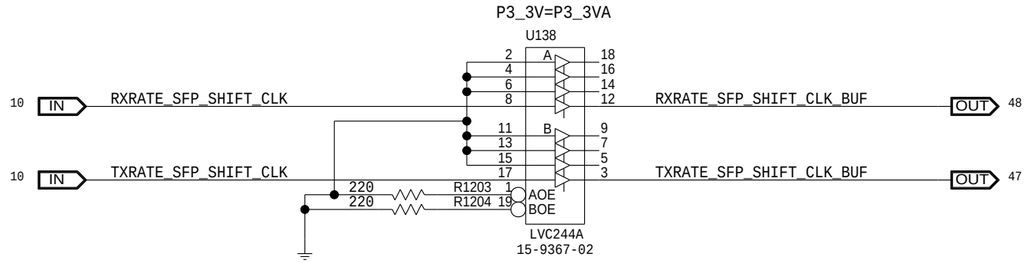




QSFP SERDES MAPPING <5:4>

CISCO

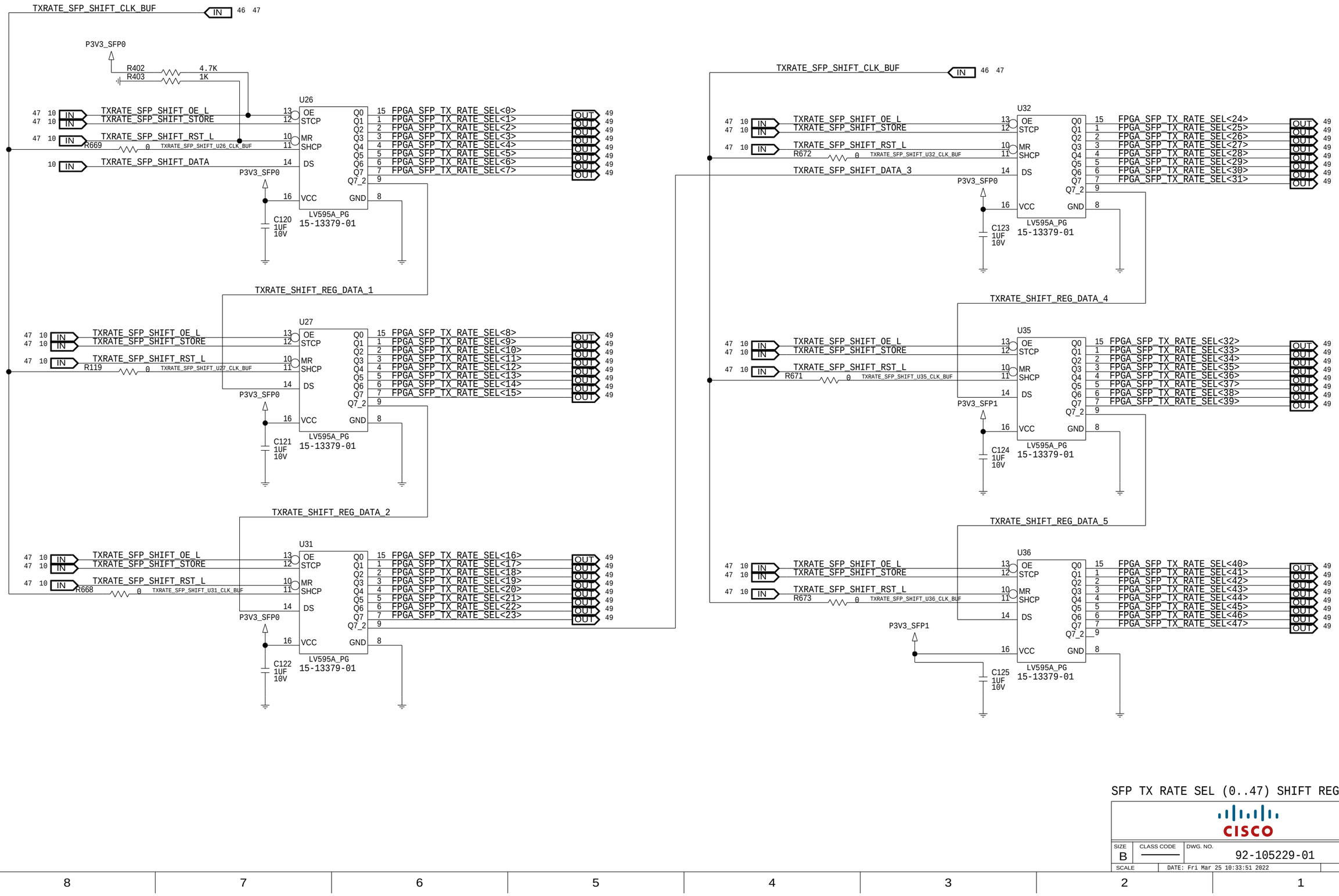
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Tue Apr 23 20:37:58 2019		45 OF 138



CLK BUF SHIFT REG

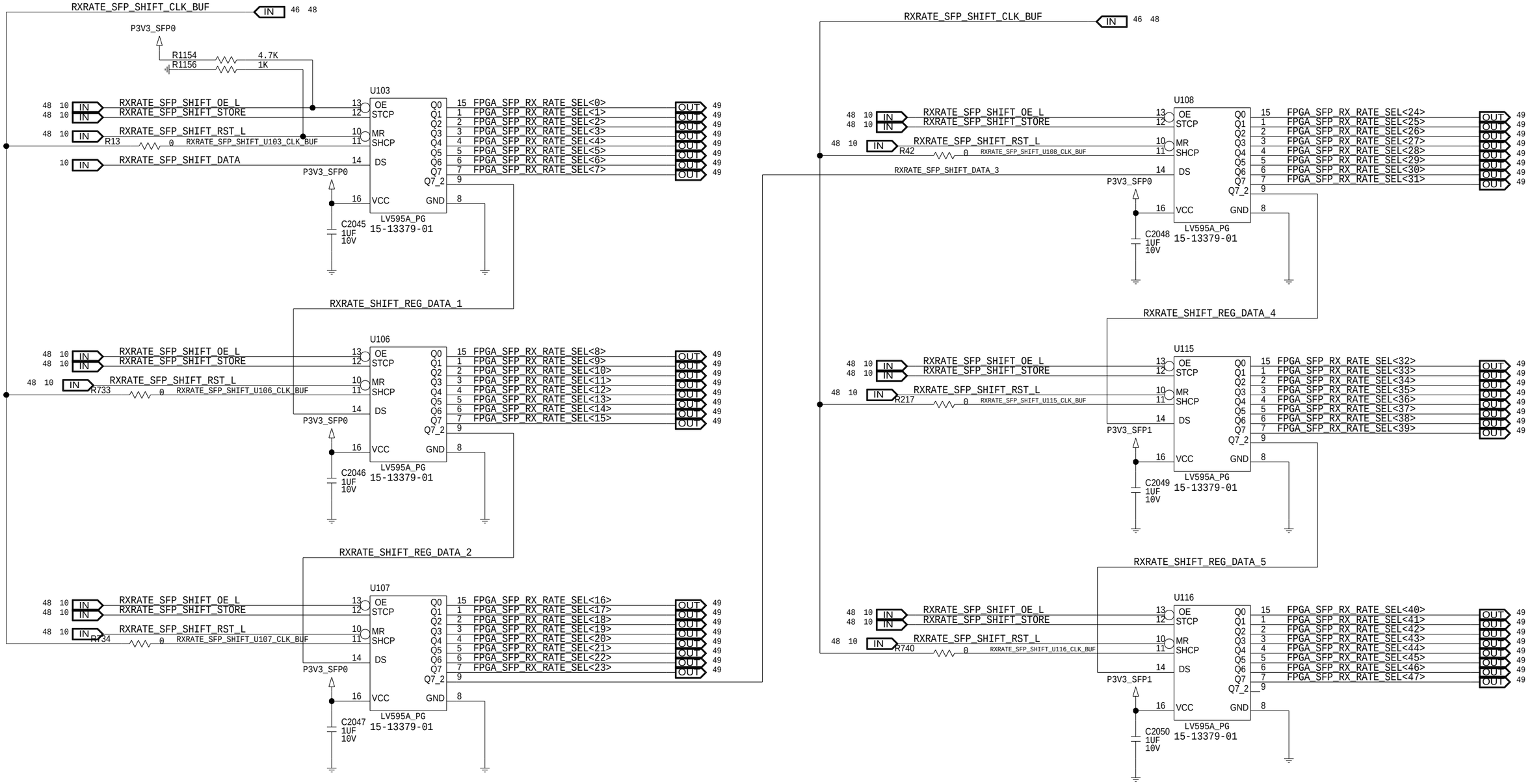
CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:41 2022		46 OF 138



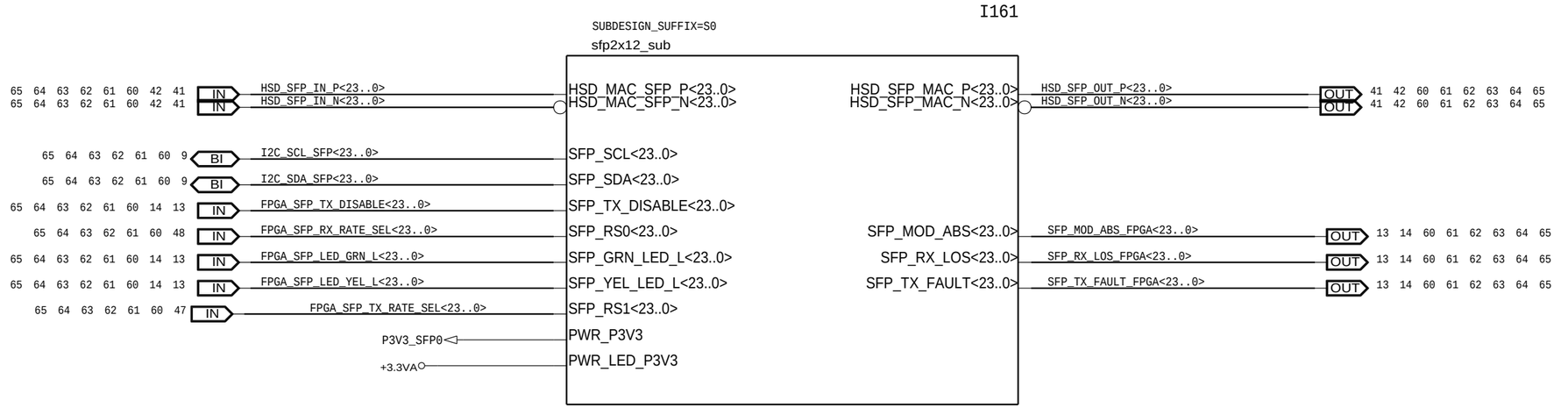
SFP TX RATE SEL (0..47) SHIFT REG

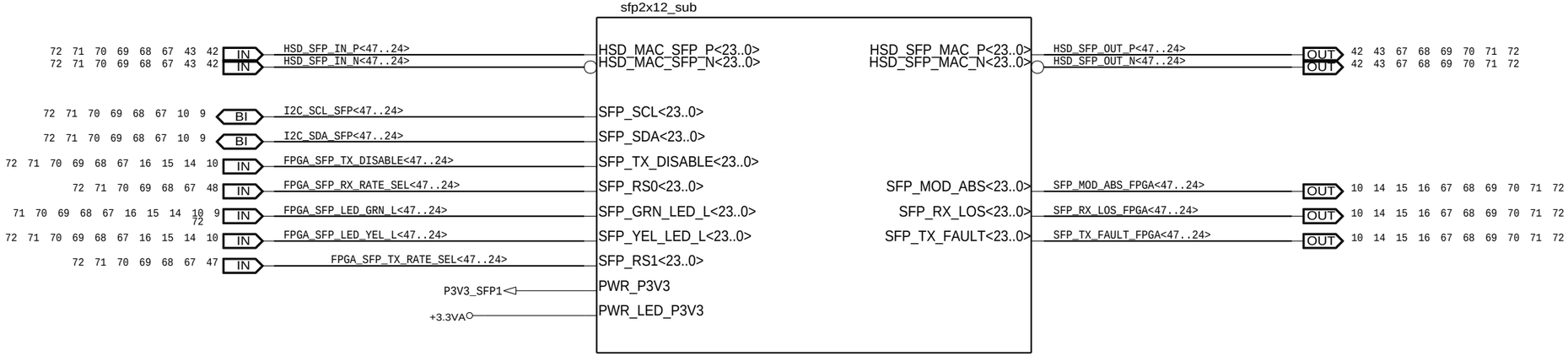
SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:51 2022		47 OF 138



SFP RX RATE SEL (0..47) SHIFT REG

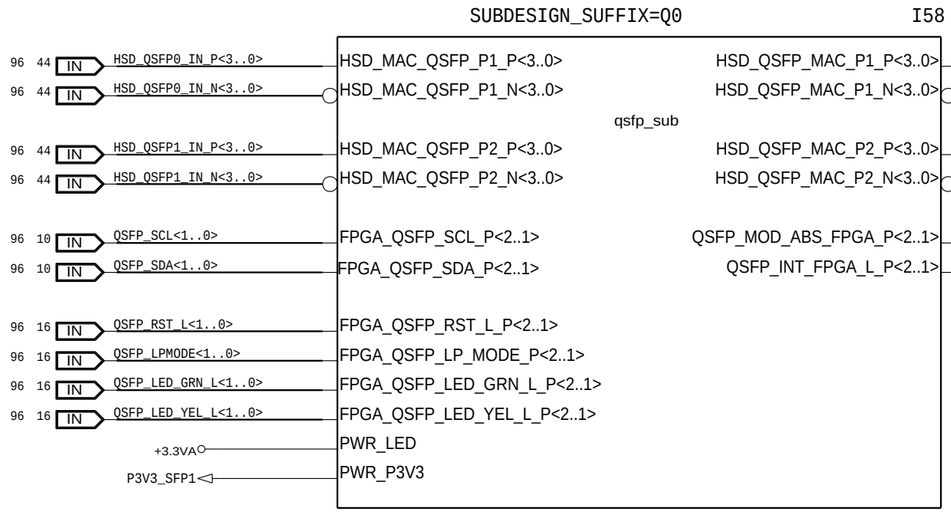
SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:51 2022		48 OF 138

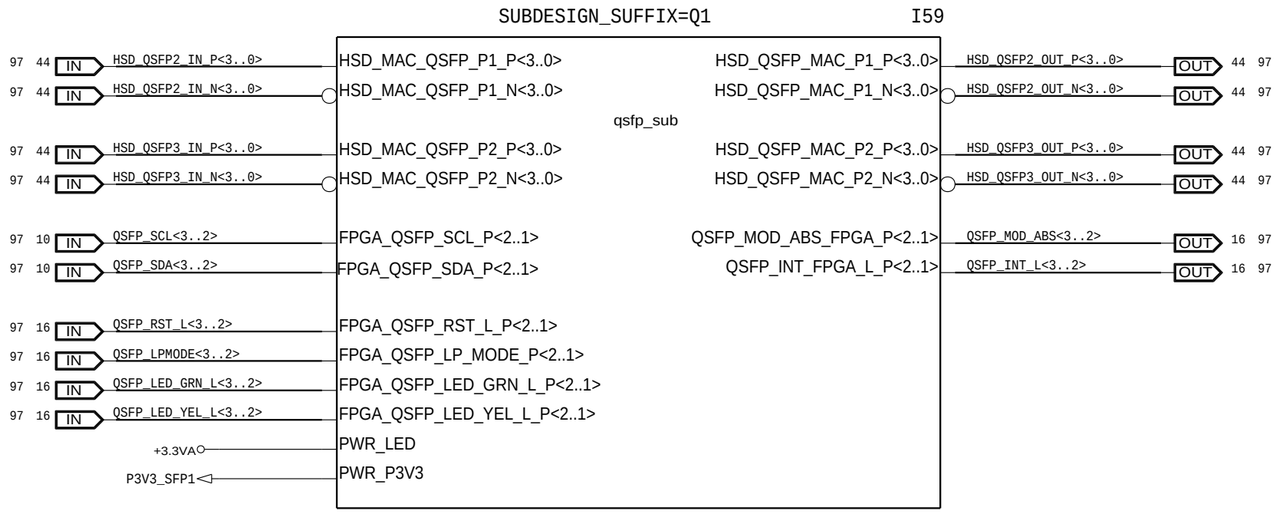


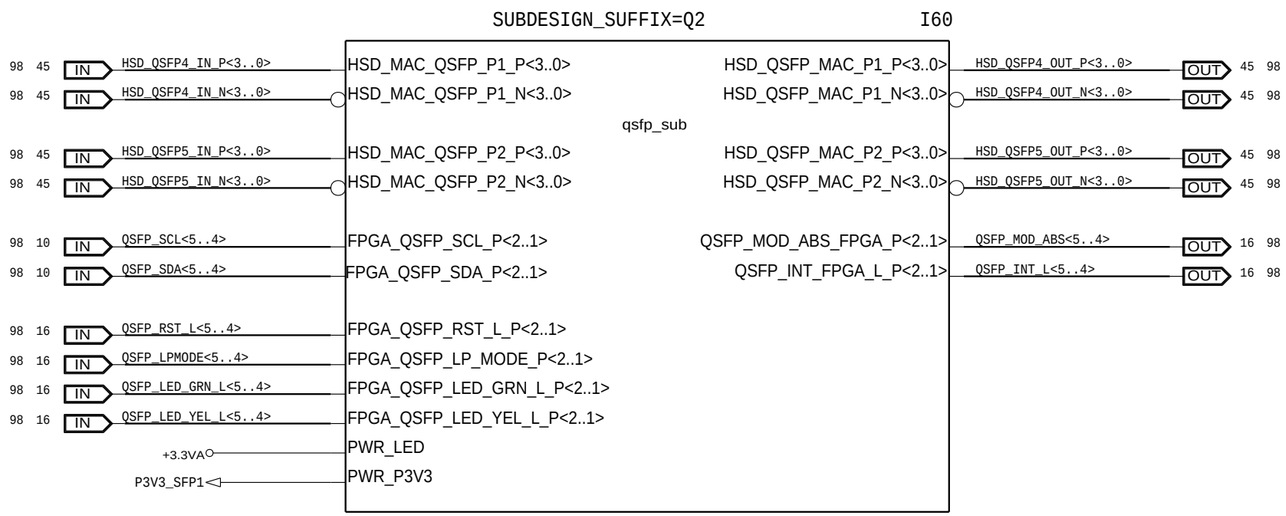


SFP+ HIERARCHY INSTANCIATION

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:01:14 2022		49 OF 138







QSFP+ UPLINK PORT

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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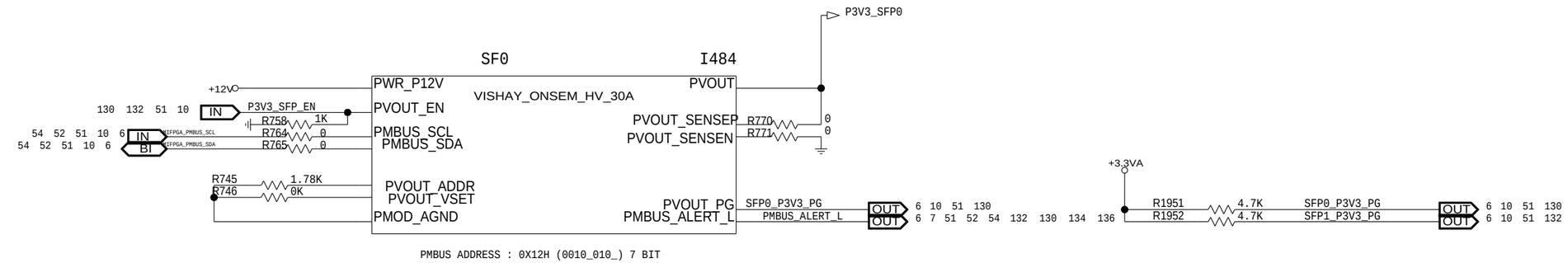
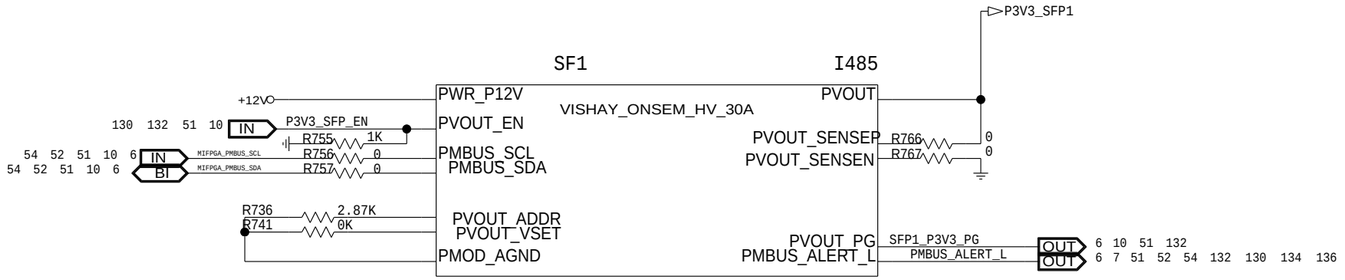
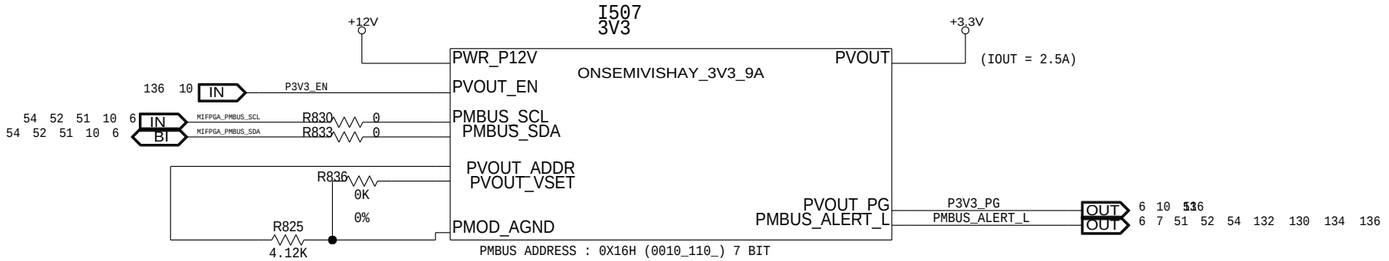
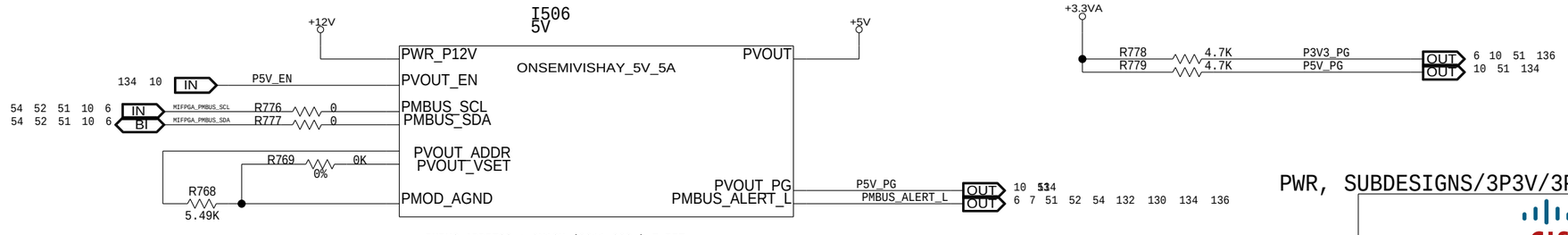
ALTERNATIVE CIRCUIT





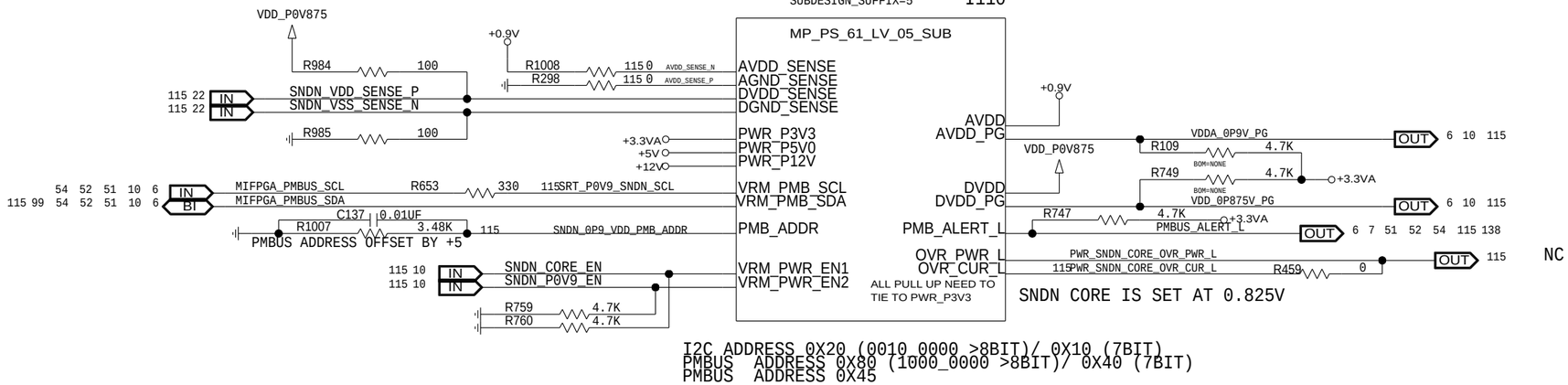


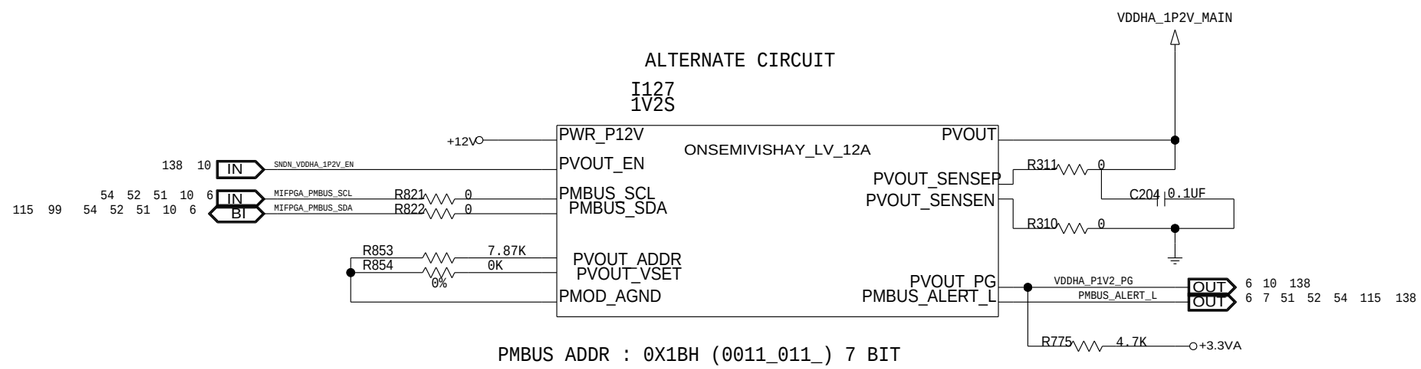


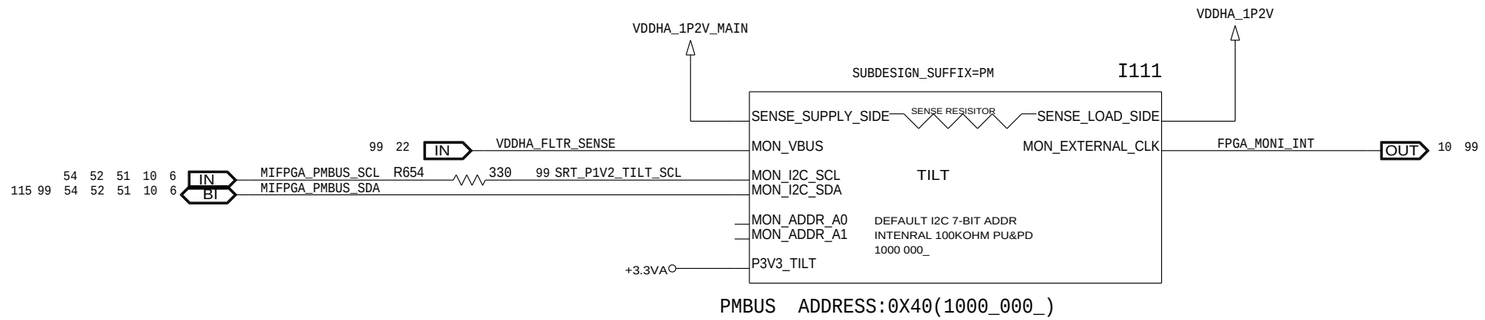
PWR, SUBDESIGNS/3P3V/3P3_SFP/5V

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:47 2022		51 OF 138







PWR, SUNDOWN1 POWER

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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SUBDESIGN_SUFFIX=A

I145

CY5_FPGA3RAIL_15A_3A_3A

+3.3VA 9A +2.5VA 3A P1_1VA 3A

+3.3VA

R1845 10K

+12V

R306 30.1K

C578 0.1UF

R1844 10K

PWR_P12V

MAX 200UF PWR_P3V3

MAX100UF PWR_P2V5

MAX 200UF PWR_P1V1

PWR_ADOMAIN_PGOOD

PWR_EN MAX 6.5V VIH 2.0V

PWRGD OD

OUT

101 NC

101 NC

IN PMBUS_ADOMAIN_SCL

IN PMBUS_ADOMAIN_SDA

PMB_CLK

PMB_DATA

PMB_ADDR

PMB_ADDR_VOUT

PMB_ALERT_L OD

PMBUS_ADOMAIN_ALERT_L

OUT NC 101

R557 105K

R562 249K

R543 4.7K +3.3VA

+3.3VA

R541 4.7K

R542 4.7K

ADDR=0X0011_001X=0X32

RHIGH=249K

RLOW=105K

10 11 101

PWR_1V8_ADOMAIN

C110 220PF 50V

+2.5VA

C148 10UF 6.3V

U87

14 IN2 OUT2 16

13 IN1 OUT1 15

C186 10NF 25V

11 SS PG 3

2 FB SNS 1

+3.3VA

12 EN 1.6V 10

R293 4.7K

800MV 9

400MV 8

200MV 6

100MV 5

50MV 4

GND1 7

EP 17

C188 10UF 6.3V

OUT

TPS7A7200RGT

15-101825-01

PROG_NUM=73-102884-01

INTERPOSER

PROG_NUM 73-102884-01

NONE

NONE

P1V8

P1V8 R932 1% 80.6K

R933 1% 30.9K

C138 10UF 6.3V

+3.3V

U3

14 IN2 OUT2 16

13 IN1 OUT1 15

R780 0

C16 10UF 6.3V

C17 2.2UF

P1V8

BOM=NONE

R397 0

7 IN P1V8_TRIM

R399 200K

C389 270PF P1V8_FB

11 SS PG 3

P1V8_PG OUT 6 10

C401 220PF

P1V8

2 FB SNS 1

R81 4.7K +3.3V

10 IN P1V8_EN

R77 4.7K

12 EN 1.6V 10

0.8V + 0.4V + 0.1V + (0.5V) = 1.8V

VOUT NOM 1.80V

VOUT +5% 1.89V

VOUT -5% 1.71V

800MV 9

400MV 8

200MV 6

100MV 5

50MV 4

GND1 7

EP 17

TPS7A7200RGT

PART_NUMBER=15-101825-01

73-102884-01

PWR, A DOMAIN,P1v8

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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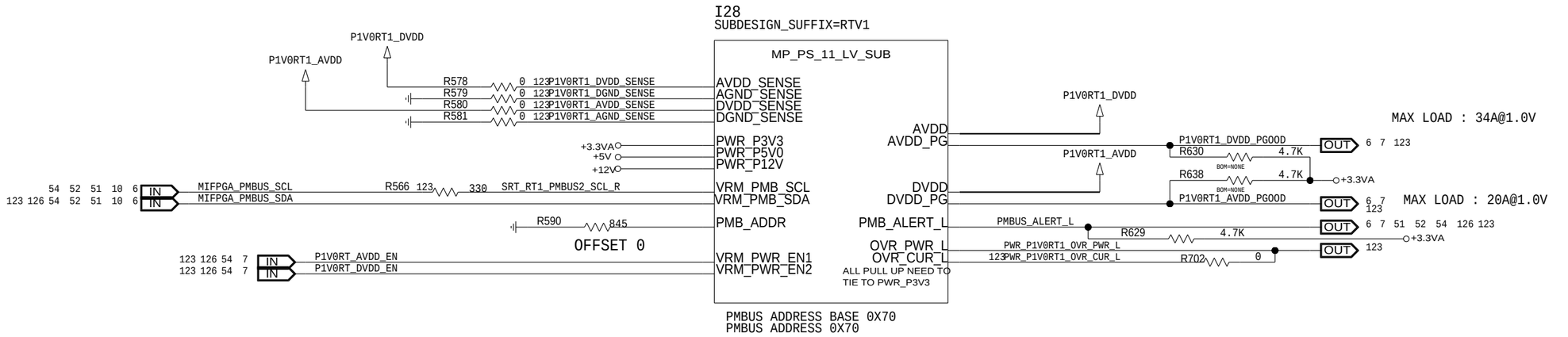
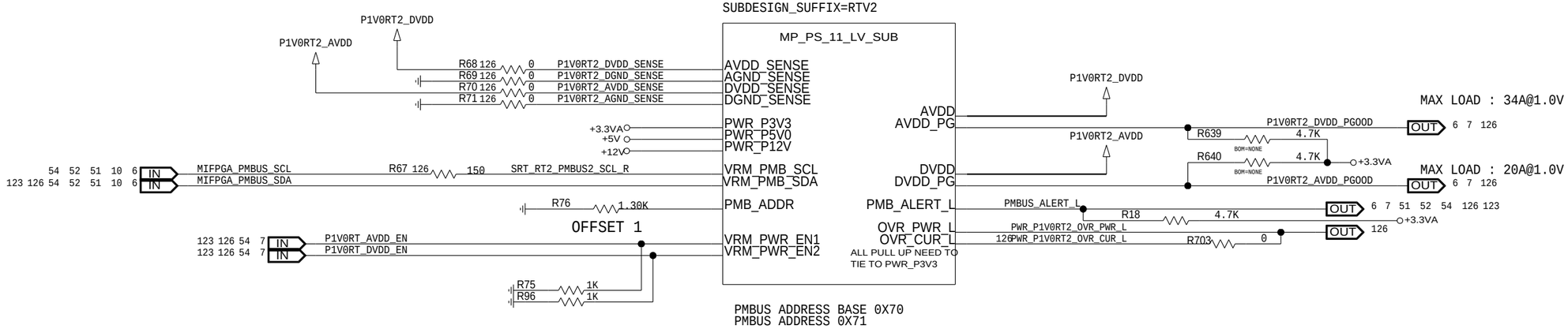
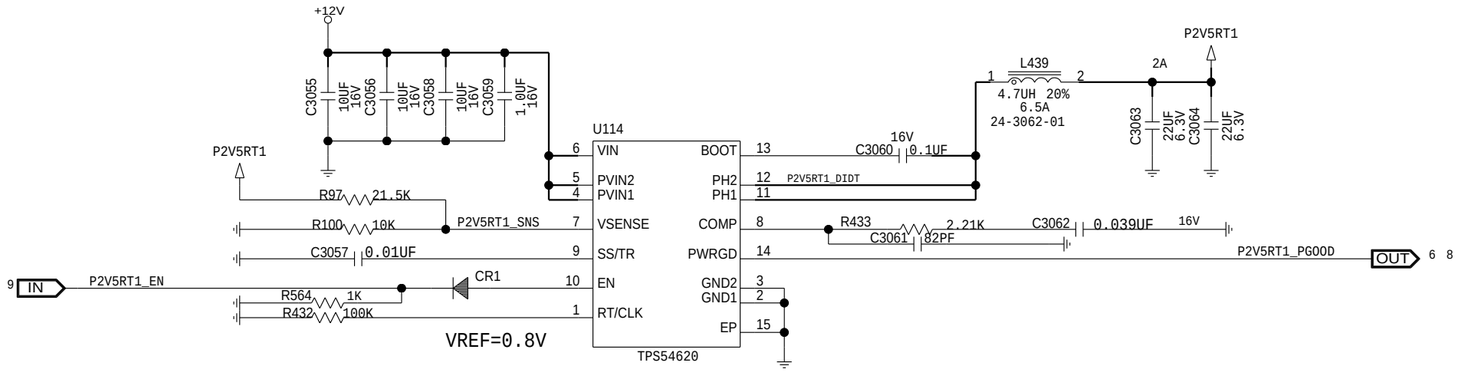
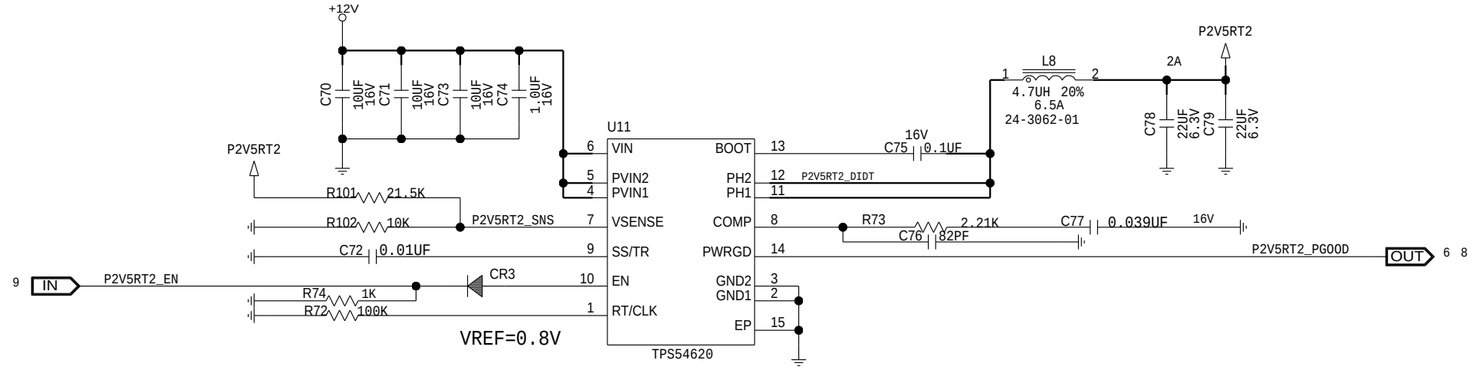




SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:39 2022		54 OF 138





SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
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LIGHTPIPE: 700-11629-01 UNDER 800-LEVEL BOM

P3V3_STBY
R658 4.7K
P3V3_STBY
R657 4.7K
CON_BCK_BLUE_LED
BLUE CR101 25-1188-01
R1324 120
P3V3_STBY
PLACEMENT NEAR FACEPLATE/CUSTOMER VISIBLE
Q15 BSS138_BP-FR
56 IN LED_BCN_BLUE_L

R141 0 NONE
R142 0 NONE
R535 10K
U12
4 IN IO_MI_SER_DATA 4 YA I1A 3 I0A 2 IO_MI2_DATA_FPGA IO_MI2_DATA_BMC OUT NC OUT 56
4 IN IO_MI_SER_CLK 7 YB I1B 6 I0B 5 IO_MI2_STROBE_FPGA IO_MI2_STROBE_BMC OUT NC OUT 56
NC 9 YC I1C 10 I0C 11 NC NC
NC 12 YD I1D 13 I0D 14 NC NC
R536 10K
C165 0.1UF P3V3_STBY
S 1 MIFPGA_POR_L 4 10 23 56
E 15 R53 130
QS3VH257
P3_3V=P3V3_STBY

P3V3_STBY
R132 4.7K
U40_DSA_BMC
U40
56 IN IO_MI2_DATA_BMC
56 IN IO_MI2_STROBE_BMC
R140 33
C598 0.1UF NONE
SRT_IO_MI2_STROBE_BMC
R539 4.7K U40_MR_BMC
P3V3_STBY
1 DSA
2 DSB
8 CP
9 MR
14 VCC
7 GND
Q7 13
Q6 12
Q5 11
Q4 10
Q3 6
Q2 5
Q1 4
Q0 3
HC164
C599 0.1UF P3V3_STBY

P3V3_STBY
R134 4.7K
56 23 10 4 IN MIFPGA_POR_L
CR8 BAT54T1G
LED_BY_BMC_L
10 IN MIFPGA_LED_CTRL
CR9 BAT54T1G
R146 0 NONE

SELECT PIN TABLE
LOW = BMC DRIVES LED
HIGH = FPGA DRIVES LED

U8
7 IN FPGA_LED_STAT_RED_L BMC_LED_STAT_RED_L 3 I1A 2 I0A YA 4 MUX_LED_STAT_RED_L 13 LVC07A U55 12 VCCIO=P3V3_STBY LED_STAT_RED_L OUT 56
7 IN FPGA_LED_STAT_GRN_L BMC_LED_STAT_GRN_L 6 I1B 5 I0B YB 7 MUX_LED_STAT_GRN_L 11 LVC07A U55 10 VCCIO=P3V3_STBY LED_STAT_GRN_L OUT 56
7 IN FPGA_LED_ENV_RED_L BMC_LED_ENV_RED_L 10 I1C 11 I0C YC 9 MUX_LED_ENV_RED_L 9 LVC07A U55 8 VCCIO=P3V3_STBY LED_ENV_RED_L OUT 56
7 IN FPGA_LED_ENV_GRN_L BMC_LED_ENV_GRN_L 13 I1D 14 I0D YD 12 MUX_LED_ENV_GRN_L 5 LVC07A U55 6 VCCIO=P3V3_STBY LED_ENV_GRN_L OUT 56
1 S
15 E
QS3VH257
P3_3V=P3V3_STBY
C602 0.1UF P3V3_STBY

U10
7 IN FPGA_LED_BCN_BLUE_L BMC_LED_BCN_BLUE_L 3 I1A 2 I0A YA 4 MUX_LED_BCN_BLUE_L R256 130 LED_BCN_BLUE_L OUT 56
IN FPGA_LED_BMC_RED_L BMC_LED_BMC_RED_L 6 I1B 5 I0B YB 7 MUX_LED_BMC_RED_L 1 LVC07A U55 2 VCCIO=P3V3_STBY LED_BMC_RED_L OUT NC
IN FPGA_LED_BMC_GRN_L BMC_LED_BMC_GRN_L 10 I1C 11 I0C YC 9 MUX_LED_BMC_GRN_L 3 LVC07A U55 4 VCCIO=P3V3_STBY LED_BMC_GRN_L OUT NC
R63 130 13 I1D 14 I0D YD 12
R64 130
R540 130 1 S 15 E
QS3VH257
P3_3V=P3V3_STBY
C601 0.1UF P3V3_STBY

P3V3_STBY
CR5
8 IN LED_STAT_RED_L R643 162 C2 RED
56 IN LED_STAT_GRN_L R695 162 C1 GRN
A
STATUS LED
CR6
56 IN LED_ENV_RED_L R691 162 C2 RED
56 IN LED_ENV_GRN_L R692 162 C1 GRN
A
ENV LED
SYNCE/TIME/GNSS LEDS ARE NOT CONTROLLED BY BMC
CR7
8 IN LED_SYNCE_RED_L R693 162 C2 RED
8 IN LED_SYNCE_GRN_L R694 162 C1 GRN
A
SYNCE LED
CR10
8 IN LED_TIME_RED_L R698 162 C2 RED
8 IN LED_TIME_GRN_L R699 162 C1 GRN
A
TIME LED
CR11
8 IN LED_GNSS_RED_L R700 162 C2 RED
8 IN LED_GNSS_GRN_L R701 162 C1 GRN
A
GNSS LED
C600 0.1UF P3V3_STBY

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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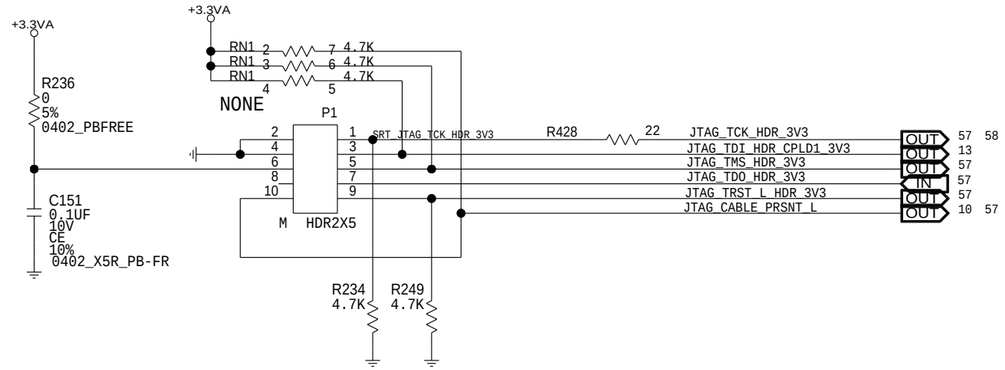

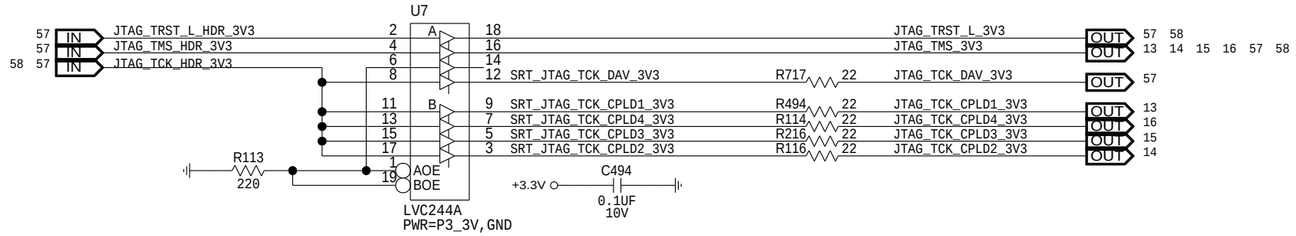

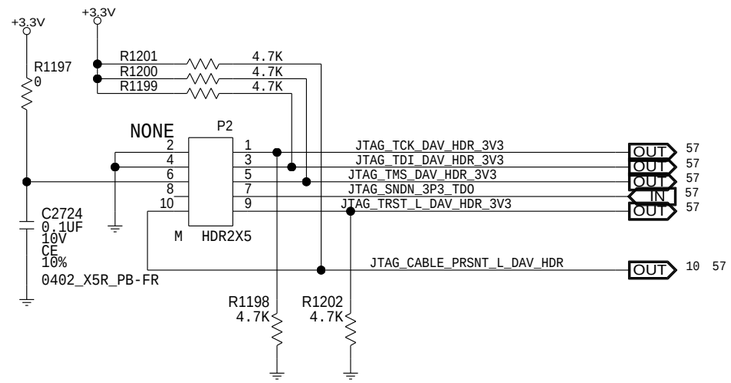

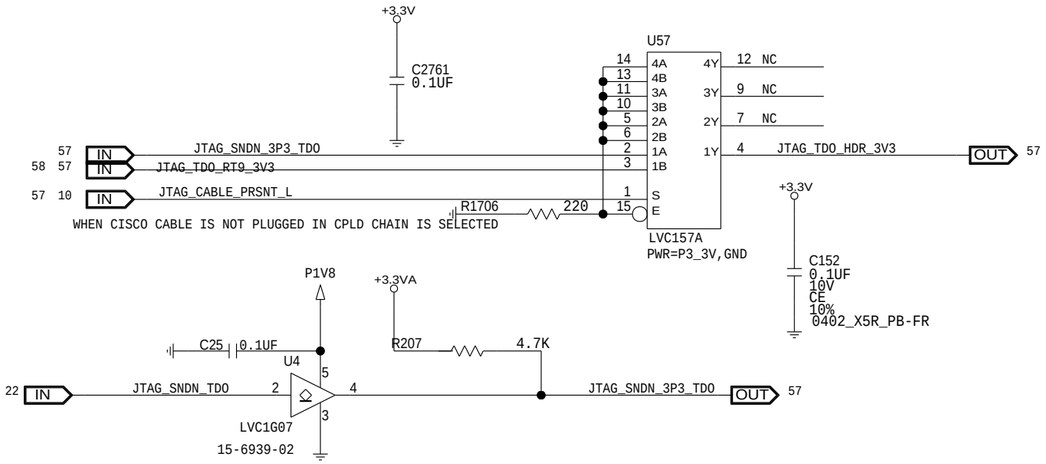

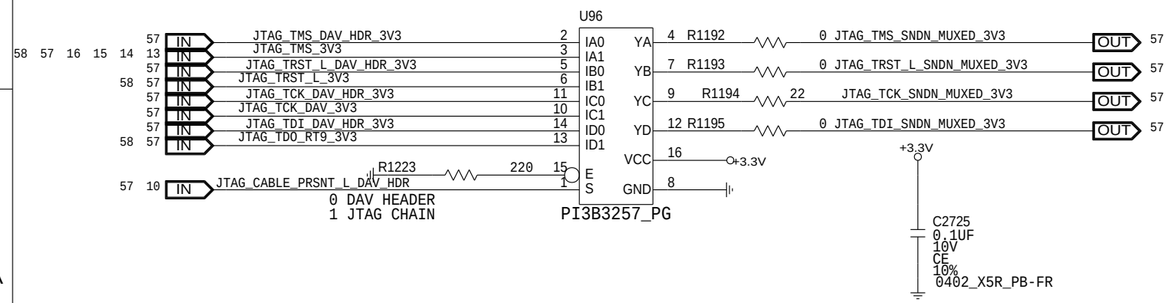

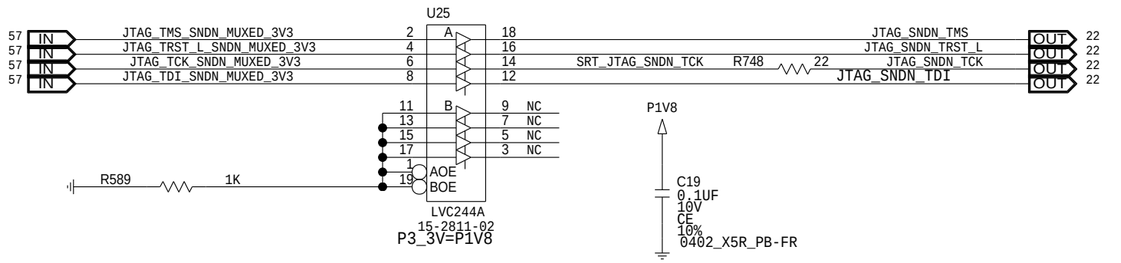

JTAG HEADER\BUFFER

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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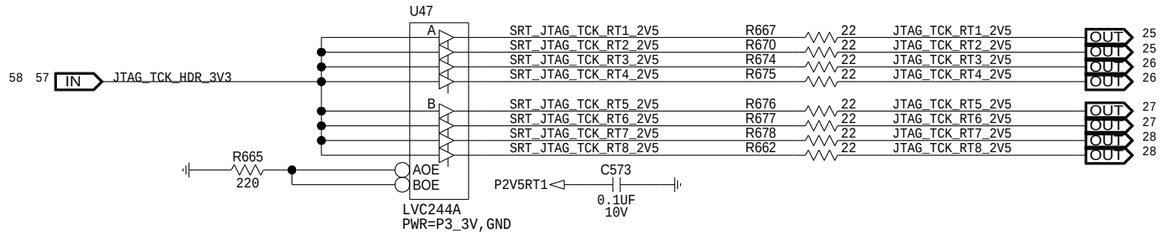
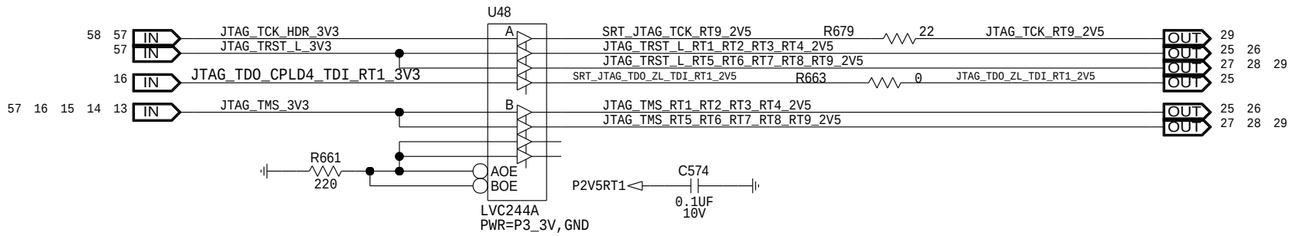
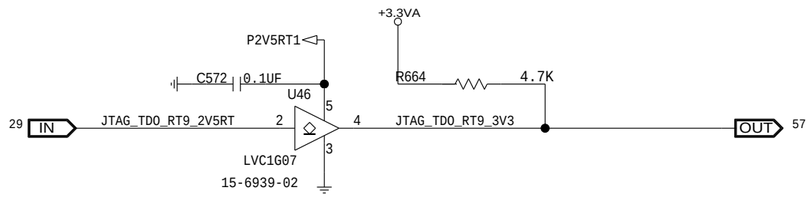
P3_3V=P2V5RT1



P3_3V=P2V5RT1





SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:33:43 2022		58 OF 138

DWG NO	SHT	REV
92-105229-01	138	A0

REVISION					
REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD

2X12 SFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:

65 64 63 62 61 60 49 IN — SFP_SDA<23..0> — BI
65 64 63 62 61 60 49 IN — SFP_SCL<23..0> — BI

65 64 63 62 61 60 49 IN — SFP_TX_DISABLE<23..0> — OUT

65 64 63 62 61 60 49 IN — SFP_RS0<23..0> — OUT
65 64 63 62 61 60 49 IN — SFP_RS1<23..0> — OUT
65 64 63 62 61 60 49 IN — SFP_YEL_LED_L<23..0> — OUT
65 64 63 62 61 60 49 IN — SFP_GRN_LED_L<23..0> — OUT

65 64 63 62 61 60 49 IN — HSD_MAC_SFP_P<23..0> — OUT
65 64 63 62 61 60 49 IN — HSD_MAC_SFP_N<23..0> — OUT

65 64 63 62 61 60 49 IN — HSD_SFP_MAC_N<23..0> — OUT
65 64 63 62 61 60 49 IN — HSD_SFP_MAC_P<23..0> — OUT

65 64 63 62 61 60 49 IN — SFP_RX_LOS<23..0> — OUT
65 64 63 62 61 60 49 IN — SFP_MOD_ABS<23..0> — OUT
65 64 63 62 61 60 49 IN — SFP_TX_FAULT<23..0> — OUT

65 64 63 62 61 60 IN — PWR_P3V3 — OUT

65 64 63 62 61 60 IN — PWR_LED_P3V3 — OUT

TITLE

QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± DECIM .xx ±.01 .xxx±.005 ANGLES ±1°

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION | DO NOT SCALE DWG

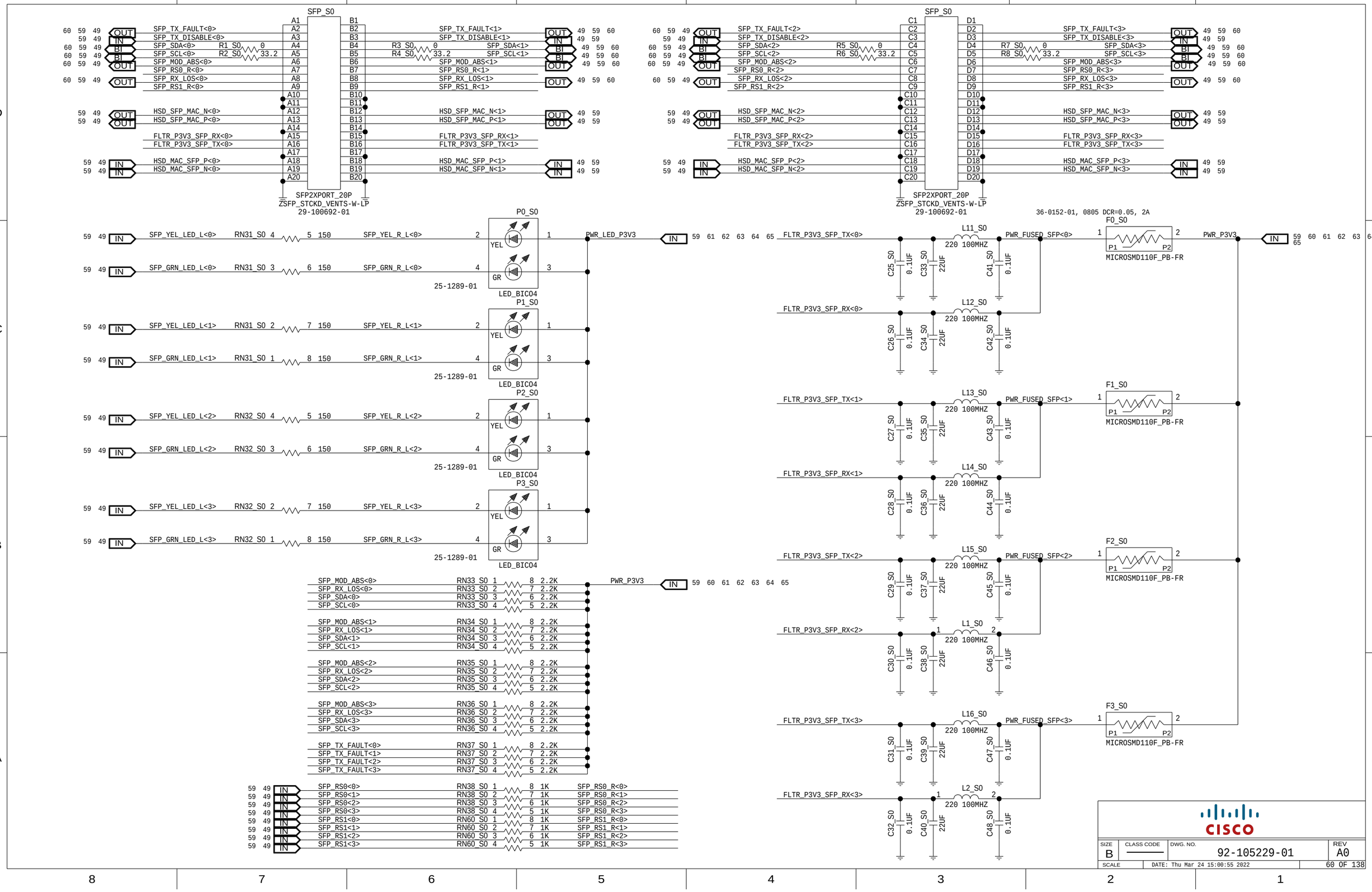
APPROVALS	DATE
DRAWN BY BCORDEIR	
CAD	
MECH	
ENGR BCORDEIR	
MFG	
TEST	

CISCO

TITLE: SFP 2X12 W/O RETIMER

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-XXXX-01	A0

SCALE | DATE: Fri May 17 11:40:52 2019 | 59 OF 138


SFP_S0
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<0>
SFP_TX_DISABLE<0>
SFP_SDA<0>
SFP_SCL<0>
SFP_MOD_ABS<0>
SFP_RS0_R<0>
SFP_RX_LOS<0>
SFP_RS1_R<0>
R1_S0 0
R2_S0 33.2
HSD_SFP_MAC_N<0>
HSD_SFP_MAC_P<0>
FLTR_P3V3_SFP_RX<0>
FLTR_P3V3_SFP_TX<0>
HSD_MAC_SFP_P<0>
HSD_MAC_SFP_N<0>
SFP_TX_FAULT<1>
SFP_TX_DISABLE<1>
SFP_SDA<1>
SFP_SCL<1>
SFP_MOD_ABS<1>
SFP_RS0_R<1>
SFP_RX_LOS<1>
SFP_RS1_R<1>
R3_S0 0
R4_S0 33.2
HSD_SFP_MAC_N<1>
HSD_SFP_MAC_P<1>
FLTR_P3V3_SFP_RX<1>
FLTR_P3V3_SFP_TX<1>
HSD_MAC_SFP_P<1>
HSD_MAC_SFP_N<1>
SFP_TX_FAULT<2>
SFP_TX_DISABLE<2>
SFP_SDA<2>
SFP_SCL<2>
SFP_MOD_ABS<2>
SFP_RS0_R<2>
SFP_RX_LOS<2>
SFP_RS1_R<2>
R5_S0 0
R6_S0 33.2
HSD_SFP_MAC_N<2>
HSD_SFP_MAC_P<2>
FLTR_P3V3_SFP_RX<2>
FLTR_P3V3_SFP_TX<2>
HSD_MAC_SFP_P<2>
HSD_MAC_SFP_N<2>
SFP_TX_FAULT<3>
SFP_TX_DISABLE<3>
SFP_SDA<3>
SFP_SCL<3>
SFP_MOD_ABS<3>
SFP_RS0_R<3>
SFP_RX_LOS<3>
SFP_RS1_R<3>
R7_S0 0
R8_S0 33.2
HSD_SFP_MAC_N<3>
HSD_SFP_MAC_P<3>
HSD_MAC_SFP_P<3>
HSD_MAC_SFP_N<3>
P0_S0
P1_S0
P2_S0
P3_S0
LED_BICO4
25-1289-01
YEL
GR
SFP_YEL_LED_L<0>
SFP_GRN_LED_L<0>
SFP_YEL_LED_L<1>
SFP_GRN_LED_L<1>
SFP_YEL_LED_L<2>
SFP_GRN_LED_L<2>
SFP_YEL_LED_L<3>
SFP_GRN_LED_L<3>
RN31_S0 4
RN31_S0 3
RN31_S0 2
RN31_S0 1
RN32_S0 4
RN32_S0 3
RN32_S0 2
RN32_S0 1
5 150
6 150
7 150
8 150
SFP_YEL_R_L<0>
SFP_GRN_R_L<0>
SFP_YEL_R_L<1>
SFP_GRN_R_L<1>
SFP_YEL_R_L<2>
SFP_GRN_R_L<2>
SFP_YEL_R_L<3>
SFP_GRN_R_L<3>
PWR_LED_P3V3
RN33_S0 1
RN33_S0 2
RN33_S0 3
RN33_S0 4
RN34_S0 1
RN34_S0 2
RN34_S0 3
RN34_S0 4
RN35_S0 1
RN35_S0 2
RN35_S0 3
RN35_S0 4
RN36_S0 1
RN36_S0 2
RN36_S0 3
RN36_S0 4
RN37_S0 1
RN37_S0 2
RN37_S0 3
RN37_S0 4
8 2.2K
7 2.2K
6 2.2K
5 2.2K
RN38_S0 1
RN38_S0 2
RN38_S0 3
RN38_S0 4
RN60_S0 1
RN60_S0 2
RN60_S0 3
RN60_S0 4
8 1K
7 1K
6 1K
5 1K
SFP_RS0_R<0>
SFP_RS0_R<1>
SFP_RS0_R<2>
SFP_RS0_R<3>
SFP_RS1_R<0>
SFP_RS1_R<1>
SFP_RS1_R<2>
SFP_RS1_R<3>
PWR_P3V3
36-0152-01, 0805 DCR=0.05, 2A
L11_S0
L12_S0
L13_S0
L14_S0
L15_S0
L1_S0
L16_S0
L2_S0
220 100MHZ
PWR_FUSED_SFP<0>
PWR_FUSED_SFP<1>
PWR_FUSED_SFP<2>
PWR_FUSED_SFP<3>
F0_S0
F1_S0
F2_S0
F3_S0
MICROSMD110F_PB-FR
P1
P2
C25_S0
C33_S0
C41_S0
C26_S0
C34_S0
C42_S0
C27_S0
C35_S0
C43_S0
C28_S0
C36_S0
C44_S0
C29_S0
C37_S0
C45_S0
C30_S0
C38_S0
C46_S0
C31_S0
C39_S0
C47_S0
C32_S0
C40_S0
C48_S0
0.1UF
22UF
FLTR_P3V3_SFP_TX<0>
FLTR_P3V3_SFP_RX<0>
FLTR_P3V3_SFP_TX<1>
FLTR_P3V3_SFP_RX<1>
FLTR_P3V3_SFP_TX<2>
FLTR_P3V3_SFP_RX<2>
FLTR_P3V3_SFP_TX<3>
FLTR_P3V3_SFP_RX<3>
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:55 2022
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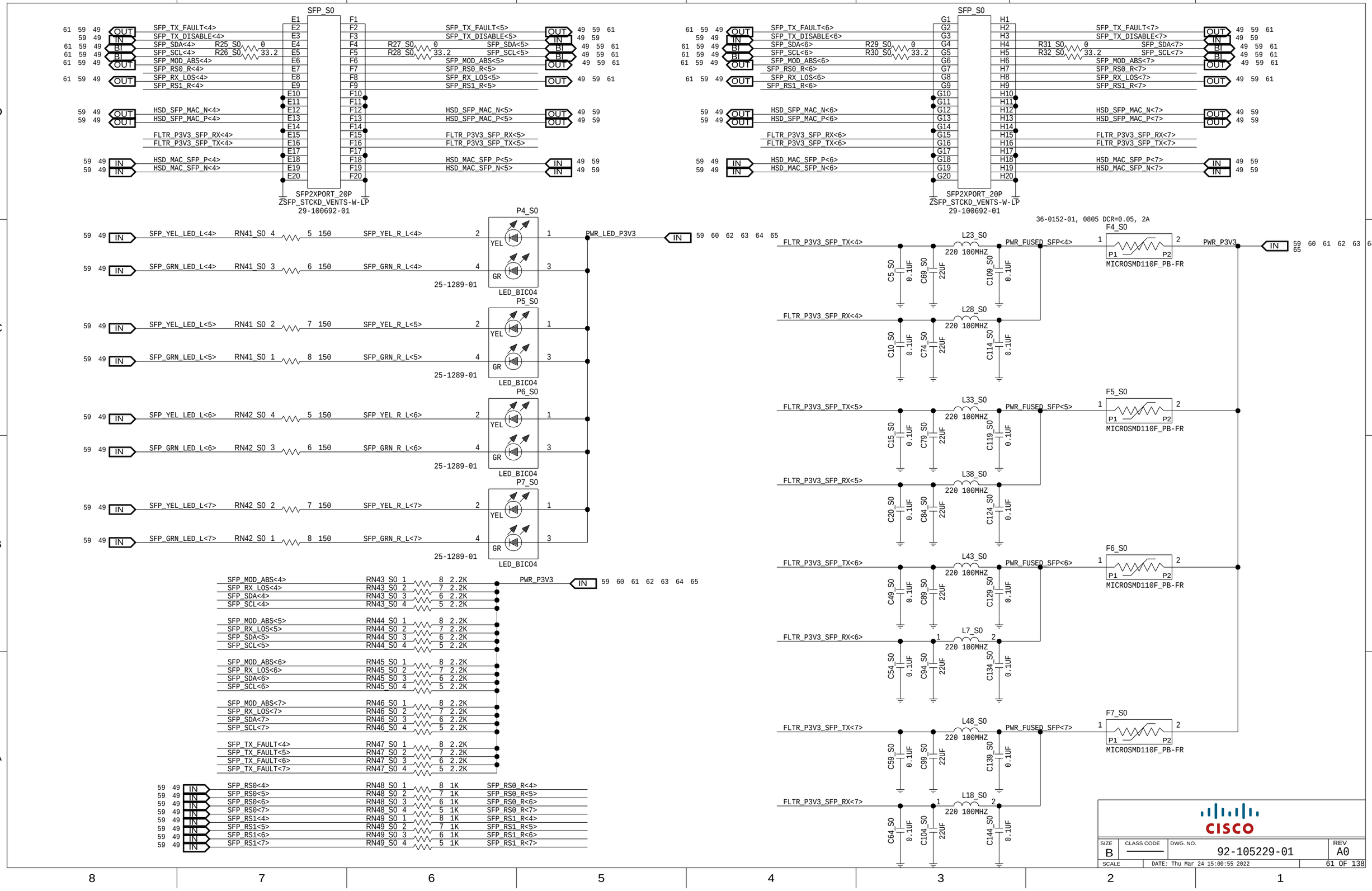
SFP_S0
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<4>
SFP_TX_DISABLE<4>
SFP_SDA<4>
SFP_SCL<4>
SFP_MOD_ABS<4>
SFP_RS0_R<4>
SFP_RX_LOS<4>
SFP_RS1_R<4>
HSD_SFP_MAC_N<4>
HSD_SFP_MAC_P<4>
FLTR_P3V3_SFP_RX<4>
FLTR_P3V3_SFP_TX<4>
HSD_MAC_SFP_P<4>
HSD_MAC_SFP_N<4>
R25_S0 0 33.2 R26_S0
R27_S0 0 33.2 R28_S0
SFP_TX_FAULT<5>
SFP_TX_DISABLE<5>
SFP_SDA<5>
SFP_SCL<5>
SFP_MOD_ABS<5>
SFP_RS0_R<5>
SFP_RX_LOS<5>
SFP_RS1_R<5>
HSD_SFP_MAC_N<5>
HSD_SFP_MAC_P<5>
FLTR_P3V3_SFP_RX<5>
FLTR_P3V3_SFP_TX<5>
HSD_MAC_SFP_P<5>
HSD_MAC_SFP_N<5>
SFP_S0
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<6>
SFP_TX_DISABLE<6>
SFP_SDA<6>
SFP_SCL<6>
SFP_MOD_ABS<6>
SFP_RS0_R<6>
SFP_RX_LOS<6>
SFP_RS1_R<6>
HSD_SFP_MAC_N<6>
HSD_SFP_MAC_P<6>
FLTR_P3V3_SFP_RX<6>
FLTR_P3V3_SFP_TX<6>
HSD_MAC_SFP_P<6>
HSD_MAC_SFP_N<6>
R29_S0 0 33.2 R30_S0
SFP_TX_FAULT<7>
SFP_TX_DISABLE<7>
SFP_SDA<7>
SFP_SCL<7>
SFP_MOD_ABS<7>
SFP_RS0_R<7>
SFP_RX_LOS<7>
SFP_RS1_R<7>
HSD_SFP_MAC_N<7>
HSD_SFP_MAC_P<7>
FLTR_P3V3_SFP_RX<7>
FLTR_P3V3_SFP_TX<7>
HSD_MAC_SFP_P<7>
HSD_MAC_SFP_N<7>
P4_S0
P5_S0
P6_S0
P7_S0
LED_BICO4
25-1289-01
SFP_YEL_LED_L<4>
SFP_GRN_LED_L<4>
SFP_YEL_LED_L<5>
SFP_GRN_LED_L<5>
SFP_YEL_LED_L<6>
SFP_GRN_LED_L<6>
SFP_YEL_LED_L<7>
SFP_GRN_LED_L<7>
RN41_S0 4 5 150
RN41_S0 3 6 150
RN41_S0 2 7 150
RN41_S0 1 8 150
RN42_S0 4 5 150
RN42_S0 3 6 150
RN42_S0 2 7 150
RN42_S0 1 8 150
SFP_YEL_R_L<4>
SFP_GRN_R_L<4>
SFP_YEL_R_L<5>
SFP_GRN_R_L<5>
SFP_YEL_R_L<6>
SFP_GRN_R_L<6>
SFP_YEL_R_L<7>
SFP_GRN_R_L<7>
PWR_LED_P3V3
RN43_S0 1 8 2.2K
RN43_S0 2 7 2.2K
RN43_S0 3 6 2.2K
RN43_S0 4 5 2.2K
RN44_S0 1 8 2.2K
RN44_S0 2 7 2.2K
RN44_S0 3 6 2.2K
RN44_S0 4 5 2.2K
RN45_S0 1 8 2.2K
RN45_S0 2 7 2.2K
RN45_S0 3 6 2.2K
RN45_S0 4 5 2.2K
RN46_S0 1 8 2.2K
RN46_S0 2 7 2.2K
RN46_S0 3 6 2.2K
RN46_S0 4 5 2.2K
RN47_S0 1 8 2.2K
RN47_S0 2 7 2.2K
RN47_S0 3 6 2.2K
RN47_S0 4 5 2.2K
RN48_S0 1 8 1K
RN48_S0 2 7 1K
RN48_S0 3 6 1K
RN48_S0 4 5 1K
RN49_S0 1 8 1K
RN49_S0 2 7 1K
RN49_S0 3 6 1K
RN49_S0 4 5 1K
SFP_RS0<4>
SFP_RS0<5>
SFP_RS0<6>
SFP_RS0<7>
SFP_RS1<4>
SFP_RS1<5>
SFP_RS1<6>
SFP_RS1<7>
SFP_RS0_R<4>
SFP_RS0_R<5>
SFP_RS0_R<6>
SFP_RS0_R<7>
SFP_RS1_R<4>
SFP_RS1_R<5>
SFP_RS1_R<6>
SFP_RS1_R<7>
36-0152-01, 0805 DCR=0.05, 2A
F4_S0
F5_S0
F6_S0
F7_S0
MICROSMD110F_PB-FR
L23_S0
L28_S0
L33_S0
L38_S0
L43_S0
L7_S0
L48_S0
L18_S0
220 100MHZ
FLTR_P3V3_SFP_TX<4>
FLTR_P3V3_SFP_RX<4>
FLTR_P3V3_SFP_TX<5>
FLTR_P3V3_SFP_RX<5>
FLTR_P3V3_SFP_TX<6>
FLTR_P3V3_SFP_RX<6>
FLTR_P3V3_SFP_TX<7>
FLTR_P3V3_SFP_RX<7>
PWR_FUSED_SFP<4>
PWR_FUSED_SFP<5>
PWR_FUSED_SFP<6>
PWR_FUSED_SFP<7>
PWR_P3V3
C5_S0 C69_S0 C109_S0
C10_S0 C74_S0 C114_S0
C15_S0 C79_S0 C119_S0
C20_S0 C84_S0 C124_S0
C49_S0 C89_S0 C129_S0
C54_S0 C94_S0 C134_S0
C59_S0 C99_S0 C139_S0
C64_S0 C104_S0 C144_S0
0.1UF
22UF
CISCO
SIZE B
CLASS CODE
DWG. NO. 92-105229-01
REV A0
SCALE
DATE: Thu Mar 24 15:00:55 2022
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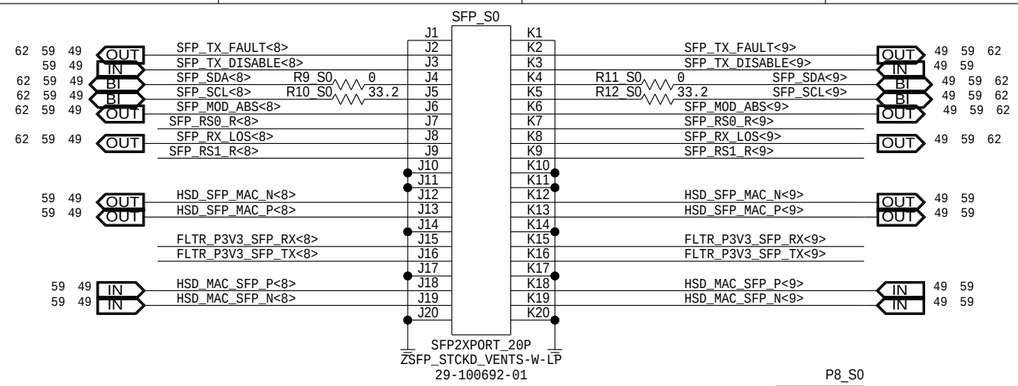
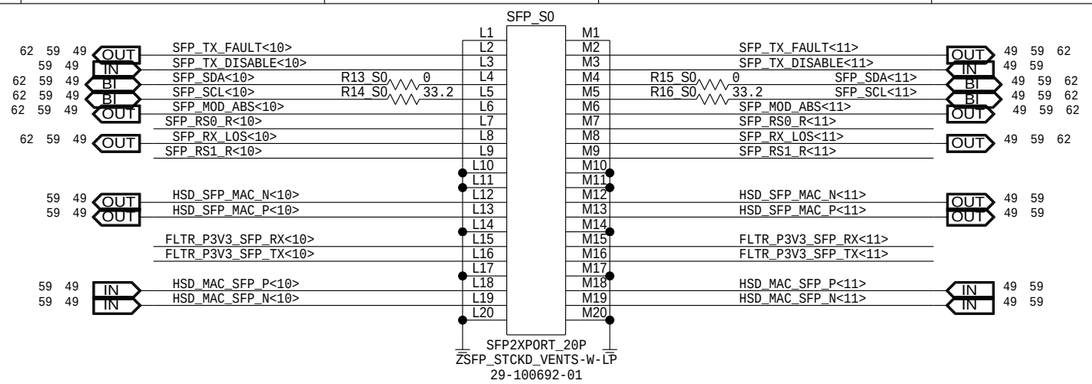
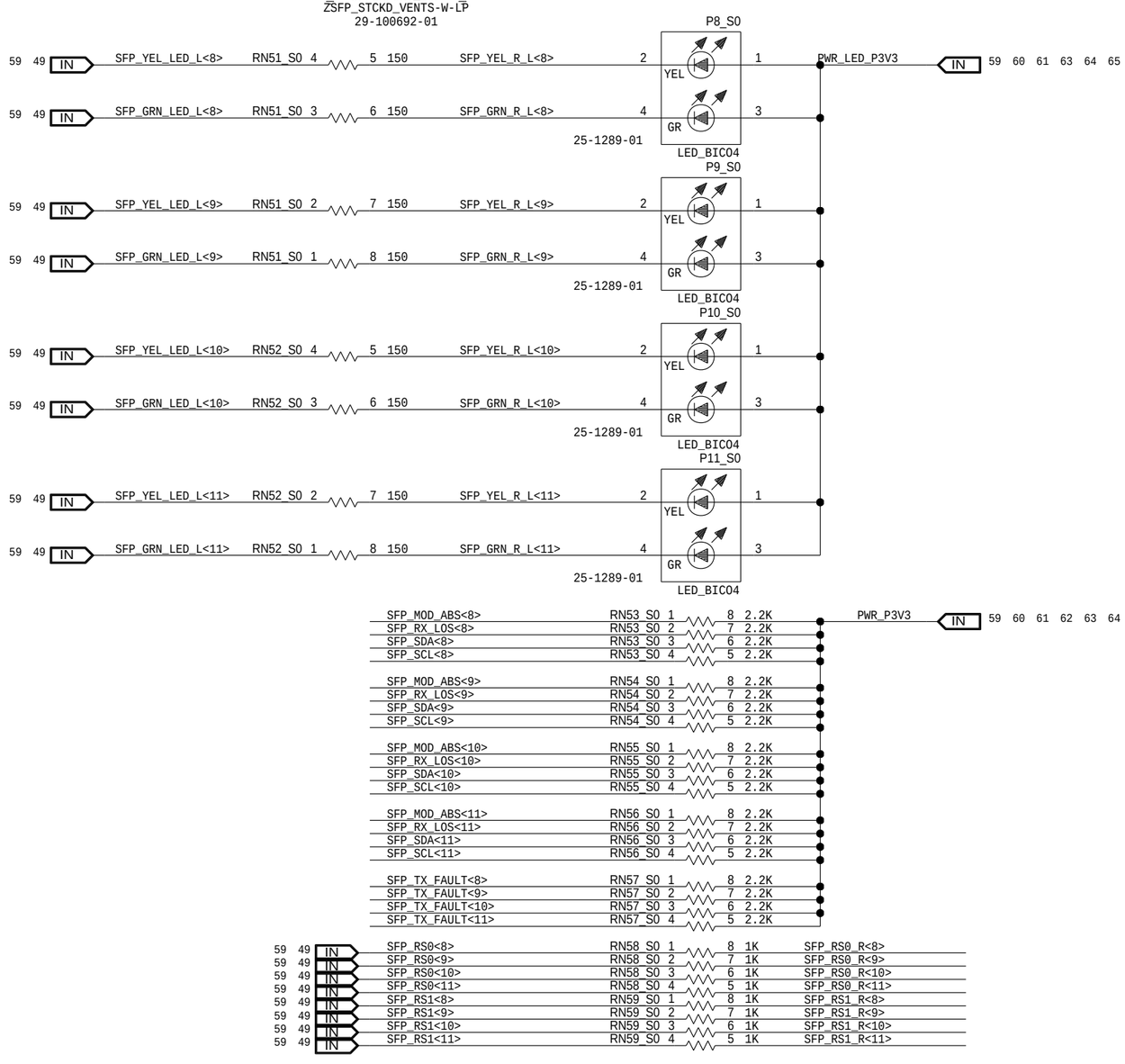
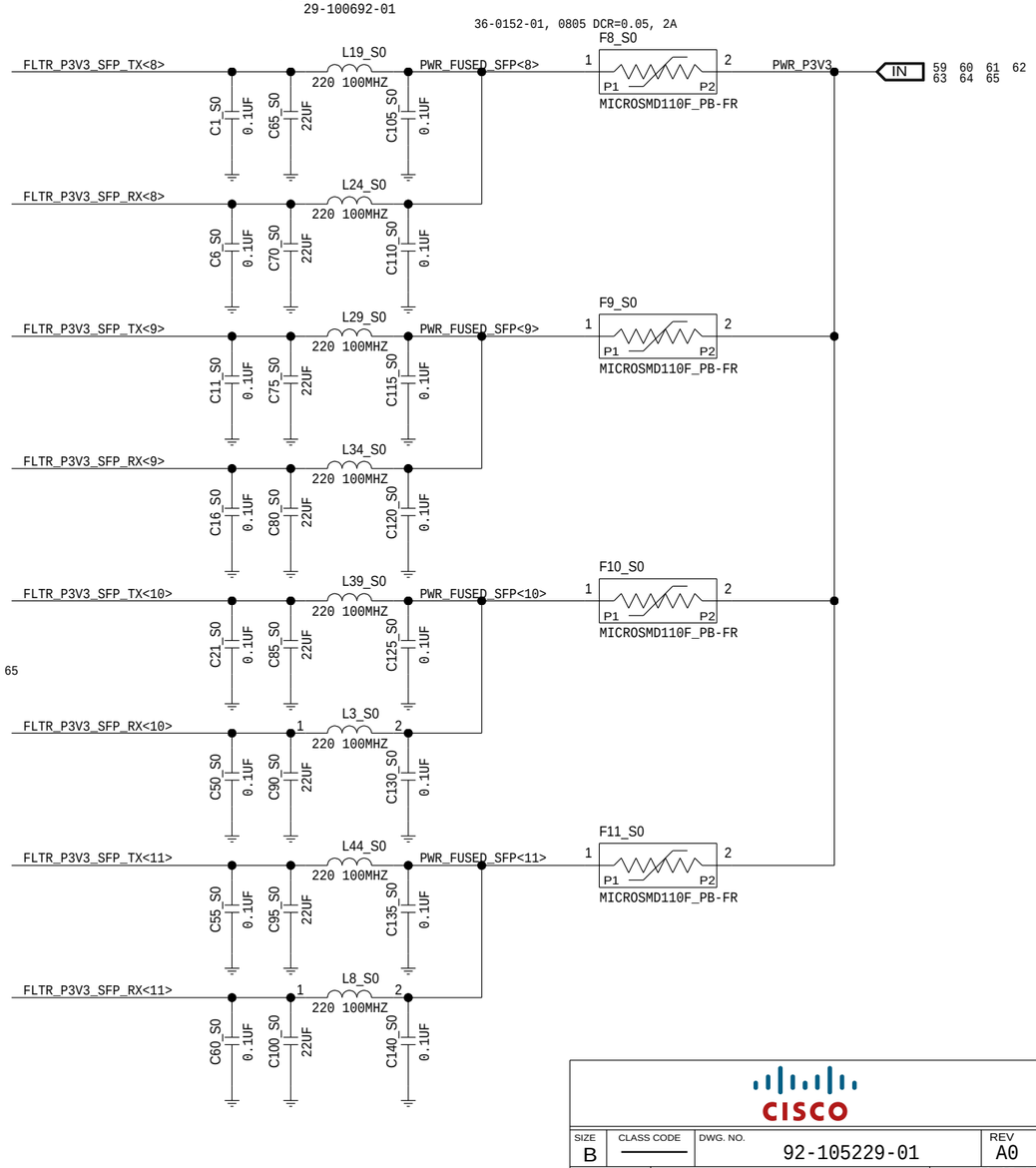
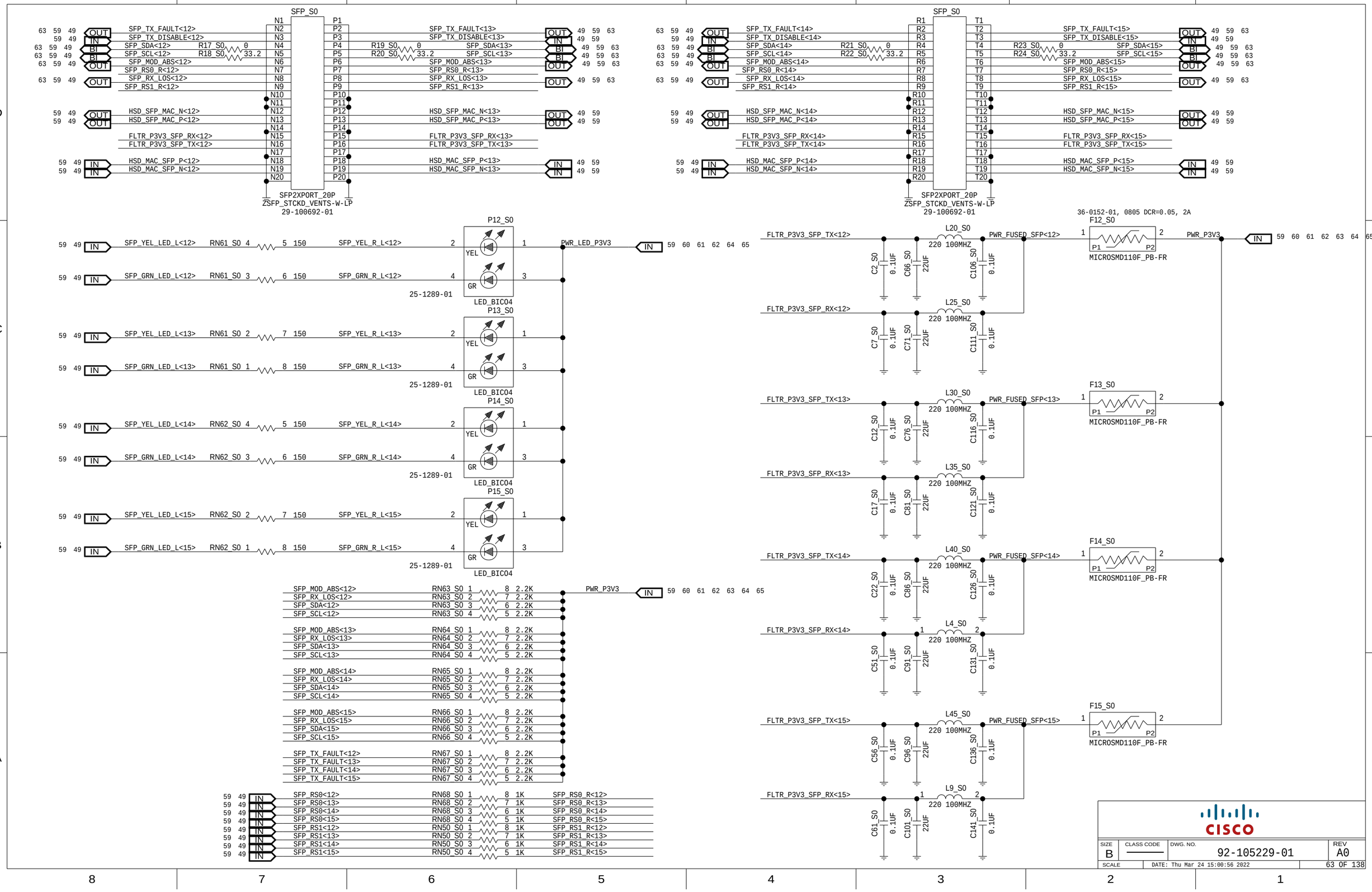


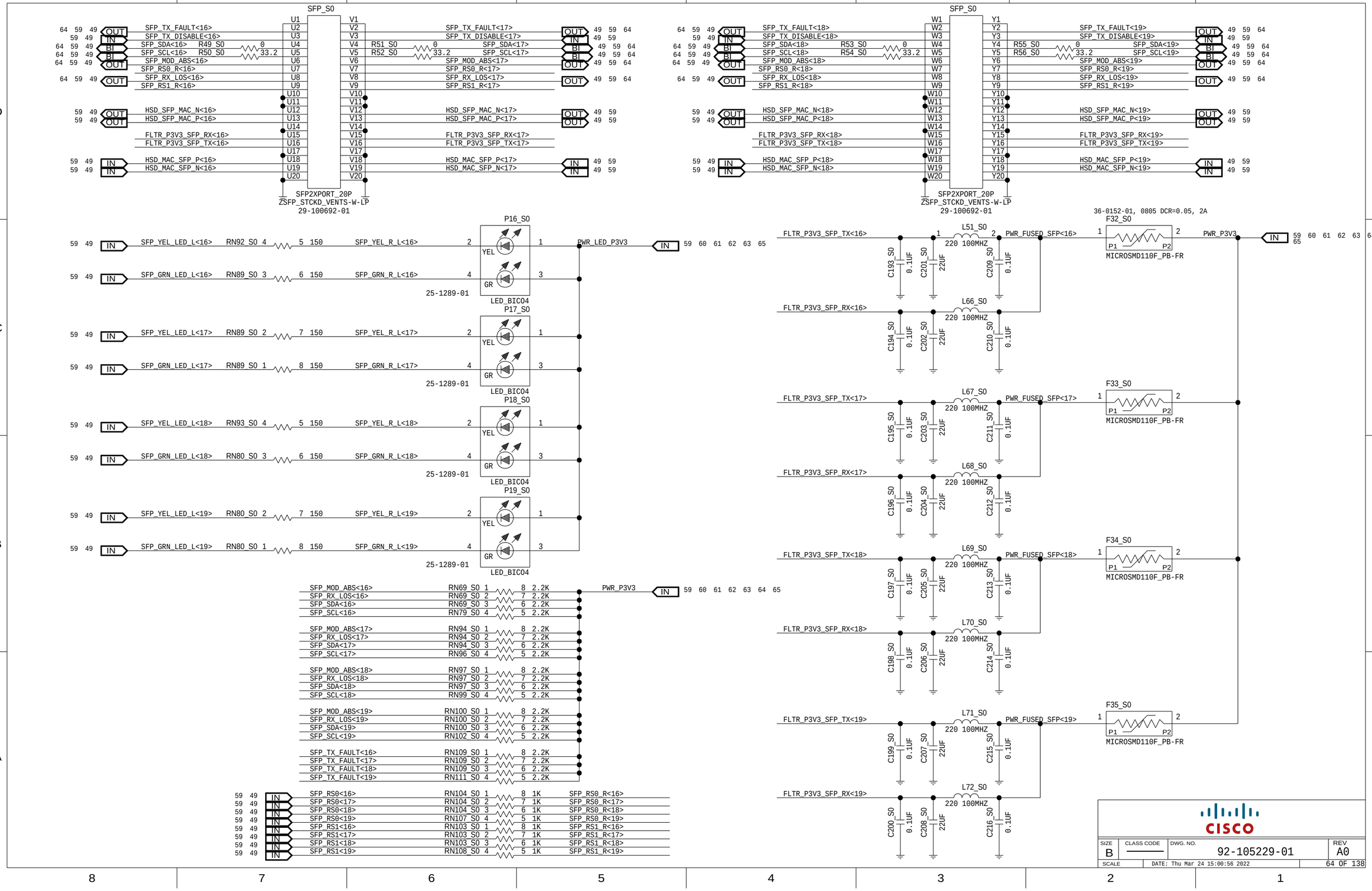


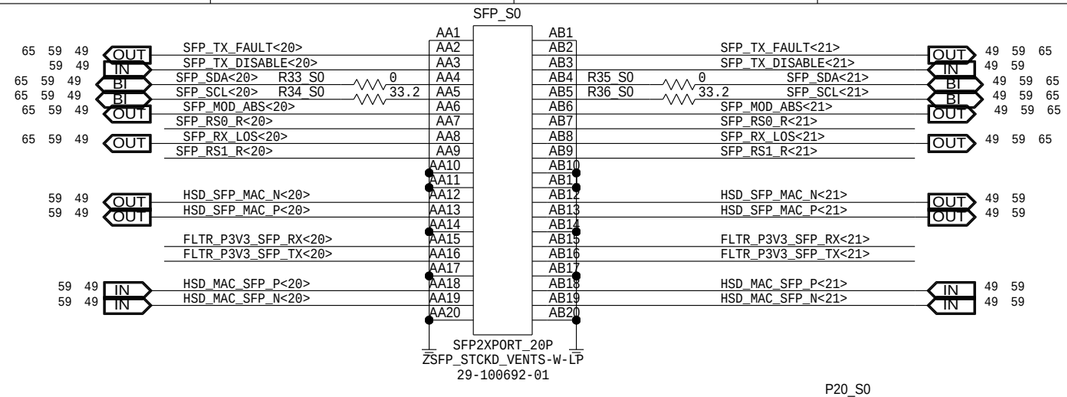


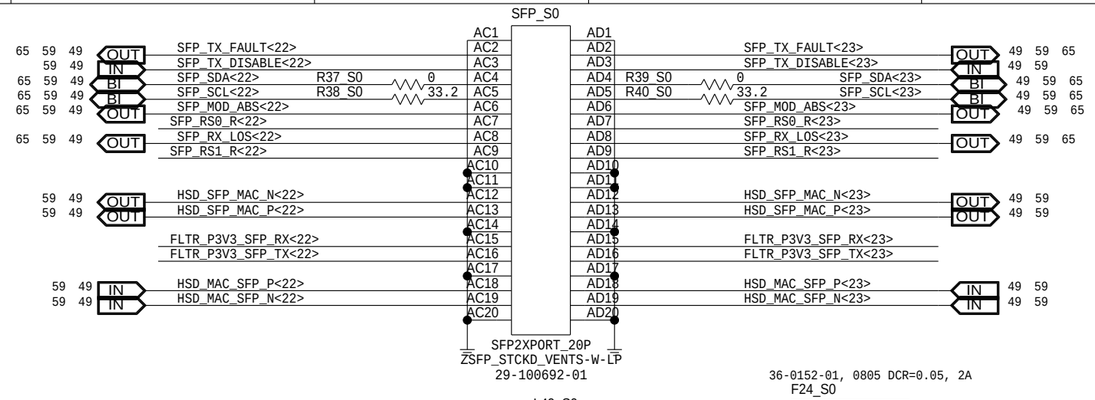


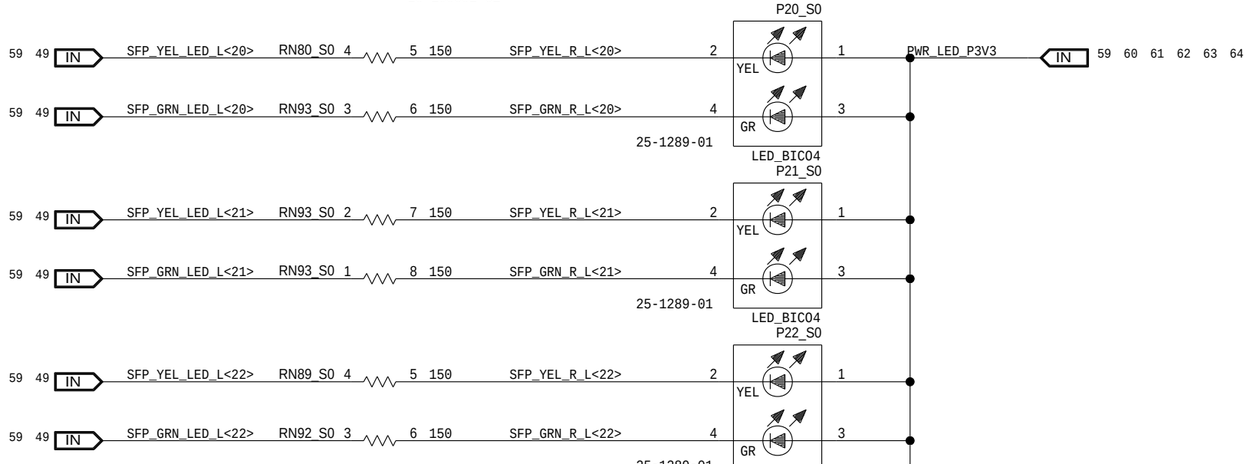
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:55 2022		62 OF 138

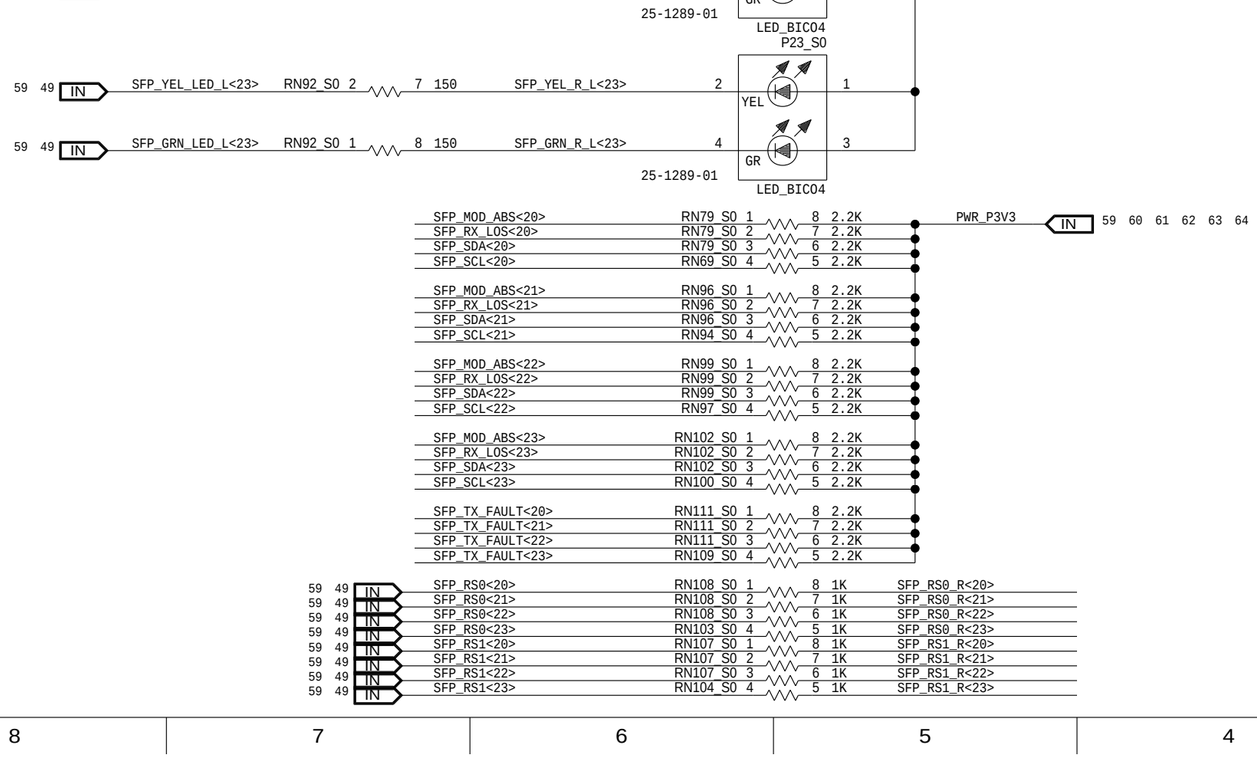

SFP_S0
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<12>
SFP_TX_DISABLE<12>
SFP_SDA<12>
SFP_SCL<12>
SFP_MOD_ABS<12>
SFP_RS0_R<12>
SFP_RX_LOS<12>
SFP_RS1_R<12>
HSD_SFP_MAC_N<12>
HSD_SFP_MAC_P<12>
FLTR_P3V3_SFP_RX<12>
FLTR_P3V3_SFP_TX<12>
HSD_MAC_SFP_P<12>
HSD_MAC_SFP_N<12>
R17_S0
R18_S0
33.2
SFP_TX_FAULT<13>
SFP_TX_DISABLE<13>
SFP_SDA<13>
SFP_SCL<13>
SFP_MOD_ABS<13>
SFP_RS0_R<13>
SFP_RX_LOS<13>
SFP_RS1_R<13>
HSD_SFP_MAC_N<13>
HSD_SFP_MAC_P<13>
FLTR_P3V3_SFP_RX<13>
FLTR_P3V3_SFP_TX<13>
HSD_MAC_SFP_P<13>
HSD_MAC_SFP_N<13>
R19_S0
R20_S0
SFP_TX_FAULT<14>
SFP_TX_DISABLE<14>
SFP_SDA<14>
SFP_SCL<14>
SFP_MOD_ABS<14>
SFP_RS0_R<14>
SFP_RX_LOS<14>
SFP_RS1_R<14>
HSD_SFP_MAC_N<14>
HSD_SFP_MAC_P<14>
FLTR_P3V3_SFP_RX<14>
FLTR_P3V3_SFP_TX<14>
HSD_MAC_SFP_P<14>
HSD_MAC_SFP_N<14>
R21_S0
R22_S0
SFP_TX_FAULT<15>
SFP_TX_DISABLE<15>
SFP_SDA<15>
SFP_SCL<15>
SFP_MOD_ABS<15>
SFP_RS0_R<15>
SFP_RX_LOS<15>
SFP_RS1_R<15>
HSD_SFP_MAC_N<15>
HSD_SFP_MAC_P<15>
FLTR_P3V3_SFP_RX<15>
FLTR_P3V3_SFP_TX<15>
HSD_MAC_SFP_P<15>
HSD_MAC_SFP_N<15>
R23_S0
R24_S0
P12_S0
P13_S0
P14_S0
P15_S0
LED_BICO4
25-1289-01
YEL
GR
SFP_YEL_LED_L<12>
SFP_GRN_LED_L<12>
SFP_YEL_LED_L<13>
SFP_GRN_LED_L<13>
SFP_YEL_LED_L<14>
SFP_GRN_LED_L<14>
SFP_YEL_LED_L<15>
SFP_GRN_LED_L<15>
RN61_S0_4
RN61_S0_3
RN61_S0_2
RN61_S0_1
RN62_S0_4
RN62_S0_3
RN62_S0_2
RN62_S0_1
SFP_YEL_R_L<12>
SFP_GRN_R_L<12>
SFP_YEL_R_L<13>
SFP_GRN_R_L<13>
SFP_YEL_R_L<14>
SFP_GRN_R_L<14>
SFP_YEL_R_L<15>
SFP_GRN_R_L<15>
PWR_LED_P3V3
RN63_S0_1
RN63_S0_2
RN63_S0_3
RN63_S0_4
RN64_S0_1
RN64_S0_2
RN64_S0_3
RN64_S0_4
RN65_S0_1
RN65_S0_2
RN65_S0_3
RN65_S0_4
RN66_S0_1
RN66_S0_2
RN66_S0_3
RN66_S0_4
RN67_S0_1
RN67_S0_2
RN67_S0_3
RN67_S0_4
RN68_S0_1
RN68_S0_2
RN68_S0_3
RN68_S0_4
RN50_S0_1
RN50_S0_2
RN50_S0_3
RN50_S0_4
SFP_RS0<12>
SFP_RS0<13>
SFP_RS0<14>
SFP_RS0<15>
SFP_RS1<12>
SFP_RS1<13>
SFP_RS1<14>
SFP_RS1<15>
SFP_RS0_R<12>
SFP_RS0_R<13>
SFP_RS0_R<14>
SFP_RS0_R<15>
SFP_RS1_R<12>
SFP_RS1_R<13>
SFP_RS1_R<14>
SFP_RS1_R<15>
PWR_P3V3
36-0152-01, 0805 DCR=0.05, 2A
F12_S0
F13_S0
F14_S0
F15_S0
MICROSMD110F_PB-FR
L20_S0
L25_S0
L30_S0
L35_S0
L40_S0
L4_S0
L45_S0
L9_S0
220 100MHZ
C2_S0
C66_S0
C106_S0
C7_S0
C71_S0
C111_S0
C12_S0
C76_S0
C116_S0
C17_S0
C81_S0
C121_S0
C22_S0
C86_S0
C126_S0
C51_S0
C91_S0
C131_S0
C56_S0
C96_S0
C136_S0
C61_S0
C101_S0
C141_S0
0.1UF
22UF
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:56 2022
63 OF 138

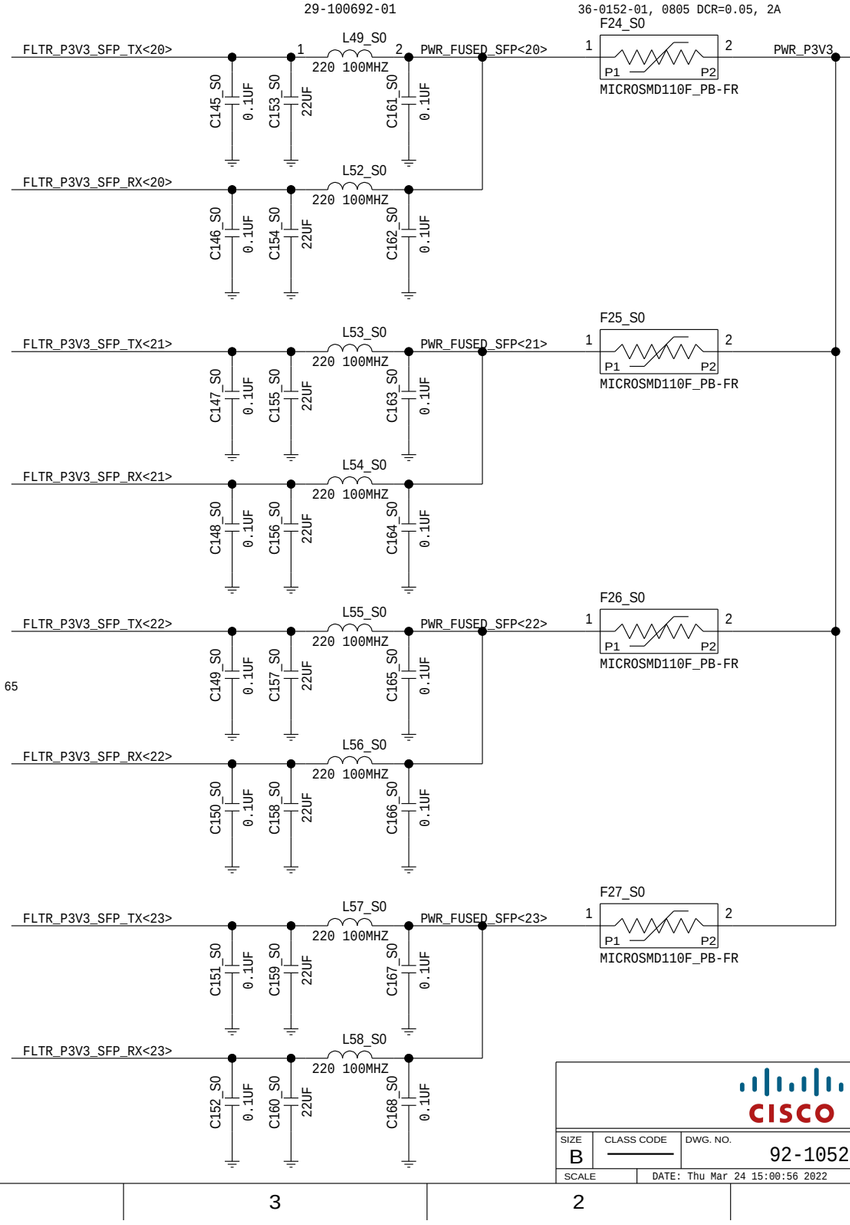

SFP_S0
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<16>
SFP_TX_DISABLE<16>
SFP_SDA<16>
SFP_SCL<16>
SFP_MOD_ABS<16>
SFP_RS0_R<16>
SFP_RX_LOS<16>
SFP_RS1_R<16>
HSD_SFP_MAC_N<16>
HSD_SFP_MAC_P<16>
FLTR_P3V3_SFP_RX<16>
FLTR_P3V3_SFP_TX<16>
HSD_MAC_SFP_P<16>
HSD_MAC_SFP_N<16>
SFP_TX_FAULT<17>
SFP_TX_DISABLE<17>
SFP_SDA<17>
SFP_SCL<17>
SFP_MOD_ABS<17>
SFP_RS0_R<17>
SFP_RX_LOS<17>
SFP_RS1_R<17>
HSD_SFP_MAC_N<17>
HSD_SFP_MAC_P<17>
FLTR_P3V3_SFP_RX<17>
FLTR_P3V3_SFP_TX<17>
HSD_MAC_SFP_P<17>
HSD_MAC_SFP_N<17>
SFP_TX_FAULT<18>
SFP_TX_DISABLE<18>
SFP_SDA<18>
SFP_SCL<18>
SFP_MOD_ABS<18>
SFP_RS0_R<18>
SFP_RX_LOS<18>
SFP_RS1_R<18>
HSD_SFP_MAC_N<18>
HSD_SFP_MAC_P<18>
FLTR_P3V3_SFP_RX<18>
FLTR_P3V3_SFP_TX<18>
HSD_MAC_SFP_P<18>
HSD_MAC_SFP_N<18>
SFP_TX_FAULT<19>
SFP_TX_DISABLE<19>
SFP_SDA<19>
SFP_SCL<19>
SFP_MOD_ABS<19>
SFP_RS0_R<19>
SFP_RX_LOS<19>
SFP_RS1_R<19>
HSD_SFP_MAC_N<19>
HSD_SFP_MAC_P<19>
FLTR_P3V3_SFP_RX<19>
FLTR_P3V3_SFP_TX<19>
HSD_MAC_SFP_P<19>
HSD_MAC_SFP_N<19>
P16_S0
P17_S0
P18_S0
P19_S0
LED_BICO4
25-1289-01
SFP_YEL_LED_L<16>
SFP_GRN_LED_L<16>
SFP_YEL_LED_L<17>
SFP_GRN_LED_L<17>
SFP_YEL_LED_L<18>
SFP_GRN_LED_L<18>
SFP_YEL_LED_L<19>
SFP_GRN_LED_L<19>
SFP_YEL_R_L<16>
SFP_GRN_R_L<16>
SFP_YEL_R_L<17>
SFP_GRN_R_L<17>
SFP_YEL_R_L<18>
SFP_GRN_R_L<18>
SFP_YEL_R_L<19>
SFP_GRN_R_L<19>
PWR_LED_P3V3
PWR_P3V3
RN92_S0_4
RN89_S0_3
RN89_S0_2
RN89_S0_1
RN93_S0_4
RN80_S0_3
RN80_S0_2
RN80_S0_1
RN69_S0_1
RN69_S0_2
RN69_S0_3
RN79_S0_4
RN94_S0_1
RN94_S0_2
RN94_S0_3
RN96_S0_4
RN97_S0_1
RN97_S0_2
RN97_S0_3
RN99_S0_4
RN100_S0_1
RN100_S0_2
RN100_S0_3
RN102_S0_4
RN109_S0_1
RN109_S0_2
RN109_S0_3
RN111_S0_4
RN104_S0_1
RN104_S0_2
RN104_S0_3
RN107_S0_4
RN103_S0_1
RN103_S0_2
RN103_S0_3
RN108_S0_4
36-0152-01, 0805 DCR=0.05, 2A
L51_S0
L66_S0
L67_S0
L68_S0
L69_S0
L70_S0
L71_S0
L72_S0
220 100MHZ
F32_S0
F33_S0
F34_S0
F35_S0
MICROSMD110F_PB-FR
PWR_FUSED_SFP<16>
PWR_FUSED_SFP<17>
PWR_FUSED_SFP<18>
PWR_FUSED_SFP<19>
PWR_P3V3
C193_S0
C194_S0
C195_S0
C196_S0
C197_S0
C198_S0
C199_S0
C200_S0
C201_S0
C202_S0
C203_S0
C204_S0
C205_S0
C206_S0
C207_S0
C208_S0
C209_S0
C210_S0
C211_S0
C212_S0
C213_S0
C214_S0
C215_S0
C216_S0
0.1UF
22UF
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:56 2022
64 OF 138











SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:56 2022		65 OF 138

DWG NO	SHT	REV
92-105229-01	138	A0

REVISION					
REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD

2X12 SFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:

72 71 70 69 68 67 49 IN — SFP_SDA<23..0> — BI
72 71 70 69 68 67 49 IN — SFP_SCL<23..0> — BI

72 71 70 69 68 67 49 IN — SFP_TX_DISABLE<23..0> — OUT

72 71 70 69 68 67 49 IN — SFP_RS0<23..0> — OUT
72 71 70 69 68 67 49 IN — SFP_RS1<23..0> — OUT
72 71 70 69 68 67 49 IN — SFP_YEL_LED_L<23..0> — OUT
72 71 70 69 68 67 49 IN — SFP_GRN_LED_L<23..0> — OUT

72 71 70 69 68 67 49 IN — HSD_MAC_SFP_P<23..0> — OUT
72 71 70 69 68 67 49 IN — HSD_MAC_SFP_N<23..0> — OUT

72 71 70 69 68 67 49 IN — HSD_SFP_MAC_N<23..0> — OUT
72 71 70 69 68 67 49 IN — HSD_SFP_MAC_P<23..0> — OUT

72 71 70 69 68 67 49 IN — SFP_RX_LOS<23..0> — OUT
72 71 70 69 68 67 49 IN — SFP_MOD_ABS<23..0> — OUT
72 71 70 69 68 67 49 IN — SFP_TX_FAULT<23..0> — OUT

72 71 70 69 68 67 IN — PWR_P3V3 — OUT

72 71 70 69 68 67 IN — PWR_LED_P3V3 — OUT

TITLE

QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± DECIM .xx +.01 -. .xxx+.005 ANGLES ±1°

MATERIAL

FINISH

DO NOT SCALE DWG

APPROVALS	DATE
DRAWN BY BCORDEIR	
CAD	
MECH	
ENGR BCORDEIR	
MFG	
TEST	

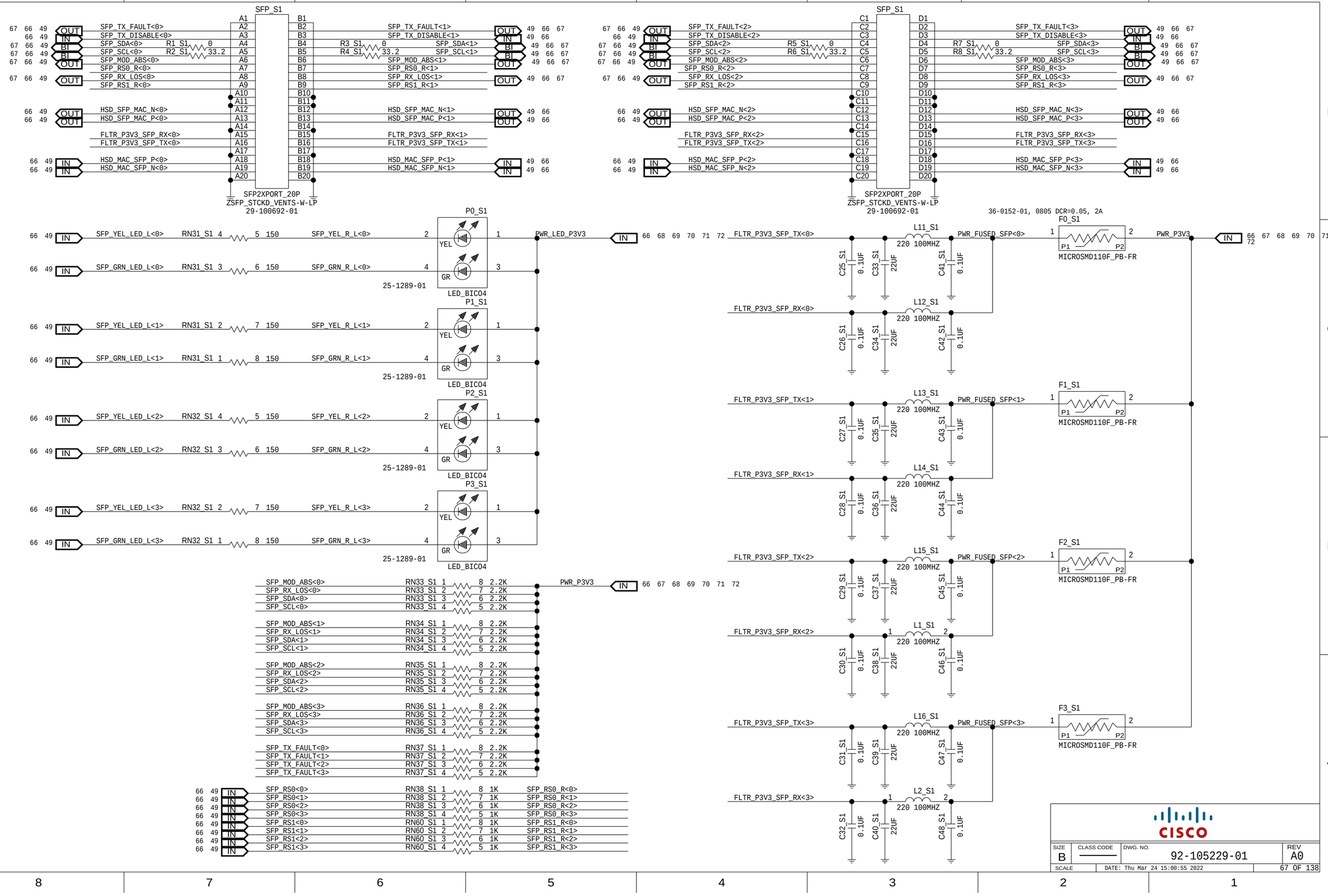
NEXT ASSY	USED ON
APPLICATION	

CISCO

TITLE: SFP 2X12 W/O RETIMER

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-XXXX-01	A0

SCALE | DATE: Fri May 17 11:40:52 2019 | 66 OF 138


SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<0>
SFP_TX_DISABLE<0>
SFP_SDA<0>
SFP_SCL<0>
SFP_MOD_ABS<0>
SFP_RS0_R<0>
SFP_RX_LOS<0>
SFP_RS1_R<0>
HSD_SFP_MAC_N<0>
HSD_SFP_MAC_P<0>
FLTR_P3V3_SFP_RX<0>
FLTR_P3V3_SFP_TX<0>
HSD_MAC_SFP_P<0>
HSD_MAC_SFP_N<0>
R1_S1
R2_S1
33.2
SFP_TX_FAULT<1>
SFP_TX_DISABLE<1>
SFP_SDA<1>
SFP_SCL<1>
SFP_MOD_ABS<1>
SFP_RS0_R<1>
SFP_RX_LOS<1>
SFP_RS1_R<1>
HSD_SFP_MAC_N<1>
HSD_SFP_MAC_P<1>
FLTR_P3V3_SFP_RX<1>
FLTR_P3V3_SFP_TX<1>
HSD_MAC_SFP_P<1>
HSD_MAC_SFP_N<1>
R3_S1
R4_S1
SFP_TX_FAULT<2>
SFP_TX_DISABLE<2>
SFP_SDA<2>
SFP_SCL<2>
SFP_MOD_ABS<2>
SFP_RS0_R<2>
SFP_RX_LOS<2>
SFP_RS1_R<2>
HSD_SFP_MAC_N<2>
HSD_SFP_MAC_P<2>
FLTR_P3V3_SFP_RX<2>
FLTR_P3V3_SFP_TX<2>
HSD_MAC_SFP_P<2>
HSD_MAC_SFP_N<2>
R5_S1
R6_S1
SFP_TX_FAULT<3>
SFP_TX_DISABLE<3>
SFP_SDA<3>
SFP_SCL<3>
SFP_MOD_ABS<3>
SFP_RS0_R<3>
SFP_RX_LOS<3>
SFP_RS1_R<3>
HSD_SFP_MAC_N<3>
HSD_SFP_MAC_P<3>
FLTR_P3V3_SFP_RX<3>
FLTR_P3V3_SFP_TX<3>
HSD_MAC_SFP_P<3>
HSD_MAC_SFP_N<3>
R7_S1
R8_S1
P0_S1
P1_S1
P2_S1
P3_S1
LED_BICO4
25-1289-01
YEL
GR
SFP_YEL_LED_L<0>
SFP_GRN_LED_L<0>
SFP_YEL_LED_L<1>
SFP_GRN_LED_L<1>
SFP_YEL_LED_L<2>
SFP_GRN_LED_L<2>
SFP_YEL_LED_L<3>
SFP_GRN_LED_L<3>
RN31_S1
RN32_S1
SFP_YEL_R_L<0>
SFP_GRN_R_L<0>
SFP_YEL_R_L<1>
SFP_GRN_R_L<1>
SFP_YEL_R_L<2>
SFP_GRN_R_L<2>
SFP_YEL_R_L<3>
SFP_GRN_R_L<3>
150
PWR_LED_P3V3
RN33_S1
RN34_S1
RN35_S1
RN36_S1
RN37_S1
RN38_S1
RN60_S1
2.2K
1K
PWR_P3V3
SFP_RS0_R<0>
SFP_RS0_R<1>
SFP_RS0_R<2>
SFP_RS0_R<3>
SFP_RS1_R<0>
SFP_RS1_R<1>
SFP_RS1_R<2>
SFP_RS1_R<3>
36-0152-01, 0805 DCR=0.05, 2A
L11_S1
L12_S1
L13_S1
L14_S1
L15_S1
L1_S1
L16_S1
L2_S1
220 100MHZ
PWR_FUSED_SFP<0>
PWR_FUSED_SFP<1>
PWR_FUSED_SFP<2>
PWR_FUSED_SFP<3>
F0_S1
F1_S1
F2_S1
F3_S1
MICROSMD110F_PB-FR
P1
P2
C25_S1
C26_S1
C27_S1
C28_S1
C29_S1
C30_S1
C31_S1
C32_S1
C33_S1
C34_S1
C35_S1
C36_S1
C37_S1
C38_S1
C39_S1
C40_S1
C41_S1
C42_S1
C43_S1
C44_S1
C45_S1
C46_S1
C47_S1
C48_S1
0.1UF
22UF
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:55 2022
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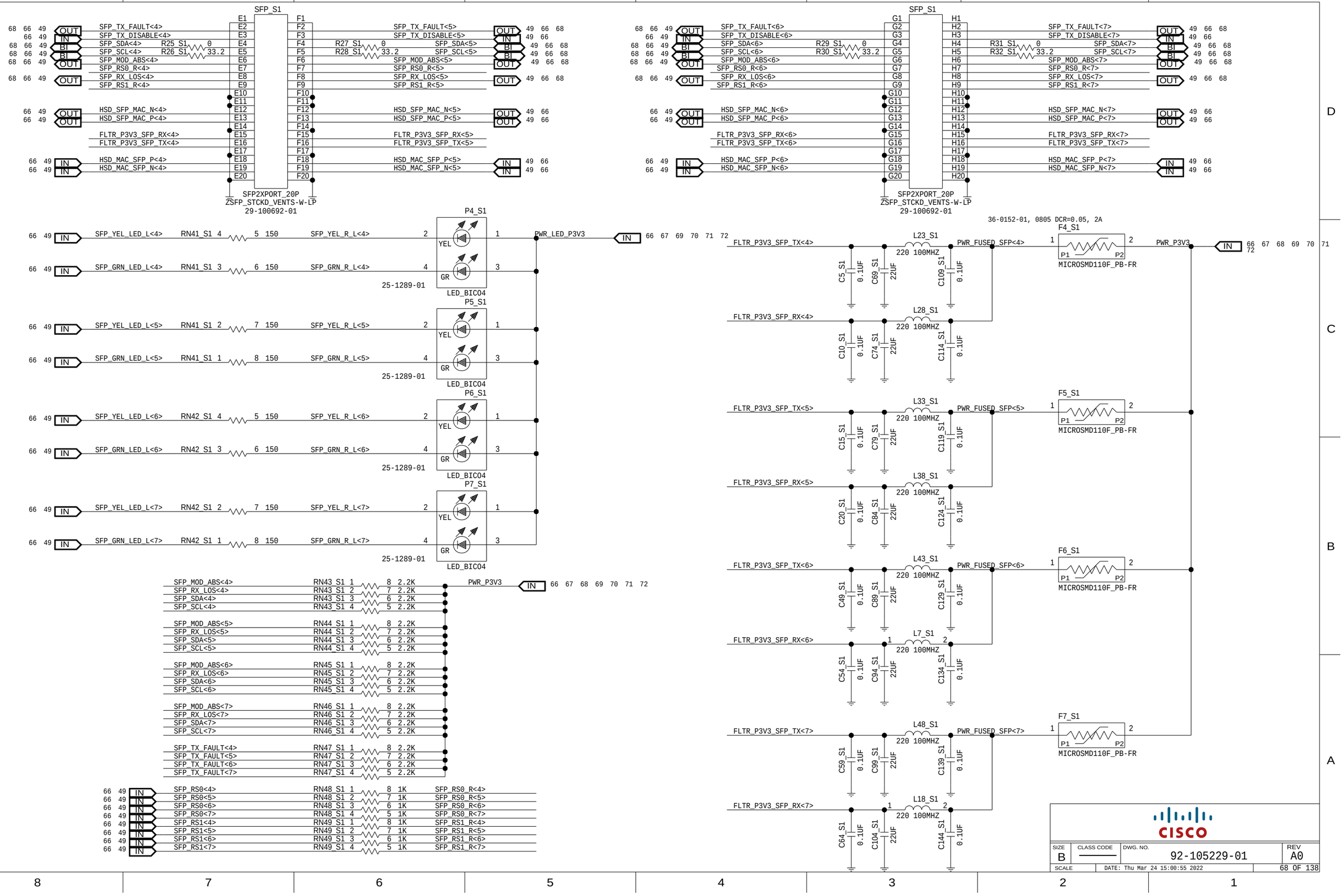
SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<4>
SFP_TX_DISABLE<4>
SFP_SDA<4>
SFP_SCL<4>
SFP_MOD_ABS<4>
SFP_RS0_R<4>
SFP_RX_LOS<4>
SFP_RS1_R<4>
R25 S1 0
R26 S1 33.2
SFP_TX_FAULT<5>
SFP_TX_DISABLE<5>
SFP_SDA<5>
SFP_SCL<5>
SFP_MOD_ABS<5>
SFP_RS0_R<5>
SFP_RX_LOS<5>
SFP_RS1_R<5>
R27 S1 0
R28 S1 33.2
HSD_SFP_MAC_N<4>
HSD_SFP_MAC_P<4>
FLTR_P3V3_SFP_RX<4>
FLTR_P3V3_SFP_TX<4>
HSD_MAC_SFP_P<4>
HSD_MAC_SFP_N<4>
HSD_SFP_MAC_N<5>
HSD_SFP_MAC_P<5>
FLTR_P3V3_SFP_RX<5>
FLTR_P3V3_SFP_TX<5>
HSD_MAC_SFP_P<5>
HSD_MAC_SFP_N<5>
SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<6>
SFP_TX_DISABLE<6>
SFP_SDA<6>
SFP_SCL<6>
SFP_MOD_ABS<6>
SFP_RS0_R<6>
SFP_RX_LOS<6>
SFP_RS1_R<6>
R29 S1 0
R30 S1 33.2
SFP_TX_FAULT<7>
SFP_TX_DISABLE<7>
SFP_SDA<7>
SFP_SCL<7>
SFP_MOD_ABS<7>
SFP_RS0_R<7>
SFP_RX_LOS<7>
SFP_RS1_R<7>
R31 S1 0
R32 S1 33.2
HSD_SFP_MAC_N<6>
HSD_SFP_MAC_P<6>
FLTR_P3V3_SFP_RX<6>
FLTR_P3V3_SFP_TX<6>
HSD_MAC_SFP_P<6>
HSD_MAC_SFP_N<6>
HSD_SFP_MAC_N<7>
HSD_SFP_MAC_P<7>
FLTR_P3V3_SFP_RX<7>
FLTR_P3V3_SFP_TX<7>
HSD_MAC_SFP_P<7>
HSD_MAC_SFP_N<7>
P4_S1
P5_S1
P6_S1
P7_S1
LED_BICO4
25-1289-01
SFP_YEL_LED_L<4>
SFP_GRN_LED_L<4>
SFP_YEL_LED_L<5>
SFP_GRN_LED_L<5>
SFP_YEL_LED_L<6>
SFP_GRN_LED_L<6>
SFP_YEL_LED_L<7>
SFP_GRN_LED_L<7>
RN41_S1 4 5 150
RN41_S1 3 6 150
RN41_S1 2 7 150
RN41_S1 1 8 150
RN42_S1 4 5 150
RN42_S1 3 6 150
RN42_S1 2 7 150
RN42_S1 1 8 150
SFP_YEL_R_L<4>
SFP_GRN_R_L<4>
SFP_YEL_R_L<5>
SFP_GRN_R_L<5>
SFP_YEL_R_L<6>
SFP_GRN_R_L<6>
SFP_YEL_R_L<7>
SFP_GRN_R_L<7>
PWR_LED_P3V3
RN43_S1 1 8 2.2K
RN43_S1 2 7 2.2K
RN43_S1 3 6 2.2K
RN43_S1 4 5 2.2K
RN44_S1 1 8 2.2K
RN44_S1 2 7 2.2K
RN44_S1 3 6 2.2K
RN44_S1 4 5 2.2K
RN45_S1 1 8 2.2K
RN45_S1 2 7 2.2K
RN45_S1 3 6 2.2K
RN45_S1 4 5 2.2K
RN46_S1 1 8 2.2K
RN46_S1 2 7 2.2K
RN46_S1 3 6 2.2K
RN46_S1 4 5 2.2K
RN47_S1 1 8 2.2K
RN47_S1 2 7 2.2K
RN47_S1 3 6 2.2K
RN47_S1 4 5 2.2K
PWR_P3V3
RN48_S1 1 8 1K
RN48_S1 2 7 1K
RN48_S1 3 6 1K
RN48_S1 4 5 1K
RN49_S1 1 8 1K
RN49_S1 2 7 1K
RN49_S1 3 6 1K
RN49_S1 4 5 1K
SFP_RS0_R<4>
SFP_RS0_R<5>
SFP_RS0_R<6>
SFP_RS0_R<7>
SFP_RS1_R<4>
SFP_RS1_R<5>
SFP_RS1_R<6>
SFP_RS1_R<7>
36-0152-01, 0805 DCR=0.05, 2A
F4_S1
F5_S1
F6_S1
F7_S1
MICROSMD110F_PB-FR
L23_S1
L28_S1
L33_S1
L38_S1
L43_S1
L7_S1
L48_S1
L18_S1
220 100MHZ
FLTR_P3V3_SFP_TX<4>
FLTR_P3V3_SFP_RX<4>
FLTR_P3V3_SFP_TX<5>
FLTR_P3V3_SFP_RX<5>
FLTR_P3V3_SFP_TX<6>
FLTR_P3V3_SFP_RX<6>
FLTR_P3V3_SFP_TX<7>
FLTR_P3V3_SFP_RX<7>
PWR_FUSED_SFP<4>
PWR_FUSED_SFP<5>
PWR_FUSED_SFP<6>
PWR_FUSED_SFP<7>
PWR_P3V3
C5_S1 0.1UF
C69_S1 22UF
C109_S1 0.1UF
C10_S1 0.1UF
C74_S1 22UF
C114_S1 0.1UF
C15_S1 0.1UF
C79_S1 22UF
C119_S1 0.1UF
C20_S1 0.1UF
C84_S1 22UF
C124_S1 0.1UF
C49_S1 0.1UF
C89_S1 22UF
C129_S1 0.1UF
C54_S1 0.1UF
C94_S1 22UF
C134_S1 0.1UF
C59_S1 0.1UF
C99_S1 22UF
C139_S1 0.1UF
C64_S1 0.1UF
C104_S1 22UF
C144_S1 0.1UF
CISCO
SIZE B
CLASS CODE
DWG. NO. 92-105229-01
REV A0
SCALE
DATE: Thu Mar 24 15:00:55 2022
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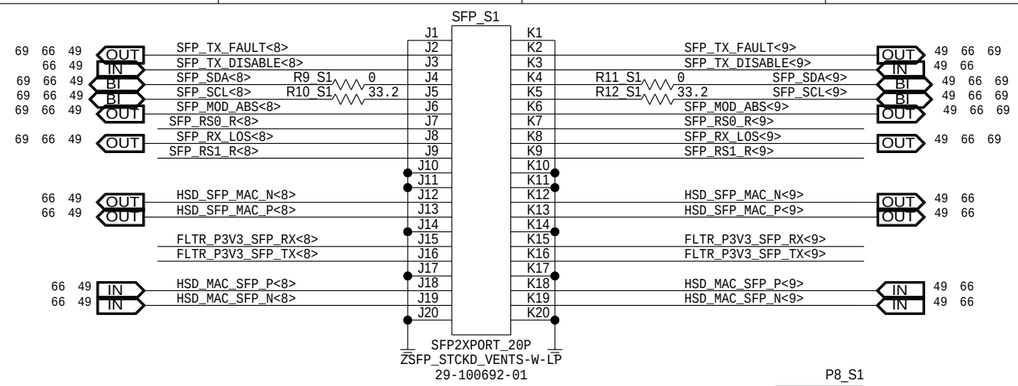
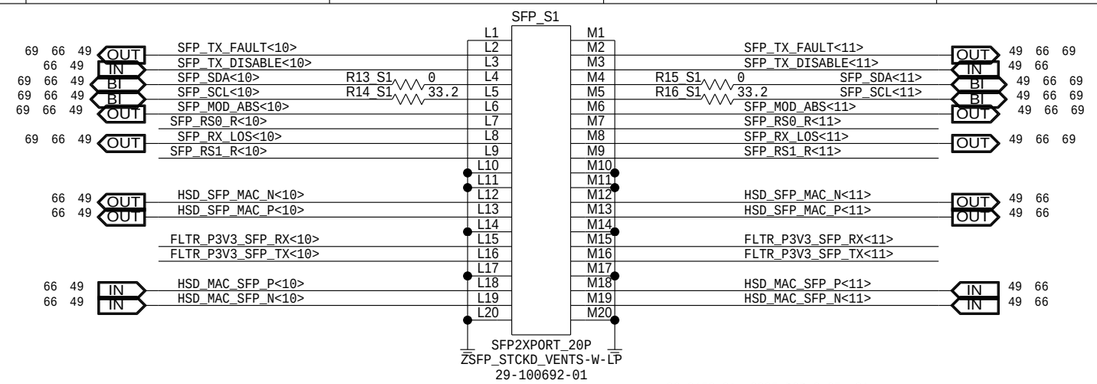
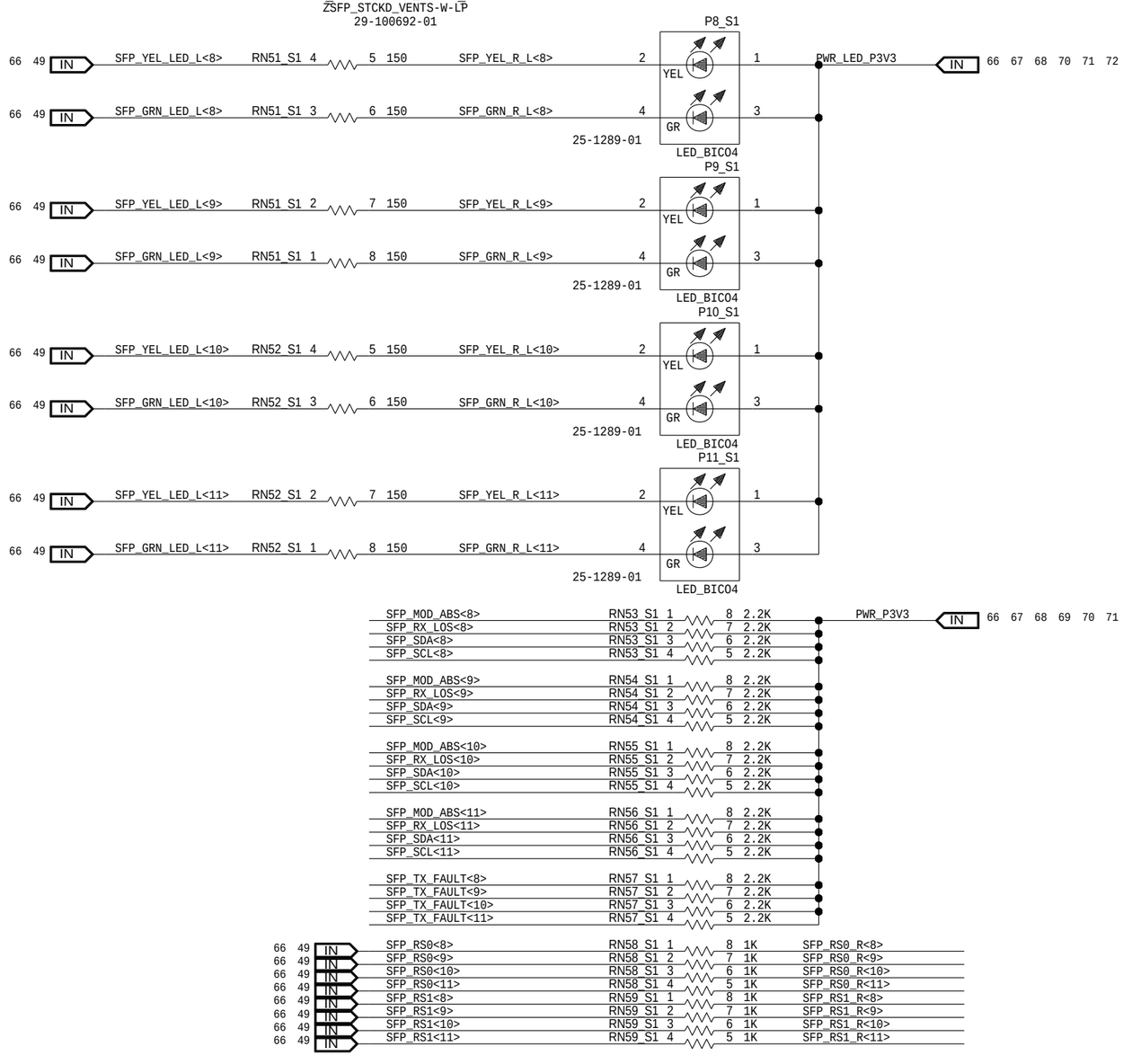
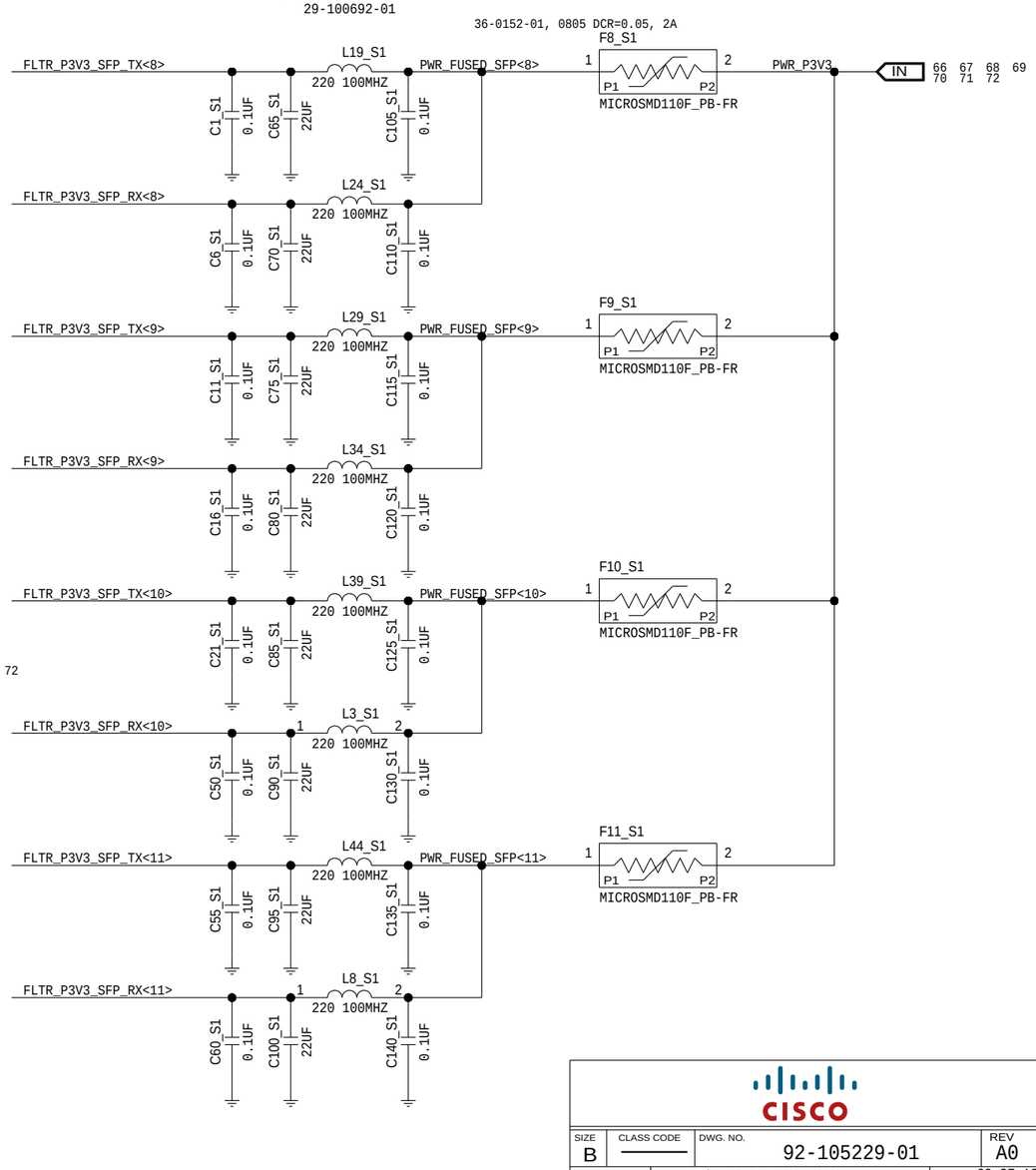
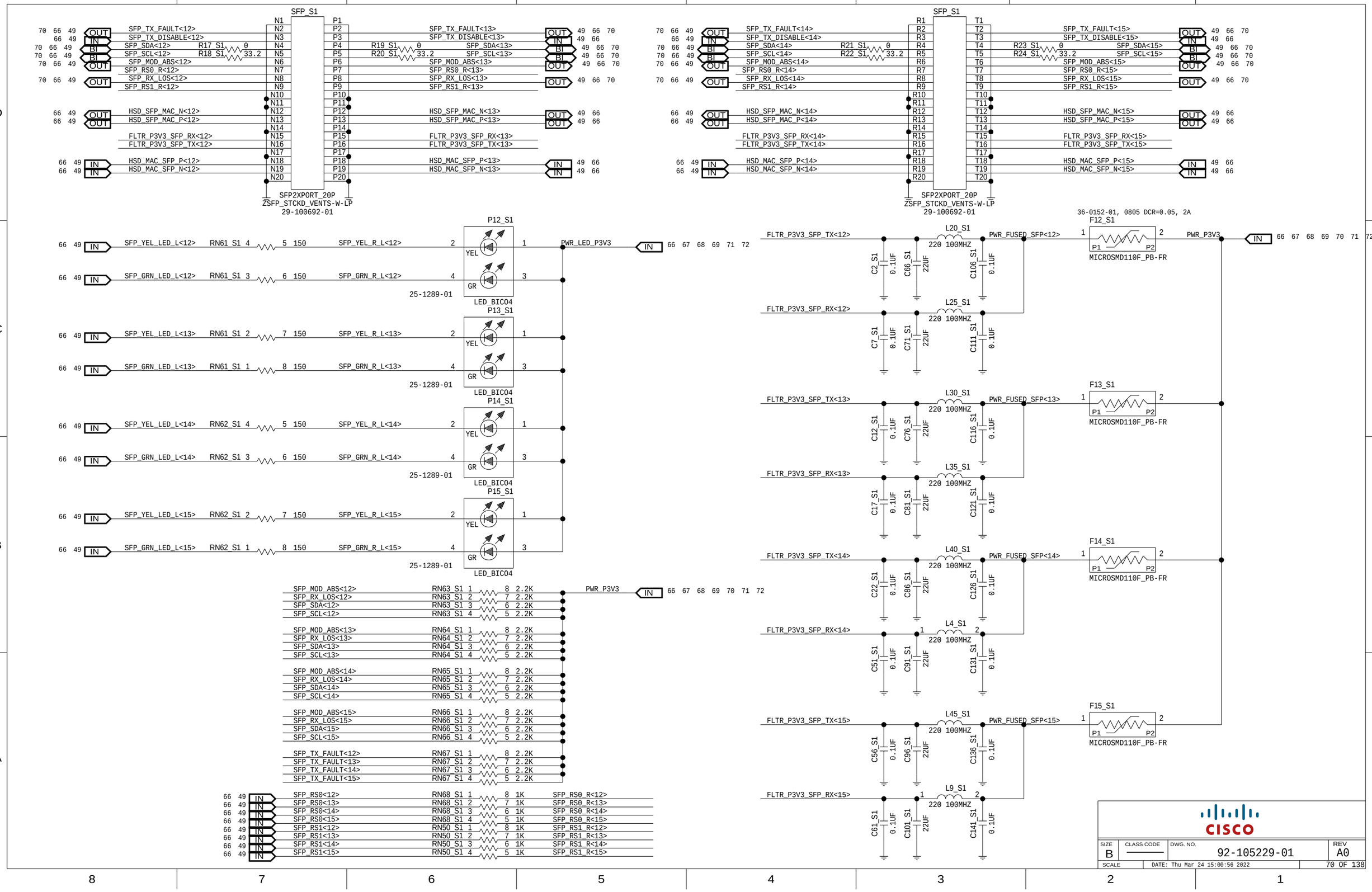








SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:55 2022		69 OF 138


SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<12>
SFP_TX_DISABLE<12>
SFP_SDA<12>
SFP_SCL<12>
SFP_MOD_ABS<12>
SFP_RS0_R<12>
SFP_RX_LOS<12>
SFP_RS1_R<12>
HSD_SFP_MAC_N<12>
HSD_SFP_MAC_P<12>
FLTR_P3V3_SFP_RX<12>
FLTR_P3V3_SFP_TX<12>
HSD_MAC_SFP_P<12>
HSD_MAC_SFP_N<12>
R17_S1
R18_S1
33.2
SFP_TX_FAULT<13>
SFP_TX_DISABLE<13>
SFP_SDA<13>
SFP_SCL<13>
SFP_MOD_ABS<13>
SFP_RS0_R<13>
SFP_RX_LOS<13>
SFP_RS1_R<13>
HSD_SFP_MAC_N<13>
HSD_SFP_MAC_P<13>
FLTR_P3V3_SFP_RX<13>
FLTR_P3V3_SFP_TX<13>
HSD_MAC_SFP_P<13>
HSD_MAC_SFP_N<13>
R19_S1
R20_S1
SFP_TX_FAULT<14>
SFP_TX_DISABLE<14>
SFP_SDA<14>
SFP_SCL<14>
SFP_MOD_ABS<14>
SFP_RS0_R<14>
SFP_RX_LOS<14>
SFP_RS1_R<14>
HSD_SFP_MAC_N<14>
HSD_SFP_MAC_P<14>
FLTR_P3V3_SFP_RX<14>
FLTR_P3V3_SFP_TX<14>
HSD_MAC_SFP_P<14>
HSD_MAC_SFP_N<14>
R21_S1
R22_S1
SFP_TX_FAULT<15>
SFP_TX_DISABLE<15>
SFP_SDA<15>
SFP_SCL<15>
SFP_MOD_ABS<15>
SFP_RS0_R<15>
SFP_RX_LOS<15>
SFP_RS1_R<15>
HSD_SFP_MAC_N<15>
HSD_SFP_MAC_P<15>
FLTR_P3V3_SFP_RX<15>
FLTR_P3V3_SFP_TX<15>
HSD_MAC_SFP_P<15>
HSD_MAC_SFP_N<15>
R23_S1
R24_S1
P12_S1
P13_S1
P14_S1
P15_S1
LED_BICO4
25-1289-01
YEL
GR
SFP_YEL_LED_L<12>
SFP_GRN_LED_L<12>
SFP_YEL_LED_L<13>
SFP_GRN_LED_L<13>
SFP_YEL_LED_L<14>
SFP_GRN_LED_L<14>
SFP_YEL_LED_L<15>
SFP_GRN_LED_L<15>
RN61_S1_4
RN61_S1_3
RN61_S1_2
RN61_S1_1
RN62_S1_4
RN62_S1_3
RN62_S1_2
RN62_S1_1
150
SFP_YEL_R_L<12>
SFP_GRN_R_L<12>
SFP_YEL_R_L<13>
SFP_GRN_R_L<13>
SFP_YEL_R_L<14>
SFP_GRN_R_L<14>
SFP_YEL_R_L<15>
SFP_GRN_R_L<15>
PWR_LED_P3V3
RN63_S1_1
RN63_S1_2
RN63_S1_3
RN63_S1_4
RN64_S1_1
RN64_S1_2
RN64_S1_3
RN64_S1_4
RN65_S1_1
RN65_S1_2
RN65_S1_3
RN65_S1_4
RN66_S1_1
RN66_S1_2
RN66_S1_3
RN66_S1_4
RN67_S1_1
RN67_S1_2
RN67_S1_3
RN67_S1_4
2.2K
SFP_TX_FAULT<12>
SFP_TX_FAULT<13>
SFP_TX_FAULT<14>
SFP_TX_FAULT<15>
RN68_S1_1
RN68_S1_2
RN68_S1_3
RN68_S1_4
RN50_S1_1
RN50_S1_2
RN50_S1_3
RN50_S1_4
1K
SFP_RS0_R<12>
SFP_RS0_R<13>
SFP_RS0_R<14>
SFP_RS0_R<15>
SFP_RS1_R<12>
SFP_RS1_R<13>
SFP_RS1_R<14>
SFP_RS1_R<15>
PWR_P3V3
36-0152-01, 0805 DCR=0.05, 2A
F12_S1
F13_S1
F14_S1
F15_S1
MICROSMD110F_PB-FR
L20_S1
L25_S1
L30_S1
L35_S1
L40_S1
L4_S1
L45_S1
L9_S1
220 100MHZ
PWR_FUSED_SFP<12>
PWR_FUSED_SFP<13>
PWR_FUSED_SFP<14>
PWR_FUSED_SFP<15>
C2_S1
C66_S1
C106_S1
C7_S1
C71_S1
C111_S1
C12_S1
C76_S1
C116_S1
C17_S1
C81_S1
C121_S1
C22_S1
C86_S1
C126_S1
C51_S1
C91_S1
C131_S1
C56_S1
C96_S1
C136_S1
C61_S1
C101_S1
C141_S1
0.1UF
22UF
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
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A0
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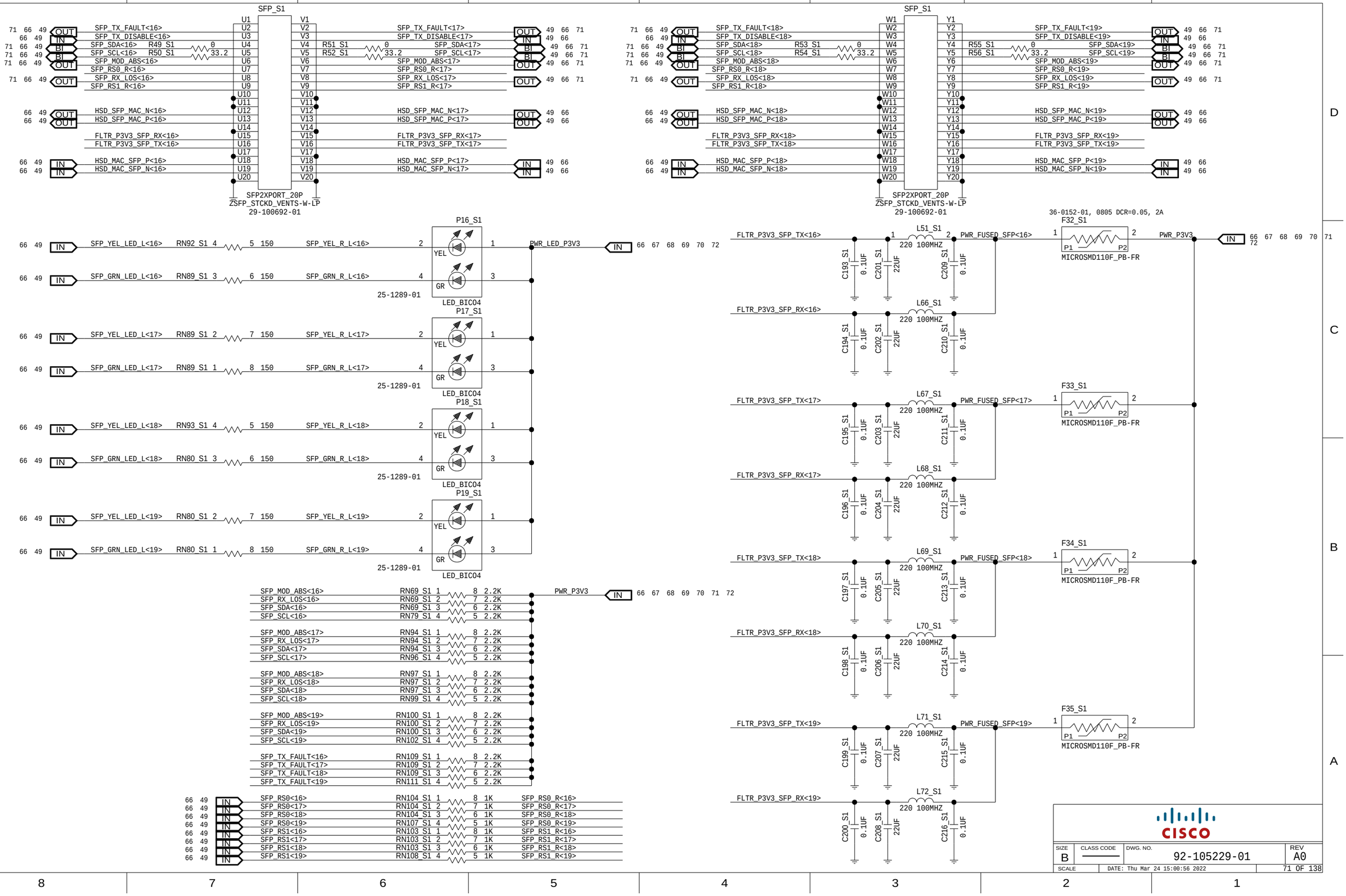
SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<16>
SFP_TX_DISABLE<16>
SFP_SDA<16>
SFP_SCL<16>
SFP_MOD_ABS<16>
SFP_RS0_R<16>
SFP_RX_LOS<16>
SFP_RS1_R<16>
HSD_SFP_MAC_N<16>
HSD_SFP_MAC_P<16>
FLTR_P3V3_SFP_RX<16>
FLTR_P3V3_SFP_TX<16>
HSD_MAC_SFP_P<16>
HSD_MAC_SFP_N<16>
SFP_TX_FAULT<17>
SFP_TX_DISABLE<17>
SFP_SDA<17>
SFP_SCL<17>
SFP_MOD_ABS<17>
SFP_RS0_R<17>
SFP_RX_LOS<17>
SFP_RS1_R<17>
HSD_SFP_MAC_N<17>
HSD_SFP_MAC_P<17>
FLTR_P3V3_SFP_RX<17>
FLTR_P3V3_SFP_TX<17>
HSD_MAC_SFP_P<17>
HSD_MAC_SFP_N<17>
SFP_TX_FAULT<18>
SFP_TX_DISABLE<18>
SFP_SDA<18>
SFP_SCL<18>
SFP_MOD_ABS<18>
SFP_RS0_R<18>
SFP_RX_LOS<18>
SFP_RS1_R<18>
HSD_SFP_MAC_N<18>
HSD_SFP_MAC_P<18>
FLTR_P3V3_SFP_RX<18>
FLTR_P3V3_SFP_TX<18>
HSD_MAC_SFP_P<18>
HSD_MAC_SFP_N<18>
SFP_TX_FAULT<19>
SFP_TX_DISABLE<19>
SFP_SDA<19>
SFP_SCL<19>
SFP_MOD_ABS<19>
SFP_RS0_R<19>
SFP_RX_LOS<19>
SFP_RS1_R<19>
HSD_SFP_MAC_N<19>
HSD_SFP_MAC_P<19>
FLTR_P3V3_SFP_RX<19>
FLTR_P3V3_SFP_TX<19>
HSD_MAC_SFP_P<19>
HSD_MAC_SFP_N<19>
R49_S1
R50_S1
R51_S1
R52_S1
R53_S1
R54_S1
R55_S1
R56_S1
P16_S1
P17_S1
P18_S1
P19_S1
LED_BICO4
25-1289-01
YEL
GR
SFP_YEL_LED_L<16>
SFP_GRN_LED_L<16>
SFP_YEL_LED_L<17>
SFP_GRN_LED_L<17>
SFP_YEL_LED_L<18>
SFP_GRN_LED_L<18>
SFP_YEL_LED_L<19>
SFP_GRN_LED_L<19>
SFP_YEL_R_L<16>
SFP_GRN_R_L<16>
SFP_YEL_R_L<17>
SFP_GRN_R_L<17>
SFP_YEL_R_L<18>
SFP_GRN_R_L<18>
SFP_YEL_R_L<19>
SFP_GRN_R_L<19>
RN92_S1
RN89_S1
RN93_S1
RN80_S1
PWR_LED_P3V3
RN69_S1
RN79_S1
RN94_S1
RN96_S1
RN97_S1
RN99_S1
RN100_S1
RN102_S1
RN109_S1
RN111_S1
SFP_TX_FAULT<16>
SFP_TX_FAULT<17>
SFP_TX_FAULT<18>
SFP_TX_FAULT<19>
RN104_S1
RN107_S1
RN103_S1
RN108_S1
SFP_RS0_R<16>
SFP_RS0_R<17>
SFP_RS0_R<18>
SFP_RS0_R<19>
SFP_RS1_R<16>
SFP_RS1_R<17>
SFP_RS1_R<18>
SFP_RS1_R<19>
36-0152-01, 0805 DCR=0.05, 2A
F32_S1
F33_S1
F34_S1
F35_S1
MICROSMD110F_PB-FR
PWR_FUSED_SFP<16>
PWR_FUSED_SFP<17>
PWR_FUSED_SFP<18>
PWR_FUSED_SFP<19>
PWR_P3V3
L51_S1
L66_S1
L67_S1
L68_S1
L69_S1
L70_S1
L71_S1
L72_S1
220 100MHZ
C193_S1
C194_S1
C195_S1
C196_S1
C197_S1
C198_S1
C199_S1
C200_S1
C201_S1
C202_S1
C203_S1
C204_S1
C205_S1
C206_S1
C207_S1
C208_S1
C209_S1
C210_S1
C211_S1
C212_S1
C213_S1
C214_S1
C215_S1
C216_S1
0.1UF
22UF
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:56 2022
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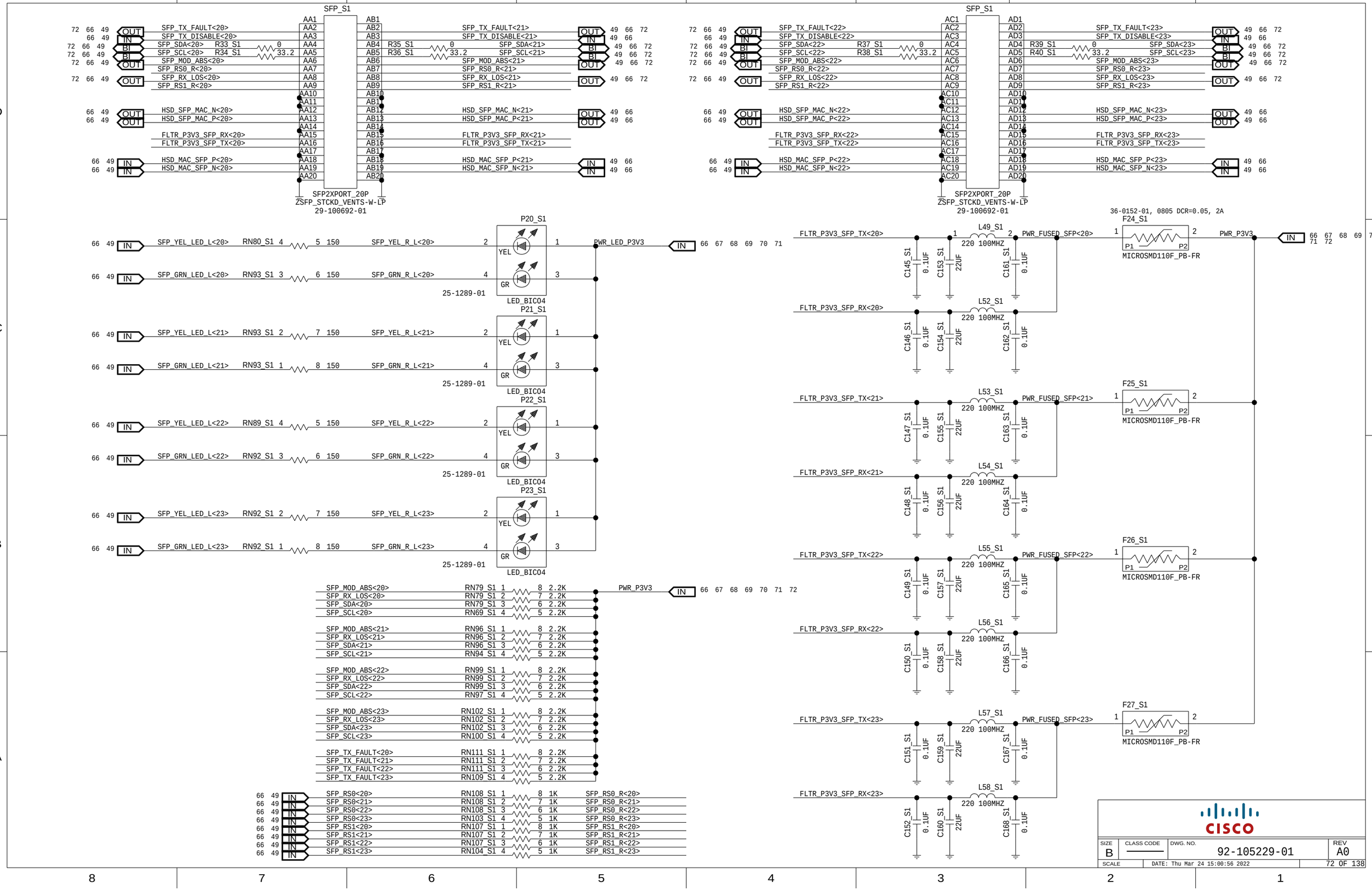
SFP_S1
SFP2XPORT_20P
ZSFP_STCKD_VENTS-W-LP
29-100692-01
SFP_TX_FAULT<20>
SFP_TX_DISABLE<20>
SFP_SDA<20>
SFP_SCL<20>
SFP_MOD_ABS<20>
SFP_RS0_R<20>
SFP_RX_LOS<20>
SFP_RS1_R<20>
HSD_SFP_MAC_N<20>
HSD_SFP_MAC_P<20>
FLTR_P3V3_SFP_RX<20>
FLTR_P3V3_SFP_TX<20>
HSD_MAC_SFP_P<20>
HSD_MAC_SFP_N<20>
SFP_TX_FAULT<21>
SFP_TX_DISABLE<21>
SFP_SDA<21>
SFP_SCL<21>
SFP_MOD_ABS<21>
SFP_RS0_R<21>
SFP_RX_LOS<21>
SFP_RS1_R<21>
HSD_SFP_MAC_N<21>
HSD_SFP_MAC_P<21>
FLTR_P3V3_SFP_RX<21>
FLTR_P3V3_SFP_TX<21>
HSD_MAC_SFP_P<21>
HSD_MAC_SFP_N<21>
SFP_TX_FAULT<22>
SFP_TX_DISABLE<22>
SFP_SDA<22>
SFP_SCL<22>
SFP_MOD_ABS<22>
SFP_RS0_R<22>
SFP_RX_LOS<22>
SFP_RS1_R<22>
HSD_SFP_MAC_N<22>
HSD_SFP_MAC_P<22>
FLTR_P3V3_SFP_RX<22>
FLTR_P3V3_SFP_TX<22>
HSD_MAC_SFP_P<22>
HSD_MAC_SFP_N<22>
SFP_TX_FAULT<23>
SFP_TX_DISABLE<23>
SFP_SDA<23>
SFP_SCL<23>
SFP_MOD_ABS<23>
SFP_RS0_R<23>
SFP_RX_LOS<23>
SFP_RS1_R<23>
HSD_SFP_MAC_N<23>
HSD_SFP_MAC_P<23>
FLTR_P3V3_SFP_RX<23>
FLTR_P3V3_SFP_TX<23>
HSD_MAC_SFP_P<23>
HSD_MAC_SFP_N<23>
P20_S1
P21_S1
P22_S1
P23_S1
LED_BIC04
25-1289-01
YEL
GR
SFP_YEL_LED_L<20>
SFP_GRN_LED_L<20>
SFP_YEL_LED_L<21>
SFP_GRN_LED_L<21>
SFP_YEL_LED_L<22>
SFP_GRN_LED_L<22>
SFP_YEL_LED_L<23>
SFP_GRN_LED_L<23>
RN80_S1
RN93_S1
RN89_S1
RN92_S1
SFP_YEL_R_L<20>
SFP_GRN_R_L<20>
SFP_YEL_R_L<21>
SFP_GRN_R_L<21>
SFP_YEL_R_L<22>
SFP_GRN_R_L<22>
SFP_YEL_R_L<23>
SFP_GRN_R_L<23>
PWR_LED_P3V3
RN79_S1
RN69_S1
RN96_S1
RN94_S1
RN99_S1
RN97_S1
RN102_S1
RN100_S1
RN111_S1
RN109_S1
PWR_P3V3
RN108_S1
RN103_S1
RN107_S1
RN104_S1
SFP_RS0_R<20>
SFP_RS0_R<21>
SFP_RS0_R<22>
SFP_RS0_R<23>
SFP_RS1_R<20>
SFP_RS1_R<21>
SFP_RS1_R<22>
SFP_RS1_R<23>
36-0152-01, 0805 DCR=0.05, 2A
F24_S1
F25_S1
F26_S1
F27_S1
MICROSMD110F_PB-FR
L49_S1
L52_S1
L53_S1
L54_S1
L55_S1
L56_S1
L57_S1
L58_S1
220 100MHZ
C145_S1
C146_S1
C147_S1
C148_S1
C149_S1
C150_S1
C151_S1
C152_S1
C153_S1
C154_S1
C155_S1
C156_S1
C157_S1
C158_S1
C159_S1
C160_S1
C161_S1
C162_S1
C163_S1
C164_S1
C165_S1
C166_S1
C167_S1
C168_S1
0.1UF
22UF
FLTR_P3V3_SFP_TX<20>
FLTR_P3V3_SFP_RX<20>
FLTR_P3V3_SFP_TX<21>
FLTR_P3V3_SFP_RX<21>
FLTR_P3V3_SFP_TX<22>
FLTR_P3V3_SFP_RX<22>
FLTR_P3V3_SFP_TX<23>
FLTR_P3V3_SFP_RX<23>
PWR_FUSED_SFP<20>
PWR_FUSED_SFP<21>
PWR_FUSED_SFP<22>
PWR_FUSED_SFP<23>
PWR_P3V3
CISCO
SIZE
B
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BEARVALLY SUBDESIGN REV05

2X BEARVALLY MODULE

CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY
11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP
05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)
REQUIRE CAD LAYOUT CHANGE

TITLE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
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ADDCOMP=700-26993-01

U1_RT1_2

SERDES HOST SIDE

25	IN	BV0P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV0P0_HOST_OUT_P<3>	OUT	25
25	IN	BV0P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV0P0_HOST_OUT_N<3>	OUT	25
25	IN	BV0P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV0P0_HOST_OUT_P<2>	OUT	25
25	IN	BV0P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV0P0_HOST_OUT_N<2>	OUT	25
25	IN	BV0P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV0P0_HOST_OUT_P<1>	OUT	25
25	IN	BV0P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV0P0_HOST_OUT_N<1>	OUT	25
25	IN	BV0P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV0P0_HOST_OUT_P<0>	OUT	25
25	IN	BV0P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV0P0_HOST_OUT_N<0>	OUT	25
25	IN	BV0P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV0P1_HOST_OUT_P<3>	OUT	25
25	IN	BV0P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV0P1_HOST_OUT_N<3>	OUT	25
25	IN	BV0P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV0P1_HOST_OUT_P<2>	OUT	25
25	IN	BV0P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV0P1_HOST_OUT_N<2>	OUT	25
25	IN	BV0P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV0P1_HOST_OUT_P<1>	OUT	25
25	IN	BV0P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV0P1_HOST_OUT_N<1>	OUT	25
25	IN	BV0P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV0P1_HOST_OUT_P<0>	OUT	25
25	IN	BV0P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV0P1_HOST_OUT_N<0>	OUT	25

SERDES LINE SIDE

25	IN	BV0P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV0P0_LINE_OUT_P<3>	OUT	25
25	IN	BV0P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV0P0_LINE_OUT_N<3>	OUT	25
25	IN	BV0P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV0P0_LINE_OUT_P<2>	OUT	25
25	IN	BV0P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV0P0_LINE_OUT_N<2>	OUT	25
25	IN	BV0P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV0P0_LINE_OUT_P<1>	OUT	25
25	IN	BV0P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV0P0_LINE_OUT_N<1>	OUT	25
25	IN	BV0P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV0P0_LINE_OUT_P<0>	OUT	25
25	IN	BV0P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV0P0_LINE_OUT_N<0>	OUT	25
25	IN	BV0P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV0P1_LINE_OUT_P<3>	OUT	25
25	IN	BV0P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV0P1_LINE_OUT_N<3>	OUT	25
25	IN	BV0P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV0P1_LINE_OUT_P<2>	OUT	25
25	IN	BV0P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV0P1_LINE_OUT_N<2>	OUT	25
25	IN	BV0P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV0P1_LINE_OUT_P<1>	OUT	25
25	IN	BV0P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV0P1_LINE_OUT_N<1>	OUT	25
25	IN	BV0P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV0P1_LINE_OUT_P<0>	OUT	25
25	IN	BV0P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV0P1_LINE_OUT_N<0>	OUT	25

PACK_IGNORE=TRUE

CLK/CONFIG/SMI/I2C

25	IN	BV0_CLK_IN_P	C11_RT1_2 0.01UF	BV0_CLK_IN_AC_P	T8	CLK+			
25	IN	BV0_CLK_IN_N	C12_RT1_2 0.01UF	BV0_CLK_IN_AC_N	T9	CLK-			
					A8	CLK2+			
					A9	CLK2-			
77 76 75 74	IN	VDDO_P2V5	R1_RT1_2 100	CONFIG_IO0_PULLUP	B7	CONFIG_IO	SCL	N10	BV0_SCL	IO	25
			R9_RT1_2 100	EEPROM_LOAD0_EN	D10	EEPROM_LOAD_EN	SDA	P10	BV0_SDA	IO	25
25	IN	BV0_ADDR<4>		(IPD)	N9	PHYAD4			
25	IN	BV0_ADDR<3>		(IPD)	P8	PHYAD3			
25	IN	BV0_ADDR<2>		(IPD)	P7	PHYAD2			
25	IN	BV0_ADDR<1>		(IPD)	R7	PHYAD1			
25	IN	BV0_RESET_L			P9	RESET	INT	T10	BV0_INT_L	OUT	25
			R3_RT1_2 1K	(IPD)	R10	SEL_2X			
25	IN	BV0_SDC_MDC			C9	MDC			
25	IO	BV0_SDC_MDIO			C10	MDIO	TP	F7	BV0_TP	TP1_RT1_2
										VIA

JTAG

25	IN	BV_TDI	B9	TDI	TDO	B8	BV0_TDO
76 25	IN	BV_TMS	B10	TMS			
25	IN	BV0_TCK	D7	TCK			
76 25	IN	BV_TRST_L	D8	TRST			

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BEARVALLEY
15-104658-01

R11_RT1_2 100 VDDO_P2V5 IN 74 75 76 77
BOM=NONE

R12_RT1_2 100 VDDO_P2V5 IN 74 75 76 77
BOM=NONE

(TO BV1)

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CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		74 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L3_RT1_2
56 100MHZ
10A, 0.004OHM, 1612

75 77 IN AVDD_P1V0

2.05A (TYP DFE ON)

FLTR_BV0_AVDDH

C60_RT1_2 150UF 4V
C147_RT1_2 22UF 6.3V
C61_RT1_2 22UF 6.3V
C41_RT1_2 22UF 6.3V
C47_RT1_2 0.1UF
C19_RT1_2 0.1UF
C38_RT1_2 0.1UF
C44_RT1_2 0.1UF
C50_RT1_2 0.1UF
C23_RT1_2 0.1UF
C62_RT1_2 0.1UF
C63_RT1_2 0.1UF
C64_RT1_2 0.1UF
C65_RT1_2 0.1UF
C134_RT1_2 0.1UF
C136_RT1_2 0.1UF
C138_RT1_2 0.1UF
0.1UF

ADDCOMP=700-26993-01
U1_RT1_2
POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5
IN 74 76 77
C29_RT1_2 0.1UF
C35_RT1_2 0.1UF
C90_RT1_2 22UF 6.3V

DVDD_P1V0
IN 77
C34_RT1_2 0.1UF
C37_RT1_2 0.1UF
C40_RT1_2 0.1UF
C43_RT1_2 0.1UF
C46_RT1_2 0.1UF
C49_RT1_2 0.1UF
C52_RT1_2 0.1UF
C66_RT1_2 0.1UF
C68_RT1_2 0.1UF
C70_RT1_2 0.1UF
C72_RT1_2 22UF 6.3V
C150_RT1_2 22UF 6.3V
C36_RT1_2 0.1UF
C39_RT1_2 0.1UF
C42_RT1_2 0.1UF
C45_RT1_2 0.1UF
C48_RT1_2 0.1UF
C51_RT1_2 0.1UF
C59_RT1_2 0.1UF
C67_RT1_2 0.1UF
C69_RT1_2 0.1UF
C71_RT1_2 22UF 6.3V
C149_RT1_2 22UF 6.3V
22UF 6.3V

36-0212-01
L5_RT1_2
56 100MHZ
10A, 0.004OHM, 1612

77 75 IN AVDD_P1V0

2.05A (TYP DFE ON)

FLTR_BV0_AVDDL

C25_RT1_2 150UF 4V
C27_RT1_2 22UF 6.3V
C16_RT1_2 22UF 6.3V
C22_RT1_2 22UF 6.3V
C8_RT1_2 0.1UF
C15_RT1_2 0.1UF
C21_RT1_2 0.1UF
C24_RT1_2 0.1UF
C13_RT1_2 0.1UF
C28_RT1_2 0.1UF
C30_RT1_2 0.1UF
C31_RT1_2 0.1UF
C33_RT1_2 0.1UF
C133_RT1_2 0.1UF
C135_RT1_2 0.1UF
C137_RT1_2 0.1UF
0.1UF

C148_RT1_2 22UF 6.3V

ADDCOMP=700-26993-01
U1_RT1_2
GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-2

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		75 OF 138

ADDCOMP=700-26993-01

U2_RT1_2

SERDES HOST SIDE

25 IN	BV1P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV1P0_HOST_OUT_P<3>	OUT 25
25 IN	BV1P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV1P0_HOST_OUT_N<3>	OUT 25
25 IN	BV1P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV1P0_HOST_OUT_P<2>	OUT 25
25 IN	BV1P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV1P0_HOST_OUT_N<2>	OUT 25
25 IN	BV1P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV1P0_HOST_OUT_P<1>	OUT 25
25 IN	BV1P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV1P0_HOST_OUT_N<1>	OUT 25
25 IN	BV1P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV1P0_HOST_OUT_P<0>	OUT 25
25 IN	BV1P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV1P0_HOST_OUT_N<0>	OUT 25
25 IN	BV1P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV1P1_HOST_OUT_P<3>	OUT 25
25 IN	BV1P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV1P1_HOST_OUT_N<3>	OUT 25
25 IN	BV1P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV1P1_HOST_OUT_P<2>	OUT 25
25 IN	BV1P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV1P1_HOST_OUT_N<2>	OUT 25
25 IN	BV1P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV1P1_HOST_OUT_P<1>	OUT 25
25 IN	BV1P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV1P1_HOST_OUT_N<1>	OUT 25
25 IN	BV1P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV1P1_HOST_OUT_P<0>	OUT 25
25 IN	BV1P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV1P1_HOST_OUT_N<0>	OUT 25

SERDES LINE SIDE

25 IN	BV1P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV1P0_LINE_OUT_P<3>	OUT 25
25 IN	BV1P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV1P0_LINE_OUT_N<3>	OUT 25
25 IN	BV1P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV1P0_LINE_OUT_P<2>	OUT 25
25 IN	BV1P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV1P0_LINE_OUT_N<2>	OUT 25
25 IN	BV1P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV1P0_LINE_OUT_P<1>	OUT 25
25 IN	BV1P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV1P0_LINE_OUT_N<1>	OUT 25
25 IN	BV1P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV1P0_LINE_OUT_P<0>	OUT 25
25 IN	BV1P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV1P0_LINE_OUT_N<0>	OUT 25
25 IN	BV1P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV1P1_LINE_OUT_P<3>	OUT 25
25 IN	BV1P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV1P1_LINE_OUT_N<3>	OUT 25
25 IN	BV1P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV1P1_LINE_OUT_P<2>	OUT 25
25 IN	BV1P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV1P1_LINE_OUT_N<2>	OUT 25
25 IN	BV1P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV1P1_LINE_OUT_P<1>	OUT 25
25 IN	BV1P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV1P1_LINE_OUT_N<1>	OUT 25
25 IN	BV1P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV1P1_LINE_OUT_P<0>	OUT 25
25 IN	BV1P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV1P1_LINE_OUT_N<0>	OUT 25

CLK/CONFIG/SMI/I2C

25 IN	BV1_CLK_IN_P	C19_RT1_2 0.01UF	BV1_CLK_IN_AC_P	T8	CLK+		
25 IN	BV1_CLK_IN_N	C20_RT1_2 0.01UF	BV1_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
77 76 75 74 IN	VDDO_P2V5	R2_RT1_2 100	CONFIG_IO1_PULLUP	B7	CONFIG_IO		
		R14_RT1_2 100	EEPROM_LOAD1_EN	D10	EEPROM_LOAD_EN		
25 IN	BV1_ADDR<4>		(IPD)	N9	PHYAD4		
25 IN	BV1_ADDR<3>		(IPD)	P8	PHYAD3		
25 IN	BV1_ADDR<2>		(IPD)	P7	PHYAD2		
25 IN	BV1_ADDR<1>		(IPD)	R7	PHYAD1		
25 IN	BV1_RESET_L			P9	RESET		
	R16_RT1_2	1K		(IPD) R10	SEL_2X		
25 IN	BV1_SDC_MDC			C9	MDC		
25 IO	BV1_SDC_MDIO			C10	MDIO		
	BV0_TDO			B9	TDI		
74 25 IN	BV_TMS			B10	TMS		
25 IN	BV1_TCK			D7	TCK		
74 25 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
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				SCL	N10	BV1_SCL	IO 25
				SDA	P10	BV1_SDA	IO 25
				INT	T10	BV1_INT_L	OUT 25
				TP	F7	BV1_TP VIA TP2_RT1_2	
				TDO	B8	BV_TDO	OUT 25

R17_RT1_2 100 VDDO_P2V5 IN 74 75 76 77
BOM=NONE
PACK_IGNORE=TRUE

R18_RT1_2 100 VDDO_P2V5 IN 74 75 76 77
BOM=NONE
PACK_IGNORE=TRUE

BEARVALLEY-3

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		76 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L6_RT1_2
AVDD_P1V0
56 100MHZ
10A, 0.0040HM, 1612
2.05A (TYP DFE ON)
FLTR_BV1_AVDDH

36-0212-01
L7_RT1_2
AVDD_P1V0
56 100MHZ
10A, 0.0040HM, 1612
2.05A (TYP DFE ON)
FLTR_BV1_AVDDL

ADDCOMP=700-26993-01
U2_RT1_2
POWER & TEST
BEARVALLEY
15-104658-01

VDDO_P2V5
DVDD_P1V0

ADDCOMP=700-26993-01
U2_RT1_2
GROUND
BEARVALLEY
15-104658-01

BEARVALLEY-4

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		77 OF 138

BEARVALLY SUBDESIGN REV05

2X BEARVALLY MODULE

CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY
11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP
05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)
REQUIRE CAD LAYOUT CHANGE

TITLE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Mon Dec 21 20:28:30 2020		78 OF 138

ADDCOMP=700-26993-01

U1_RT3_4

SERDES HOST SIDE

26 IN	BV0P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV0P0_HOST_OUT_P<3>	OUT 26
26 IN	BV0P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV0P0_HOST_OUT_N<3>	OUT 26
26 IN	BV0P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV0P0_HOST_OUT_P<2>	OUT 26
26 IN	BV0P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV0P0_HOST_OUT_N<2>	OUT 26
26 IN	BV0P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV0P0_HOST_OUT_P<1>	OUT 26
26 IN	BV0P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV0P0_HOST_OUT_N<1>	OUT 26
26 IN	BV0P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV0P0_HOST_OUT_P<0>	OUT 26
26 IN	BV0P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV0P0_HOST_OUT_N<0>	OUT 26
26 IN	BV0P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV0P1_HOST_OUT_P<3>	OUT 26
26 IN	BV0P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV0P1_HOST_OUT_N<3>	OUT 26
26 IN	BV0P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV0P1_HOST_OUT_P<2>	OUT 26
26 IN	BV0P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV0P1_HOST_OUT_N<2>	OUT 26
26 IN	BV0P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV0P1_HOST_OUT_P<1>	OUT 26
26 IN	BV0P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV0P1_HOST_OUT_N<1>	OUT 26
26 IN	BV0P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV0P1_HOST_OUT_P<0>	OUT 26
26 IN	BV0P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV0P1_HOST_OUT_N<0>	OUT 26

SERDES LINE SIDE

26 IN	BV0P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV0P0_LINE_OUT_P<3>	OUT 26
26 IN	BV0P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV0P0_LINE_OUT_N<3>	OUT 26
26 IN	BV0P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV0P0_LINE_OUT_P<2>	OUT 26
26 IN	BV0P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV0P0_LINE_OUT_N<2>	OUT 26
26 IN	BV0P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV0P0_LINE_OUT_P<1>	OUT 26
26 IN	BV0P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV0P0_LINE_OUT_N<1>	OUT 26
26 IN	BV0P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV0P0_LINE_OUT_P<0>	OUT 26
26 IN	BV0P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV0P0_LINE_OUT_N<0>	OUT 26
26 IN	BV0P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV0P1_LINE_OUT_P<3>	OUT 26
26 IN	BV0P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV0P1_LINE_OUT_N<3>	OUT 26
26 IN	BV0P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV0P1_LINE_OUT_P<2>	OUT 26
26 IN	BV0P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV0P1_LINE_OUT_N<2>	OUT 26
26 IN	BV0P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV0P1_LINE_OUT_P<1>	OUT 26
26 IN	BV0P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV0P1_LINE_OUT_N<1>	OUT 26
26 IN	BV0P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV0P1_LINE_OUT_P<0>	OUT 26
26 IN	BV0P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV0P1_LINE_OUT_N<0>	OUT 26

PACK_IGNORE=TRUE

CLK/CONFIG/SMI/I2C

26 IN	BV0_CLK_IN_P	C11_RT3_4 0.01UF	BV0_CLK_IN_AC_P	T8	CLK+		
26 IN	BV0_CLK_IN_N	C12_RT3_4 0.01UF	BV0_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
82 81 80 79 IN	VDDO_P2V5	R2_RT3_4 100	CONFIG_IO0_PULLUP	B7	CONFIG_IO	SCL N10	R11_RT3_4 100 VDDO_P2V5 IN 79 80 81 82 BOM=NONE
		R9_RT3_4 100	EEPROM_LOAD0_EN	D10	EEPROM_LOAD_EN	SDA P10	BV0_SCL IO 26
26 IN	BV0_ADDR<4>		(IPD)	N9	PHYAD4		BV0_SDA IO 26
26 IN	BV0_ADDR<3>		(IPD)	P8	PHYAD3		PACK_IGNORE=TRUE
26 IN	BV0_ADDR<2>		(IPD)	P7	PHYAD2		R12_RT3_4 100 VDDO_P2V5 IN 79 80 81 82 BOM=NONE
26 IN	BV0_ADDR<1>		(IPD)	R7	PHYAD1		
26 IN	BV0_RESET_L			P9	RESET	INT T10	BV0_INT_L OUT 26
	R3_RT3_4	1K	(IPD)	R10	SEL_2X		
26 IN	BV0_SDC_MDC			C9	MDC		
26 IO	BV0_SDC_MDIO			C10	MDIO	TP F7	BV0_TP VIA TP1_RT3_4

JTAG

26 IN	BV_TDI			B9	TDI	TDO B8	BV0_TDO
81 26 IN	BV_TMS			B10	TMS		(TO BV1)
26 IN	BV0_TCK			D7	TCK		
81 26 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

BEARVALLEY-1

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		79 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L3_RT3_4
80 82 IN AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV0_AVDDH

C60_RT3_4 150UF 4V
C147_RT3_4 22UF 6.3V
C61_RT3_4 22UF 6.3V
C41_RT3_4 22UF 6.3V
C47_RT3_4 0.1UF
C19_RT3_4 0.1UF
C38_RT3_4 0.1UF
C44_RT3_4 0.1UF
C50_RT3_4 0.1UF
C23_RT3_4 0.1UF
C62_RT3_4 0.1UF
C63_RT3_4 0.1UF
C64_RT3_4 0.1UF
C65_RT3_4 0.1UF
C134_RT3_4 0.1UF
C136_RT3_4 0.1UF
C138_RT3_4 0.1UF
0.1UF

ADDCOMP=700-26993-01
U1_RT3_4
POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5
IN 79 81 82
C29_RT3_4 0.1UF
C35_RT3_4 0.1UF
C90_RT3_4 22UF 6.3V

DVDD_P1V0
IN 82
C34_RT3_4 0.1UF
C37_RT3_4 0.1UF
C40_RT3_4 0.1UF
C43_RT3_4 0.1UF
C46_RT3_4 0.1UF
C49_RT3_4 0.1UF
C52_RT3_4 0.1UF
C66_RT3_4 0.1UF
C68_RT3_4 0.1UF
C70_RT3_4 0.1UF
C72_RT3_4 22UF 6.3V
C150_RT3_4 22UF 6.3V
C36_RT3_4 0.1UF
C39_RT3_4 0.1UF
C42_RT3_4 0.1UF
C45_RT3_4 0.1UF
C48_RT3_4 0.1UF
C51_RT3_4 0.1UF
C59_RT3_4 0.1UF
C67_RT3_4 0.1UF
C69_RT3_4 0.1UF
C71_RT3_4 22UF 6.3V
C149_RT3_4 22UF 6.3V
22UF 6.3V

36-0212-01
L5_RT3_4
82 80 IN AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV0_AVDDL

C25_RT3_4 150UF 4V
C27_RT3_4 22UF 6.3V
C16_RT3_4 22UF 6.3V
C22_RT3_4 22UF 6.3V
C8_RT3_4 0.1UF
C15_RT3_4 0.1UF
C21_RT3_4 0.1UF
C24_RT3_4 0.1UF
C13_RT3_4 0.1UF
C28_RT3_4 0.1UF
C30_RT3_4 0.1UF
C31_RT3_4 0.1UF
C33_RT3_4 0.1UF
C133_RT3_4 0.1UF
C135_RT3_4 0.1UF
C137_RT3_4 0.1UF
0.1UF
C148_RT3_4 22UF 6.3V

ADDCOMP=700-26993-01
U1_RT3_4
GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-2

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		80 OF 138

ADDCOMP=700-26993-01

U2_RT3_4

SERDES HOST SIDE

26 IN	BV1P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV1P0_HOST_OUT_P<3>	OUT 26
26 IN	BV1P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV1P0_HOST_OUT_N<3>	OUT 26
26 IN	BV1P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV1P0_HOST_OUT_P<2>	OUT 26
26 IN	BV1P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV1P0_HOST_OUT_N<2>	OUT 26
26 IN	BV1P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV1P0_HOST_OUT_P<1>	OUT 26
26 IN	BV1P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV1P0_HOST_OUT_N<1>	OUT 26
26 IN	BV1P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV1P0_HOST_OUT_P<0>	OUT 26
26 IN	BV1P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV1P0_HOST_OUT_N<0>	OUT 26
26 IN	BV1P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV1P1_HOST_OUT_P<3>	OUT 26
26 IN	BV1P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV1P1_HOST_OUT_N<3>	OUT 26
26 IN	BV1P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV1P1_HOST_OUT_P<2>	OUT 26
26 IN	BV1P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV1P1_HOST_OUT_N<2>	OUT 26
26 IN	BV1P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV1P1_HOST_OUT_P<1>	OUT 26
26 IN	BV1P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV1P1_HOST_OUT_N<1>	OUT 26
26 IN	BV1P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV1P1_HOST_OUT_P<0>	OUT 26
26 IN	BV1P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV1P1_HOST_OUT_N<0>	OUT 26

SERDES LINE SIDE

26 IN	BV1P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV1P0_LINE_OUT_P<3>	OUT 26
26 IN	BV1P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV1P0_LINE_OUT_N<3>	OUT 26
26 IN	BV1P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV1P0_LINE_OUT_P<2>	OUT 26
26 IN	BV1P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV1P0_LINE_OUT_N<2>	OUT 26
26 IN	BV1P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV1P0_LINE_OUT_P<1>	OUT 26
26 IN	BV1P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV1P0_LINE_OUT_N<1>	OUT 26
26 IN	BV1P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV1P0_LINE_OUT_P<0>	OUT 26
26 IN	BV1P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV1P0_LINE_OUT_N<0>	OUT 26
26 IN	BV1P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV1P1_LINE_OUT_P<3>	OUT 26
26 IN	BV1P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV1P1_LINE_OUT_N<3>	OUT 26
26 IN	BV1P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV1P1_LINE_OUT_P<2>	OUT 26
26 IN	BV1P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV1P1_LINE_OUT_N<2>	OUT 26
26 IN	BV1P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV1P1_LINE_OUT_P<1>	OUT 26
26 IN	BV1P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV1P1_LINE_OUT_N<1>	OUT 26
26 IN	BV1P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV1P1_LINE_OUT_P<0>	OUT 26
26 IN	BV1P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV1P1_LINE_OUT_N<0>	OUT 26

CLK/CONFIG/SMI/I2C

26 IN	BV1_CLK_IN_P	C18_RT3_4 0.01UF	BV1_CLK_IN_AC_P	T8	CLK+		
26 IN	BV1_CLK_IN_N	C14_RT3_4 0.01UF	BV1_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
82 81 80 79 IN	VDDO_P2V5	R2_RT3_4 100	CONFIG_IO1_PULLUP	B7	CONFIG_IO		
		R14_RT3_4 100	EEPROM_LOAD1_EN	D10	EEPROM_LOAD_EN		
26 IN	BV1_ADDR<4>		(IPD)	N9	PHYAD4		
26 IN	BV1_ADDR<3>		(IPD)	P8	PHYAD3		
26 IN	BV1_ADDR<2>		(IPD)	P7	PHYAD2		
26 IN	BV1_ADDR<1>		(IPD)	R7	PHYAD1		
26 IN	BV1_RESET_L			P9	RESET		
		R16_RT3_4 1K		(IPD) R10	SEL_2X		
26 IN	BV1_SDC_MDC			C9	MDC		
26 IO	BV1_SDC_MDIO			C10	MDIO		

JTAG

	BV0_TDO			B9	TDI		
79 26 IN	BV_TMS			B10	TMS		
26 IN	BV1_TCK			D7	TCK		
79 26 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

			SCL	N10	R17_RT3_4 100	PACK_IGNORE=TRUE VDDO_P2V5	IN 79 80 81 82
					BOM=NONE		
						BV1_SCL	IO 26
			SDA	P10		BV1_SDA	IO 26
						PACK_IGNORE=TRUE	
					BOM=NONE		
					R18_RT3_4 100	VDDO_P2V5	IN 79 80 81 82
			INT	T10		BV1_INT_L	OUT 26
			TP	F7		BV1_TP	VIA TP2_RT3_4
			TDO	B8		BV_TDO	OUT 26

BEARVALLEY-3

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		81 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01

L6_RT3_4

82 80 IN AVDD_P1V0 56 100MHZ

10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV1_AVDDH

C75_RT3_4 150UF 4V

C151_RT3_4 22UF 6.3V

C77_RT3_4 22UF 6.3V

C79_RT3_4 0.1UF

C85_RT3_4 0.1UF

C87_RT3_4 0.1UF

C91_RT3_4 0.1UF

C93_RT3_4 0.1UF

C95_RT3_4 0.1UF

C97_RT3_4 0.1UF

C99_RT3_4 0.1UF

C101_RT3_4 0.1UF

C103_RT3_4 0.1UF

C105_RT3_4 0.1UF

C141_RT3_4 0.1UF

C143_RT3_4 0.1UF

C145_RT3_4 0.1UF

0.1UF

ADDCOMP=700-26993-01

U2_RT3_4

POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5

IN 79 80 81

C128_RT3_4 0.1UF

C129_RT3_4 0.1UF

C130_RT3_4 22UF 6.3V

DVDD_P1V0

IN 80

C107_RT3_4 0.1UF

C109_RT3_4 0.1UF

C111_RT3_4 0.1UF

C113_RT3_4 0.1UF

C115_RT3_4 0.1UF

C117_RT3_4 0.1UF

C119_RT3_4 0.1UF

C121_RT3_4 0.1UF

C123_RT3_4 0.1UF

C125_RT3_4 22UF 6.3V

C127_RT3_4 22UF 6.3V

C154_RT3_4 22UF 6.3V

C108_RT3_4 0.1UF

C110_RT3_4 0.1UF

C112_RT3_4 0.1UF

C114_RT3_4 0.1UF

C116_RT3_4 0.1UF

C118_RT3_4 0.1UF

C120_RT3_4 0.1UF

C122_RT3_4 0.1UF

C124_RT3_4 0.1UF

C126_RT3_4 22UF 6.3V

C153_RT3_4 22UF 6.3V

6.3V

36-0212-01

L7_RT3_4

82 80 IN AVDD_P1V0 56 100MHZ

10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV1_AVDDL

C76_RT3_4 150UF 4V

C78_RT3_4 22UF 6.3V

C80_RT3_4 0.1UF

C86_RT3_4 0.1UF

C88_RT3_4 0.1UF

C92_RT3_4 0.1UF

C94_RT3_4 0.1UF

C96_RT3_4 0.1UF

C98_RT3_4 0.1UF

C100_RT3_4 0.1UF

C102_RT3_4 0.1UF

C104_RT3_4 0.1UF

C106_RT3_4 0.1UF

C142_RT3_4 0.1UF

C144_RT3_4 0.1UF

C146_RT3_4 0.1UF

C152_RT3_4 0.1UF

22UF 6.3V

ADDCOMP=700-26993-01

U2_RT3_4

GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-4

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		82 OF 138

BEARVALLY SUBDESIGN REV05

2X BEARVALLY MODULE

CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY
11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP
05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)
REQUIRE CAD LAYOUT CHANGE

TITLE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Mon Dec 21 20:28:30 2020		83 OF 138

ADDCOMP=700-26993-01

U1_RT5_6

SERDES HOST SIDE

27 IN	BV0P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV0P0_HOST_OUT_P<3>	OUT 27
27 IN	BV0P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV0P0_HOST_OUT_N<3>	OUT 27
27 IN	BV0P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV0P0_HOST_OUT_P<2>	OUT 27
27 IN	BV0P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV0P0_HOST_OUT_N<2>	OUT 27
27 IN	BV0P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV0P0_HOST_OUT_P<1>	OUT 27
27 IN	BV0P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV0P0_HOST_OUT_N<1>	OUT 27
27 IN	BV0P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV0P0_HOST_OUT_P<0>	OUT 27
27 IN	BV0P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV0P0_HOST_OUT_N<0>	OUT 27
27 IN	BV0P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV0P1_HOST_OUT_P<3>	OUT 27
27 IN	BV0P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV0P1_HOST_OUT_N<3>	OUT 27
27 IN	BV0P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV0P1_HOST_OUT_P<2>	OUT 27
27 IN	BV0P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV0P1_HOST_OUT_N<2>	OUT 27
27 IN	BV0P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV0P1_HOST_OUT_P<1>	OUT 27
27 IN	BV0P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV0P1_HOST_OUT_N<1>	OUT 27
27 IN	BV0P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV0P1_HOST_OUT_P<0>	OUT 27
27 IN	BV0P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV0P1_HOST_OUT_N<0>	OUT 27

SERDES LINE SIDE

27 IN	BV0P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV0P0_LINE_OUT_P<3>	OUT 27
27 IN	BV0P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV0P0_LINE_OUT_N<3>	OUT 27
27 IN	BV0P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV0P0_LINE_OUT_P<2>	OUT 27
27 IN	BV0P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV0P0_LINE_OUT_N<2>	OUT 27
27 IN	BV0P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV0P0_LINE_OUT_P<1>	OUT 27
27 IN	BV0P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV0P0_LINE_OUT_N<1>	OUT 27
27 IN	BV0P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV0P0_LINE_OUT_P<0>	OUT 27
27 IN	BV0P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV0P0_LINE_OUT_N<0>	OUT 27
27 IN	BV0P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV0P1_LINE_OUT_P<3>	OUT 27
27 IN	BV0P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV0P1_LINE_OUT_N<3>	OUT 27
27 IN	BV0P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV0P1_LINE_OUT_P<2>	OUT 27
27 IN	BV0P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV0P1_LINE_OUT_N<2>	OUT 27
27 IN	BV0P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV0P1_LINE_OUT_P<1>	OUT 27
27 IN	BV0P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV0P1_LINE_OUT_N<1>	OUT 27
27 IN	BV0P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV0P1_LINE_OUT_P<0>	OUT 27
27 IN	BV0P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV0P1_LINE_OUT_N<0>	OUT 27

PACK_IGNORE=TRUE

CLK/CONFIG/SMI/I2C

27 IN	BV0_CLK_IN_P	C11 RT5 6 0.01UF	BV0_CLK_IN_AC_P	T8	CLK+		
27 IN	BV0_CLK_IN_N	C12 RT5 6 0.01UF	BV0_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
87 86 85 84 IN	VDDO_P2V5	R2 RT5 6 100	CONFIG_IO0_PULLUP	B7	CONFIG_IO	SCL N10	R11_RT5_6 100 VDDO_P2V5 IN 84 85 86 87 BOM=NONE; BV0_SCL IO 27
		R9_RT5_6 100	EEPROM_LOAD0_EN	D10	EEPROM_LOAD_EN	SDA P10	BV0_SDA IO 27 PACK_IGNORE=TRUE; R12_RT5_6 100 VDDO_P2V5 IN 84 85 86 87 BOM=NONE
27 IN	BV0_ADDR<4>	(IPD)		N9	PHYAD4		
27 IN	BV0_ADDR<3>	(IPD)		P8	PHYAD3		
27 IN	BV0_ADDR<2>	(IPD)		P7	PHYAD2		
27 IN	BV0_ADDR<1>	(IPD)		R7	PHYAD1		
27 IN	BV0_RESET_L			P9	RESET	INT T10	BV0_INT_L OUT 27
	R3_RT5_6 1K	(IPD)		R10	SEL_2X		
27 IN	BV0_SDC_MDC			C9	MDC		
27 IO	BV0_SDC_MDIO			C10	MDIO	TP F7	BV0_TP TP1_RT5_6 VIA

JTAG

27 IN	BV_TDI			B9	TDI	TDO B8	BV0_TDO (TO BV1)
86 27 IN	BV_TMS			B10	TMS		
27 IN	BV0_TCK			D7	TCK		
86 27 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

BEARVALLEY-1

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		84 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L3_RT5_6
AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612
2.05A (TYP DFE ON)
FLTR_BV0_AVDDH

ADDCOMP=700-26993-01
U1_RT5_6
POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5
DVDD_P1V0

36-0212-01
L5_RT5_6
AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612
2.05A (TYP DFE ON)
FLTR_BV0_AVDDL
C148_RT5_6 22UF 6.3V

ADDCOMP=700-26993-01
U1_RT5_6
GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		85 OF 138

ADDCOMP=700-26993-01

U2_RT5_6

SERDES HOST SIDE

27 IN	BV1P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV1P0_HOST_OUT_P<3>	OUT 27
27 IN	BV1P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV1P0_HOST_OUT_N<3>	OUT 27
27 IN	BV1P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV1P0_HOST_OUT_P<2>	OUT 27
27 IN	BV1P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV1P0_HOST_OUT_N<2>	OUT 27
27 IN	BV1P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV1P0_HOST_OUT_P<1>	OUT 27
27 IN	BV1P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV1P0_HOST_OUT_N<1>	OUT 27
27 IN	BV1P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV1P0_HOST_OUT_P<0>	OUT 27
27 IN	BV1P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV1P0_HOST_OUT_N<0>	OUT 27
27 IN	BV1P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV1P1_HOST_OUT_P<3>	OUT 27
27 IN	BV1P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV1P1_HOST_OUT_N<3>	OUT 27
27 IN	BV1P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV1P1_HOST_OUT_P<2>	OUT 27
27 IN	BV1P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV1P1_HOST_OUT_N<2>	OUT 27
27 IN	BV1P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV1P1_HOST_OUT_P<1>	OUT 27
27 IN	BV1P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV1P1_HOST_OUT_N<1>	OUT 27
27 IN	BV1P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV1P1_HOST_OUT_P<0>	OUT 27
27 IN	BV1P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV1P1_HOST_OUT_N<0>	OUT 27

SERDES LINE SIDE

27 IN	BV1P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV1P0_LINE_OUT_P<3>	OUT 27
27 IN	BV1P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV1P0_LINE_OUT_N<3>	OUT 27
27 IN	BV1P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV1P0_LINE_OUT_P<2>	OUT 27
27 IN	BV1P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV1P0_LINE_OUT_N<2>	OUT 27
27 IN	BV1P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV1P0_LINE_OUT_P<1>	OUT 27
27 IN	BV1P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV1P0_LINE_OUT_N<1>	OUT 27
27 IN	BV1P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV1P0_LINE_OUT_P<0>	OUT 27
27 IN	BV1P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV1P0_LINE_OUT_N<0>	OUT 27
27 IN	BV1P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV1P1_LINE_OUT_P<3>	OUT 27
27 IN	BV1P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV1P1_LINE_OUT_N<3>	OUT 27
27 IN	BV1P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV1P1_LINE_OUT_P<2>	OUT 27
27 IN	BV1P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV1P1_LINE_OUT_N<2>	OUT 27
27 IN	BV1P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV1P1_LINE_OUT_P<1>	OUT 27
27 IN	BV1P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV1P1_LINE_OUT_N<1>	OUT 27
27 IN	BV1P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV1P1_LINE_OUT_P<0>	OUT 27
27 IN	BV1P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV1P1_LINE_OUT_N<0>	OUT 27

CLK/CONFIG/SMI/I2C

27 IN	BV1_CLK_IN_P	C19_RT5_6 0.01UF	BV1_CLK_IN_AC_P	T8	CLK+		
27 IN	BV1_CLK_IN_N	C20_RT5_6 0.01UF	BV1_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
87 86 85 84 IN	VDDO_P2V5	R12_RT5_6 100	CONFIG_IO1_PULLUP	B7	CONFIG_IO	SCL N10	R17_RT5_6 PACK_IGNORE=TRUE 100 VDDO_P2V5 IN 84 85 86 87 BOM=NONE BV1_SCL IO 27
		R14_RT5_6 100	EEPROM_LOAD_EN	D10	EEPROM_LOAD_EN	SDA P10	BV1_SDA IO 27 PACK_IGNORE=TRUE BOM=NONE 100 VDDO_P2V5 IN 84 85 86 87 R18_RT5_6
27 IN	BV1_ADDR<4>	(IPD)		N9	PHYAD4		
27 IN	BV1_ADDR<3>	(IPD)		P8	PHYAD3		
27 IN	BV1_ADDR<2>	(IPD)		P7	PHYAD2		
27 IN	BV1_ADDR<1>	(IPD)		R7	PHYAD1		
27 IN	BV1_RESET_L			P9	RESET	INT T10	BV1_INT_L OUT 27
	R16_RT5_6 1K			(IPD) R10	SEL_2X		
27 IN	BV1_SDC_MDC			C9	MDC		
27 IO	BV1_SDC_MDIO			C10	MDIO	TP F7	BV1_TP VIA TP2_RT5_6

JTAG

	BV0_TDO			B9	TDI	TDO B8	BV_TDO OUT 27
84 27 IN	BV_TMS			B10	TMS		
27 IN	BV1_TCK			D7	TCK		
84 27 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

BEARVALLEY-3

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		86 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L6_RT5_6
56 100MHZ
10A, 0.0040HM, 1612

87 85 IN AVDD_P1V0

2.05A (TYP DFE ON)

FLTR_BV1_AVDDH

C75_RT5_6 150UF 4V
C151_RT5_6 22UF 6.3V
C77_RT5_6 22UF 6.3V
C79_RT5_6 0.1UF
C85_RT5_6 0.1UF
C87_RT5_6 0.1UF
C91_RT5_6 0.1UF
C93_RT5_6 0.1UF
C95_RT5_6 0.1UF
C97_RT5_6 0.1UF
C99_RT5_6 0.1UF
C101_RT5_6 0.1UF
C103_RT5_6 0.1UF
C105_RT5_6 0.1UF
C141_RT5_6 0.1UF
C143_RT5_6 0.1UF
C145_RT5_6 0.1UF
0.1UF

ADDCOMP=700-26993-01
U2_RT5_6
POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5
IN 84 85 86
C128_RT5_6 0.1UF
C129_RT5_6 0.1UF
C130_RT5_6 22UF 6.3V

DVDD_P1V0
IN 85
C107_RT5_6 0.1UF
C109_RT5_6 0.1UF
C111_RT5_6 0.1UF
C113_RT5_6 0.1UF
C115_RT5_6 0.1UF
C117_RT5_6 0.1UF
C119_RT5_6 0.1UF
C121_RT5_6 0.1UF
C123_RT5_6 0.1UF
C125_RT5_6 22UF 6.3V
C127_RT5_6 22UF 6.3V
C154_RT5_6 22UF 6.3V
C108_RT5_6 0.1UF
C110_RT5_6 0.1UF
C112_RT5_6 0.1UF
C114_RT5_6 0.1UF
C116_RT5_6 0.1UF
C118_RT5_6 0.1UF
C120_RT5_6 0.1UF
C122_RT5_6 0.1UF
C124_RT5_6 0.1UF
C126_RT5_6 22UF 6.3V
C153_RT5_6 22UF 6.3V

36-0212-01
L7_RT5_6
56 100MHZ
10A, 0.0040HM, 1612

87 85 IN AVDD_P1V0

2.05A (TYP DFE ON)

FLTR_BV1_AVDDL

C76_RT5_6 150UF 4V
C78_RT5_6 22UF 6.3V
C80_RT5_6 0.1UF
C86_RT5_6 0.1UF
C88_RT5_6 0.1UF
C92_RT5_6 0.1UF
C94_RT5_6 0.1UF
C96_RT5_6 0.1UF
C98_RT5_6 0.1UF
C100_RT5_6 0.1UF
C102_RT5_6 0.1UF
C104_RT5_6 0.1UF
C106_RT5_6 0.1UF
C142_RT5_6 0.1UF
C144_RT5_6 0.1UF
C146_RT5_6 0.1UF
C152_RT5_6 22UF 6.3V

ADDCOMP=700-26993-01
U2_RT5_6
GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-4

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		87 OF 138

BEARVALLY SUBDESIGN REV05

2X BEARVALLY MODULE

CHANGES:

11/21/2017: REPLACE 47UF CAP (11-100179-01) WITH (11-3497-01), BOM CHANGE ONLY
11/27/2017: REPLACED AVDD FILTER INDUCTORS WITH LOWER DCR FERRITE BEADS TO REDUCE VOLTAGE DROP
05/28/2019: MLCC CAPS 11-3497-01 (47UF) TO 11-2686-02 (22UF) (USE ADDITIONAL 11-2686-02 TO COMPENSATE CAPACITANCE)
REQUIRE CAD LAYOUT CHANGE

TITLE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Mon Dec 21 20:28:30 2020		88 OF 138

ADDCOMP=700-26993-01

U1_RT7_8

SERDES HOST SIDE

28 IN	BV0P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV0P0_HOST_OUT_P<3>	OUT 28
28 IN	BV0P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV0P0_HOST_OUT_N<3>	OUT 28
28 IN	BV0P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV0P0_HOST_OUT_P<2>	OUT 28
28 IN	BV0P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV0P0_HOST_OUT_N<2>	OUT 28
28 IN	BV0P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV0P0_HOST_OUT_P<1>	OUT 28
28 IN	BV0P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV0P0_HOST_OUT_N<1>	OUT 28
28 IN	BV0P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV0P0_HOST_OUT_P<0>	OUT 28
28 IN	BV0P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV0P0_HOST_OUT_N<0>	OUT 28
28 IN	BV0P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV0P1_HOST_OUT_P<3>	OUT 28
28 IN	BV0P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV0P1_HOST_OUT_N<3>	OUT 28
28 IN	BV0P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV0P1_HOST_OUT_P<2>	OUT 28
28 IN	BV0P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV0P1_HOST_OUT_N<2>	OUT 28
28 IN	BV0P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV0P1_HOST_OUT_P<1>	OUT 28
28 IN	BV0P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV0P1_HOST_OUT_N<1>	OUT 28
28 IN	BV0P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV0P1_HOST_OUT_P<0>	OUT 28
28 IN	BV0P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV0P1_HOST_OUT_N<0>	OUT 28

SERDES LINE SIDE

28 IN	BV0P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV0P0_LINE_OUT_P<3>	OUT 28
28 IN	BV0P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV0P0_LINE_OUT_N<3>	OUT 28
28 IN	BV0P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV0P0_LINE_OUT_P<2>	OUT 28
28 IN	BV0P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV0P0_LINE_OUT_N<2>	OUT 28
28 IN	BV0P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV0P0_LINE_OUT_P<1>	OUT 28
28 IN	BV0P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV0P0_LINE_OUT_N<1>	OUT 28
28 IN	BV0P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV0P0_LINE_OUT_P<0>	OUT 28
28 IN	BV0P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV0P0_LINE_OUT_N<0>	OUT 28
28 IN	BV0P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV0P1_LINE_OUT_P<3>	OUT 28
28 IN	BV0P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV0P1_LINE_OUT_N<3>	OUT 28
28 IN	BV0P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV0P1_LINE_OUT_P<2>	OUT 28
28 IN	BV0P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV0P1_LINE_OUT_N<2>	OUT 28
28 IN	BV0P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV0P1_LINE_OUT_P<1>	OUT 28
28 IN	BV0P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV0P1_LINE_OUT_N<1>	OUT 28
28 IN	BV0P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV0P1_LINE_OUT_P<0>	OUT 28
28 IN	BV0P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV0P1_LINE_OUT_N<0>	OUT 28

PACK_IGNORE=TRUE

CLK/CONFIG/SMI/I2C

28 IN	BV0_CLK_IN_P	C11_RT7_8 0.01UF	BV0_CLK_IN_AC_P	T8	CLK+		
28 IN	BV0_CLK_IN_N	C12_RT7_8 0.01UF	BV0_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
92 91 90 89 IN	VDDO_P2V5	R7_RT7_8 100	CONFIG_IO0_PULLUP	B7	CONFIG_IO	SCL N10	R11_RT7_8 100 VDDO_P2V5 IN 89 90 91 92 BOM=NONE; BV0_SCL IO 28
		R9_RT7_8 100	EEPROM_LOAD0_EN	D10	EEPROM_LOAD_EN	SDA P10	BV0_SDA IO 28 PACK_IGNORE=TRUE; R12_RT7_8 100 VDDO_P2V5 IN 89 90 91 92 BOM=NONE
28 IN	BV0_ADDR<4>	(IPD)		N9	PHYAD4		
28 IN	BV0_ADDR<3>	(IPD)		P8	PHYAD3		
28 IN	BV0_ADDR<2>	(IPD)		P7	PHYAD2		
28 IN	BV0_ADDR<1>	(IPD)		R7	PHYAD1		
28 IN	BV0_RESET_L			P9	RESET	INT T10	BV0_INT_L OUT 28
	R3_RT7_8 1K	(IPD)		R10	SEL_2X		
28 IN	BV0_SDC_MDC			C9	MDC		
28 IO	BV0_SDC_MDIO			C10	MDIO	TP F7	BV0_TP VIA TP1_RT7_8

JTAG

28 IN	BV_TDI			B9	TDI	TDO B8	BV0_TDO (TO BV1)
91 28 IN	BV_TMS			B10	TMS		
28 IN	BV0_TCK			D7	TCK		
91 28 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

BEARVALLEY-1

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		89 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01
L3_RT7_8
90 92 IN AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV0_AVDDH

C60_RT7_8 150UF 4V
C147_RT7_8 22UF 6.3V
C61_RT7_8 22UF 6.3V
C41_RT7_8 22UF 6.3V
C47_RT7_8 0.1UF
C19_RT7_8 0.1UF
C38_RT7_8 0.1UF
C44_RT7_8 0.1UF
C50_RT7_8 0.1UF
C23_RT7_8 0.1UF
C62_RT7_8 0.1UF
C63_RT7_8 0.1UF
C64_RT7_8 0.1UF
C65_RT7_8 0.1UF
C134_RT7_8 0.1UF
C136_RT7_8 0.1UF
C138_RT7_8 0.1UF
0.1UF

ADDCOMP=700-26993-01
U1_RT7_8
POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY
15-104658-01

VDDO_P2V5
IN 89 91 92
C29_RT7_8 0.1UF
C35_RT7_8 0.1UF
C90_RT7_8 22UF 6.3V

DVDD_P1V0
IN 92
C34_RT7_8 0.1UF
C37_RT7_8 0.1UF
C40_RT7_8 0.1UF
C43_RT7_8 0.1UF
C46_RT7_8 0.1UF
C49_RT7_8 0.1UF
C52_RT7_8 0.1UF
C66_RT7_8 0.1UF
C68_RT7_8 0.1UF
C70_RT7_8 0.1UF
C72_RT7_8 22UF 6.3V
22UF 6.3V
C150_RT7_8 22UF 6.3V
C36_RT7_8 0.1UF
C39_RT7_8 0.1UF
C42_RT7_8 0.1UF
C45_RT7_8 0.1UF
C48_RT7_8 0.1UF
C51_RT7_8 0.1UF
C59_RT7_8 0.1UF
C67_RT7_8 0.1UF
C69_RT7_8 0.1UF
C71_RT7_8 22UF 6.3V
C149_RT7_8 22UF 6.3V
6.3V

36-0212-01
L5_RT7_8
92 90 IN AVDD_P1V0
56 100MHZ
10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV0_AVDDL

C25_RT7_8 150UF 4V
C27_RT7_8 22UF 6.3V
C16_RT7_8 22UF 6.3V
C22_RT7_8 22UF 6.3V
C8_RT7_8 0.1UF
C15_RT7_8 0.1UF
C21_RT7_8 0.1UF
C24_RT7_8 0.1UF
C13_RT7_8 0.1UF
C28_RT7_8 0.1UF
C30_RT7_8 0.1UF
C31_RT7_8 0.1UF
C33_RT7_8 0.1UF
C133_RT7_8 0.1UF
C135_RT7_8 0.1UF
C137_RT7_8 0.1UF
0.1UF

C148_RT7_8 22UF 6.3V

ADDCOMP=700-26993-01
U1_RT7_8
GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY
15-104658-01

BEARVALLEY-2

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:15 2021		90 OF 138

ADDCOMP=700-26993-01

U2_RT7_8

SERDES HOST SIDE

28 IN	BV1P0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BV1P0_HOST_OUT_P<3>	OUT 28
28 IN	BV1P0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BV1P0_HOST_OUT_N<3>	OUT 28
28 IN	BV1P0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BV1P0_HOST_OUT_P<2>	OUT 28
28 IN	BV1P0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BV1P0_HOST_OUT_N<2>	OUT 28
28 IN	BV1P0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BV1P0_HOST_OUT_P<1>	OUT 28
28 IN	BV1P0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BV1P0_HOST_OUT_N<1>	OUT 28
28 IN	BV1P0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BV1P0_HOST_OUT_P<0>	OUT 28
28 IN	BV1P0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BV1P0_HOST_OUT_N<0>	OUT 28
28 IN	BV1P1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BV1P1_HOST_OUT_P<3>	OUT 28
28 IN	BV1P1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BV1P1_HOST_OUT_N<3>	OUT 28
28 IN	BV1P1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BV1P1_HOST_OUT_P<2>	OUT 28
28 IN	BV1P1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BV1P1_HOST_OUT_N<2>	OUT 28
28 IN	BV1P1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BV1P1_HOST_OUT_P<1>	OUT 28
28 IN	BV1P1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BV1P1_HOST_OUT_N<1>	OUT 28
28 IN	BV1P1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BV1P1_HOST_OUT_P<0>	OUT 28
28 IN	BV1P1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BV1P1_HOST_OUT_N<0>	OUT 28

SERDES LINE SIDE

28 IN	BV1P0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BV1P0_LINE_OUT_P<3>	OUT 28
28 IN	BV1P0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BV1P0_LINE_OUT_N<3>	OUT 28
28 IN	BV1P0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BV1P0_LINE_OUT_P<2>	OUT 28
28 IN	BV1P0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BV1P0_LINE_OUT_N<2>	OUT 28
28 IN	BV1P0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BV1P0_LINE_OUT_P<1>	OUT 28
28 IN	BV1P0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BV1P0_LINE_OUT_N<1>	OUT 28
28 IN	BV1P0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BV1P0_LINE_OUT_P<0>	OUT 28
28 IN	BV1P0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BV1P0_LINE_OUT_N<0>	OUT 28
28 IN	BV1P1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BV1P1_LINE_OUT_P<3>	OUT 28
28 IN	BV1P1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BV1P1_LINE_OUT_N<3>	OUT 28
28 IN	BV1P1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BV1P1_LINE_OUT_P<2>	OUT 28
28 IN	BV1P1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BV1P1_LINE_OUT_N<2>	OUT 28
28 IN	BV1P1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BV1P1_LINE_OUT_P<1>	OUT 28
28 IN	BV1P1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BV1P1_LINE_OUT_N<1>	OUT 28
28 IN	BV1P1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BV1P1_LINE_OUT_P<0>	OUT 28
28 IN	BV1P1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BV1P1_LINE_OUT_N<0>	OUT 28

CLK/CONFIG/SMI/I2C

28 IN	BV1_CLK_IN_P	C18 RT7_8 0.01UF	BV1_CLK_IN_AC_P	T8	CLK+		
28 IN	BV1_CLK_IN_N	C19 RT7_8 0.01UF	BV1_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
92 91 90 89 IN	VDDO_P2V5	R12 RT7_8 100	CONFIG_IO1_PULLUP	B7	CONFIG_IO		
		R14 RT7_8 100	EEPROM_LOAD1_EN	D10	EEPROM_LOAD_EN		
28 IN	BV1_ADDR<4>		(IPD)	N9	PHYAD4		
28 IN	BV1_ADDR<3>		(IPD)	P8	PHYAD3		
28 IN	BV1_ADDR<2>		(IPD)	P7	PHYAD2		
28 IN	BV1_ADDR<1>		(IPD)	R7	PHYAD1		
28 IN	BV1_RESET_L			P9	RESET		
		R16 RT7_8 1K		(IPD) R10	SEL_2X		
28 IN	BV1_SDC_MDC			C9	MDC		
28 IO	BV1_SDC_MDIO			C10	MDIO		
	BV0_TDO			B9	TDI		
89 28 IN	BV_TMS			B10	TMS		
28 IN	BV1_TCK			D7	TCK		
89 28 IN	BV_TRST_L			D8	TRST		

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BEARVALLEY
15-104658-01

				SCL	N10	R17_RT7_8 100 BOM=NONE	PACK_IGNORE=TRUE VDDO_P2V5 IN 89 90 91 92
						BV1_SCL	IO 28
				SDA	P10	BV1_SDA	IO 28
						R18_RT7_8 100 BOM=NONE	PACK_IGNORE=TRUE VDDO_P2V5 IN 89 90 91 92
				INT	T10	BV1_INT_L	OUT 28
				TP	F7	BV1_TP	VIA TP2_RT7_8
				TDO	B8	BV_TDO	OUT 28

BEARVALLEY-3

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		91 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

36-0212-01 L6_RT7_8

92 90 IN AVDD_P1V0 — 56 100MHZ 10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV1_AVDDH

C75_RT7_8 150UF 4V; C151_RT7_8 22UF 6.3V; C77_RT7_8 22UF 6.3V; C79_RT7_8 0.1UF; C85_RT7_8 0.1UF; C87_RT7_8 0.1UF; C91_RT7_8 0.1UF; C93_RT7_8 0.1UF; C95_RT7_8 0.1UF; C97_RT7_8 0.1UF; C99_RT7_8 0.1UF; C101_RT7_8 0.1UF; C103_RT7_8 0.1UF; C105_RT7_8 0.1UF; C141_RT7_8 0.1UF; C143_RT7_8 0.1UF; C145_RT7_8 0.1UF

36-0212-01 L7_RT7_8

92 90 IN AVDD_P1V0 — 56 100MHZ 10A, 0.004OHM, 1612

2.05A (TYP DFE ON)

FLTR_BV1_AVDDL

C76_RT7_8 150UF 4V; C78_RT7_8 22UF 6.3V; C80_RT7_8 0.1UF; C86_RT7_8 0.1UF; C88_RT7_8 0.1UF; C92_RT7_8 0.1UF; C94_RT7_8 0.1UF; C96_RT7_8 0.1UF; C98_RT7_8 0.1UF; C100_RT7_8 0.1UF; C102_RT7_8 0.1UF; C104_RT7_8 0.1UF; C106_RT7_8 0.1UF; C142_RT7_8 0.1UF; C144_RT7_8 0.1UF; C146_RT7_8 0.1UF; C152_RT7_8 22UF 6.3V

ADDCOMP=700-26993-01

U2_RT7_8

POWER & TEST

N6	AVDD28	VDDO_2	D9
N3	AVDD27	VDDO_1	C8
L6	AVDD26		
L3	AVDD25	TEST1	N7
J6	AVDD24		
J3	AVDD23	DVDD16	N8
G6	AVDD22	DVDD15	M9
G3	AVDD21	DVDD14	M7
E6	AVDD20	DVDD13	L10
E3	AVDD19	DVDD12	L8
C6	AVDD18	DVDD11	K9
C3	AVDD17	DVDD10	K7
A6	AVDD16	DVDD9	J10
A3	AVDD15	DVDD8	J8
		DVDD7	H9
T14	AVDD14	DVDD6	H7
T11	AVDD13	DVDD5	G10
P14	AVDD12	DVDD4	G8
P11	AVDD11	DVDD3	F9
M14	AVDD10	DVDD2	E10
M11	AVDD9	DVDD1	E8
K14	AVDD8		
K11	AVDD7		
H14	AVDD6		
H11	AVDD5		
F14	AVDD4		
F11	AVDD3		
D14	AVDD2		
D11	AVDD1		

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BEARVALLEY 15-104658-01

VDDO_P2V5

IN 89 90 91

C128_RT7_8 0.1UF; C129_RT7_8 0.1UF; C130_RT7_8 22UF 6.3V

DVDD_P1V0

IN 90

C107_RT7_8 0.1UF; C109_RT7_8 0.1UF; C111_RT7_8 0.1UF; C113_RT7_8 0.1UF; C115_RT7_8 0.1UF; C117_RT7_8 0.1UF; C119_RT7_8 0.1UF; C121_RT7_8 0.1UF; C123_RT7_8 0.1UF; C125_RT7_8 22UF; C127_RT7_8 22UF 6.3V; C154_RT7_8 22UF 6.3V

C108_RT7_8 0.1UF; C110_RT7_8 0.1UF; C112_RT7_8 0.1UF; C114_RT7_8 0.1UF; C116_RT7_8 0.1UF; C118_RT7_8 0.1UF; C120_RT7_8 0.1UF; C122_RT7_8 0.1UF; C124_RT7_8 0.1UF; C126_RT7_8 22UF; C153_RT7_8 22UF 6.3V

6.3V 6.3V 6.3V

ADDCOMP=700-26993-01

U2_RT7_8

GROUND

M10	VSS17	AVSS62	K13
M8	VSS16	AVSS61	K12
L9	VSS15	AVSS60	K6
L7	VSS14	AVSS59	K3
K10	VSS13	AVSS58	J14
K8	VSS12	AVSS57	J11
J9	VSS11	AVSS56	J5
J7	VSS10	AVSS55	J4
H10	VSS9	AVSS54	J2
H8	VSS8	AVSS53	J1
G9	VSS7	AVSS52	H16
G7	VSS6	AVSS51	H15
F10	VSS5	AVSS50	H13
F8	VSS4	AVSS49	H12
E9	VSS3	AVSS48	H6
E7	VSS2	AVSS47	H3
C7	VSS1	AVSS46	G14
		AVSS45	G11
		AVSS44	G5
T16	AVSS105	AVSS43	G4
T15	AVSS104	AVSS42	G2
T13	AVSS103	AVSS41	G1
T12	AVSS102	AVSS40	F16
T7	AVSS101	AVSS39	F15
T4	AVSS100	AVSS38	F13
T1	AVSS99	AVSS37	F12
R14	AVSS98	AVSS36	F6
R11	AVSS97	AVSS35	F3
R9	AVSS96	AVSS34	E14
R8	AVSS95	AVSS33	E11
R6	AVSS94	AVSS32	E5
R5	AVSS93	AVSS31	E4
R4	AVSS92	AVSS30	E2
R3	AVSS91	AVSS29	E1
R2	AVSS90	AVSS28	D16
R1	AVSS89	AVSS27	D15
P16	AVSS88	AVSS26	D13
P15	AVSS87	AVSS25	D12
P13	AVSS86	AVSS24	D6
P12	AVSS85	AVSS23	D3
P6	AVSS84	AVSS22	C14
P3	AVSS83	AVSS21	C11
N14	AVSS82	AVSS20	C5
N11	AVSS81	AVSS19	C4
N5	AVSS80	AVSS18	C2
N4	AVSS79	AVSS17	C1
N2	AVSS78	AVSS16	B16
N1	AVSS77	AVSS15	B15
M16	AVSS76	AVSS14	B14
M15	AVSS75	AVSS13	B13
M13	AVSS74	AVSS12	B12
M12	AVSS73	AVSS11	B11
M6	AVSS72	AVSS10	B6
M3	AVSS71	AVSS9	B3
L14	AVSS70	AVSS8	A16
L11	AVSS69	AVSS7	A13
L5	AVSS68	AVSS6	A10
L4	AVSS67	AVSS5	A7
L2	AVSS66	AVSS4	A5
L1	AVSS65	AVSS3	A4
K16	AVSS64	AVSS2	A2
K15	AVSS63	AVSS1	A1

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BEARVALLEY 15-104658-01

BEARVALLEY-4

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:16 2021		92 OF 138

BEARVALLY SUBDESIGN REV08

1X BEARVALLY MODULE

REPLACED AVDD FILTER 0.02 OHM DCR INDUCTORS WITH 0.004 OHM DCR FERRITE BEADS TO REDUCE VOLTAGE DROP
REPLACED 47UF CAP 11-100179-01 WITH 11-3497-01 FOR BOM RISK
REPLACED 47UF CAP 11-3497-01 WITH 11-2686-04 FOR BOM RISK (ADD ADDITIONAL 11-2686-04 TO COMPENSATE CAPACITANCE)
REQUIRE CAD LAYOUT CHANGE/RESPIN

TITLE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Fri Jun 21 15:36:50 2019		93 OF 138

ADDCOMP=700-26993-01
HEATSINK

U1_RT9

SERDES HOST SIDE

29 IN	BVP0_HOST_IN_P<3>	K1	P0_HI3+	P0_HO3+	K4	BVP0_HOST_OUT_P<3>	OUT 29
29 IN	BVP0_HOST_IN_N<3>	K2	P0_HI3-	P0_HO3-	K5	BVP0_HOST_OUT_N<3>	OUT 29
29 IN	BVP0_HOST_IN_P<2>	M1	P0_HI2+	P0_HO2+	M4	BVP0_HOST_OUT_P<2>	OUT 29
29 IN	BVP0_HOST_IN_N<2>	M2	P0_HI2-	P0_HO2-	M5	BVP0_HOST_OUT_N<2>	OUT 29
29 IN	BVP0_HOST_IN_P<1>	P1	P0_HI1+	P0_HO1+	P4	BVP0_HOST_OUT_P<1>	OUT 29
29 IN	BVP0_HOST_IN_N<1>	P2	P0_HI1-	P0_HO1-	P5	BVP0_HOST_OUT_N<1>	OUT 29
29 IN	BVP0_HOST_IN_P<0>	T2	P0_HI0+	P0_HO0+	T5	BVP0_HOST_OUT_P<0>	OUT 29
29 IN	BVP0_HOST_IN_N<0>	T3	P0_HI0-	P0_HO0-	T6	BVP0_HOST_OUT_N<0>	OUT 29
29 IN	BVP1_HOST_IN_P<3>	B1	P1_HI3+	P1_HO3+	B4	BVP1_HOST_OUT_P<3>	OUT 29
29 IN	BVP1_HOST_IN_N<3>	B2	P1_HI3-	P1_HO3-	B5	BVP1_HOST_OUT_N<3>	OUT 29
29 IN	BVP1_HOST_IN_P<2>	D1	P1_HI2+	P1_HO2+	D4	BVP1_HOST_OUT_P<2>	OUT 29
29 IN	BVP1_HOST_IN_N<2>	D2	P1_HI2-	P1_HO2-	D5	BVP1_HOST_OUT_N<2>	OUT 29
29 IN	BVP1_HOST_IN_P<1>	F1	P1_HI1+	P1_HO1+	F4	BVP1_HOST_OUT_P<1>	OUT 29
29 IN	BVP1_HOST_IN_N<1>	F2	P1_HI1-	P1_HO1-	F5	BVP1_HOST_OUT_N<1>	OUT 29
29 IN	BVP1_HOST_IN_P<0>	H1	P1_HI0+	P1_HO0+	H4	BVP1_HOST_OUT_P<0>	OUT 29
29 IN	BVP1_HOST_IN_N<0>	H2	P1_HI0-	P1_HO0-	H5	BVP1_HOST_OUT_N<0>	OUT 29

SERDES LINE SIDE

29 IN	BVP0_LINE_IN_P<3>	J15	P0_LI3+	P0_LO3+	J12	BVP0_LINE_OUT_P<3>	OUT 29
29 IN	BVP0_LINE_IN_N<3>	J16	P0_LI3-	P0_LO3-	J13	BVP0_LINE_OUT_N<3>	OUT 29
29 IN	BVP0_LINE_IN_P<2>	L15	P0_LI2+	P0_LO2+	L12	BVP0_LINE_OUT_P<2>	OUT 29
29 IN	BVP0_LINE_IN_N<2>	L16	P0_LI2-	P0_LO2-	L13	BVP0_LINE_OUT_N<2>	OUT 29
29 IN	BVP0_LINE_IN_P<1>	N15	P0_LI1+	P0_LO1+	N12	BVP0_LINE_OUT_P<1>	OUT 29
29 IN	BVP0_LINE_IN_N<1>	N16	P0_LI1-	P0_LO1-	N13	BVP0_LINE_OUT_N<1>	OUT 29
29 IN	BVP0_LINE_IN_P<0>	R15	P0_LI0+	P0_LO0+	R12	BVP0_LINE_OUT_P<0>	OUT 29
29 IN	BVP0_LINE_IN_N<0>	R16	P0_LI0-	P0_LO0-	R13	BVP0_LINE_OUT_N<0>	OUT 29
29 IN	BVP1_LINE_IN_P<3>	A14	P1_LI3+	P1_LO3+	A11	BVP1_LINE_OUT_P<3>	OUT 29
29 IN	BVP1_LINE_IN_N<3>	A15	P1_LI3-	P1_LO3-	A12	BVP1_LINE_OUT_N<3>	OUT 29
29 IN	BVP1_LINE_IN_P<2>	C15	P1_LI2+	P1_LO2+	C12	BVP1_LINE_OUT_P<2>	OUT 29
29 IN	BVP1_LINE_IN_N<2>	C16	P1_LI2-	P1_LO2-	C13	BVP1_LINE_OUT_N<2>	OUT 29
29 IN	BVP1_LINE_IN_P<1>	E15	P1_LI1+	P1_LO1+	E12	BVP1_LINE_OUT_P<1>	OUT 29
29 IN	BVP1_LINE_IN_N<1>	E16	P1_LI1-	P1_LO1-	E13	BVP1_LINE_OUT_N<1>	OUT 29
29 IN	BVP1_LINE_IN_P<0>	G15	P1_LI0+	P1_LO0+	G12	BVP1_LINE_OUT_P<0>	OUT 29
29 IN	BVP1_LINE_IN_N<0>	G16	P1_LI0-	P1_LO0-	G13	BVP1_LINE_OUT_N<0>	OUT 29

PACK_IGNORE=TRUE

CLK/CONFIG/SMI/I2C

29 IN	BV_CLK_IN_P	C1_RT9 0.01UF	BV_CLK_IN_AC_P	T8	CLK+		
29 IN	BV_CLK_IN_N	C2_RT9 0.01UF	BV_CLK_IN_AC_N	T9	CLK-		
				A8	CLK2+		
				A9	CLK2-		
95 94 IN	VDDO_P2V5	R2_RT9 100	CONFIG_IO_PULLUP	B7	CONFIG_IO		
		R9_RT9 100	EEPROM_LOAD_EN	D10	EEPROM_LOAD_EN		
29 IN	BV_PHY_ADDR4			N9	PHYAD4		
29 IN	BV_PHY_ADDR3			P8	PHYAD3		
29 IN	BV_PHY_ADDR2			P7	PHYAD2		
29 IN	BV_PHY_ADDR1			R7	PHYAD1		
29 IN	BV_RESET_L			P9	RESET		
		R3_RT9 1K		(NC) R10	SEL_2X		
29 IO	BV_SDC_MDC			C9	MDC		
29 IO	BV_SDC_MDIO			C10	MDIO		

					SCL	N10	R11_RT9 100 VDDO_P2V5 IN 94 95
							BV_SCL IO 29
					SDA	P10	BV_SDA IO 29
							R12_RT9 100 VDDO_P2V5 IN 94 95

PACK_IGNORE=TRUE

JTAG

29 IN	BV_TDI	B9	TDI				
29 IN	BV_TMS	B10	TMS				
29 IN	BV_TCK	D7	TCK				
29 IN	BV_TRST_L	D8	TRST				
					INT	T10	BV_INT_L OUT 29
					TP	F7	BV_TP VIA TP1_RT9
					TDO	B8	BV_TDO OUT 29

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BEARVALLEY
15-104658-01

PHYAD PINS HAVE AN INTERNAL 29
PULL DOWN RESISTORS AT LIST 29 20KOHMS

BEARVALLEY-1

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:25 2021		94 OF 138

WAS: 24-100474-01 (4.8A, 0.02 OHM, 1212)

ADDCOMP=700-26993-01

U1_RT9

POWER & TEST

95 IN AVDD_P1V0

36-0212-01 L3_RT9

56 100MHZ 10A, 0.004OHM, 1612

FLTR_BV_AVDDH

C60_RT9 150UF 4V, C79_RT9 22UF 6.3V, C61_RT9 22UF, C41_RT9 0.1UF, C47_RT9 0.1UF, C19_RT9 0.1UF, C38_RT9 0.1UF, C44_RT9 0.1UF, C50_RT9 0.1UF, C23_RT9 0.1UF, C62_RT9 0.1UF, C63_RT9 0.1UF, C64_RT9 0.1UF, C65_RT9 0.1UF, C73_RT9 0.1UF, C75_RT9 0.1UF, C77_RT9 0.1UF

N6 AVDD28, N3 AVDD27, L6 AVDD26, L3 AVDD25, J6 AVDD24, J3 AVDD23, G6 AVDD22, G3 AVDD21, E6 AVDD20, E3 AVDD19, C6 AVDD18, C3 AVDD17, A6 AVDD16, A3 AVDD15

95 IN AVDD_P1V0

36-0212-01 L5_RT9

56 100MHZ 10A, 0.004OHM, 1612

FLTR_BV_AVDDL

C25_RT9 150UF 4V, C80_RT9 22UF 6.3V, C27_RT9 22UF, C16_RT9 0.1UF, C22_RT9 0.1UF, C8_RT9 0.1UF, C15_RT9 0.1UF, C21_RT9 0.1UF, C24_RT9 0.1UF, C13_RT9 0.1UF, C28_RT9 0.1UF, C30_RT9 0.1UF, C31_RT9 0.1UF, C33_RT9 0.1UF, C74_RT9 0.1UF, C76_RT9 0.1UF, C78_RT9 0.1UF

T14 AVDD14, T11 AVDD13, P14 AVDD12, P11 AVDD11, M14 AVDD10, M11 AVDD9, K14 AVDD8, K11 AVDD7, H14 AVDD6, H11 AVDD5, F14 AVDD4, F11 AVDD3, D14 AVDD2, D11 AVDD1

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BEARVALLEY 15-104658-01

VDDO_2 D9, VDDO_1 C8

VDDO_P2V5 — IN — 94

C29_RT9 0.1UF, C35_RT9 0.1UF, C90_RT9 22UF

TEST1 N7 — TP2_RT9 19RD

DVDD16 N8, DVDD15 M9, DVDD14 M7, DVDD13 L10, DVDD12 L8, DVDD11 K9, DVDD10 K7, DVDD9 J10, DVDD8 J8, DVDD7 H9, DVDD6 H7, DVDD5 G10, DVDD4 G8, DVDD3 F9, DVDD2 E10, DVDD1 E8

DVDD_P1V0 — IN — UNIQUE?

C34_RT9 0.1UF, C37_RT9 0.1UF, C40_RT9 0.1UF, C43_RT9 0.1UF, C46_RT9 0.1UF, C49_RT9 0.1UF, C52_RT9 0.1UF, C66_RT9 0.1UF, C68_RT9 0.1UF, C70_RT9 0.1UF, C72_RT9 22UF, C86_RT9 22UF, 22UF 6.3V

C36_RT9 0.1UF, C39_RT9 0.1UF, C42_RT9 0.1UF, C45_RT9 0.1UF, C48_RT9 0.1UF, C51_RT9 0.1UF, C59_RT9 0.1UF, C67_RT9 0.1UF, C69_RT9 0.1UF, C71_RT9 22UF, C85_RT9 22UF, 22UF 6.3V

ADDCOMP=700-26993-01

U1_RT9

GROUND

M10 VSS17, M8 VSS16, L9 VSS15, L7 VSS14, K10 VSS13, K8 VSS12, J9 VSS11, J7 VSS10, H10 VSS9, H8 VSS8, G9 VSS7, G7 VSS6, F10 VSS5, F8 VSS4, E9 VSS3, E7 VSS2, C7 VSS1

T16 AVSS105, T15 AVSS104, T13 AVSS103, T12 AVSS102, T7 AVSS101, T4 AVSS100, T1 AVSS99, R14 AVSS98, R11 AVSS97, R9 AVSS96, R8 AVSS95, R6 AVSS94, R5 AVSS93, R4 AVSS92, R3 AVSS91, R2 AVSS90, R1 AVSS89, P16 AVSS88, P15 AVSS87, P13 AVSS86, P12 AVSS85, P6 AVSS84, P3 AVSS83, N14 AVSS82, N11 AVSS81, N5 AVSS80, N4 AVSS79, N2 AVSS78, N1 AVSS77, M16 AVSS76, M15 AVSS75, M13 AVSS74, M12 AVSS73, M6 AVSS72, M3 AVSS71, L14 AVSS70, L11 AVSS69, L5 AVSS68, L4 AVSS67, L2 AVSS66, L1 AVSS65, K16 AVSS64, K15 AVSS63

AVSS62 K13, AVSS61 K12, AVSS60 K6, AVSS59 K3, AVSS58 J14, AVSS57 J11, AVSS56 J5, AVSS55 J4, AVSS54 J2, AVSS53 J1, AVSS52 H16, AVSS51 H15, AVSS50 H13, AVSS49 H12, AVSS48 H6, AVSS47 H3, AVSS46 G14, AVSS45 G11, AVSS44 G5, AVSS43 G4, AVSS42 G2, AVSS41 G1, AVSS40 F16, AVSS39 F15, AVSS38 F13, AVSS37 F12, AVSS36 F6, AVSS35 F3, AVSS34 E14, AVSS33 E11, AVSS32 E5, AVSS31 E4, AVSS30 E2, AVSS29 E1, AVSS28 D16, AVSS27 D15, AVSS26 D13, AVSS25 D12, AVSS24 D6, AVSS23 D3, AVSS22 C14, AVSS21 C11, AVSS20 C5, AVSS19 C4, AVSS18 C2, AVSS17 C1, AVSS16 B16, AVSS15 B15, AVSS14 B14, AVSS13 B13, AVSS12 B12, AVSS11 B11, AVSS10 B6, AVSS9 B3, AVSS8 A16, AVSS7 A13, AVSS6 A10, AVSS5 A7, AVSS4 A5, AVSS3 A4, AVSS2 A2, AVSS1 A1

3/3

BEARVALLEY 15-104658-01

BEARVALLEY-2

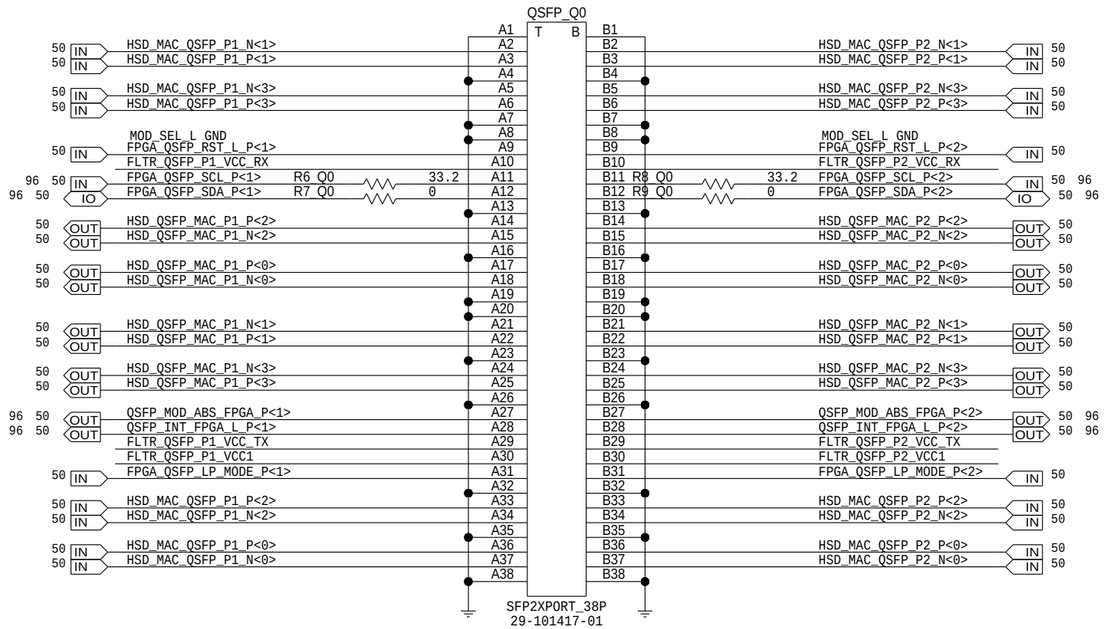
CISCO

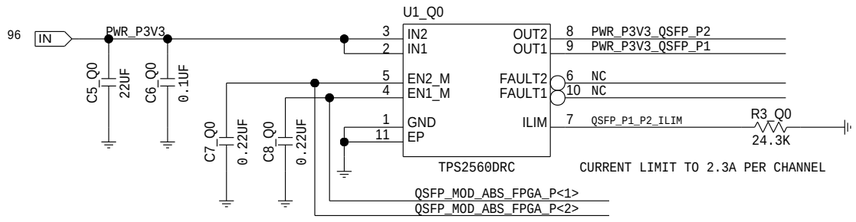
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:25 2021		95 OF 138

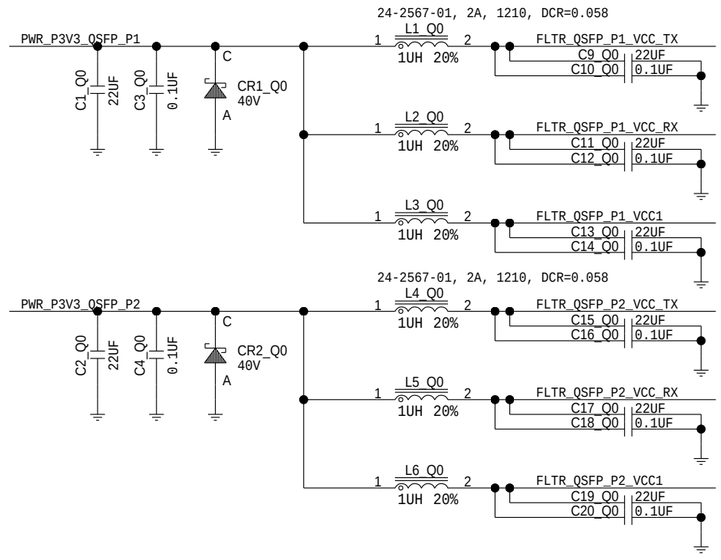
PROG_NUM=29-101417-01

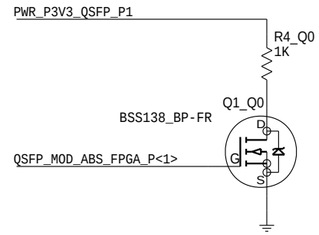
2X1 QSFP W/O RE-TIMER SUBDESIGN 01

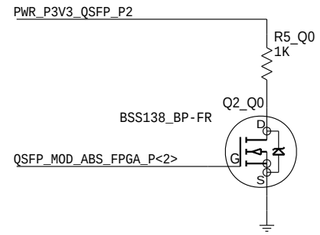
CHANGE LOG:
05/23/2016: COPY FROM QSFP_2X1_DUAL_LED_PWR
CHANGED QSFP CONNECTOR TO "REVC" VERSION
CONDENCED SUBDESIGN TO 1 PAGE
05/2017: ADDED DUAL FOOTPRINT TO USE BELLEVUE B2B CONNECTORS
06/2017: CHANGED SHORT PROTECTION TO SOFTSTART UPON INSERTION
07/2017: ADD SRT FOR I2C



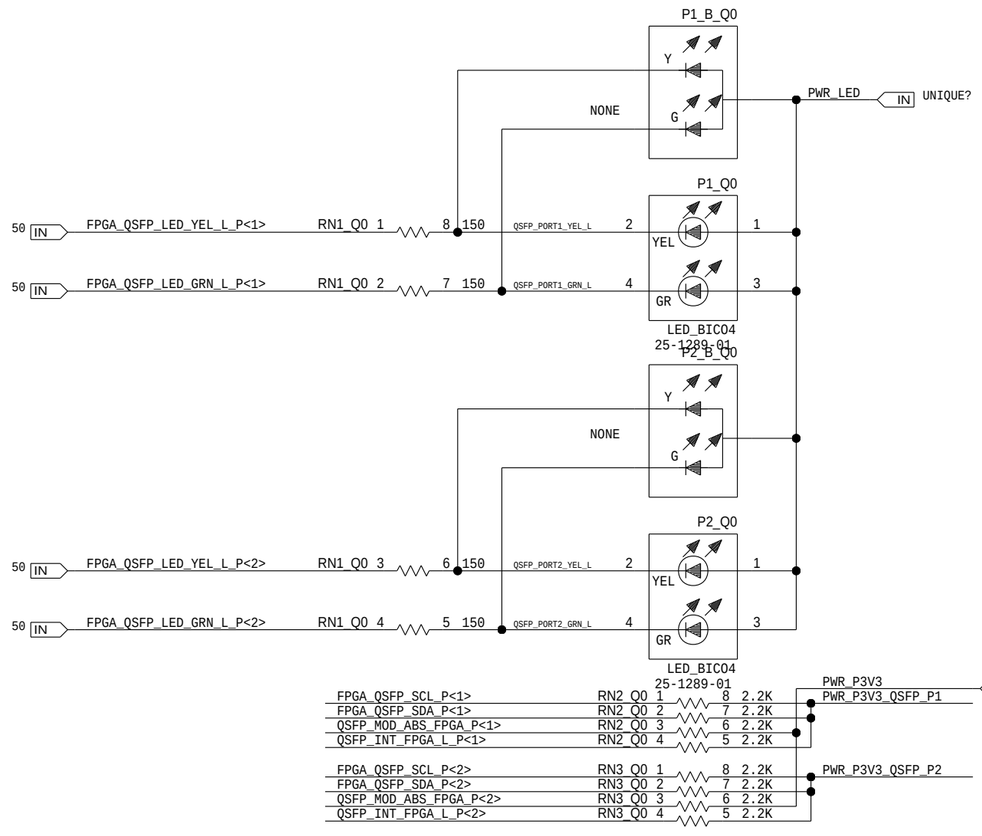








TOP LEDS STUFFED



QSFP PORT 1-2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Nov 5 15:07:38 2021		96 OF 138

PROG_NUM=29-101417-01

2X1 QSFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:
05/23/2016: COPY FROM QSFP_2X1_DUAL_LED_PWR
CHANGED QSFP CONNECTOR TO "REVC" VERSION
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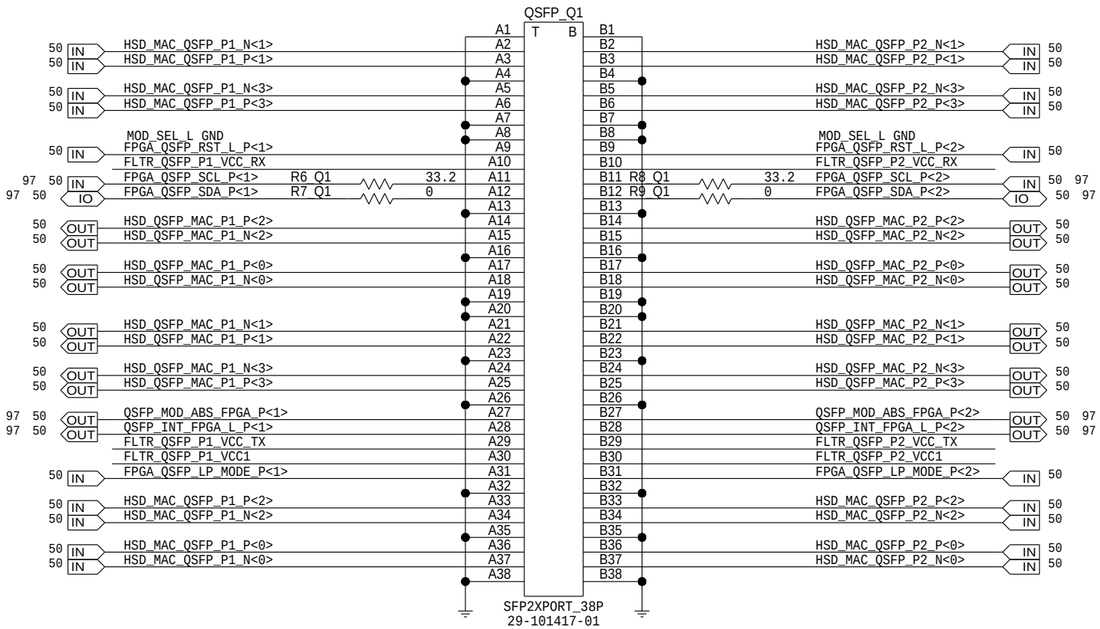
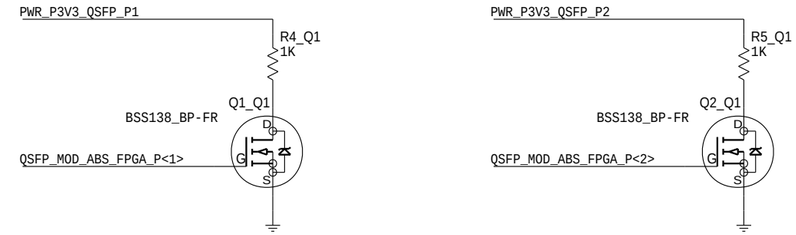
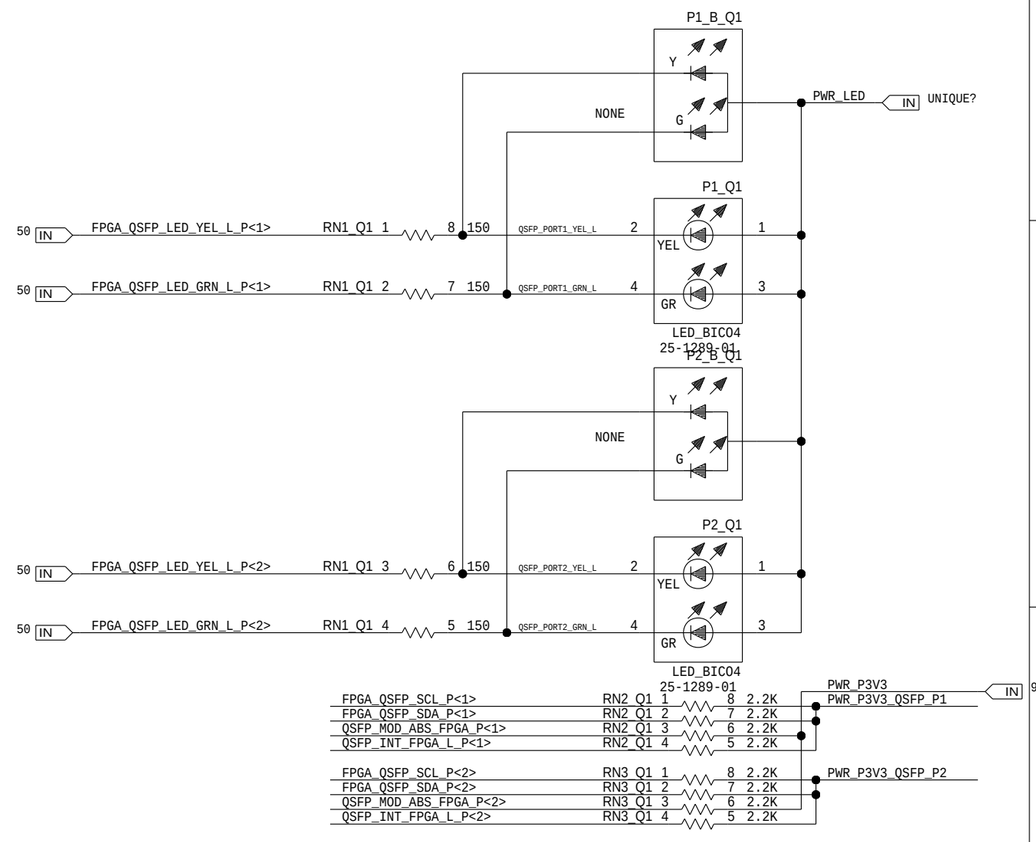
07/2017: ADD SRT FOR I2C





TOP LEDS STUFFED



QSFP PORT 1-2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Nov 5 15:07:38 2021		97 OF 138

PROG_NUM=29-101417-01

2X1 QSFP W/O RE-TIMER SUBDESIGN 01

CHANGE LOG:
05/23/2016: COPY FROM QSFP_2X1_DUAL_LED_PWR
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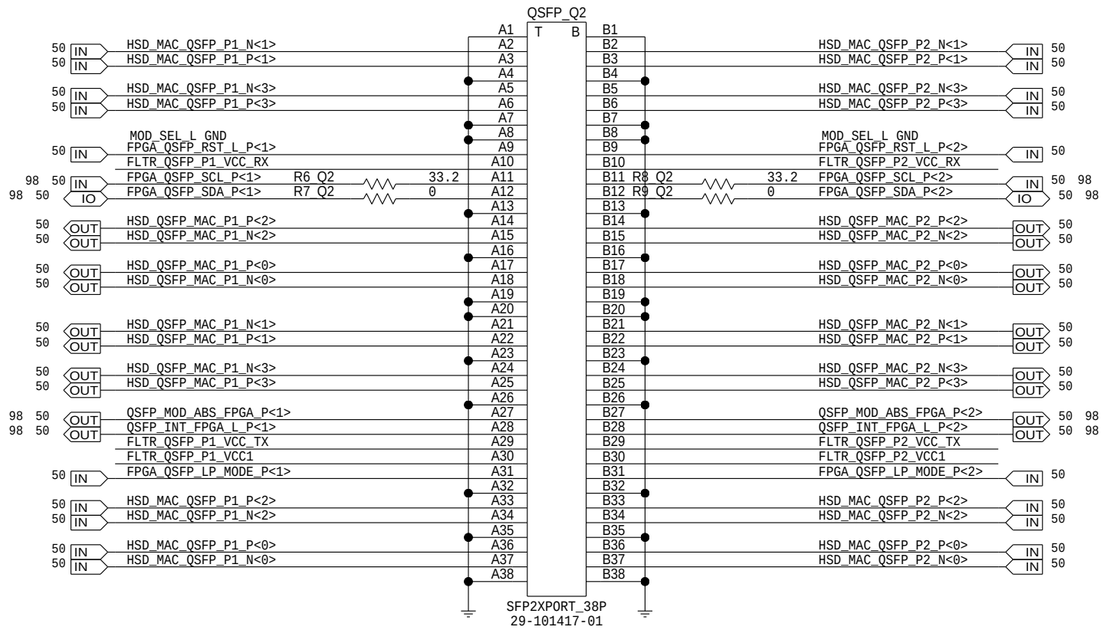
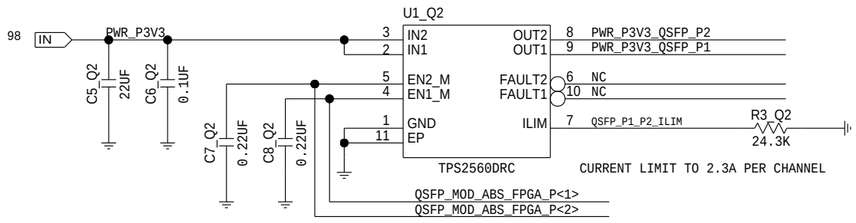
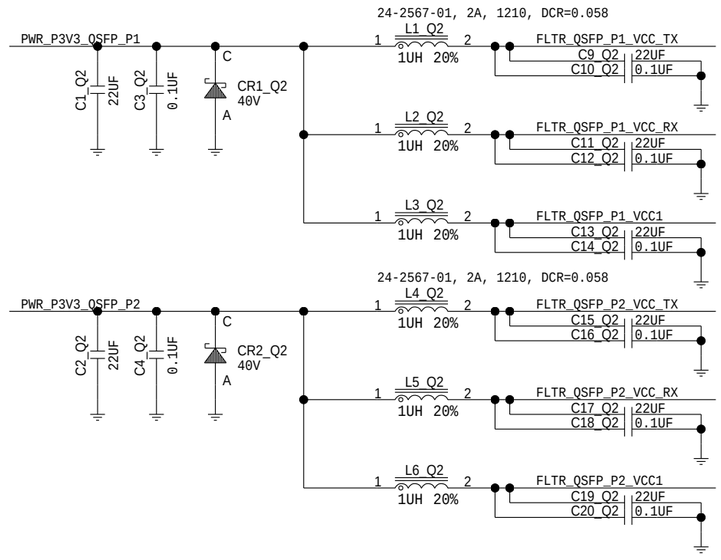
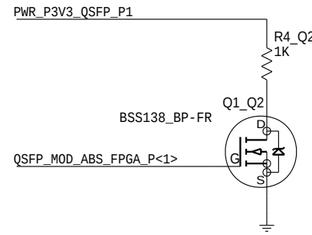
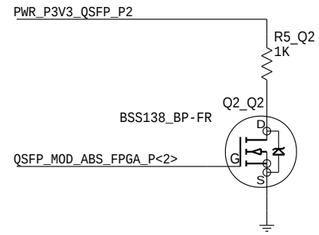


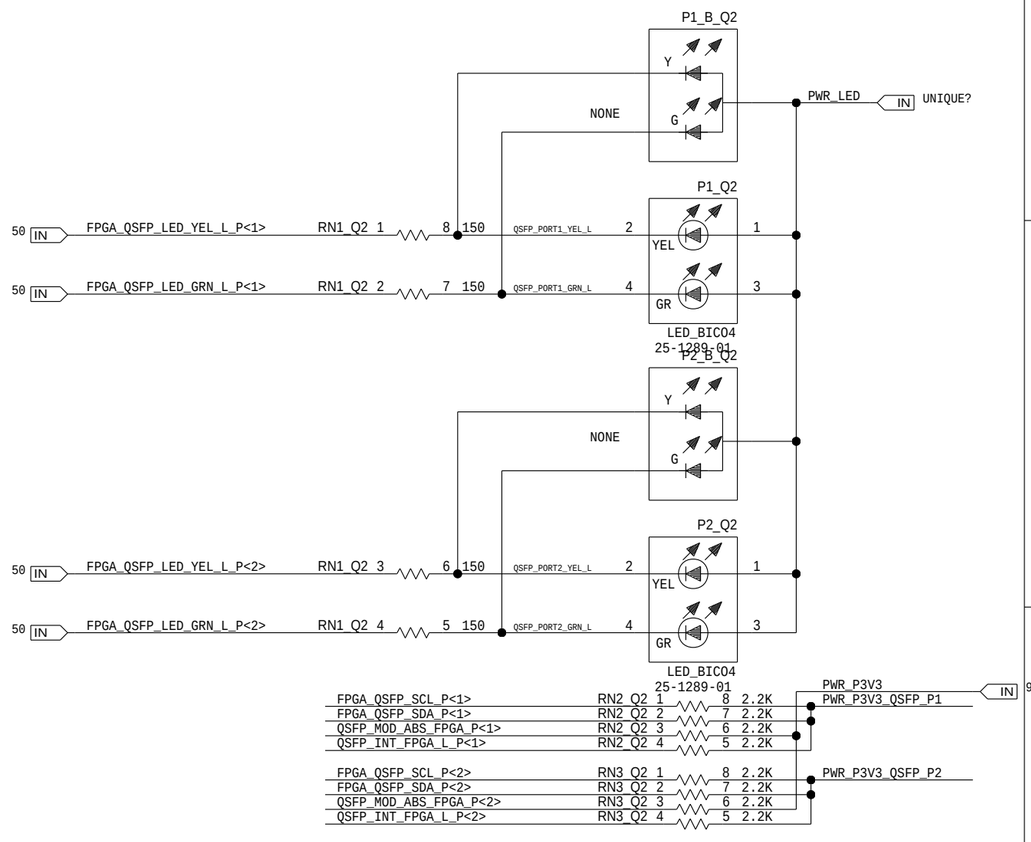








TOP LEDS STUFFED



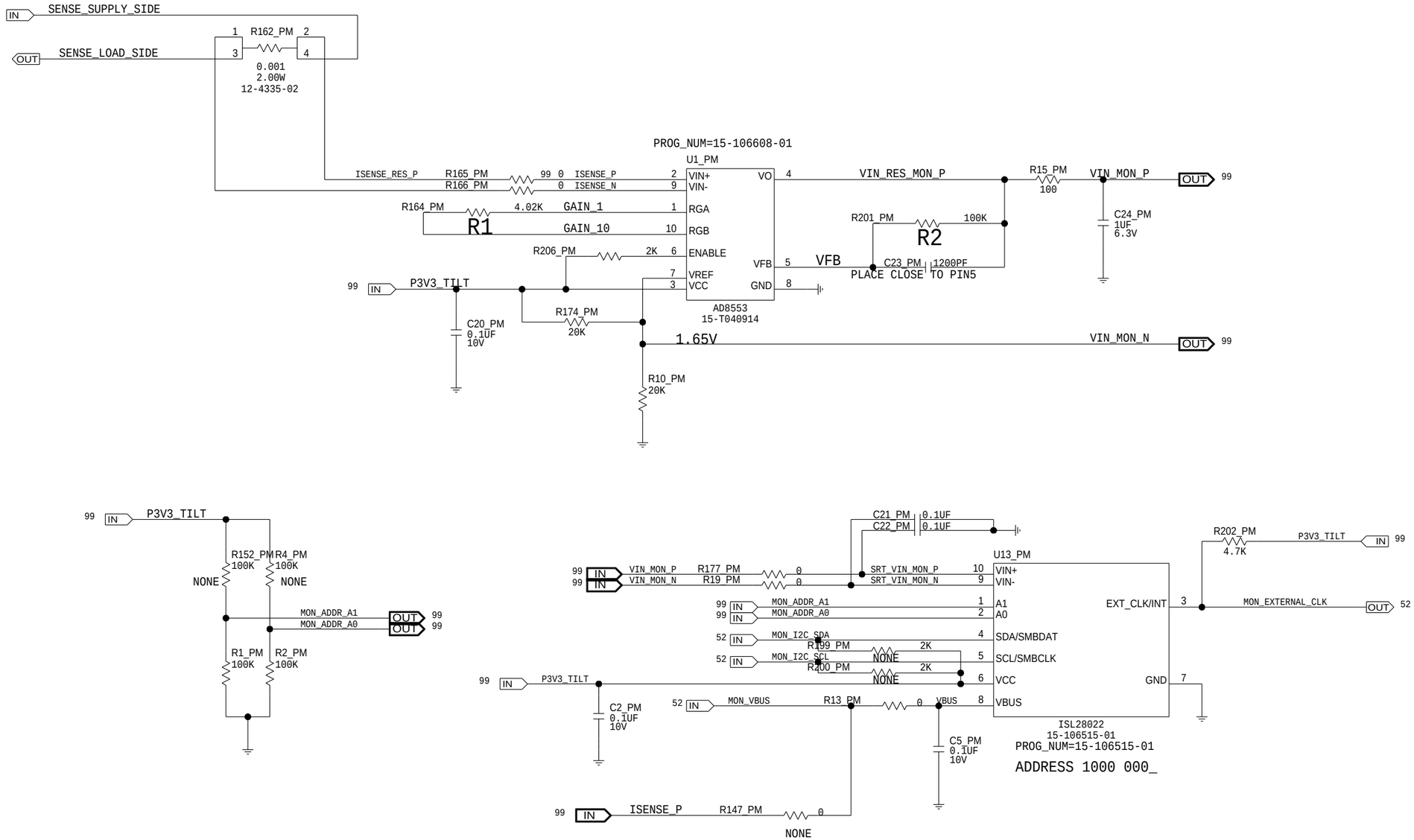
QSFP PORT 1-2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Nov 5 15:07:38 2021		98 OF 138

DWG NO	SHT	REV
92-105229-01	138	A0

REVISION

REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD



QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± DECIM .xx ±.01 .xxx±.005 ANGLES ±1°

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION | DO NOT SCALE DWG

APPROVALS	DATE
DRAWN BY ?	
CAD ?	
MECH ?	
ENGR ?	
MFG ?	
TEST ?	

CISCO

TITLE:

SIZE	CLASS CODE	DWG. NO.	REV
B			A0

SCALE | DATE: | 99 OF 138

DWG NO	SHT	REV
92-105229-01	138	A0

REVISION

REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD

CYCLONE 5
FPGA AUX VOLTAGE RAILS
REV 01

3.3V: 15A (TPS53915)
2.5V: 3A (1 PHASE TPS54394)
1.1V: 3A (1 PHASE TPS54394)

CHANGE HISTORY:

REV01: COPY FROM CY5_9A_3A_3A REV 03 SUBDESIGN. NOT FOOTPRINT COMPATIBLE

QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± DECIM .xx +.01 -.xxx+.005 ANGLES ±1 °

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DWG

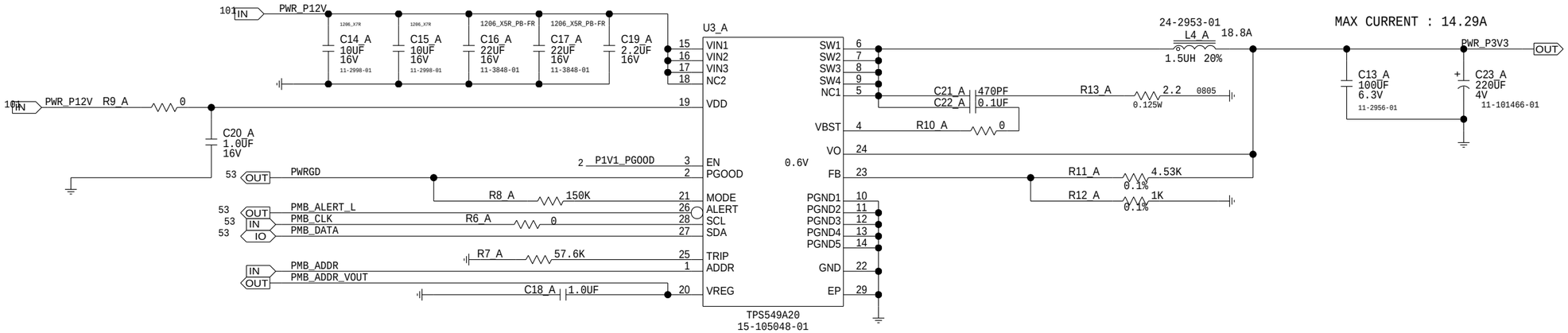
APPROVALS	DATE
DRAWN BY ?	
CAD ?	
MECH ?	
ENGR ?	
MFG ?	
TEST ?	

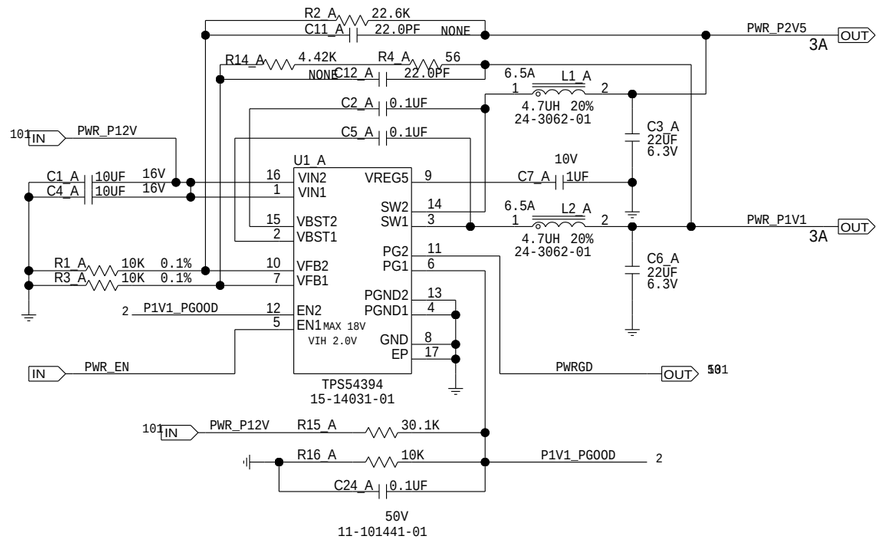
CISCO

TITLE:

SIZE	CLASS CODE	DWG. NO.	REV
B	———		A0

SCALE | DATE: | 100 OF 138





CONTROLLER

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Nov 4 15:26:21 2021		101 OF 138

DWG NO	SHT	REV
92-105229-01	138	A0

REVISION

REV	ECO	DESCRIPTION	APPROVALS DFTG	CHK	APVD

SUNDOWN1 MIN FW1201 SUBDESIGN REV01

01:BASED ON SUNDOWN1 SUBDESIGN REV06, WITH NEW CPN MIN FW1201.

TITLE PAGE

QTY REQD		PART OR IDENTYFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION	

UNLESS OTHERVISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTION ± DECIM .xx ±.01 .xxx±.005 ANGLES ±1°

MATERIAL

FINISH

DO NOT SCALE DWG

APPROVALS	DATE
DRAWN BY BEYENE LULSEGED	
CAD ?	
MECH ?	
ENGR BEYENE LULSEGED	
MFG ?	
TEST ?	

NEXT ASSY	USED ON
APPLICATION	

CISCO

TITLE:

SIZE	CLASS CODE	DWG. NO.	REV
B	—		A0

SCALE | DATE: | 102 OF 138

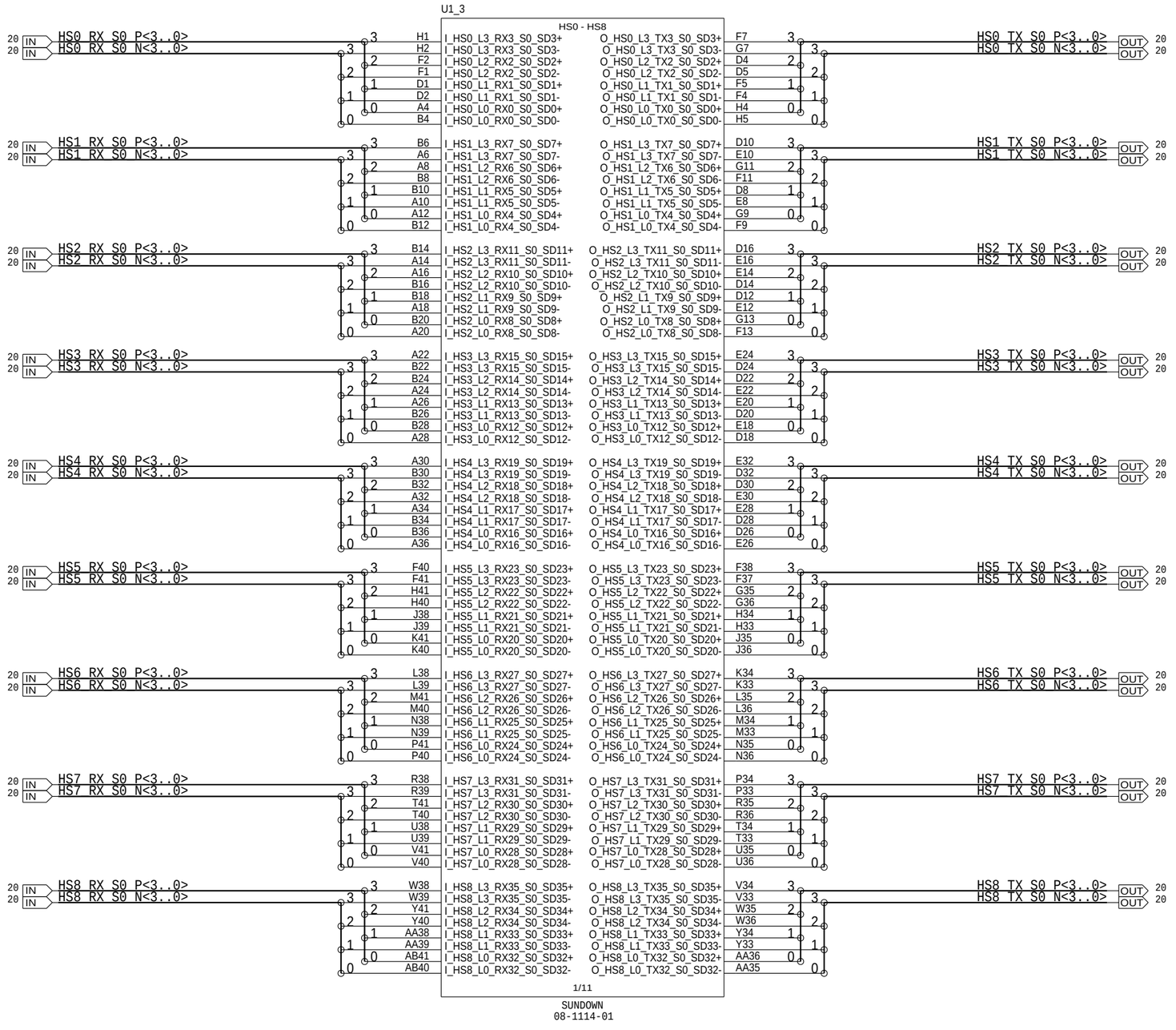
TABLE OF CONTENTS	
1	TITLE PAGE
3	SNDN_HS0_TO_HS8 _N S0
4	SNDN_HS9_TO_HS17 _N S0
5	SNDN PCIE_CLK_JTAG_MISC
6	SNDN STRAP OPTIONS
7	SNDN VDDA / VDDHA
8	SNDN VDD / VDDIO
9	SNDN GND
10	SNDN DECAP 1
11	SNDN DECAP 2

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Tue Mar 26 21:44:36 2019		103 OF 138

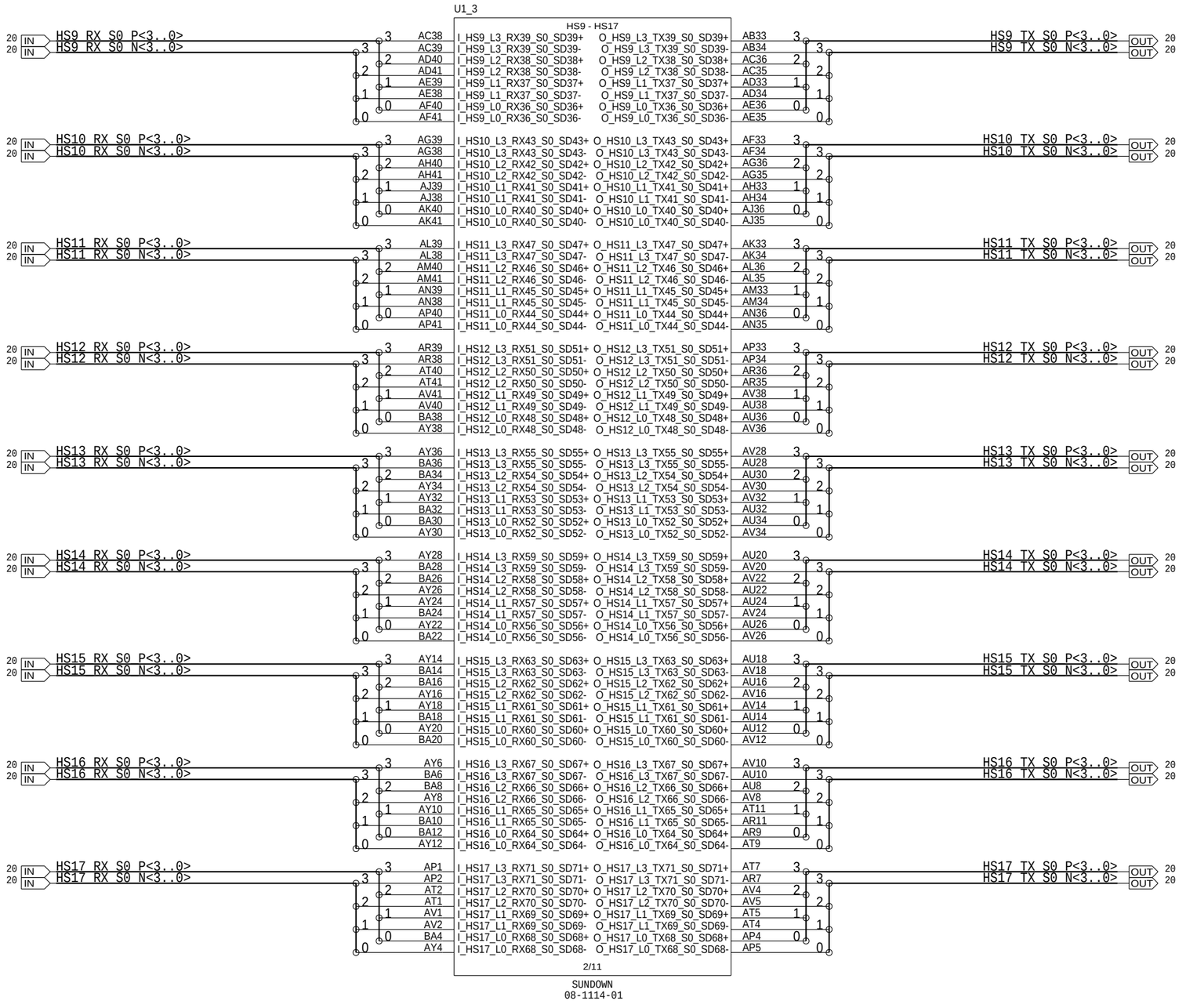
PROG_NUM=08-1199-01 MIN FW 1201

ADDCOMP=700-105818-01; 700-104727-01



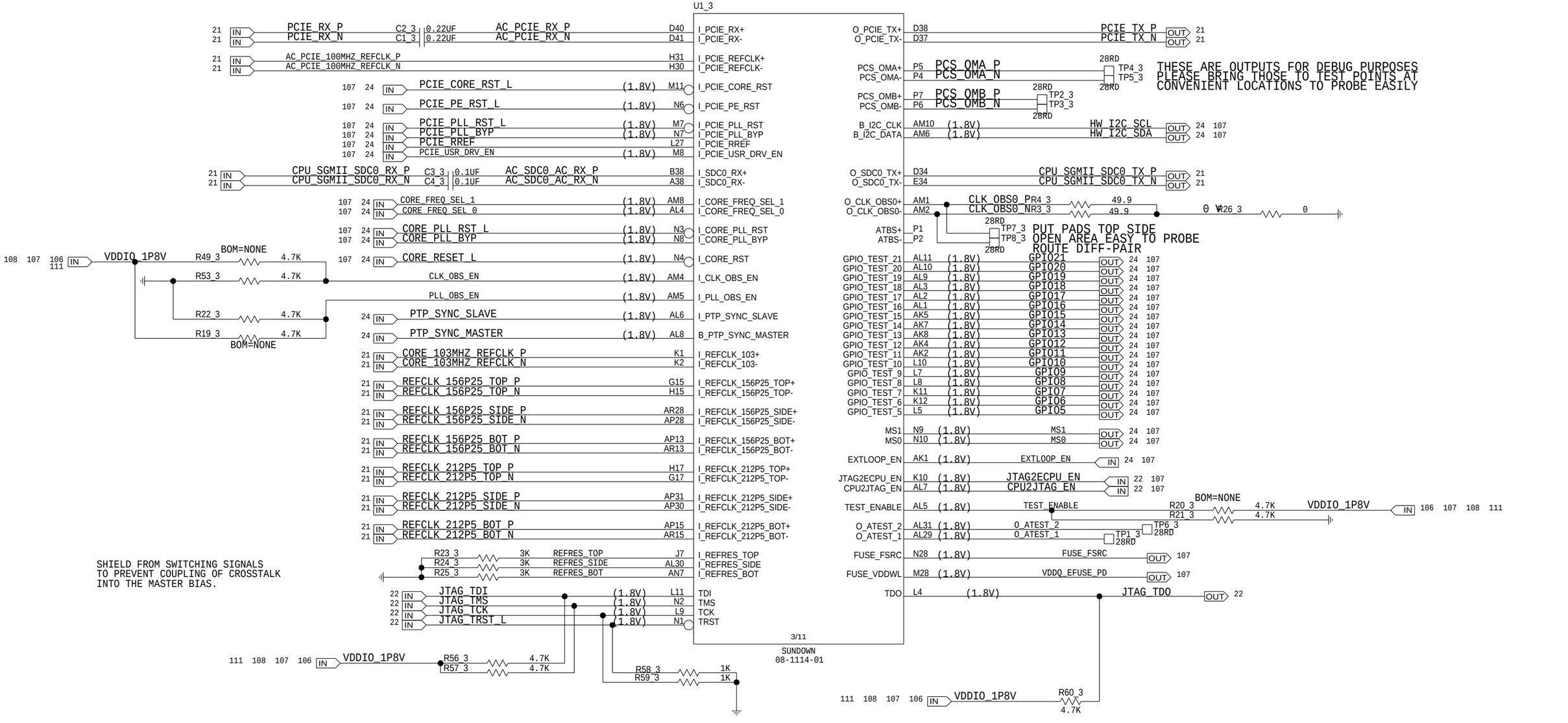
SNDN_HS0_TO_HS8 _N S0

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Mar 25 10:31:20 2022		104 OF 138



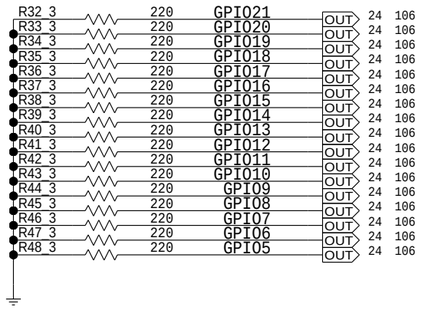
SNDN_HS9_TO_HS17 _N S0

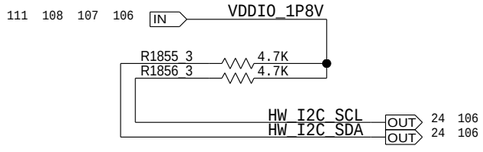
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:50 2022		105 OF 138

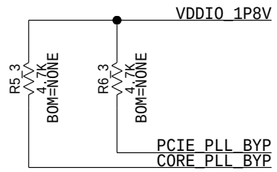


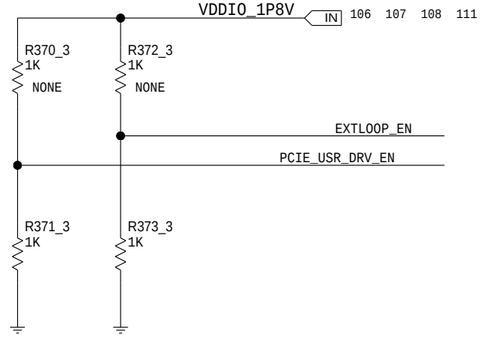
SNDN PCIE_CLK_JTAG_MISC

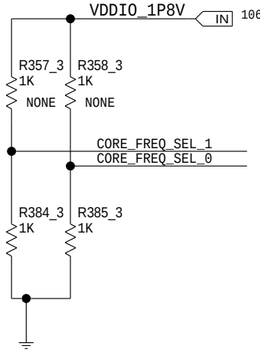
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE		DATE: Thu Mar 24 15:00:50 2022	106 OF 138

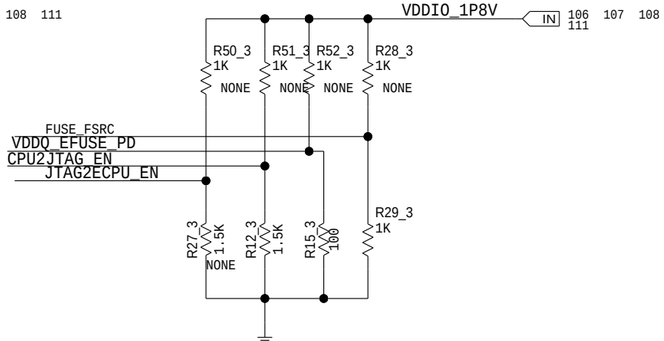


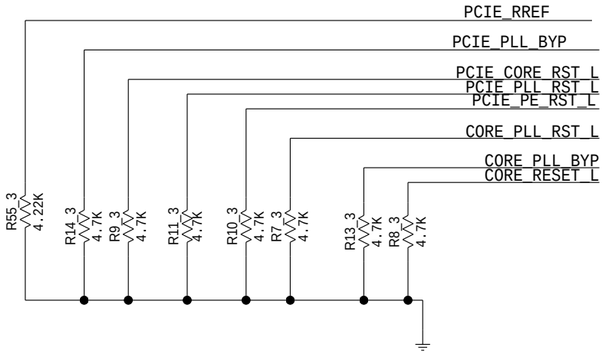


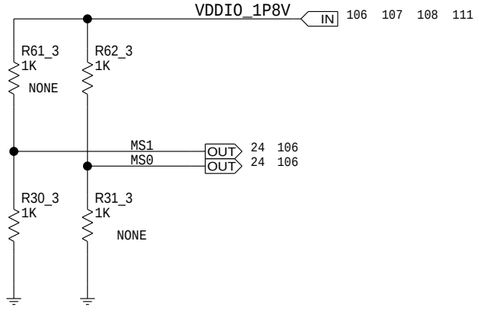












SNDN STRAP OPTIONS

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:50 2022		107 OF 138

FILTER GROUPINMG PER BGA PIN LOCATION

USE BLM03HB191SN1

U1_3

GROUND 1 OF 5

L29	VSSA_PLL_PCIE	VSSA496	AY35
		VSSA495	AY33
K14	VSSA_PLL_CORE	VSSA494	AY31
		VSSA493	AY29
V28	VSSA_PLL_SIDE_TEST2	VSSA492	AY27
AB28	VSSA_PLL_SIDE_TEST1	VSSA491	AY25
		VSSA490	AY23
K20	VSSA_PLL_TOP_FC	VSSA489	AY21
Y28	VSSA_PLL_SIDE_FC	VSSA488	AY19
AM16	VSSA_PLL_BOT_FC	VSSA487	AY17
		VSSA486	AY15
L13	VSSA_PLL_TOP_MM	VSSA485	AY13
AD28	VSSA_PLL_SIDE_MM	VSSA484	AY11
AM24	VSSA_PLL_BOT_MM	VSSA483	AY9
		VSSA482	AY7
		VSSA481	AY5
BA41	VSSA523	VSSA480	AY3
BA40	VSSA522	VSSA479	AY2
BA39	VSSA521	VSSA478	AY1
BA37	VSSA520	VSSA477	AW41
BA35	VSSA519	VSSA476	AW40
BA33	VSSA518	VSSA475	AW38
BA31	VSSA517	VSSA474	AW36
BA29	VSSA516	VSSA473	AW34
BA27	VSSA515	VSSA472	AW32
BA25	VSSA514	VSSA471	AW30
BA23	VSSA513	VSSA470	AW28
BA21	VSSA512	VSSA469	AW26
BA19	VSSA511	VSSA468	AW24
BA17	VSSA510	VSSA467	AW22
BA15	VSSA509	VSSA466	AW20
BA13	VSSA508	VSSA465	AW18
BA11	VSSA507	VSSA464	AW16
BA9	VSSA506	VSSA463	AW14
BA7	VSSA505	VSSA462	AW12
BA5	VSSA504	VSSA461	AW10
BA3	VSSA503	VSSA460	AW8
BA2	VSSA502	VSSA459	AW6
BA1	VSSA501	VSSA458	AW5
AY41	VSSA500	VSSA457	AW4
AY40	VSSA499	VSSA456	AW2
AY39	VSSA498	VSSA455	AW1
AY37	VSSA497	VSSA454	AV39

7/11

SUNDOWN

08-1114-01

R1_3 NONE 0 FLTR_PLLGND1P8V

R2_3 NONE 0 FLTR_PLLGNDCORE

R16_3 NONE 0 FLTR_PLLGNDTEST

R17_3 NONE 0 FLTR_PLLGND_FC

IN VDDA_PLL_1P8V — L1_3 26OHMS 100MHZ — FLTR_PLL_PCIE_TOP

L2_3 26OHMS 100MHZ — FLTR_PLL_CORE_TOP

L5_3 26OHMS 100MHZ — FLTR_PLL_TEST_SIDE

L7_3 26OHMS 100MHZ — FLTR_FC_MM_BOT

IN VDDA_CLK_0P9V — L4_3 120 100MHZ 36-100166-01 — FLTR_VDDA_CLK_0P9V

L28_3 120 100MHZ 36-100166-01

IN VDDA_TX_0P9V — L3_3 120 100MHZ 36-100166-01 — FLTR_VDDA_TX_0P9V

L26_3 120 100MHZ 36-100166-01

U1_3

POWER 1 OF 3

L28	VDDA_PLL_PCIE	VDDHA_17	AR26
		VDDHA_16	AR20
K13	VDDA_PLL_CORE	VDDHA_15	AR17
		VDDHA_14	AN14
W28	VDDA_PLL_SIDE_TEST2	VDDHA_13	AN9
AB27	VDDA_PLL_SIDE_TEST1	VDDHA_12	AM31
		VDDHA_11	AH31
K21	VDDA_PLL_TOP_FC	VDDHA_10	AB31
AA28	VDDA_PLL_SIDE_FC	VDDHA_9	Y31
AM17	VDDA_PLL_BOT_FC	VDDHA_8	T31
		VDDHA_7	M31
L14	VDDA_PLL_TOP_MM	VDDHA_6	K31
AC28	VDDA_PLL_SIDE_MM	VDDHA_5	J11
AM23	VDDA_PLL_BOT_MM	VDDHA_4	J9
		VDDHA_3	G24
		VDDHA_2	G20
		VDDHA_1	G16
AT25	VDDA_CLK34		
AT21	VDDA_CLK33		
AT17	VDDA_CLK32		
AR24	VDDA_CLK31		
AR22	VDDA_CLK30		
AR18	VDDA_CLK29	VDDHA_VCO_17	AN12
AP21	VDDA_CLK28	VDDHA_VCO_16	AN16
AP19	VDDA_CLK27	VDDHA_VCO_15	AP17
AP10	VDDA_CLK26	VDDHA_VCO_14	AP23
AN32	VDDA_CLK25	VDDHA_VCO_13	AP25
AN29	VDDA_CLK24	VDDHA_VCO_12	AJ30
AN11	VDDA_CLK23	VDDHA_VCO_11	AG30
AK31	VDDA_CLK22	VDDHA_VCO_10	AE30
AG32	VDDA_CLK21	VDDHA_VCO_9	AC29
AF31	VDDA_CLK20	VDDHA_VCO_8	AA29
AD31	VDDA_CLK19	VDDHA_VCO_7	U30
AC30	VDDA_CLK18	VDDHA_VCO_6	R30
AA32	VDDA_CLK17	VDDHA_VCO_5	L30
AA30	VDDA_CLK16	VDDHA_VCO_4	H25
W30	VDDA_CLK15	VDDHA_VCO_3	H23
V31	VDDA_CLK14	VDDHA_VCO_2	J21
R32	VDDA_CLK13	VDDHA_VCO_1	H19
P31	VDDA_CLK12	VDDHA_VCO_0	J13
N30	VDDA_CLK11		
L32	VDDA_CLK10		
J18	VDDA_CLK9		
J14	VDDA_CLK8	PCIE_VDDA_4	J29
H27	VDDA_CLK7	PCIE_VDDA_3	G32
H21	VDDA_CLK6	PCIE_VDDA_2	F33
G26	VDDA_CLK5	PCIE_VDDA_1	E36
G22	VDDA_CLK4		
G18	VDDA_CLK3	PCIE_VDDHA_3	K27
F27	VDDA_CLK2	PCIE_VDDHA_2	J28
F21	VDDA_CLK1	PCIE_VDDHA_1	G28
AN26	VDDA_TX21		
AN24	VDDA_TX20		
AN22	VDDA_TX19		
AN20	VDDA_TX18		
AN18	VDDA_TX17		
AM29	VDDA_TX16	VDDIO1_6	AM9
AK29	VDDA_TX15	VDDIO1_5	AM3
AH29	VDDA_TX14	VDDIO1_4	AL12
AF29	VDDA_TX13	VDDIO1_3	AK9
AD29	VDDA_TX12	VDDIO1_2	AK6
AB29	VDDA_TX11	VDDIO1_1	AK3
Y29	VDDA_TX10		
V29	VDDA_TX9	VDDIO2_6	P3
T29	VDDA_TX8	VDDIO2_5	N5
P29	VDDA_TX7	VDDIO2_4	M9
M29	VDDA_TX6	VDDIO2_3	M3
J26	VDDA_TX5	VDDIO2_2	L6
J24	VDDA_TX4	VDDIO2_1	K9
J22	VDDA_TX3		
J20	VDDA_TX2		
J16	VDDA_TX1		

4/11

SUNDOWN

08-1114-01

FLTR_VDDHA_1P2V — L8_3 120 100MHZ 36-100166-01 — VDDHA_1P2V — IN 108 112 113

L29_3 120 100MHZ 36-100166-01 — IN 22 111 113

VDDA_0P9V — IN 109 111 113

VDDHA_1P2V — IN 108 112 113

VDDIO_1P8V — IN 106 107 111

FLTR_PLL_TEST_SIDE — C702_3 0.47UF 6.3V — C703_3 22UF 6.3V — FLTR_PLLGNDTEST

FLTR_PLL_PCIE_TOP — C704_3 0.47UF 6.3V — C705_3 22UF 6.3V — FLTR_PLLGND1P8V

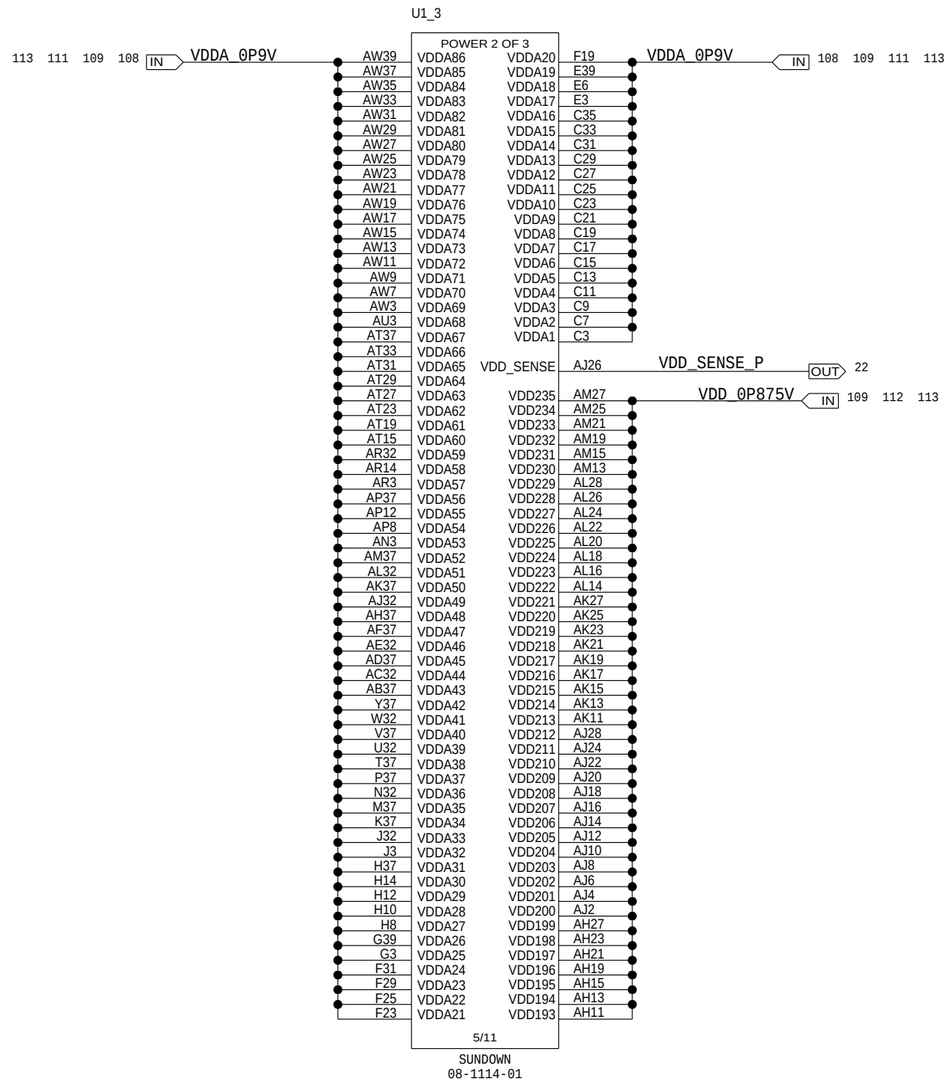
FLTR_FC_MM_BOT — C706_3 0.47UF 6.3V — C707_3 22UF 6.3V — FLTR_PLLGND_FC

FLTR_PLL_CORE_TOP — C708_3 0.47UF 6.3V — C709_3 22UF 6.3V — FLTR_PLLGNDCORE

SNDN VDDA / VDDHA

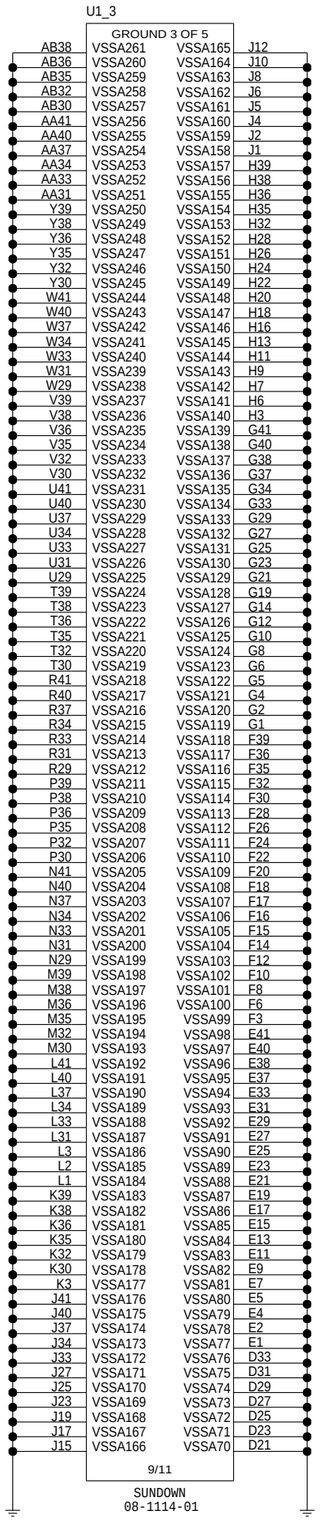
CISCO

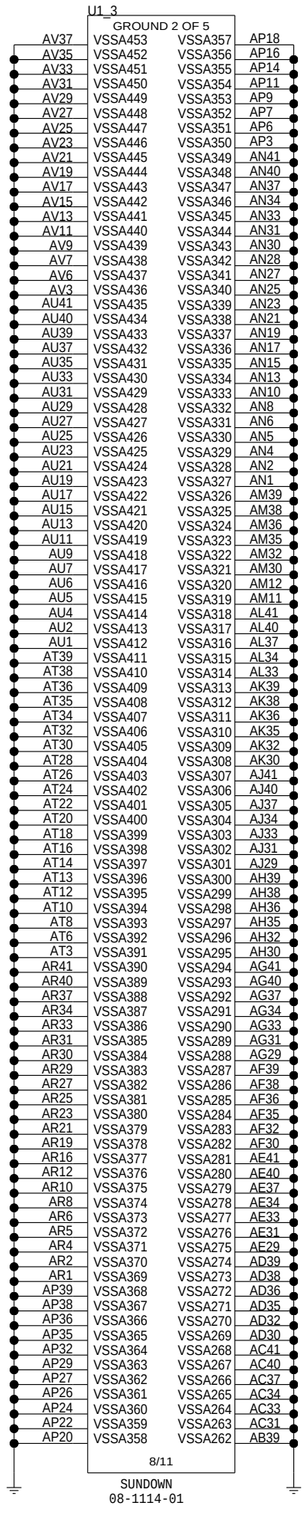
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:50 2022		108 OF 138

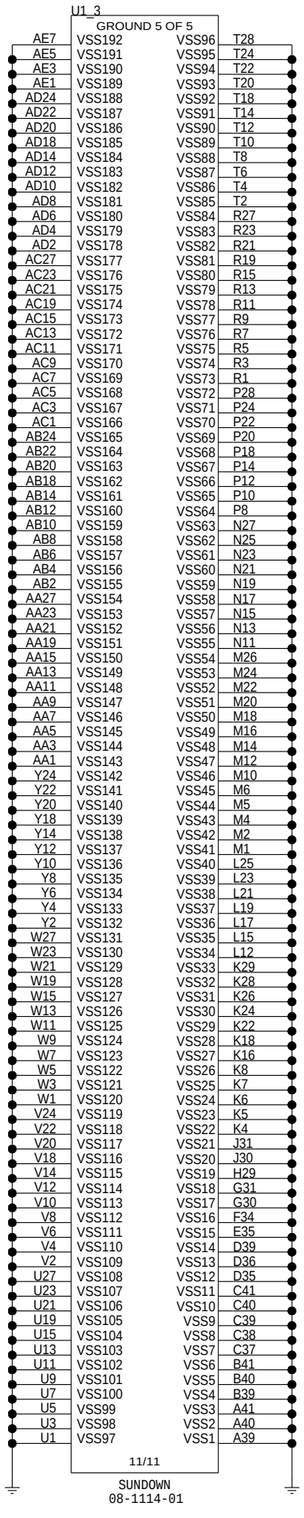


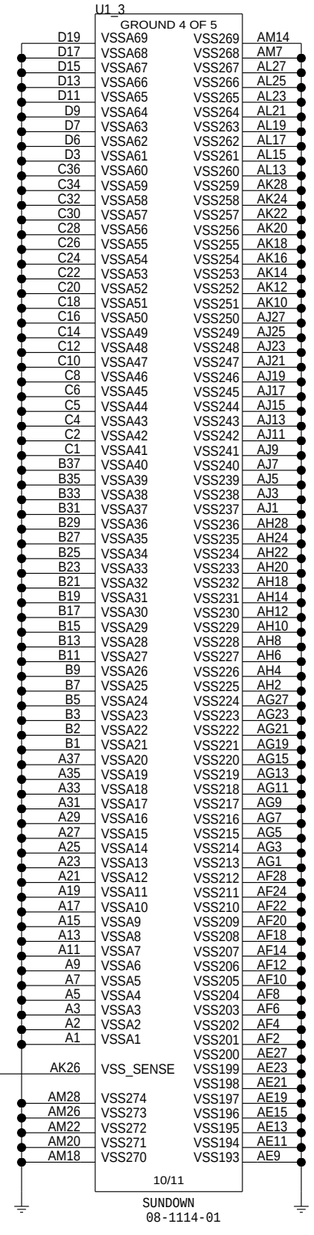
SNDN VDD / VDDIO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Fri Nov 5 16:08:51 2021		109 OF 138



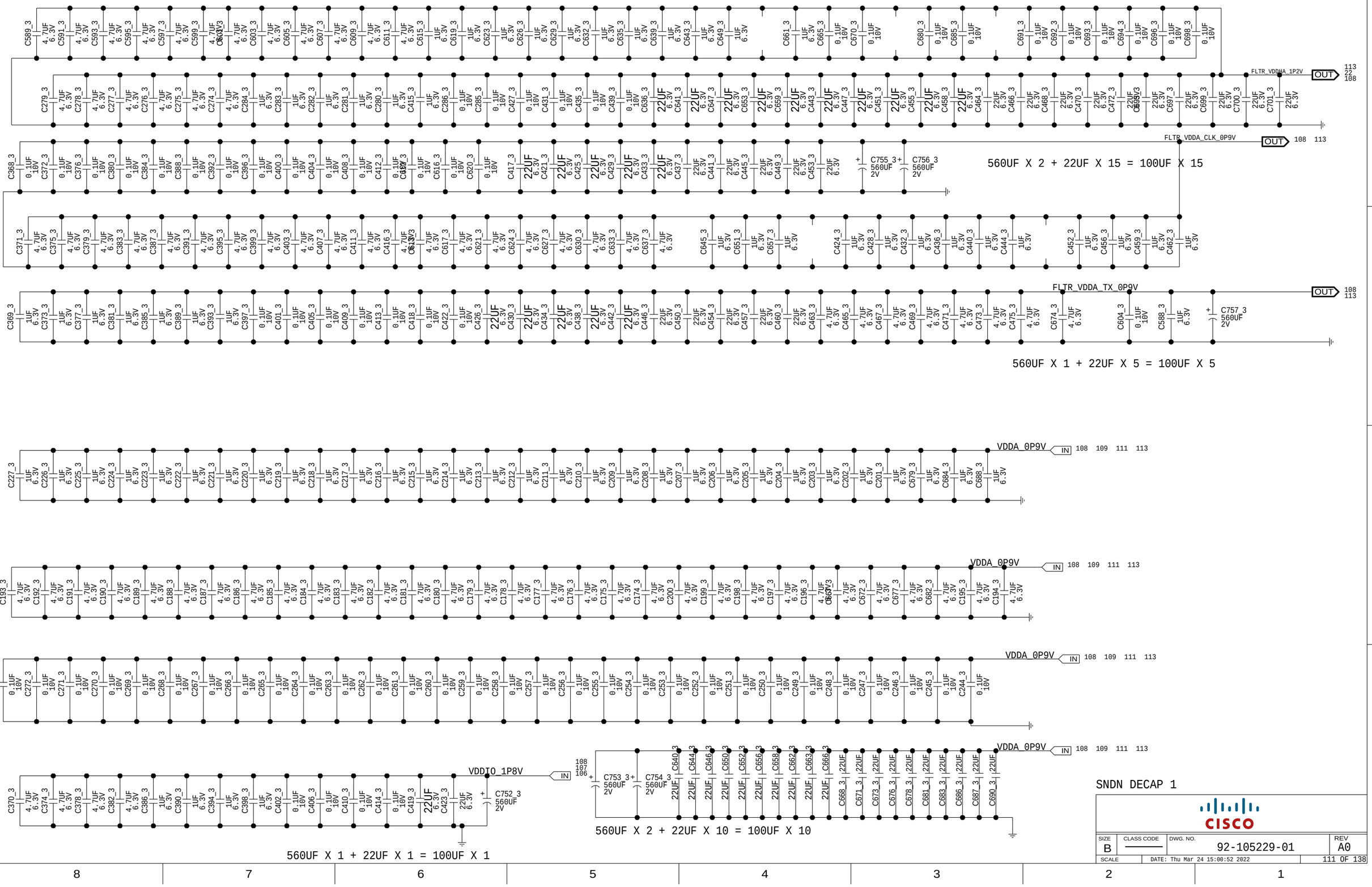




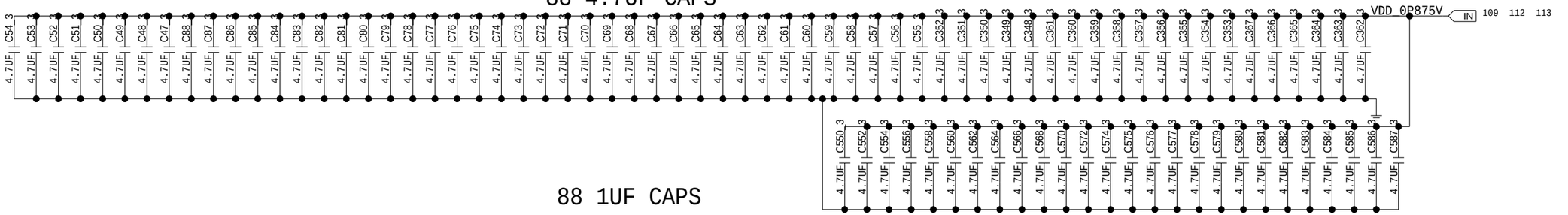


SNDN GND

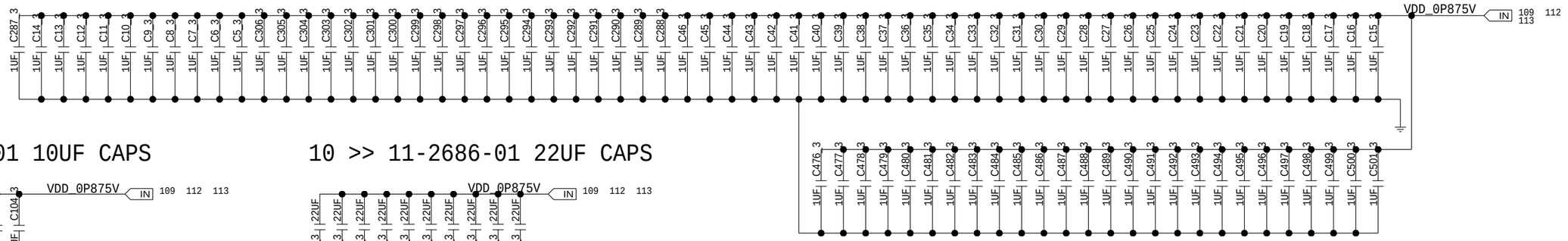
SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:52 2022		110 OF 138


FLTR_VDDHA_1P2V
OUT
113
22
108
FLTR_VDDA_CLK_0P9V
OUT
108 113
560UF X 2 + 22UF X 15 = 100UF X 15
FLTR_VDDA_TX_0P9V
OUT
108
113
560UF X 1 + 22UF X 5 = 100UF X 5
VDDA_0P9V
IN
108 109 111 113
VDDIO_1P8V
IN
560UF X 1 + 22UF X 1 = 100UF X 1
560UF X 2 + 22UF X 10 = 100UF X 10
SNDN DECAP 1
CISCO
SIZE
B
CLASS CODE
DWG. NO.
92-105229-01
REV
A0
SCALE
DATE: Thu Mar 24 15:00:52 2022
111 OF 138

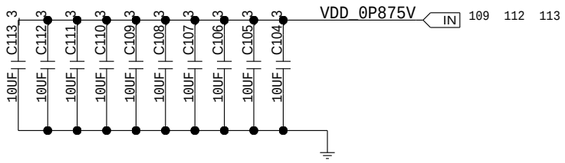
88 4.7UF CAPS



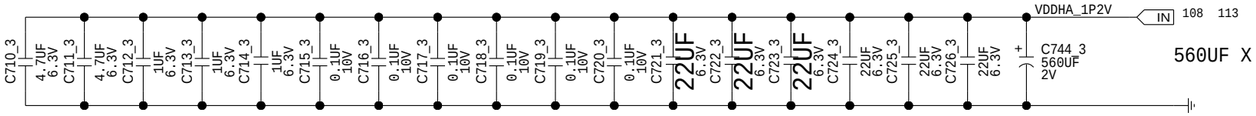
88 1UF CAPS



10 >> 11-3844-01 10UF CAPS



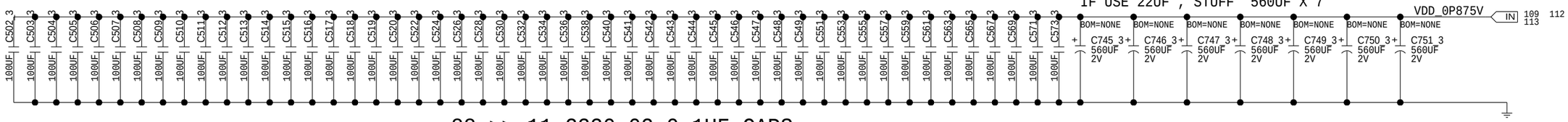
10 >> 11-2686-01 22UF CAPS



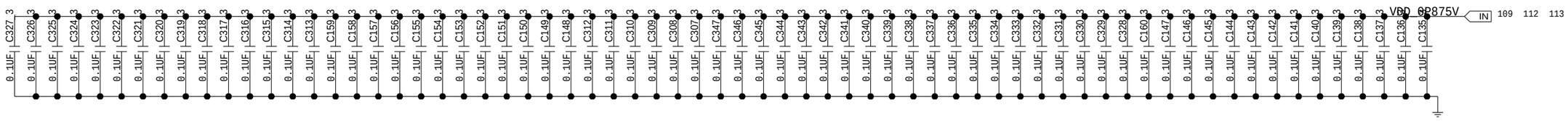
560UF X 1 + 22UF X 3 = 100UF X 3

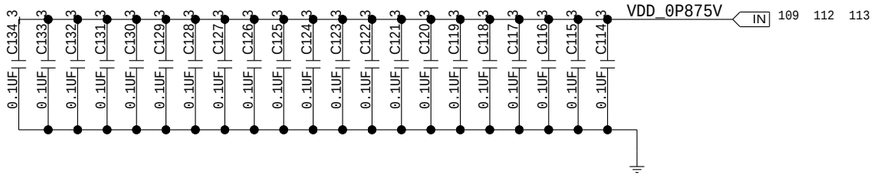
50 >> 11-101311-01 100UF CAPS

560UF X 7 + 22UF X 50 = 100UF X 50
IF USE 22UF , STUFF 560UF X 7



88 >> 11-2330-02 0.1UF CAPS

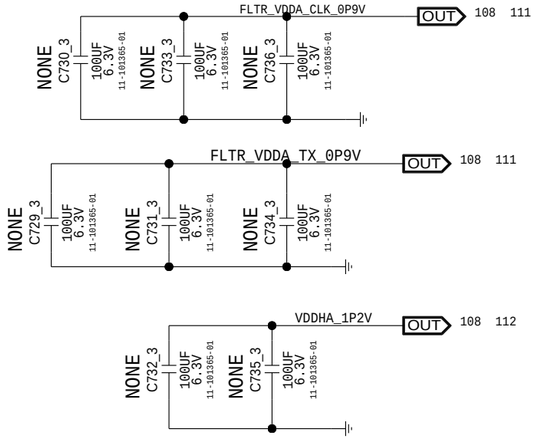


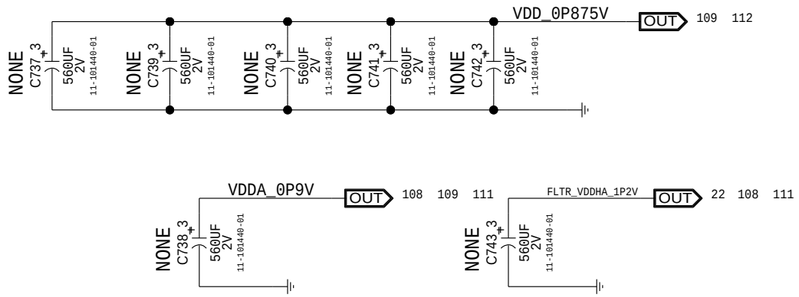


SNDN DECAP 2

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:53 2022		112 OF 138

0805 100UF CAP MIDIGATION ADDITIONS

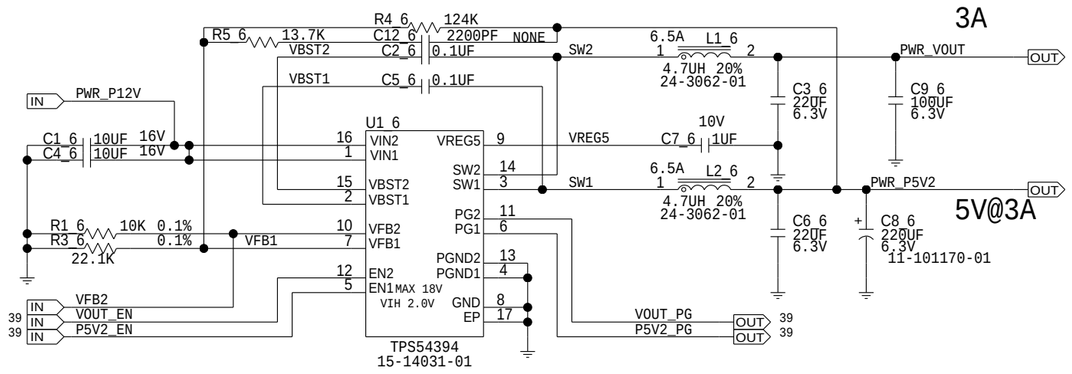




CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B	———	92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:53 2022		113 OF 138

5.2V & VARIABLE VOLTAGE REGULATORS

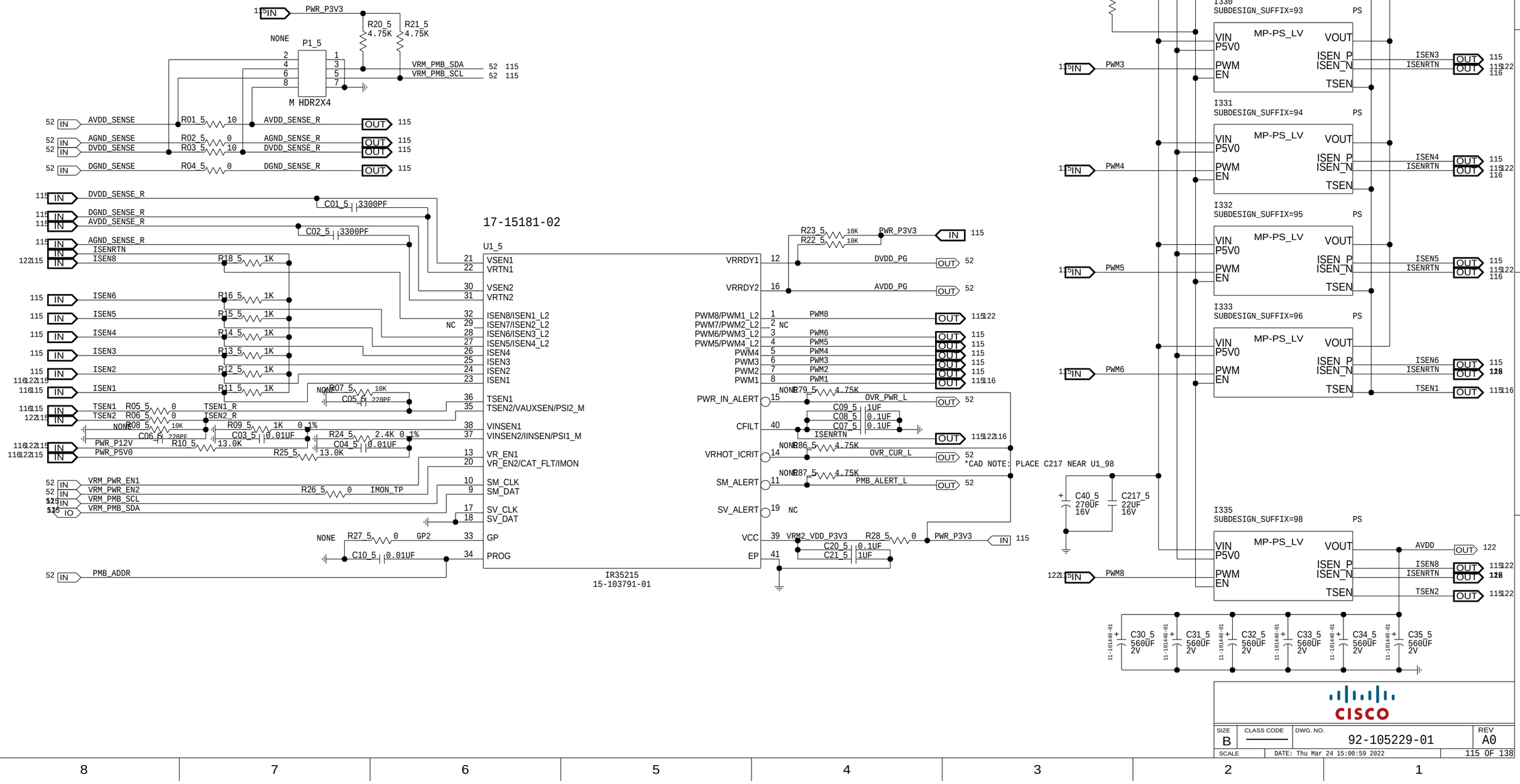


CONTROLLER

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:58 2022		114 OF 138

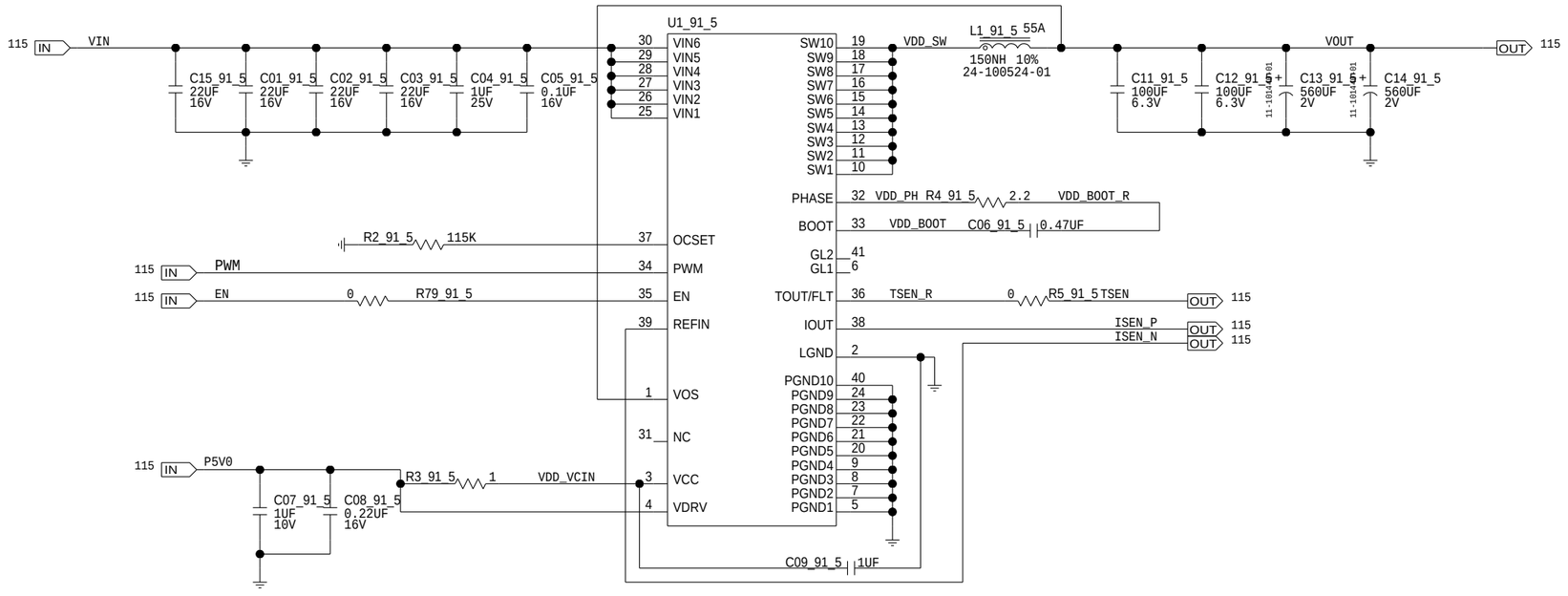
ACADIA MULTI-PHASE 6+1 POWER STAGE MACRO

NOTE:SELECT INFINEON,FAIRCHILD OR TI IN THE VARIANT



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:59 2022		115 OF 138

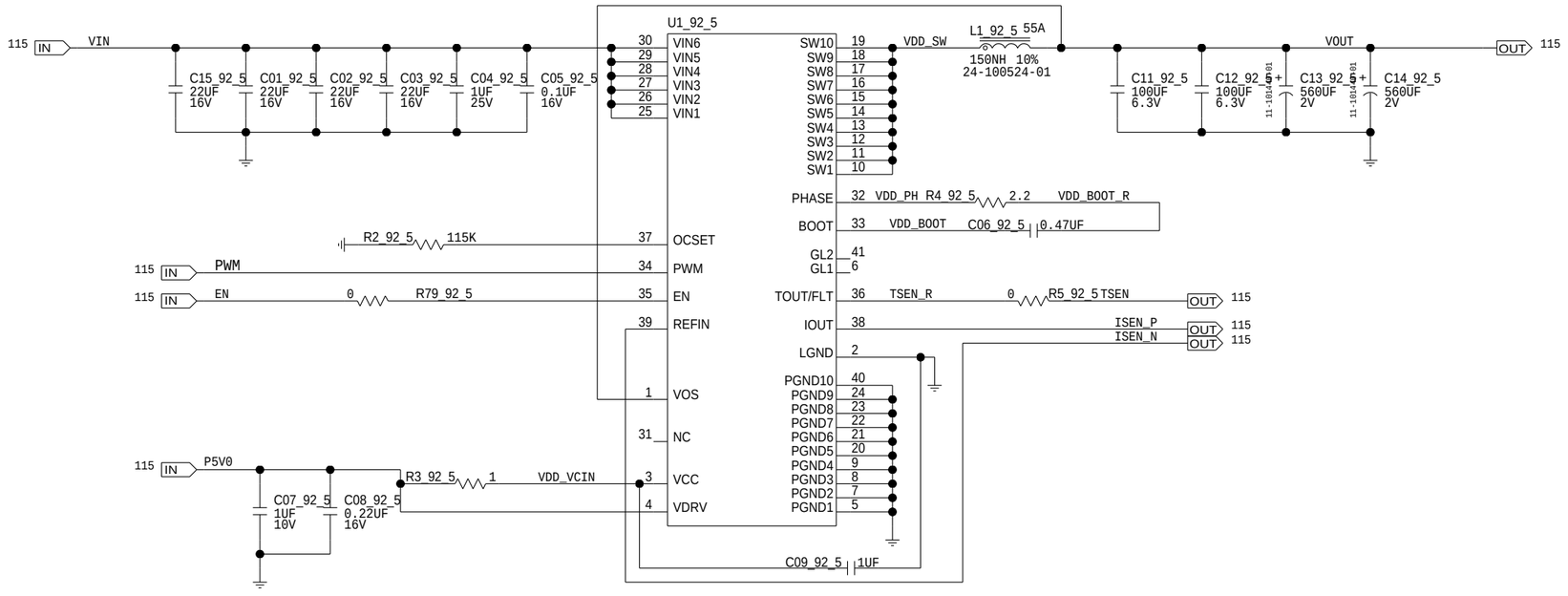
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		116 OF 138

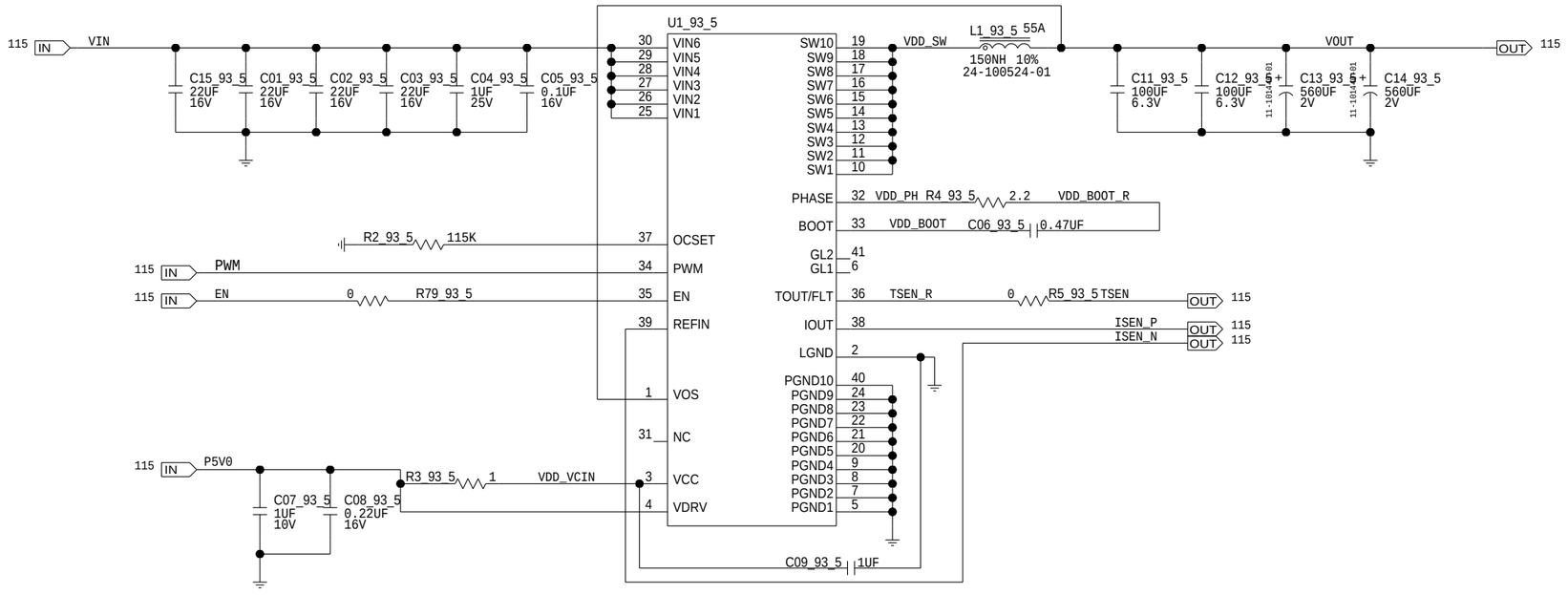
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		117 OF 138

MULTI-PHASE POWER STAGE_LV

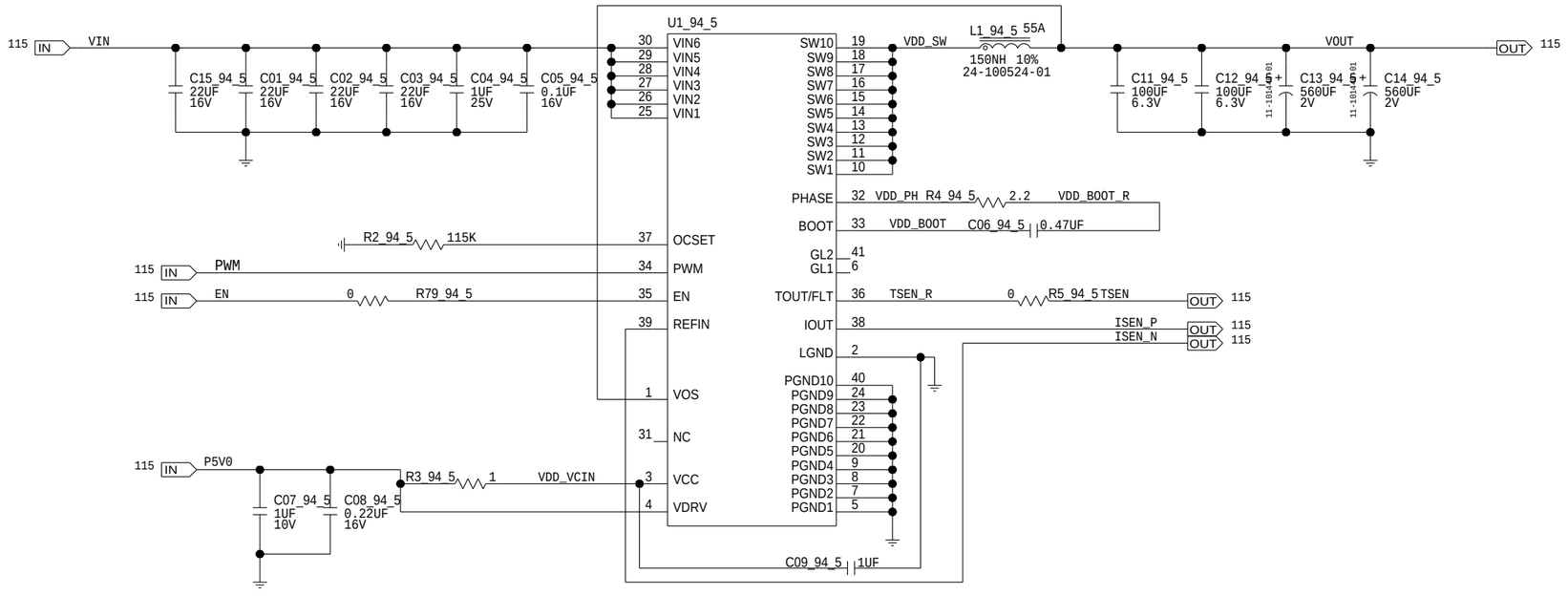


MULTI-PHASE POWER STAGE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		118 OF 138

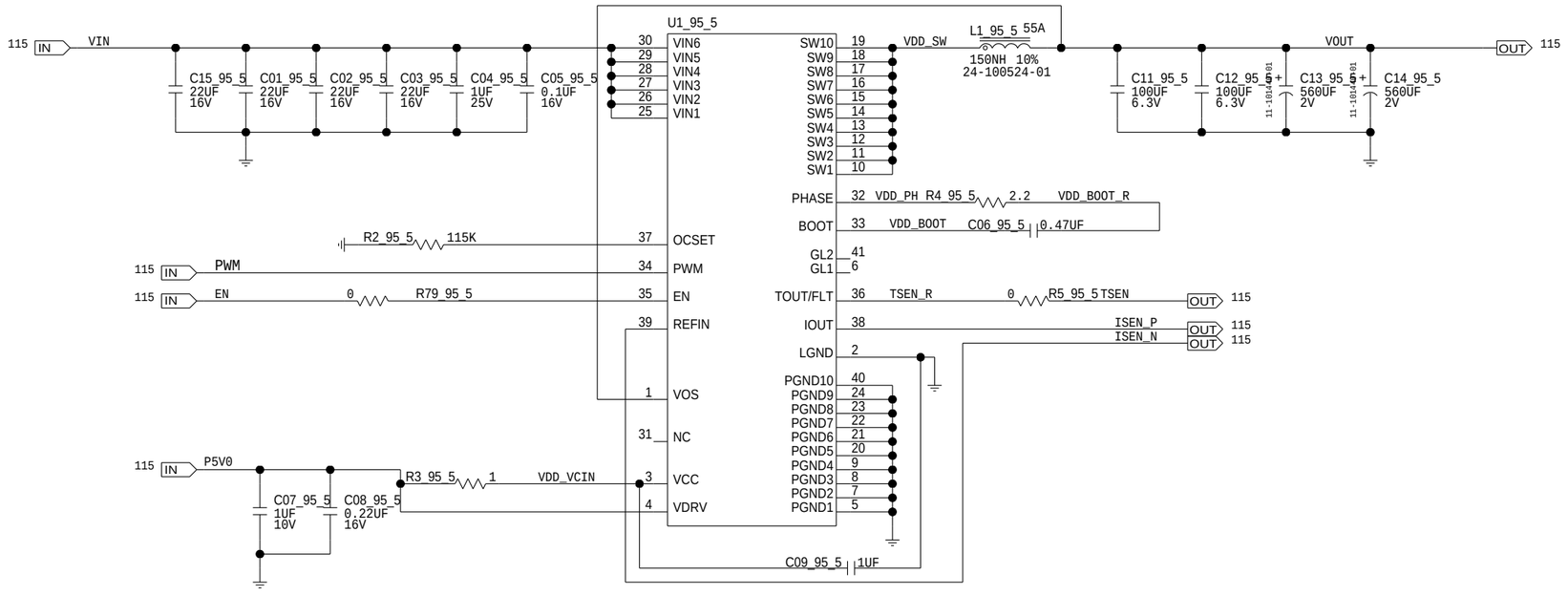
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		119 OF 138

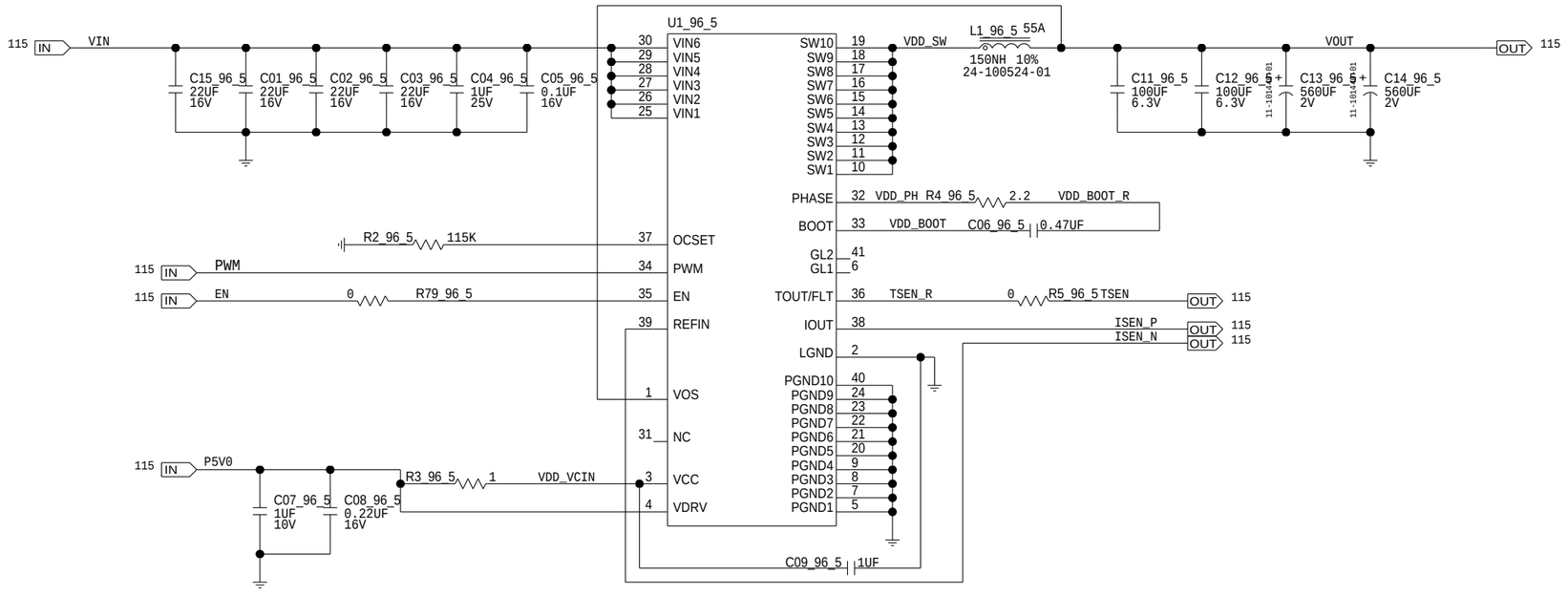
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		120 OF 138

MULTI-PHASE POWER STAGE_LV

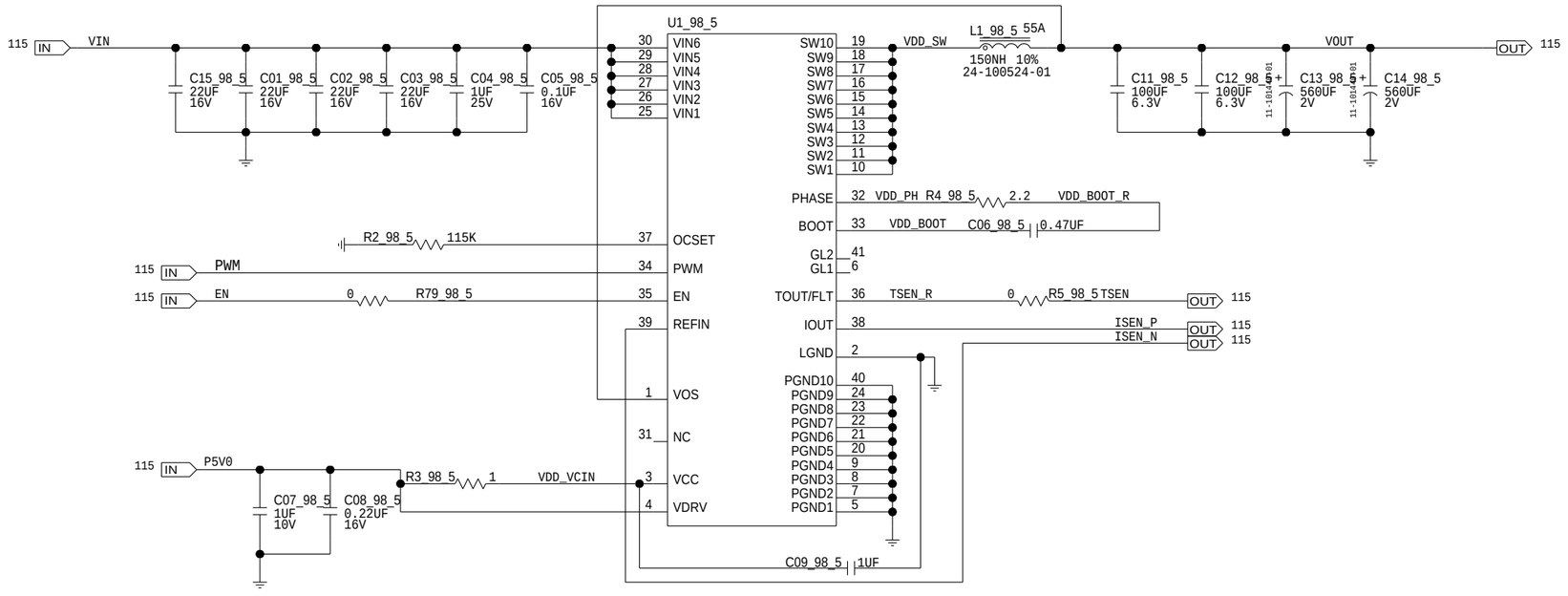


MULTI-PHASE POWER STAGE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		121 OF 138

MULTI-PHASE POWER STAGE_LV



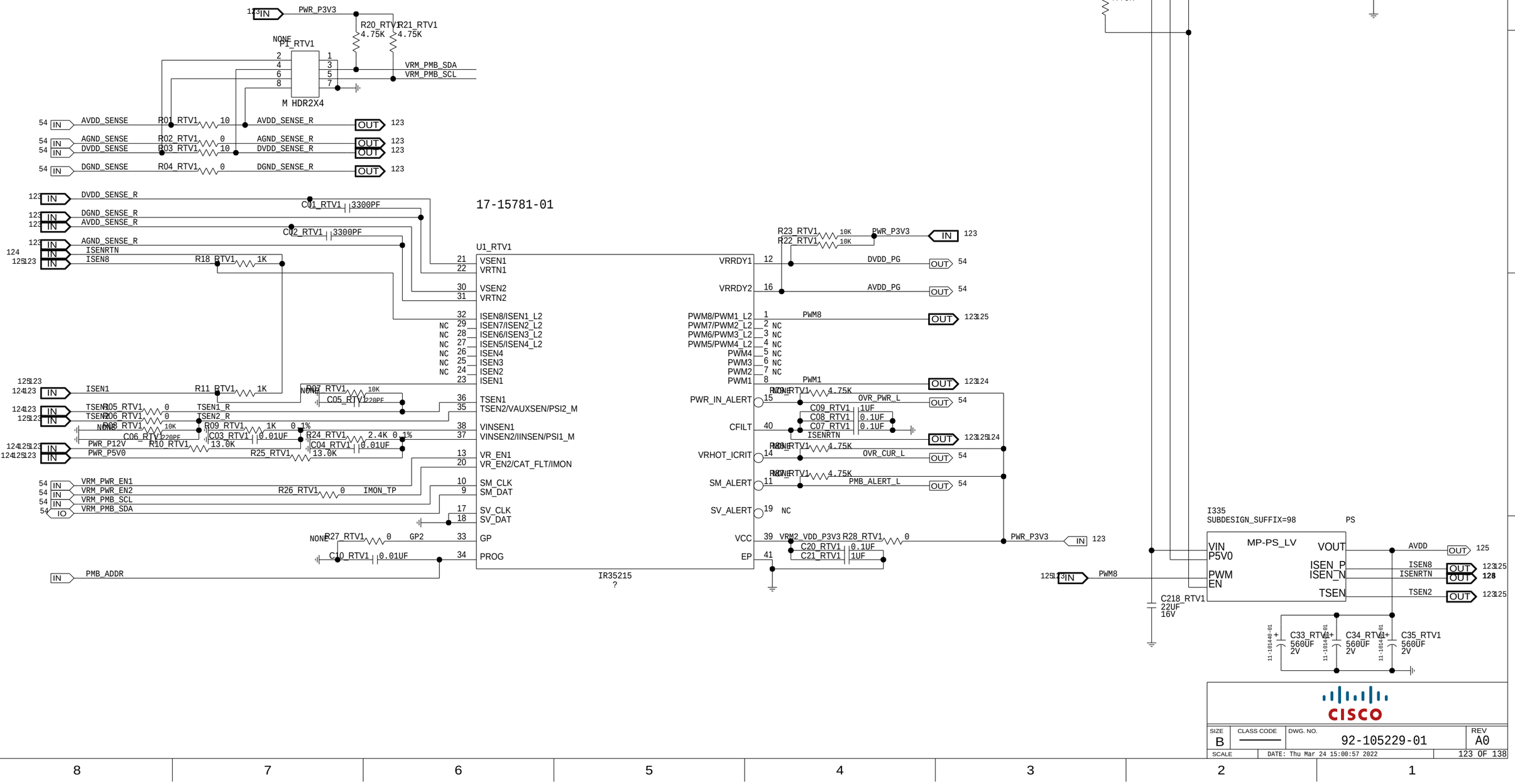
MULTI-PHASE POWER STAGE

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		122 OF 138

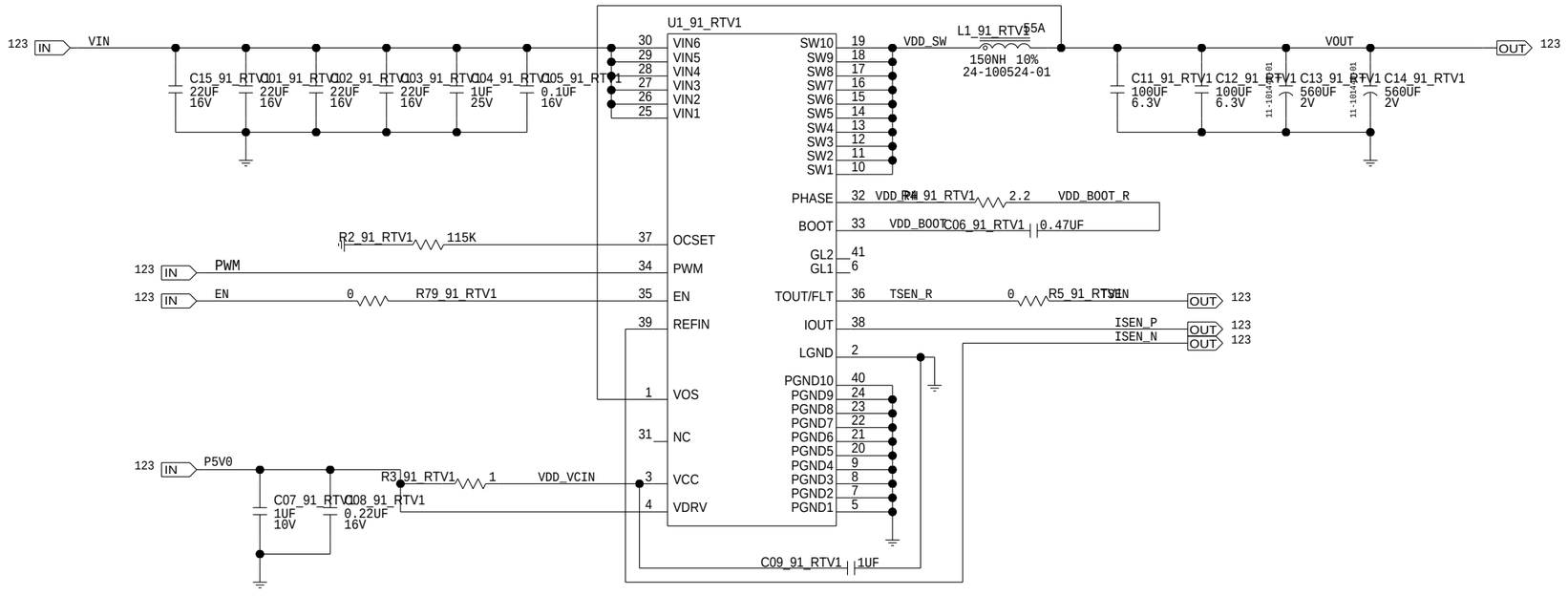
ACADIA MULTI-PHASE 1+1 POWER STAGE MACRO

NOTE:SELECT INFINEON,FAIRCHILD OR TI IN THE VARIANT
PLACE C217,C218 CLOSE TO EACH POWER STAGE



SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:57 2022		123 OF 138

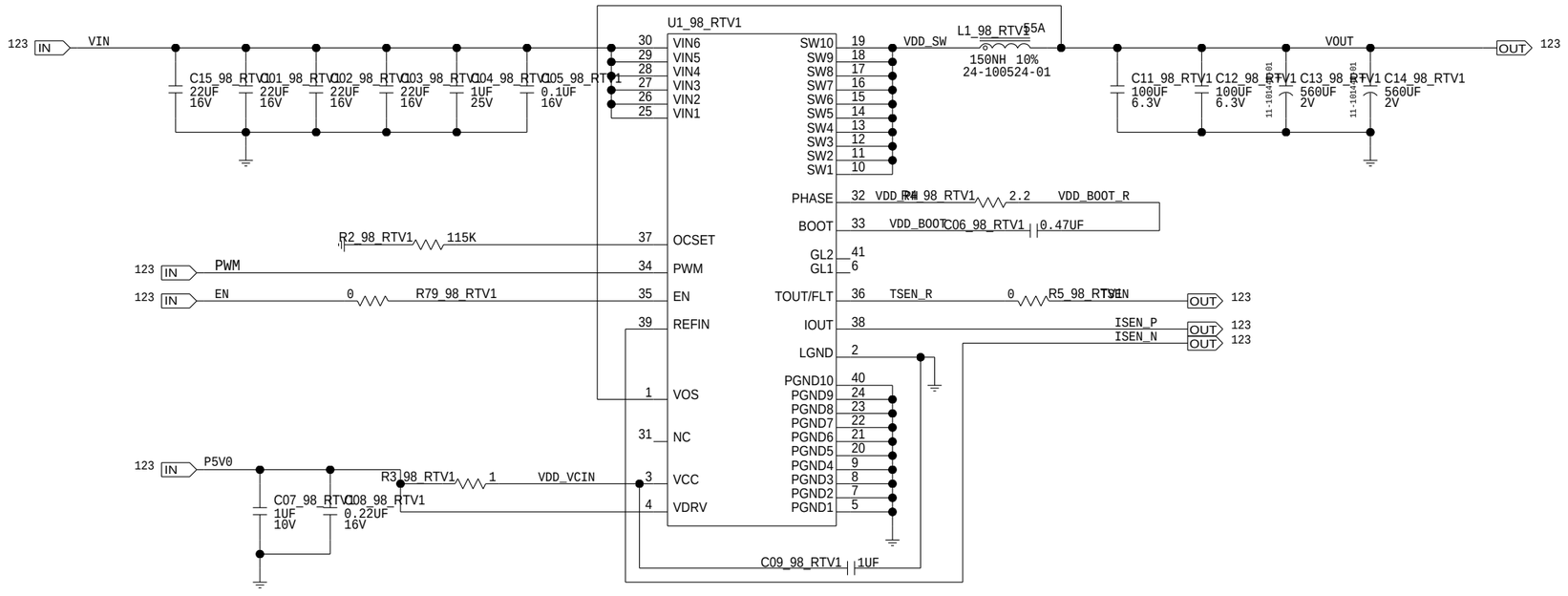
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		124 OF 138

MULTI-PHASE POWER STAGE_LV



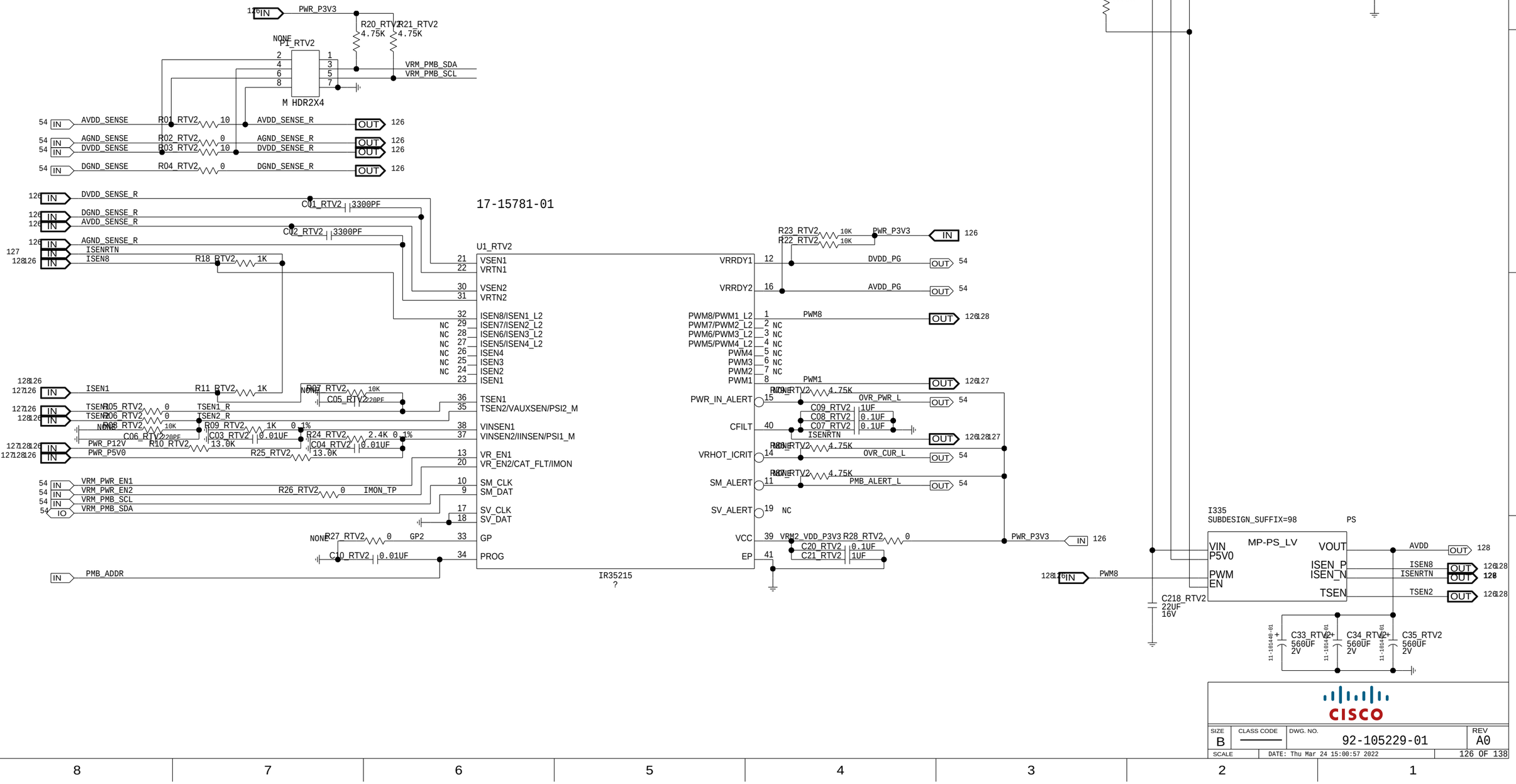
MULTI-PHASE POWER STAGE

CISCO

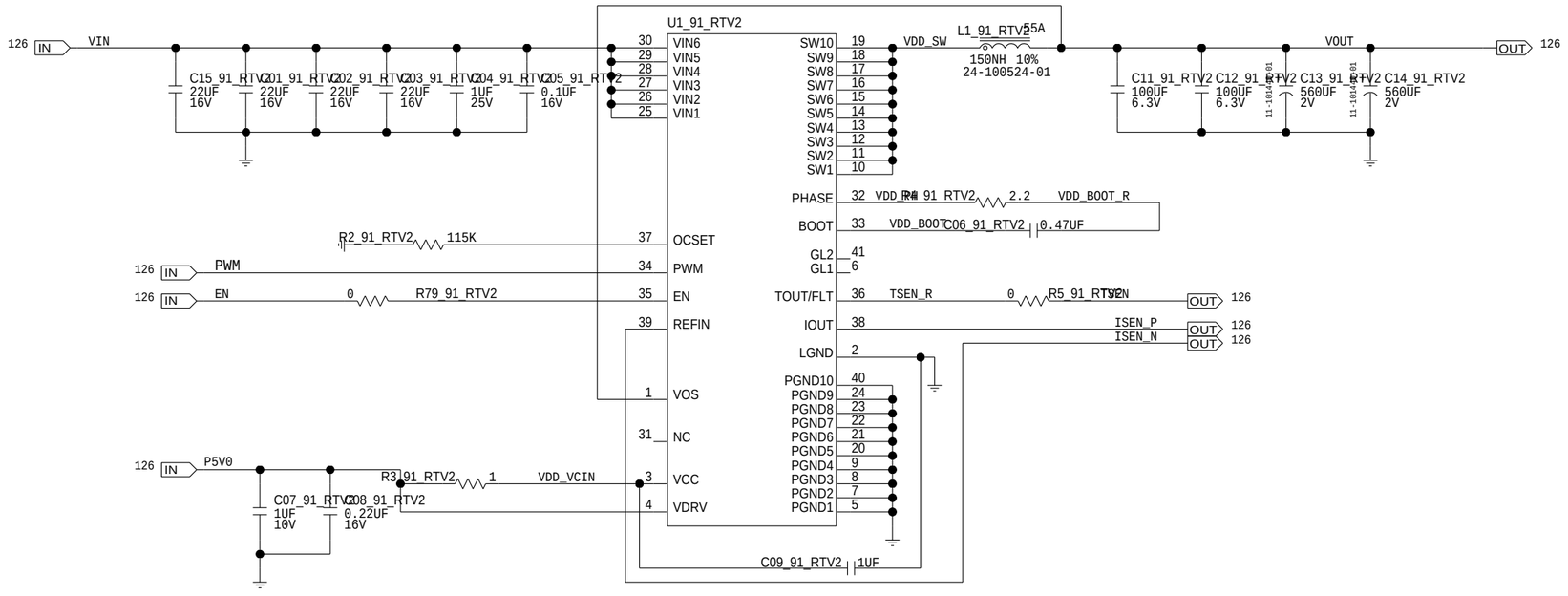
SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		125 OF 138

ACADIA MULTI-PHASE 1+1 POWER STAGE MACRO

NOTE:SELECT INFINEON,FAIRCHILD OR TI IN THE VARIANT
PLACE C217,C218 CLOSE TO EACH POWER STAGE



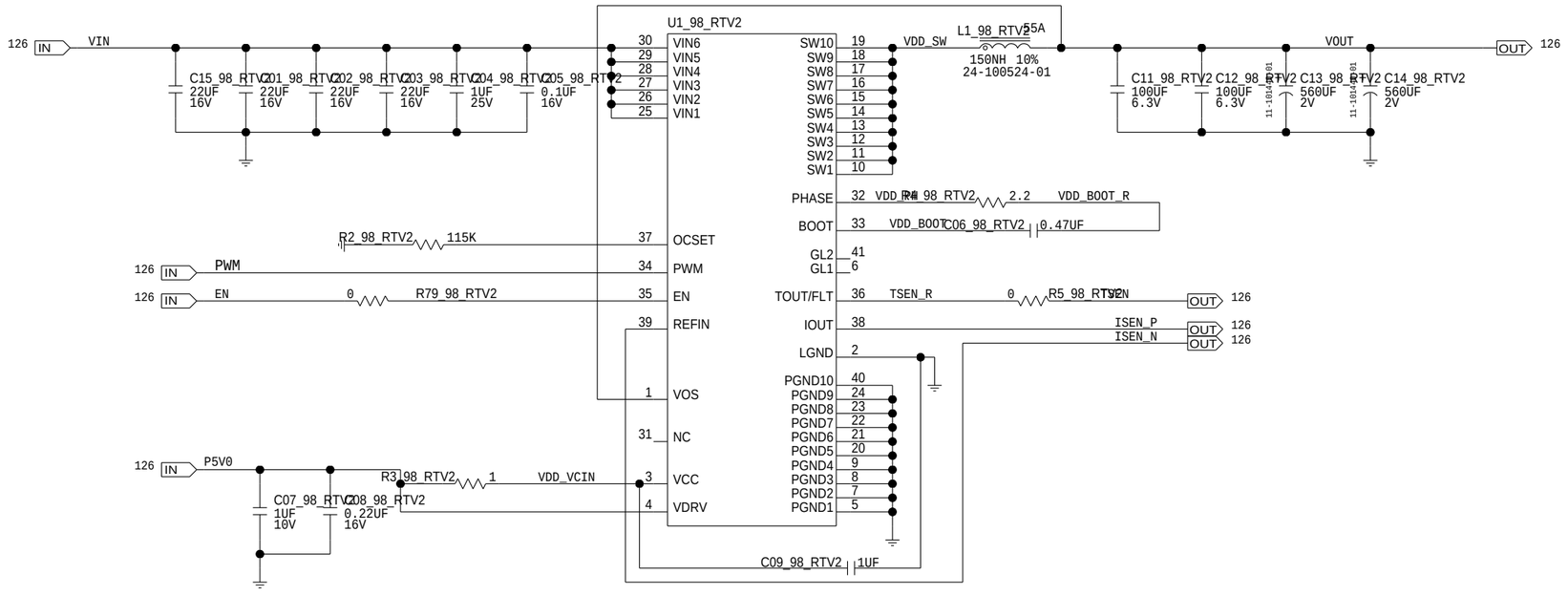
MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		127 OF 138

MULTI-PHASE POWER STAGE_LV



MULTI-PHASE POWER STAGE

SIZE	CLASS CODE	DWG. NO.	REV
B	—	92-105229-01	A0
SCALE	DATE: Thu Mar 24 15:00:49 2022		128 OF 138

VISHAY SIC450 AND ONSEMI FAN251030 2.5V-3.3V/30A DUAL BOM VR

VOUT SET RESISTOR

ONSEMI

VSET Resistor Value (kΩ)	V_{OUT} preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY

OUTPUT VOLTAGE SETTINGS	
V_{SET} RESISTOR (kΩ)	V_{OUT} (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)

Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10	0D	Base+0D

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

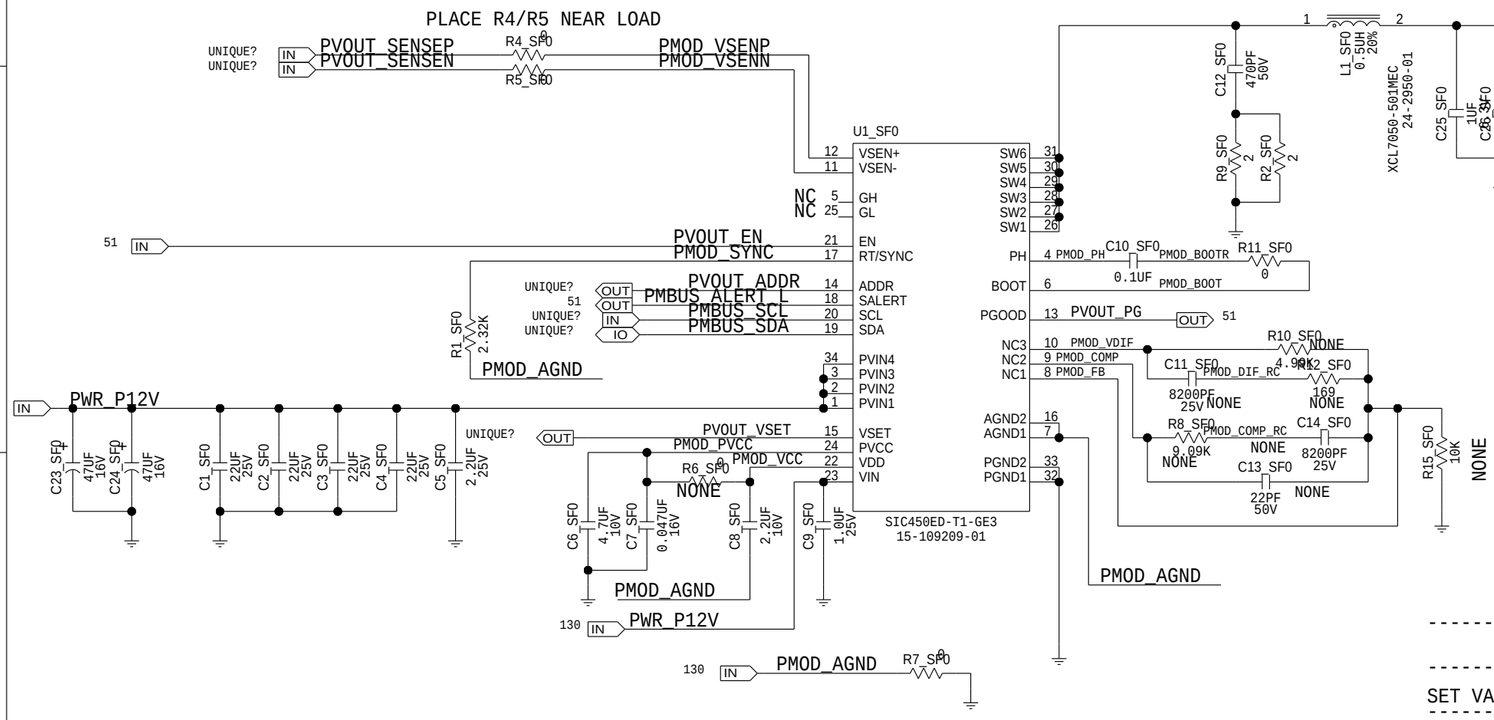
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10	1250
11	1500

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Sep 30 15:51:32 2021		129 OF 138

SIC450/FAN251030 HIGH VOLTAGE 30A



STUFFING OPTIONS FOR ONSEMI VS VISHAY

	ONSEMI	VISHAY
SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY) SET R2 TO 0-OHM FOR VFB = .6V STUFF R15 AND SET TO DESIRED VOUT	X	

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 10 11:59:58 2022		130 OF 138

VISHAY SIC450 AND ONSEMI FAN251030 2.5V-3.3V/30A DUAL BOM VR

VOUT SET RESISTOR

ONSEMI

VSET Resistor Value (kΩ)	V_{OUT} preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY

OUTPUT VOLTAGE SETTINGS	
V_{SET} RESISTOR (kΩ)	V_{OUT} (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)

Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10	0D	Base+0D

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

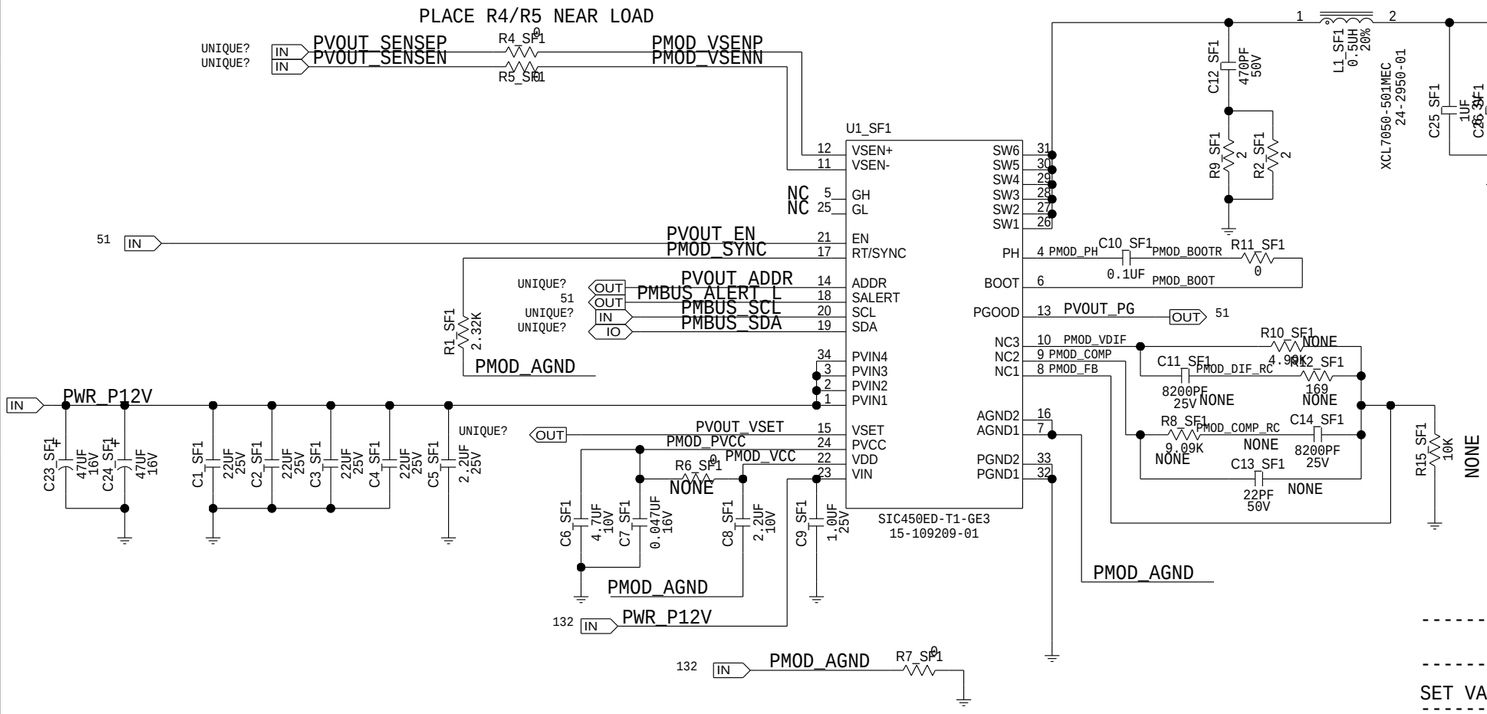
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10	1250
11	1500

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Sep 30 15:51:32 2021		131 OF 138

SIC450/FAN251030 HIGH VOLTAGE 30A

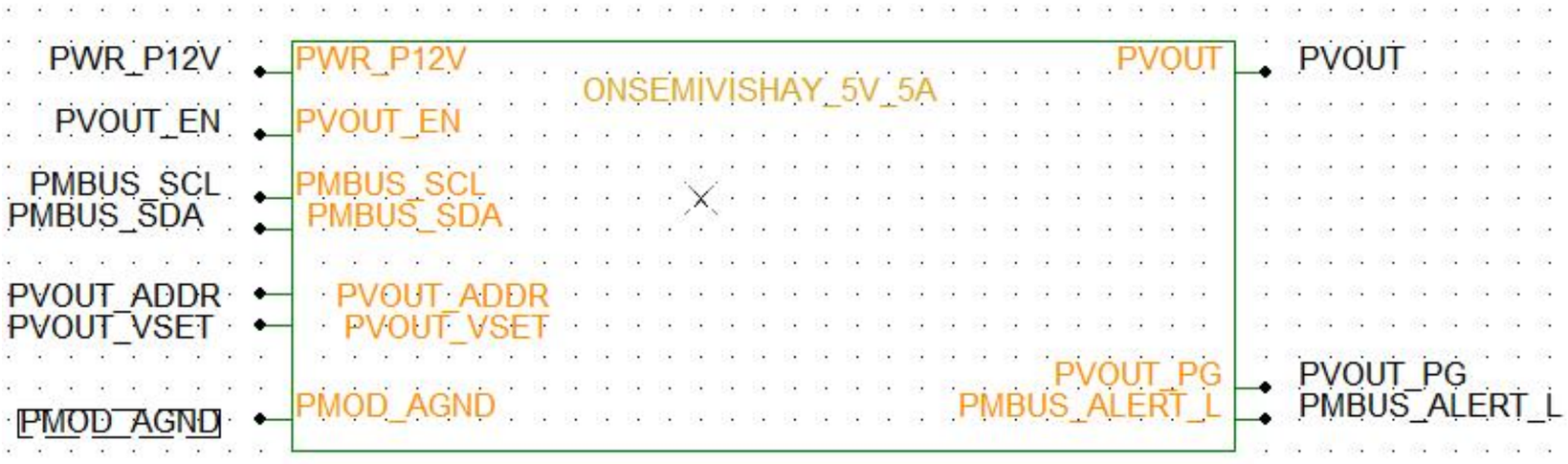


STUFFING OPTIONS FOR ONSEMI VS VISHAY

	ONSEMI	VISHAY
SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY) SET R2 TO 0-OHM FOR VFB = .6V STUFF R15 AND SET TO DESIRED VOUT	X	

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 10 11:59:58 2022		132 OF 138

ONSEMI FAN25015 AND VISHAY SIC453 5V, 5A DUAL BOM VR



VOUT SET RESISTOR

ONSEMI

VSET Resistor Value (kΩ)	V_{OUT} preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY

OUTPUT VOLTAGE SETTINGS	
V_{SET} RESISTOR (kΩ)	V_{OUT} (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)

Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10	0D	Base+0D

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3:0]	NVM [6:4]	BIN [6:0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3:0]	NVM [6:4]	BIN [6:0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

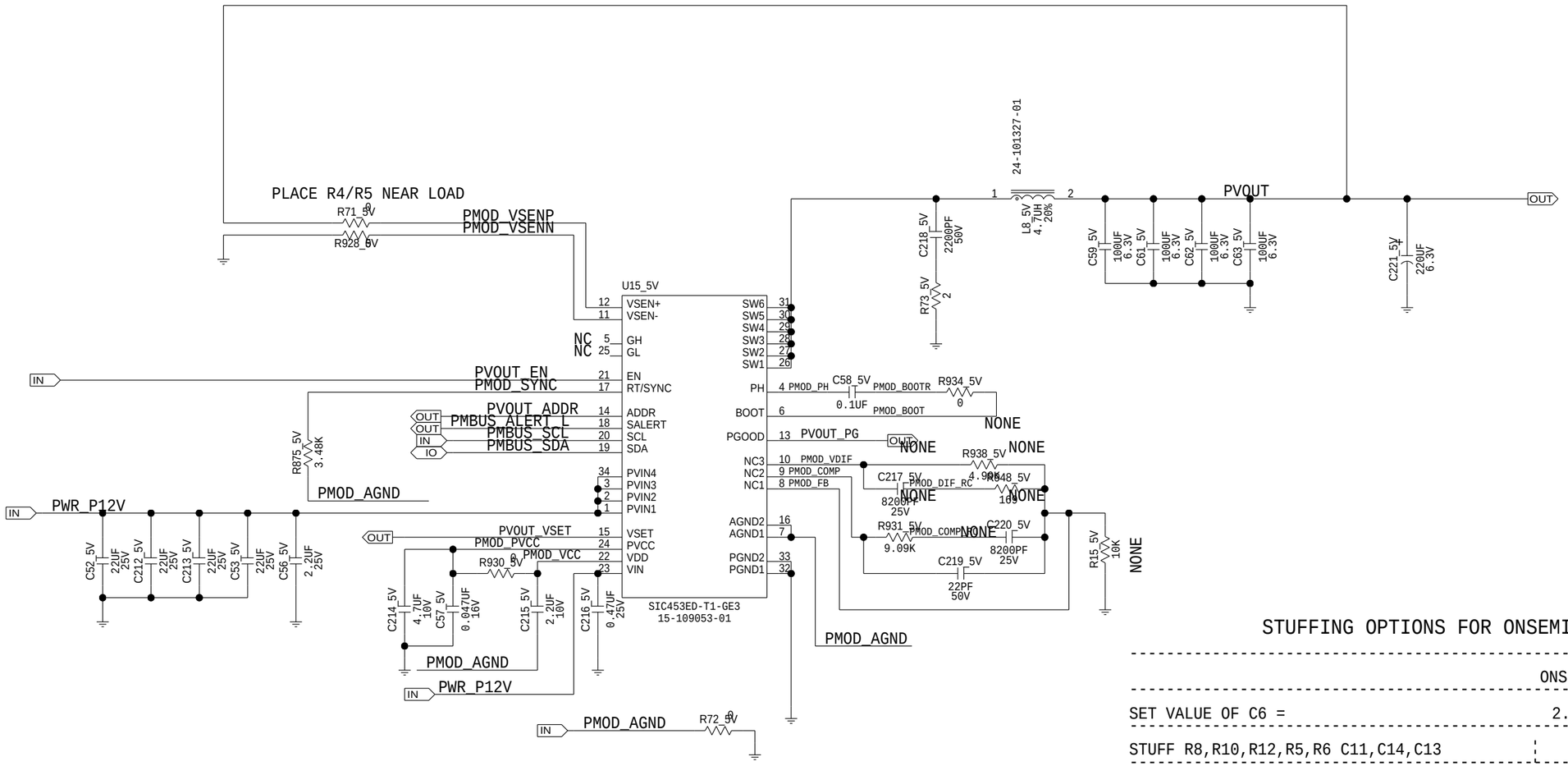
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10	1250
11	1500

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Wed Sep 08 17:36:42 2021		133 OF 138

FAN251015/SIC453 5V, 5A



STUFFING OPTIONS FOR ONSEMI VS VISHAY

	ONSEMI	VISHAY
SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY) SET R2 TO 0-OHM FOR VFB = .6V STUFF R15 AND SET TO DESIRED VOUT	X	

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 10 11:31:00 2022		134 OF 138

ONSEMI FAN25015 AND VISHAY SIC453 2.5-3.3V/9A DUAL BOM VR

VOUT SET RESISTOR

ONSEMI

VSET Resistor Value (kΩ)	V_{OUT} preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY

OUTPUT VOLTAGE SETTINGS	
V_{SET} RESISTOR (kΩ)	V_{OUT} (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)

Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10	0D	Base+0D

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

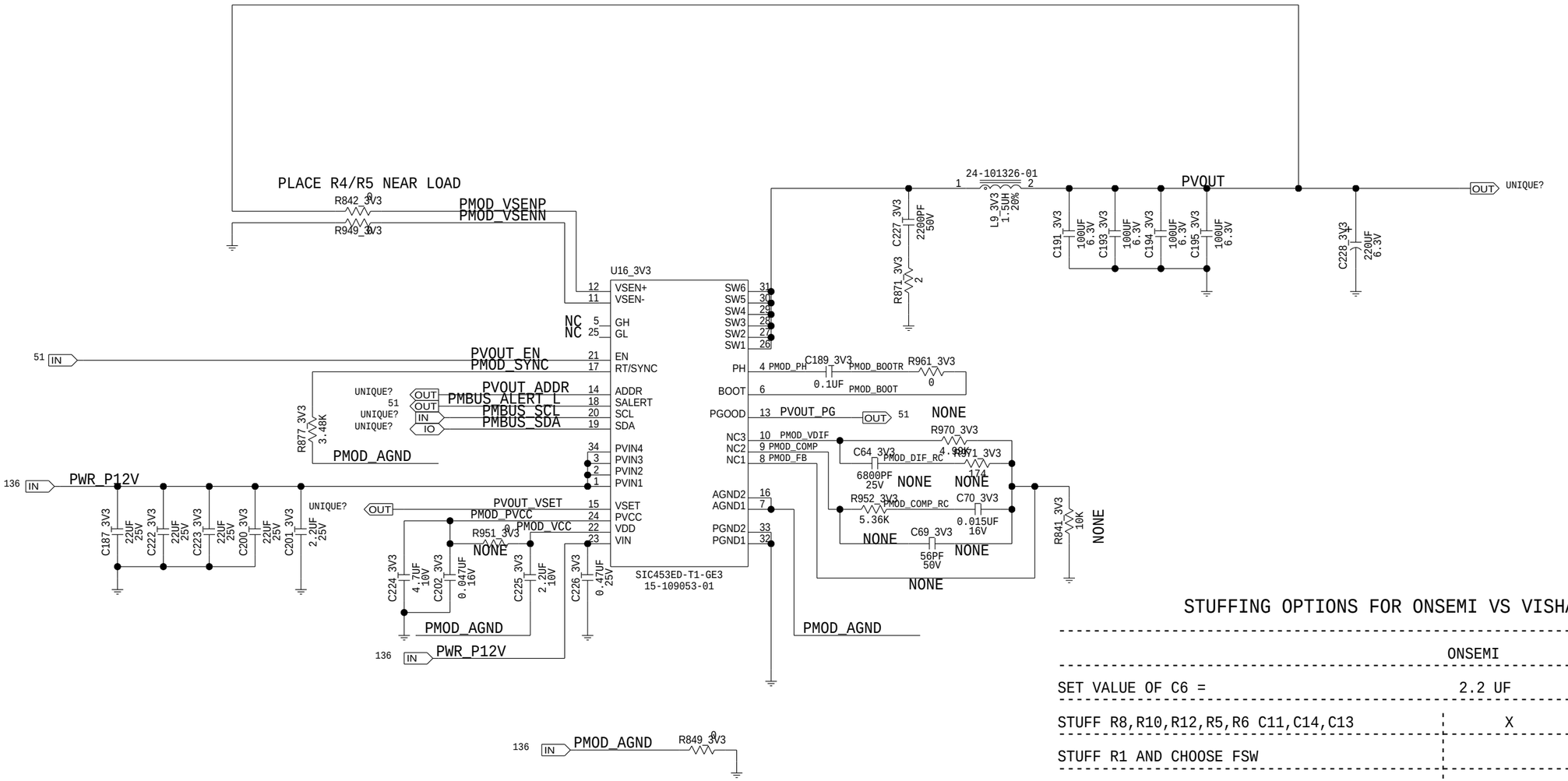
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10	1250
11	1500

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Wed Sep 08 17:31:20 2021		135 OF 138

FAN251015/SIC453 HIGH VOLTAGE 9A

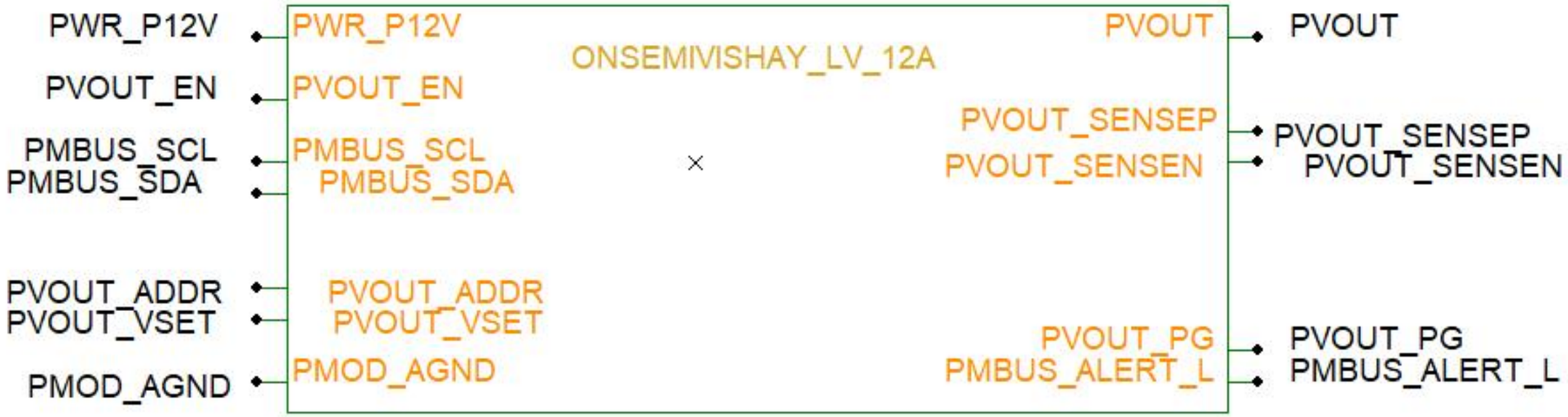


STUFFING OPTIONS FOR ONSEMI VS VISHAY

	ONSEMI	VISHAY
SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY) SET R2 TO 0-OHM FOR VFB = .6V STUFF R15 AND SET TO DESIRED VOUT	X	

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Thu Mar 10 11:24:36 2022		136 OF 138

ONSEMI FAN25015 AND VISHAY SIC453 .8V-1.8V/12A DUAL BOM VR



VOUT SET RESISTOR

ONSEMI

VSET Resistor Value (kΩ)	V_{OUT} preset value (V)
Short	0.6
0.845	0.6
1.3	0.9
1.78	0.95
2.32	1
2.87	1.05
3.48	1.2
4.12	1.25
4.75	1.5
5.49	1.8
6.19	2.1
6.98	2.5
7.87	3.3
8.87	5
10 & greater value	0.8

VISHAY

OUTPUT VOLTAGE SETTINGS	
V_{SET} RESISTOR (kΩ)	V_{OUT} (V)
0.845	0.60
1.30	0.90
1.78	0.95
2.32	1.00
2.87	1.05
3.48	1.20
4.12	1.25
4.75	1.50
5.49	1.80
6.19	2.10
6.98	2.50
7.87	3.30
8.87	5.00
11.0	12.00

BASE ADDRESS OFFSET RESISTOR

ONSEMI (REGISTER C9H, DEFAULT 40H)

Table 1. PMBUS™ ADDRESS SETTING

ADDR Resistor Value (kΩ)	Offset Address (h)	PMBUS Address (h)
0.845	00	Base+00
1.3	01	Base+01
1.78	02	Base+02
2.32	03	Base+03
2.87	04	Base+04
3.48	05	Base+05
4.12	06	Base+06
4.75	07	Base+07
5.49	08	Base+08
6.19	09	Base+09
6.98	0A	Base+0A
7.87	0B	Base+0B
8.87	0C	Base+0C
10	0D	Base+0D

VISHAY(REGISTER D7H, DEFAULT 10H)

MFR_BASE_ADDRESS				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	001b	0010 000b
1.3K	2	1	001b	0010 001b
1.78K	3	2	001b	0010 010b
2.32K	4	3	001b	0010 011b
2.87K	5	4	001b	0010 100b
3.48K	6	5	001b	0010 101b
4.12K	7	6	001b	0010 110b
4.75K	8	7	001b	0010 111b
5.49K	9	8	001b	0011 000b
6.19K	10	9	001b	0011 001b
6.98K	11	A	001b	0011 010b
7.87K	12	B	001b	0011 011b
8.87K	13	C	001b	0011 100b
10K	14	D	001b	0011 101b
11K	15	E	001b	0011 110b

VISHAY (REGISTER E2H, DEFAULT 50H)

MFR_BASE_ADDRESS_2				
CONNECTION	ADDRESS	HEX [3 : 0]	NVM [6 : 4]	BIN [6 : 0]
0.845K	1	0	101b	1010 000b
1.3K	2	1	101b	1010 001b
1.78K	3	2	101b	1010 010b
2.32K	4	3	101b	1010 011b
2.87K	5	4	101b	1010 100b
3.48K	6	5	101b	1010 101b
4.12K	7	6	101b	1010 110b
4.75K	8	7	101b	1010 111b
5.49K	9	8	101b	1011 000b
6.19K	10	9	101b	1011 001b
6.98K	11	A	101b	1011 010b
7.87K	12	B	101b	1011 011b
8.87K	13	C	101b	1011 100b
10K	14	D	101b	1011 101b
11K	15	E	101b	1011 110b

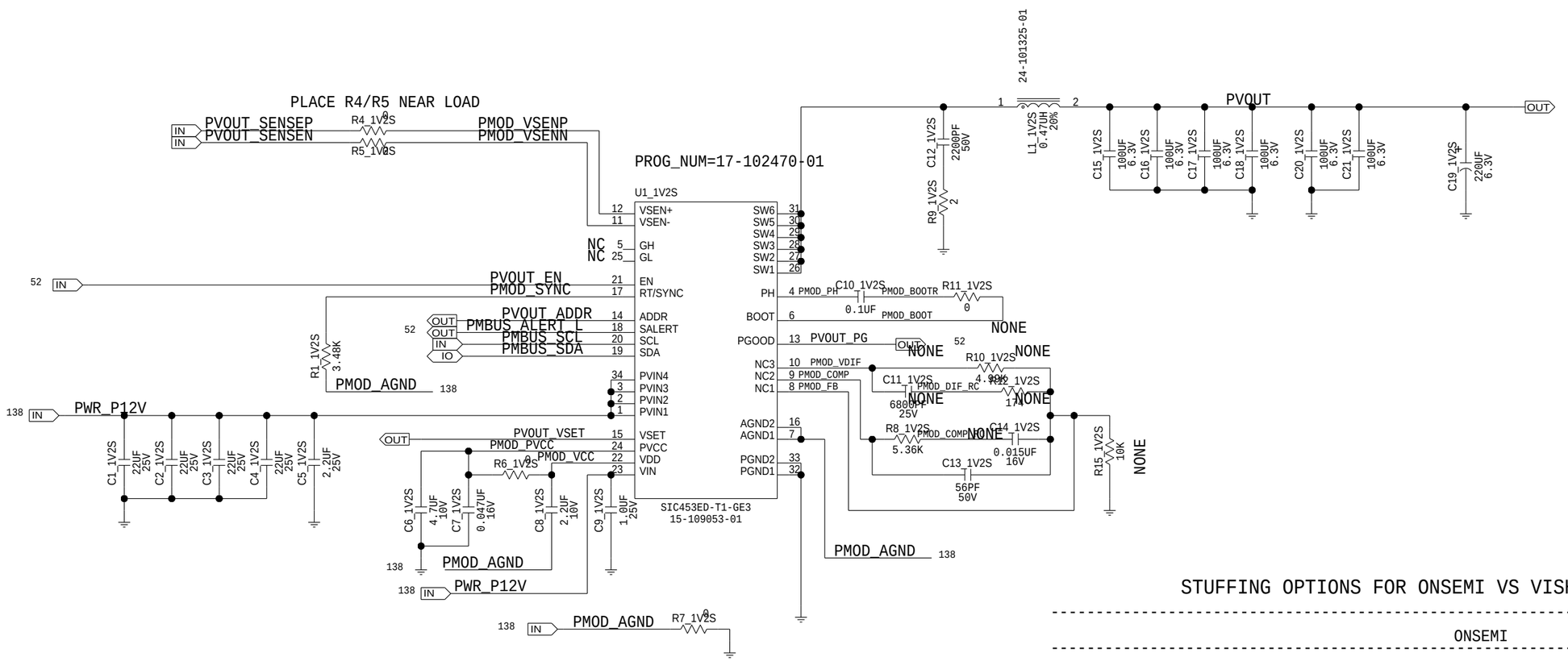
FREQ SET RESISTOR(VISHAY ONLY)

FREQUENCY SETTINGS	
RT RESISTOR (kΩ)	FREQUENCY (kHz)
0.845	300
1.30	400
1.78	500
2.32	550
2.87	600
3.48	650
4.12	700
4.75	750
5.49	800
6.19	850
6.98	900
7.87	950
8.87	1000
10	1250
11	1500

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
SCALE	DATE: Wed Sep 08 17:45:40 2021		137 OF 138

FAN251015/SIC453 LOW VOLTAGE 12A



STUFFING OPTIONS FOR ONSEMI VS VISHAY

	ONSEMI	VISHAY
SET VALUE OF C6 =	2.2 UF	4.7 UF
STUFF R8,R10,R12,R5,R6 C11,C14,C13	X	
STUFF R1 AND CHOOSE FSW		X
USE FB TO SET VOUT (5-1.99V ONLY) SET R2 TO 0-OHM FOR VFB = .6V STUFF R15 AND SET TO DESIRED VOUT	X	

CISCO

SIZE	CLASS CODE	DWG. NO.	REV
B		92-105229-01	A0
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