Technical Note 1

DV-MEGA GMSK data-rate set-up

The DV-MEGA GMSK board [1] is a shield for Arduino, designed to perform GMSK modulation and demodulation tasks baseband to speed 9.6 kbps. This board consists of a CMX589A GMSK modem [2, 3]. This chip includes a clock divider with three inputs: one input is connected to the output of the crystal oscillator (frequency F_{in}). This is the oscillation frequency, which for the DV-MEGA [2] GMSK device is 4.9152 MHz. The other inputs are logical statements that establish the value of division on the input frequency F_{in} (see Figure 1).

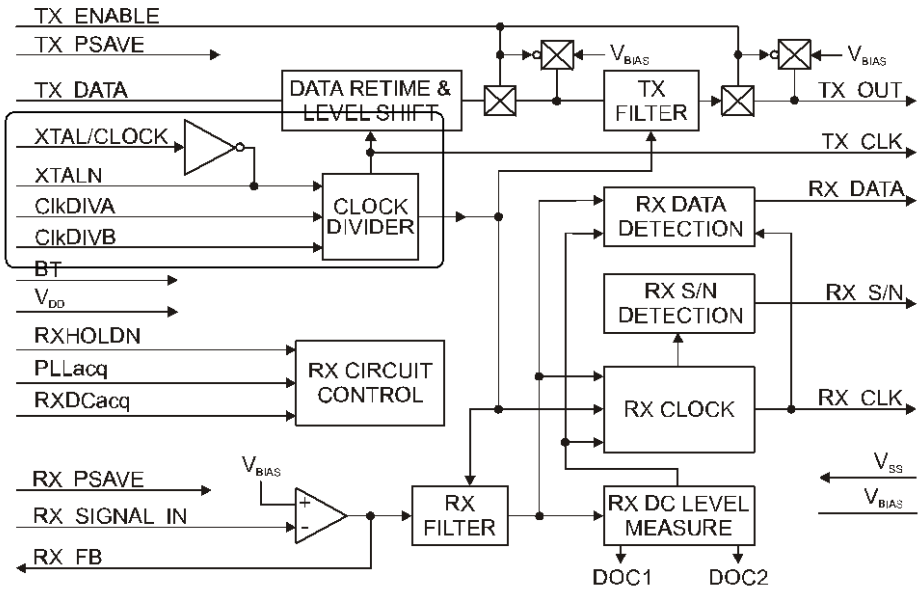

Figure 1. CMX589A subsystems

When a frequency F_{in} is introduced into Clock Divider with N division factor, the output frequency F_{out} is represented by this equation:

$$F_{out} = \frac{F_{in}}{N}$$

The output frequency F_{out} coincides with the output bit rate CMX589A chip. Therefore, if a F_{in} = 5 MHz is introduced (for example), and the division ratio is N = 500, the output binary rate would be 1 Mbps. This is the basis operation of the subsystem clock divider in the CMX589A chip.

The DV-MEGA GMSK device includes a CMX589A chip, and the division clock inputs (ClkDIVA and ClkDIVB) are connected to the supply voltage. This means that ClkDIVB

ClkDIVA = 1 and = 1 (high logic level), so the division factor N = 1024 would be (see Figure 2).

			Xtal/Clock Frequency (MHz)					
			24.576*	8.192	4.9152	4.096	2.4576	2.048
Inputs						12.288/3	12.288/5	6.144/3
ClkDivA	ClkDivB	Xtal/Clk Freq / Data Rate	Data Rate (kbps)					
0	0	128	192*	64*	38.4*	32	19.2	16
0	1	256	96*	32	19.2	16	9.6	8
1	0	512	48*	16	9.6	8	4.8	4
1	1	1024	24*	8	4.8	4		

Figure 2. Clock Divisor configuration by CMX589A

Therefore, if the inputs are the clock divider to a fixed value, the only way to establish a data rate of 9.6 kbps is to change the crystal oscillator. This selection is based on the initial equation, so if N = 1024 and if we want to have an output frequency (or bit rate) such that F_{out} = 9.6 kbps, then:

$$F_{out} = \frac{F_{in}}{N} \rightarrow F_{in} = F_{out} \cdot N = 9.6 \cdot 10^3 \cdot 1024 = 9.8304\, MHz$$

Thus, we have selected a 9.8304 MHz frequency for the crystal oscillator to obtain a bit rate of 9.6 kbps. So we had to change the 4.9152 MHz oscillator which is integrated on the external clock circuitry DV-MEGA GMSK (see Figure 3).

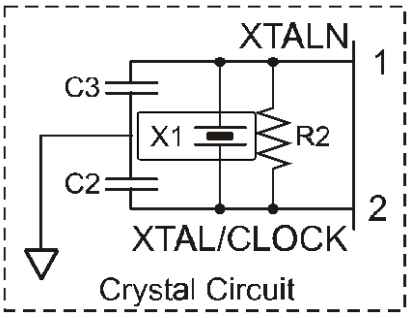

Figure 3. Extern clock circuit recommended by CMX589A and used by DV-MEGA GMSK

The rest of the circuit, such as R2 (1 MΩ) resistance or capacitors C2 and C3 (33 pF) are not modified because these values are valid for the bit rate of 9.6 kbps. This is another advantage of this solution, since it is not necessary to change other components of the DV-MEGA.

References:

[1] http://www.dvmega.auria.nl/GMSK_shield.html
[2] http://www.cmlmicro.com/products/CMX589A_Full-Duplex_GMSK_Modem/
[3] http://www.cmlmicro.com/assets/FX589DS.pdf

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