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Safety Interlocks and Discrete Control Integration Procedure for the Acutrol3000 Motion Control System

Technical Manual

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1 Introduction

This manual provides documentation to configure the discrete I/O signals that are used to implement the failsafe servo interlocks and status (inputs), and to programmatically control relay closures (outputs) of the Acutrol3000 motion controller. A transition module provides the hardware connection between the AIM signal connectors and the legacy Acutrol Act2000 connector interface on the back of the Acutrol3000 chassis. This hardware also provides conditioning of signals as required, and routes signals between the individual axis boards (AIMs) and the consolidated system connectors.

The discrete control of output relay closures is addressed in this document because these features use the same hardware and configuration/command panels as the interlocks. Finally, the status monitoring features of the Acutrol3000 are documented and provide a means to observe the operational state of discrete signals as they relate to interlock and relay control.

1.1 System Level Overview

Figure 1 is a top-level block diagram of the safety interlock and discrete control sub-systems. The rectangular blocks identify the various Operator Interface panels used to configure and control the discrete system functions. The rectangles with rounded corners represent the hardware modules, which implement the digital logic and external interface circuitry.

The safety interlocks may be configured directly using ACL commands or more generally the system integrator will use the GUI interface and the associated configuration/control panels. Once the interlocks are configured and verified, the configuration state must be saved to preserve the system configuration. The default (saved) configuration state is restored whenever the system is booted. Interlock logic in the Axis Interface Module autonomously monitors the controller and system safety interlocks and opens the servo of all affected axes in the event of a fault.

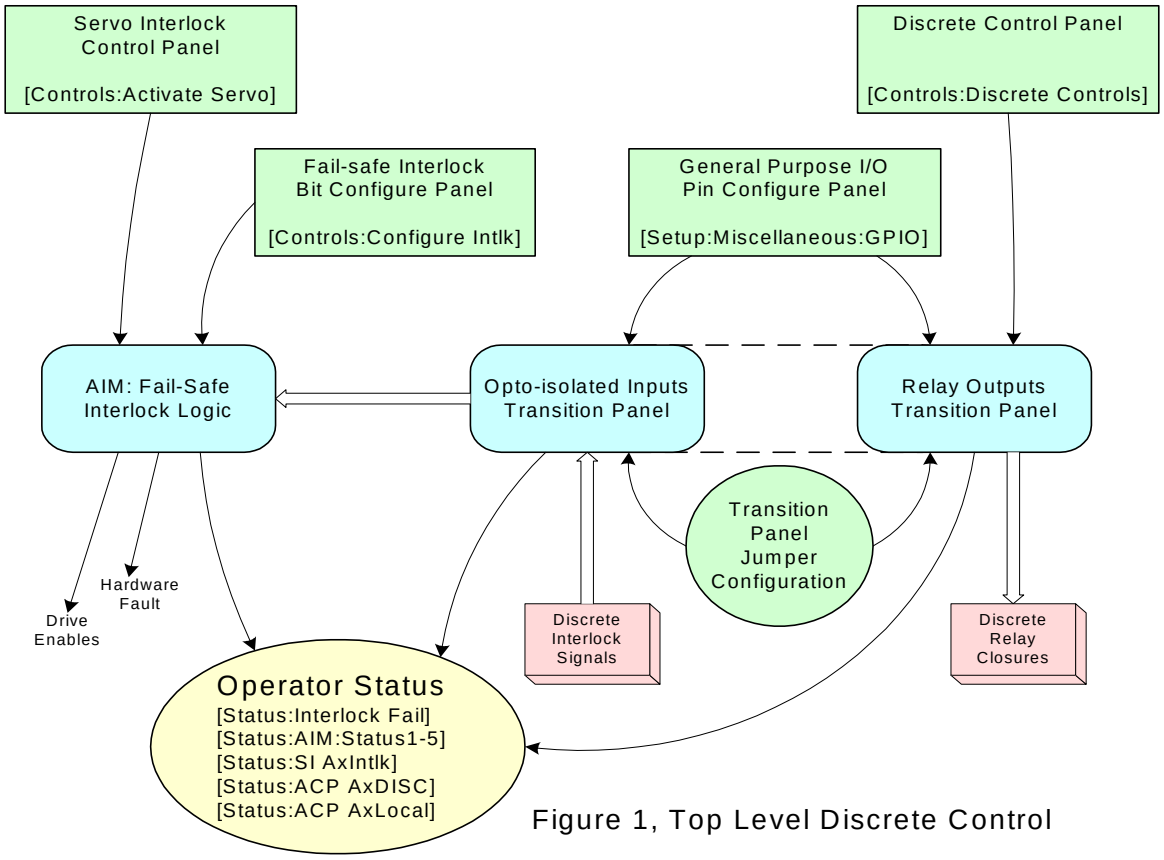


Figure 1, Top Level Discrete Control

1.2 Discrete I/O Topology

This section provides an overview of the operation of discrete processes in the Acutrol3000 as they relate to safety interlocks and discrete relay control. Figure 2 shows the signal interconnection/flow of a typical discrete signal as it processes through the various hardware sub-systems and the logic of the associated hardware circuitry.

Each AIM board has eight (8) General Purpose I/O pins (GPIO0-7). Pins 6 and 7 are dedicated to providing discrete I/O using the BNC connectors Digital IO/1, 2 respectively, which are located on the Acutrol3000 front panel.

The remaining six (6) pins are used as inputs for safety interlocks or as outputs for discrete relay control. The direction of each pin is programmed independently, but must be done in concert with the Transition module, which mandates a default use of the GPIO pins. This default configuration is defined in section 2.2 Acutrol3000 Default Configuration. There is some flexibility using jumpers on the Transition panel to trade off inputs and outputs depending on system requirements. In general, there are four GPIO pins per axis used for inputs, and the remaining two are used for discrete control outputs. The system specific configuration can be documented by using the table in Appendix B.

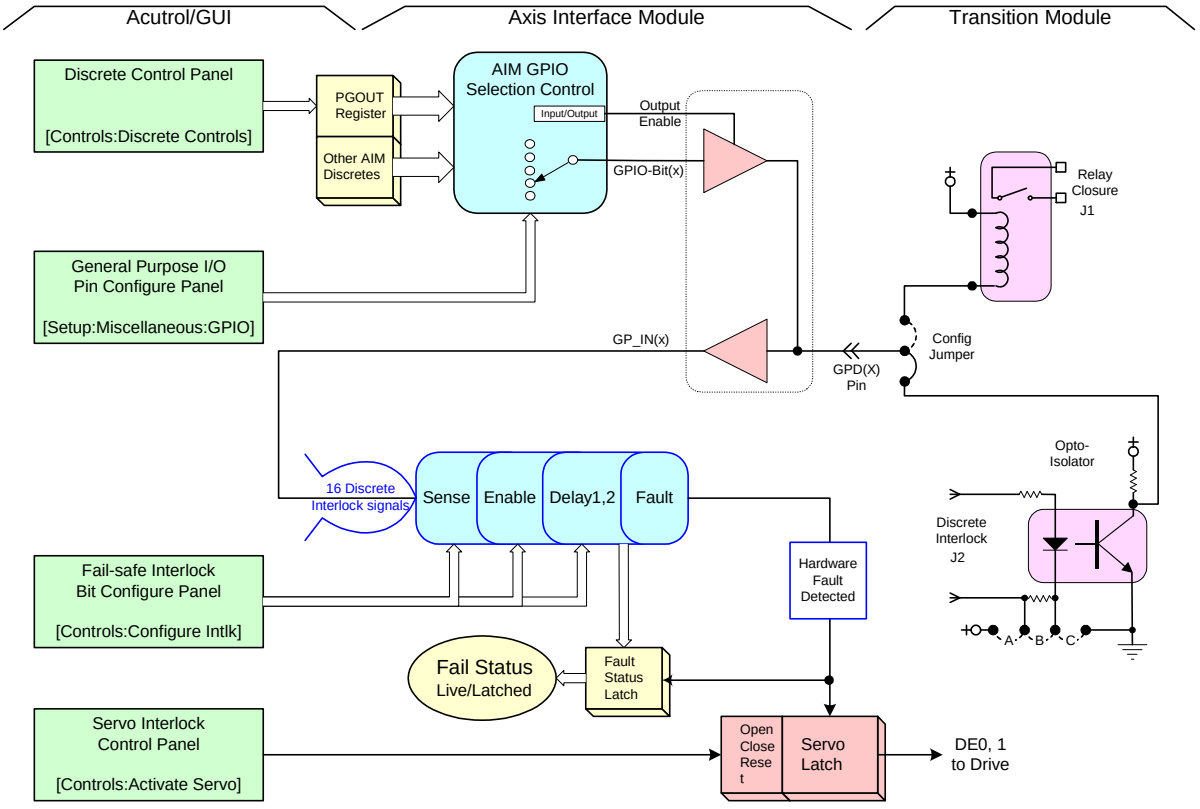


Figure 2. Acutrol3000 Discrete I/O Structure

1.3 Configuration Features

The typical structure of a discrete I/O signal is shown in Figure 2 (above and in Appendix-L at the end of this document in a larger format). The diagram is divided into three sections: **Acutrol/GUI** (interface/software), **Axis Interface Module** (programmable logic), and **Transitional Panel** (I/O hardware). Communication between the Supervisor and the hardware is via programmed I/O registers in the Axis Interface Module (AIM). This is because the logic, which implements the fail-safe interlock testing and discrete control, is implemented in the FPGA circuitry of the AIM.

The first section of Figure 2 is defined as **Acutrol/GUI** and represents the Acutrol Command Language interface that provides access to the hardware for configuration and control. All of the panels in the GUI use ACL commands to configure, control, and monitor I/O functions.

The **AIM** group implements the programmable logic of each GPD(X) pin, which includes the direction and the multiplex signal selection. The configurable failsafe interlock logic that tests for servo faults is also implemented in the AIM. This is accomplished using the **Setup/Miscellaneous/GPIO** panel in the Graphical User Interface (GUI).

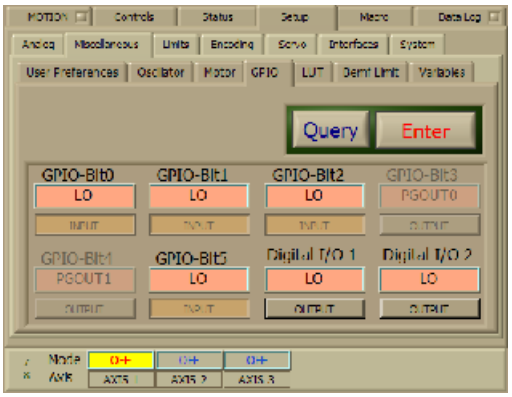


Figure 3. Setup/Miscellaneous/GPIO

OUTPUTS: If a pin is configured as an output then the corresponding multiplexed signal is output to the GPIO pin. Generally, the signal, which is selected for output, is a user-defined bit from the AIM PROGOUT register. This register can be programmatically altered on a bit by bit basis by using either the ACL command [Configure:Discrete] or the Discrete Control panel **Controls/Discrete Controls** in the GUI.

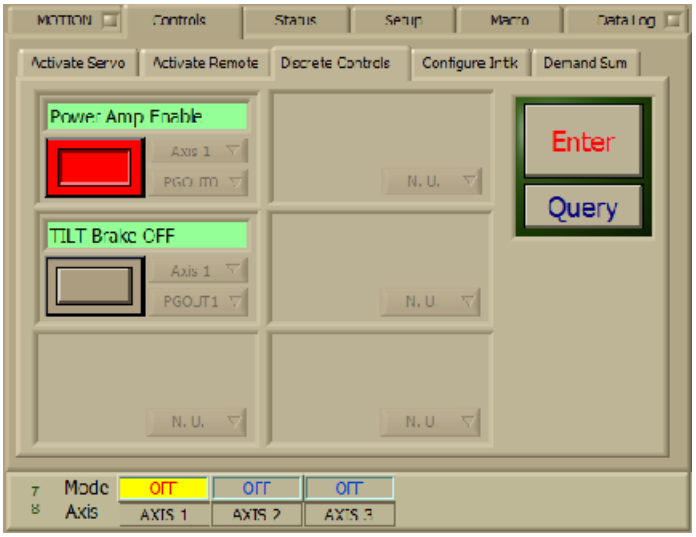


Figure 4. Controls/Discrete Controls

The **Transition Module** is the third section in the discrete I/O structure, and consists of the hardware programming jumpers, opto-isolated inputs, and output relays located on the Transition panel.

Depending on the particular GPIO pin and the configuration options, jumpers on the rear panel of the Acutrol3000 chassis may be change to accommodate input/output requirements. Most of the routinely changed option jumpers are accessible by removing the cover plate above the sub-D connectors on the rear panel of the Acutrol3000 chassis.

The GPIO input buffer always looks at the logic state of the pin and reports this state to the Fail-safe interlock test logic. This is true even if the GPIO pin is setup as an output. If the state of the pin (as an output) is not used in the interlock test, it is still logic corrected and will report the status of the pin.

INPUT: When a GPIO pin is used to input an interlock signal, the output of the corresponding opto-isolated input is routed though the Transition panel to the AIM. The AIM contains digital logic, which implements the fail-safe testing of the GPIO pin in question. A total of sixteen discrete signals are configured for testing in the fail-safe logic of the AIM.

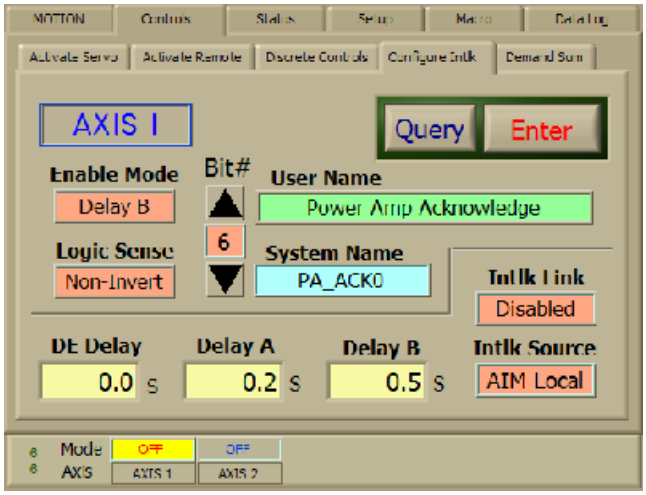


Figure 5. Controls/Configure Intlk

Each bit is configured using the **Controls/Configure Intlk** panel.

This panel provides the means to configure the logical sense of the interlock signal, and to enable it in the interlock test. The enabled options include Immediate test, delayed by T_a or delayed by T_b. If the bit Enable Mode is "Disabled", then it is only used for status in the system.

The user name for the interlock signal can be entered in the GUI keyboard and transferred to the User Name control to customize the status nomenclature of this bit and consequently the name that is displayed in the Interlock Fail status panel.

FAULT: A fault is tested/detected only if an axis is servoed. When a fault occurs, the Drive Enable signals (DE0, DE1) are de-asserted causing the system to immediately disable the drive or power amplifier, removing power from the motor/drive(s). Detecting a fault also causes the Interlock Fail Status to be latched, the servo loop to be 'opened', the "Disable" control/indicator on the GUI front panel to flash, and a fault to be reported in the status.

SERVO: The Servo Interlock Control panel **Controls/Activate servo** is used to Open and Close interlocks, whenever a fault occurs, the servo state is forced open and the latched fault prevents re-closing the servo. A Reset button is provided to clear the fault, and allow the axis to be servoed again.

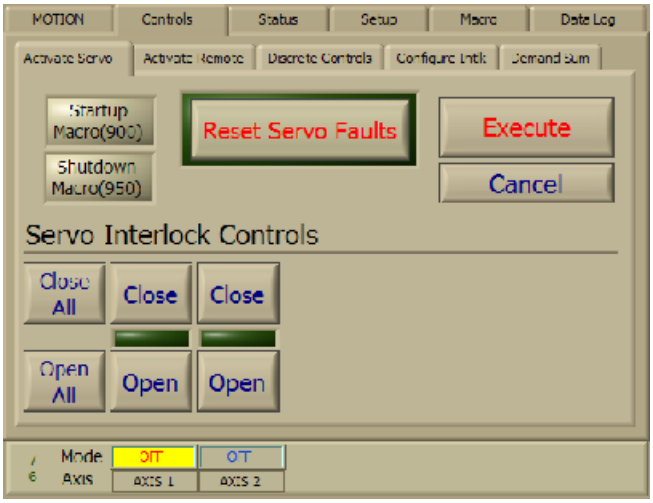


Figure 6. Controls/Activate Servo

2 System Interlock Planning

2.1 Gathering Information

The first step in setting up interlocks is to identify the interlock states that are required for each individual axis and those that are used globally.

Safety interlock states are most easily handled when they are implemented as a floating relay or floating switch closure. Equally simple to handle is a signal that has two discrete voltage states corresponding to **safe** and **failed** operational status. States that are in a **safe** state, only after the system has been servoed, can be accommodated by specifying a delayed test for that interlock.

Sensors such as PTC thermistors can also be used, but may require some care to ensure compatibility between the opto-isolator activation currents, the supply voltage, and the thermal switch characteristics.

Other sensors may require additional signal conditioning to set thresholds, and/or establish compatible discrete states representing safe and unsafe conditions.

Interlocks should be designed so that they are fail-safe. In general, this means that an interruption of current flowing into the input circuitry of Acutrol should be interpreted as a fault. The Ideal interlock sensor supplies a voltage/current while the state is safe, and removes the voltage/current to indicate a fault. If this precaution is taken, the most common wiring faults (a broken wire, a short between wires, or a short to ground) will generally be detected by the interlock circuitry.

2.2 Acutrol3000 Default Configuration

The Acutrol3000 is built and configured to a default state. The software settings are saved in the configuration files of the GUI and real-time computers. The hardware configuration is defined by the default jumper settings in the schematics and assembly drawings of the various printed circuit boards.

The primary circuit board that dictates the use of the available discrete I/O signals is the Transition Module. Refer to the assembly drawing 1201E03A and the board schematic 1201E03S for details of the default jumper settings.

The Transition module consolidates signals to/from multiple AIM boards and provides an Interlock Input connector (J2) that is compatible with the legacy Acutrol ACT2000 MIS J5 connector. Table 1 in Appendix-A lists the partitioning of the opto-isolated inputs for axis specific and global interlocks. Also shown is the mapping of pins from the 37 pin sub-D connector to a 34-pin ribbon connector. The Signal Source identifies the default use of GPDx (General Purpose Discrete) and other paths to route signals through the Transition module to the AIM module(s).

Each axis has fail-safe interlock logic in the corresponding Axis Interface Module to test for a fault and initiate a hardware abort. The 16 discrete signals that make up the hardware interlock register are summarized in Table 2 below. A blank version of this table is found in Appendix-B and can be used as a work sheet. Table 2 shows the default configuration for the 16 interlock bits.

Table 2 INTERLOCK FAULT (Default Configuration)

REGISTER NAME: FAIL_STATUS2

Project# _____ Axis _____ Date ____/____/____

					INTERLOCK SOURCE	
Bit#	User Signal Name	Enable Mode*	Logic	Status Name	Local States	Multiplex
0	INTLK1	Disabled	INVERT	INTLK_STATUS0	GP_IN0	MIR0
1	INTLK2	Disabled	INVERT	INTLK_STATUS1	GP_IN1	MIR1
2	INTLK3	Disabled	INVERT	INTLK_STATUS2	GP_IN2	MIR2
3	Relay1 (dedicated)	Disabled	INVERT	INTLK_STATUS3	GP_IN3	MIR3
4	Relay2 (opt. Global3)	Disabled	INVERT	INTLK_STATUS4	GP_IN4	MIR4
5	INTLK4 (opt. Relay3)	Disabled	INVERT	INTLK_STATUS5	GP_IN5	MIR5
6	Power Amp Acknowledge	DelayA	NON-INV	INTLK_STATUS6	PA_ACK0	MIR8
7	Global1 (opt ServoB PAFlt)	Disabled	INVERT	INTLK_STATUS7	INTLK1	MIR9
8	Global2 (opt ServoB PAAck)	Disabled	INVERT	INTLK_STATUS8	INTLK2	MIR10
9	Master INTLK/ Front Panel	Immediate	NON-INV	INTLK_STATUS9	MASTER_INTLK	MIR11
10	AIM - DMA Sync Fault	Immediate	NON-INV	INTLK_STATUS10	AIM - DMA_SYNC_ERROR	
11	AIM-RT Software Watchdog	Immediate	NON-INV	INTLK_STATUS11	AIM - SW_WD_FAULT	
12	AIM - 10 kHzCLK_WDOG	Immediate	NON-INV	INTLK_STATUS12	AIM - 10 kHzCLK_WDOG	
13	Serial Data Link	Disabled	NON-INV	INTLK_STATUS13	AIM - SDL_FAIL	
14	Servo Intlk Link	Disabled	NON-INV	INTLK_STATUS14	AIM - SIL Servo Intlk Link	
15	AIM - 10K_LOCK_FAULT	Immediate	NON-INV	INTLK_STATUS15	AIM - 10K_LOCK_FAULT	

* Enable mode options : Disabled, Immediate, Delay1, or Delay2

Bits 1-9 are system specific; although, most systems have an acknowledgement from the axis drive (bit-6), and a Master interlock control (bit-9) is general required in for facility safety. All other undefined bits are disabled from the interlock test, and the logic is inverted to prevent indicating a failed state in the Fault Status register.

Bits 10-15 are used for hardware testing of the internal states of the Axis Interface Module.

- Bit 10 detects a coherency error in the current DMA transfer of analog measurement data from the AIM FIFO to the Axis Control Processor (ACP) memory.

- Bit 11 reports the occurrence of a watch-dog fault which is detected whenever the ACP RT thread fails to reset a re-triggerable one-shot in the logic of the AIM hardware.

- Bit 12 is the result of a hardware test in the AIM that verifies that the 10 KHz reference is present on the signal line that links the master AIM to the slave AIM(s).

- Bit 13 is reserved for future use when expanded discrete I/O is required. The associated hardware is currently not available.

- Bit 14 Servo Interlock Link may be used to interlock specific axes together such that ‘all or none’ operation can be easily implemented. This feature is defined in detail in section 3.2.1 Servo Interlock Configuration Panel.

- Bit 15 is active in slave AIM boards, and indicates a fault if the slave 10 KHz is not able to maintain lock with the master AIM.

All enabled faults that occur after an axis has been servoed are considered catastrophic and results in opening the servo of one or more axes.

3 Setting Up Interlocks

3.1 Input Signal Conditioning

Discrete interlock signals are normally input via the opto-isolated inputs in the Discrete Input connector (J2) on the back of the Acutrol3000 chassis. Signals are also input as PA Ack, PA Fault, and/or auxillary servo Intlk1,2 located in the ServoA,B connectors on the rear panel of the Acutrol3000.

The input logic levels that may be used for the two voltage ranges are defined in Table 3.

Input Configuration	Logic “0”	Logic “1”
24 Volt Logic	-6 to +3 V DC	+9 to +38 V DC
5 Volt Logic	-6 to +1.2 V DC	+3 to +10 V DC

Table 3. Input Logic Voltage Levels

Care must be taken to ensure that a positive voltage is applied to the anode (A) terminal relative to the cathode (C) terminal for proper/safe operation.

Interlock signals/closures can be input in any of four basic configurations as defined in the following jumper Table 4 and in the Figures 7.x below:

Input Signal Conditioning	Jumper A	Jumper B	Jumper C
24 Volt Logic			
5 Volt Logic		X	
Floating Closure (Acutrol +5V, Gnd)	X		X
Common Closures (Acutrol +5 V)			X

Table 4. Input Voltage Jumper Options

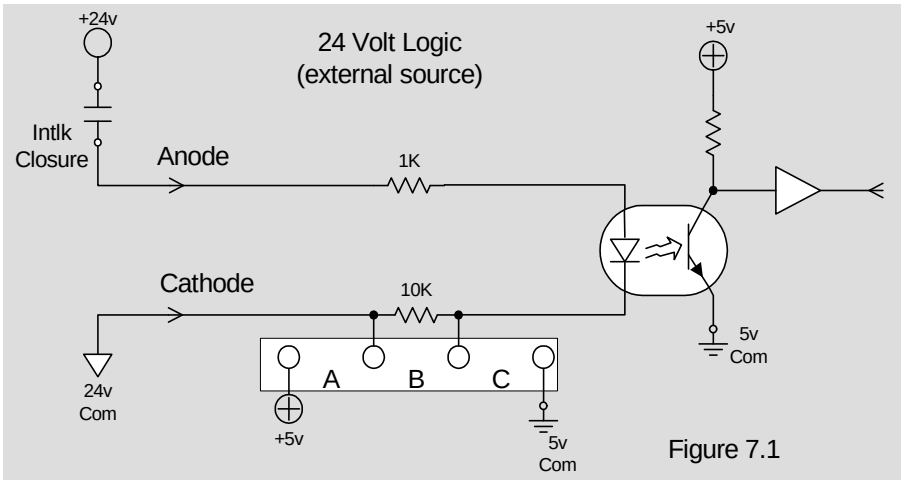


Figure 7.1

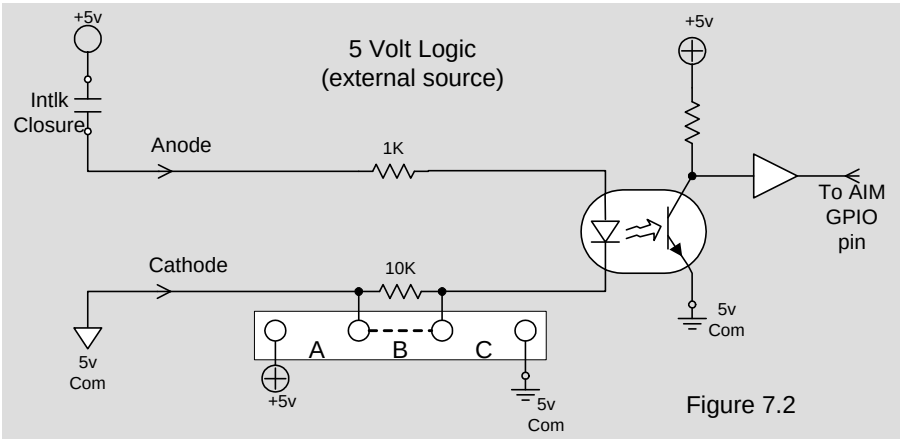


Figure 7.2

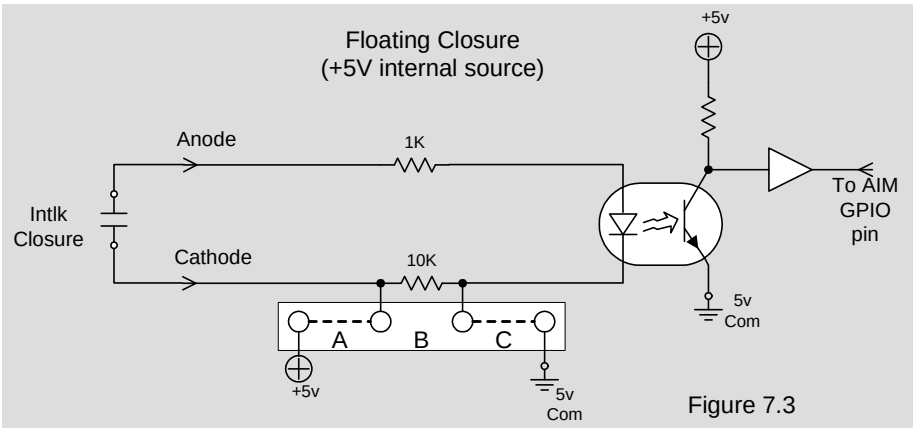


Figure 7.3

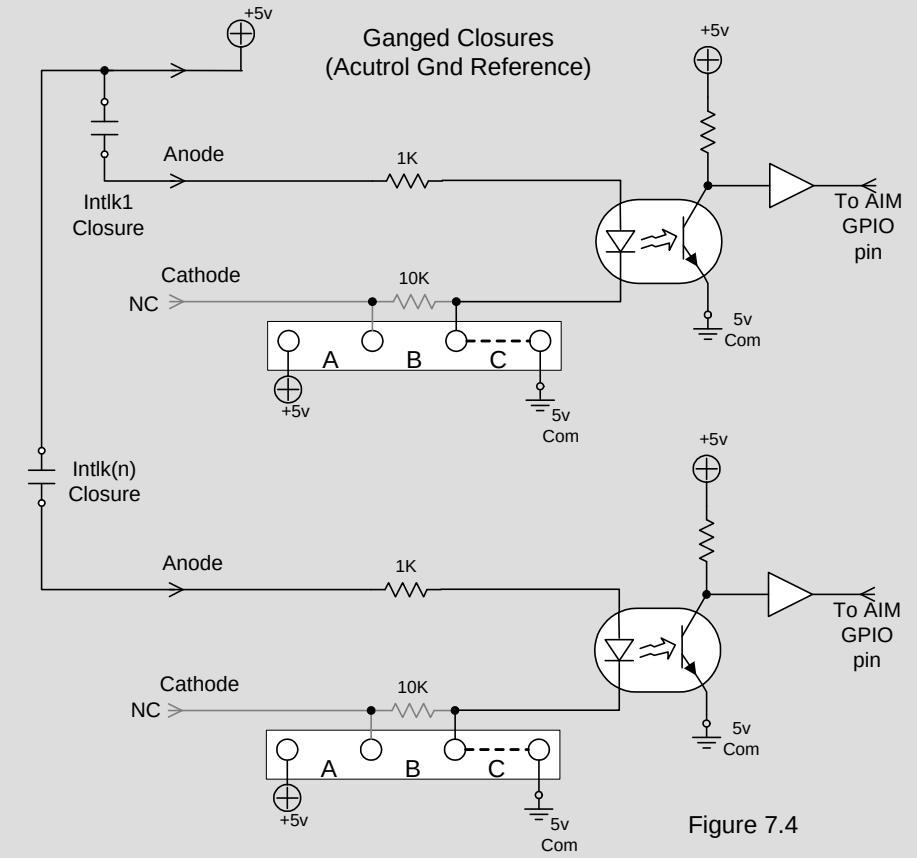


Figure 7.4

Note: each input can be configured independently as identified in the diagrams above. The jumper numbers are identified in Table 1 (Appendix A) for each input, and the system integrator is encouraged to use this table and the axis Interlock Test Register summary in Appendix B as work sheets for planning the layout of system interlocks.

3.2 Servo Interlock Configuration

This section describes the controls on the **Controls/Configure Interlock** panel and shows by example, the typical implementation of various interlock signals.

3.2.1 Servo Interlock Configuration Panel

The Controls/Configure Interlock panel is used principally by the Configurer during system integration. This panel is generally hidden from the User and may be required by the Administrator (customer) to make text preference adjustments or to implement facility interlocks in the field.

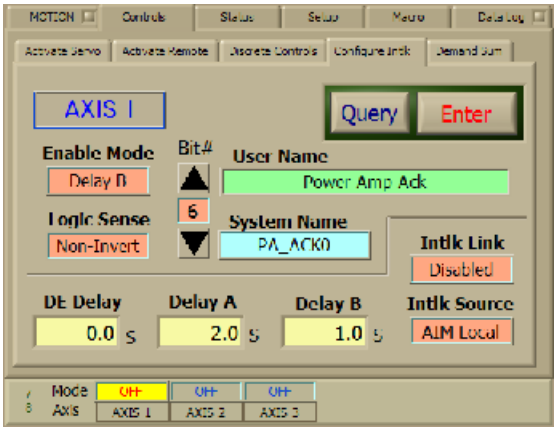
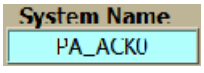


Figure 8. Controls/Configure Intlk

Whenever entering this panel (as is the case for most panels in the GUI) the current configuration state is queried to fill all of the controls/indicators with current/correct information. Even though the configuration for one bit is displayed at a time, the data for all of the bits of the specified axis are queried. This means that multiple bits can be modified without requiring that the changes be entered after each bit configuration; however, one must be sure to Enter changes before selecting a different axis or leaving this configuration panel to avoid loosing the pending changes.

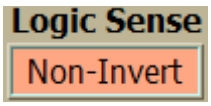
The Axis indicator identifies which axis is being configured and the selected axis can be changed using the AXIS SELECT and STATUS BAR at the bottom of the screen. Clearly the setup of fail-safe interlocks in the hardware of the Axis Interface Modules is done independently for each axis. Consolidation of axis and system signals is accomplished in the circuitry of the Transition panel and provides Acutrol Act2000 compatibility.

To configure a specific interlock bit, first step to the appropriate interlock bit using the Bit# selection control. The selection range of the Bit# is form 0 to 15.



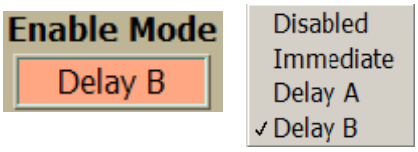
The System Name indicator identifies the source for the interlock test signal.

The User Name control provides the means to customize the interlock bit name for the application. Text may be entered using a USB keyboard if one is available, or it may be entered using the GUI touch keyboard (**Kbd** button in the display toolbar at the top of the screen). Descriptive text is saved with the RT computer configuration and is integrated into the Interlock Fail status display.



The Logic Sense control allows for inversion of the interlock signal to make it compatible with the fault test logic and/or status indication. To configure this control, first determine the logic sense of the raw interlock signal after passing through the opto-isolation input circuitry. If this is not consistent with proper interlock behavior then select the alternate sense in the Logic Sense pick box. Fail-safe interlock signal convention requires current flow to represent a safe condition; these signals do not require inversion for proper operation. Be sure to verify the sense of an interlock signal by operating the physical sensor (if possible) and monitoring the indicated state in the **Status/Interlock Fail** status display. A red lighted indicator implies the interlock is in the faulted state; if the status indication is inconsistent with the sensor then the Logic Sense may be reversed. Be sure to verify that the latched Servo Fault has been reset to avoid confusion.

Figure 9. Status/Interlock Fail

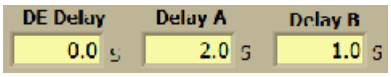


The **Enable Mode** control provides the means to specify the method that the AIM logic uses to test the interlock bit whenever an axis is first servoed.

- **Disabled** means that the bit is not used in the Interlock test; it is still accessible for status monitoring. The High/Low servo gain selection is an example where the status is used to control another function but does not affect the safety interlock test.

- **Immediate** mode is selected whenever an interlock bit must be satisfied both initially and during normal servo operation. A typical example is a motor over-temp interlock.

- **Delay A, Delay B** test modes are used when an interlock bit may not be satisfied at the time that the axis servo is activated. The interlock test is delayed by the time defined in **Delay A** or **Delay B** control beginning at the time that the servo “CLOSE” is initiated.



Delays are all scaled in seconds and have a command resolution of 0.1 seconds.

All delays are referenced to the time that the servo “CLOSE” is initiated for the axis; this is also the instant that the drive enable **DE1** is asserted. The Drive Enable Delay **DE Delay** specifies the delay of **DE0** after **DE1**.

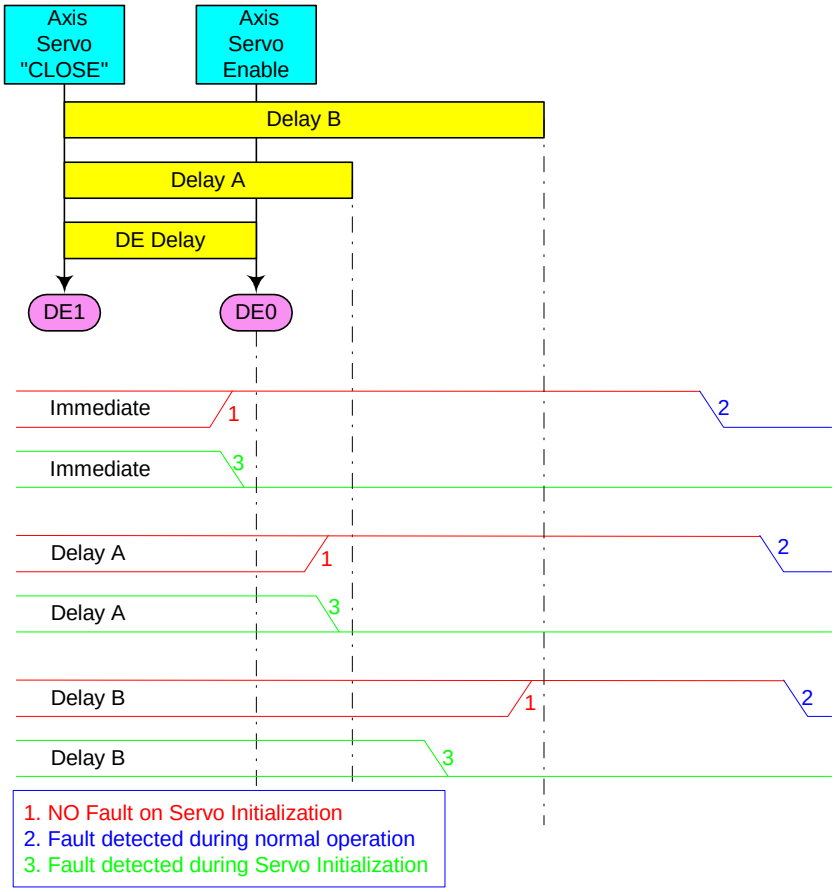
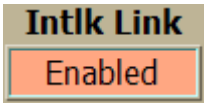


Figure 10. Drive Enable Delays

Drive Enables **DE0** and **DE1** are output through relay buffers to the instrumentation outside the Acutrol3000 chassis and are generally used to automatically enable servo related processes such as turning ON/Off electrical/hydraulic power sources (**DE1**) or enabling power amplifier/drives (**DE0**).



A hardware connection (link) in the AIM Sync connector provides a “wired-OR” logic signal that has the option to link two or more AIMs. This signal is called the Servo Interlock Link and its logic state is reported to the failsafe interlock structure on Bit14 for fault testing. Enabling the **Intlk Link** control on an axis allows the axis (servo enabled state) to participate in the interlock. The logic of this interlock signal is as follows: *All axes, whose **Intlk Link** is enabled, must be servoed for a safe operating state to be indicated. Or*

inversely, if any of the axes has a fault, then the Servo Interlock Link interlock will report a fault. Whether or not an axis shuts down when this interlock signal indicates a faulted state is solely dependent on the configuration of the Servo Interlock Link for each axis. Bit14 must be enabled in the interlock test for each axis that is to be linked and the test mode must be a delayed test so that all axes have a chance to servo before testing.

3.2.2 Servo Interlock Examples

In the following example panel, Axis 1 Interlock BIT0 is configured as an axis interlock string consisting of three series connected switches which include a CW position limit, CCW position limit, and a (home) position stow lock. This circuit is connected to Axis1-INTLK1 input on the Discrete Input connector on the back of the Acutrol3000 chassis. If any of the switches in the string is opened, a fault is indicated and servo operation is immediately terminated on this axis. The string interlock is fail-safe logic by definition and does not require inversion. Because the axis could be in a position limit while unservoed, the fault test is delayed by two seconds to give the servo a chance to move the axis away from the limit and into a safe operating zone where the position limit switch/string is satisfied.

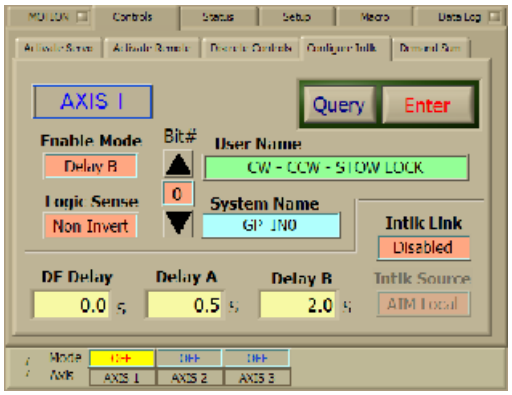


Figure 11.1 Controls/Configure Intlk

In this second example, Bit6 inputs the Power Amp Acknowledge signal form a power amplifier. The use of a 2 second **DE Delay** is required to allow the power amplifier AC power to be enabled by **DE1** relay closure, and to give the DC bus a chance to stabilize. The time difference (3.0 – 2.0 = 1.0) between **Delay A** and **DE Delay** leaves 1 second for the amplifier to acknowledge proper/safe operation before a fault is detected. If for any reason, the power amplifier removes the Power Amp Acknowledge, a fault will be detected and the axis will be unservoed immediately.

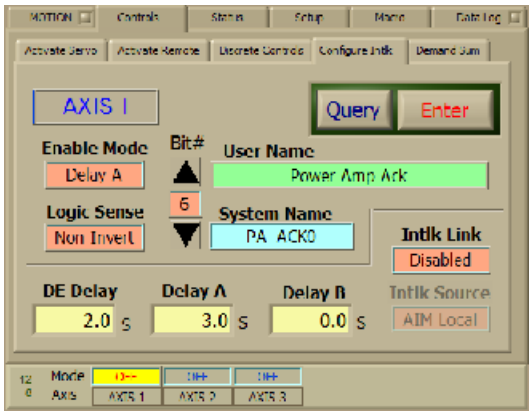


Figure 11.2 Controls/Configure Intlk

3.3 Optional I/O Utilization

As stated earlier, the use of General Purpose I/O pins has a default configuration, which utilizes four pins for input and two pins for output. This arrangement satisfies a large percentage of system configuration requirements. However, a system may require that an axis deviate from this default configuration by trading off the mix of inputs and outputs. Configuration options are programmed in the Transition panel using jumpers and in the AIM by programming configuration registers using the GUI or ACL commands. The sections below describe the configuration options for three specific signal groups.

3.3.1 Auxiliary Servo Interlocks

The Auxiliary Servo connector on the AIM contains two opto-isolated inputs that are routed to the fail-safe interlock register for fault testing. These signals are Intlk1 and Intlk2, which correspond to bits 7 and 8 respectively in the AIM Interlock Test Register, see Appendix B.

These signals can be configured via jumpers to return signals from either Global Interlocks in the digital input connector or to return ServoB Power Amp Acknowledge/Fault signals. ServoB connector is generally used whenever a system has two independent motor/drives for an axis; the default jumper configuration connects to the Global Interlock signals. The Jumper settings are defined in Table 5 below:

Jumper Number	Position “A”	Position “B”
JPX15 JPX16	Global INTLK1	ServoB PA Fault
JPX17 JPX18	Global INTLK2	ServoB PA Acknowledge

Table 5. Aux Servo INTLK Jumper Options

Note: The “X” in the jumper designation corresponds to the AIM number.

3.3.2 General Purpose I/O Pin options

Two General Purpose Discrete pins can be used in various ways and are configured in the hardware of the Transition panel using jumper plugs. Whenever these pins are configured as outputs, they are connected to relays which provide software controlled contact closures in the Discrete I/O connector (J1) on the back of the Acutrol3000 chassis. Whenever one of these pins is configured as an input, then it can be jumpered to an opto-isolated input and controlled by signals connected to the Discrete Input Connector (J2) also on the back of the chassis.

GPD4 is configured as an output by the default installation of jumper JPx04-B and controls the state of AIMx Relay2 closure. Each AIM/axis has independent control of its corresponding Relay2 closure. Alternatively, installing JPx04-A connects GPD4 to the Global INTLK3 opto-isolated input. Any combination if axes can be configured as inputs and connected to this input as a safety interlock. Axes not connected as inputs can still be used to control its corresponding relay closure. Under all circumstances, care must be taken to ensure that GPD4 pins are properly configured as inputs before JPx04 is set to the input position (A).

Option	JPx04	GPD4
Global INTLK3	A	Input
AIMx-Relay2 (default)	B	Output

Table 6. GPD4 Jumper Options

GPD5 is configured as an input by default with the installation of jumper JPx05-A. In this configuration, AIMx-INTLK4 is connected to GPD5 independently for each corresponding AIM/axis. A link option is provided to connect multiple GPD5 pins to a selected interlock input and function as a global interlock. The *master* axis that sources the INTLK4 input is installed with jumpers JPx05-A and JPx05-C; the *slave* axes have only JPx05-C installed.

GPD5 can be configured as an output and connect to AIMx-Relay3 by the installation of a jumper in JPx05-D (other jumpers A, B, and C should be removed). Be sure to set the jumper prior to changing the direction of the GPDx pin to an output to prevent a hardware gate conflict.

Option	JPx05	GPD5
AIMx-INTLK4 (default)	A	Input
AIMx-INTLK4 (global master)	A & C	Input
AIMx-INTLK4 (global slave)	C	Input
AIMx-Relay3	D	Output

Table 7. GPD5 Jumper Options

3.3.3 Drive Enable Options

Whenever an axis is servoed, the Drive Enable1 (DE1) signal is asserted immediately for that axis. If a Drive Enable delay is programmed in the **Controls/Config Interlock** panel, then the Drive Enable0 (DE0) will be asserted after the corresponding delay has timed out. In the Transition panel logic, the Drive Enable signals are the source for controlling the axis servoed relays. Jumpers JP5-A and JP5-B are provided on the back of the Acutrol3000 chassis to select which of the DE0 or DE1 signals should be used to control the Axis Servoed relays.

The default configuration for JP5-A & B is not installed and the axis servoed relays are normally controlled by the DE0 signals. Installing JP5-A causes the Axis servoed relays to be controlled by the corresponding DE1. Installing JP5-B causes the Any/All Axis Servoed relays to be controlled by DE1 signals.

3.3.4 Master Interlock

The Master Interlock is considered one of the most important interlocks in the system and is required to participate in the safety interlock structure. The logic sense of the Master Interlock requires that a signal (current) be applied to the input to ensure a fail-safe testing of this signal. The logic can not be reversed nor can this input be disabled or by-passed; even if the test is disabled in the AIM interlock fault circuitry, a software status test monitors the state of the Master Interlock and prevents any axis from being servoed if the Master Interlock is in a failed state.

The Master Interlock is actually a combination of the safe state of the opto-isolated Master Interlock input and the Front Panel Disable control; both of these must be satisfied to allow the system to be servoed.

A Master Interlock Output Relay provides a closure that can be used with external circuitry/logic to enable/disable system level operations. For example, running the hydraulic pump can be prevented if the Acutrol FP Disable button is in the depressed position. The closure logic of the Master Interlock Control relay can be inverted by installing JP5-C; the default is to produce a closure whenever the composite Master Interlock is in the failed state.

3.3.5 Software Detected Fault Indication

When an axis is servoed, the FP Disable control is lighted. Whenever this control is flashing it is an indication that a fault was detected in the system and an axis was shut down. When the fault was detected by hardware, the FP Disable indicator will always flash. If the fault is detected by a software test, the FP Disable indicator will flash depending on the configuration of the jumper JP5-D. This jumper is installed by default and permits the indication of both hardware and software detected faults. If JP5-D is removed, then only hardware faults will flash the FP Disable control.

After a fault, the latched interlock fault state may be cleared and an axis servoed again. Assuming the reason for the fault has been remedied, the axis will continue to be servoed, and the flashing FP Disable light should automatically stop flashing and continue in the lighted state.

4 Discrete Output Controls

This section describes the GUI controls that allow a system operator to change the state of discrete processes in the system. The Acutrol3000 controls external devices by providing programmatic control of relay closures which are output on the Discrete I/O connector on the back of the chassis. A typical example of such a discrete control is a “Brake OFF Override” required on a system that automatically clamps the axis whenever it is not servoed.

4.1 Discrete Output GPIO Pin Configuration

A maximum of three discrete relay outputs can be configured for each axis. Relay1and Relay2 are enabled in the hardware by default, and are controlled by the respective state of bits 0 and 1 of the PROGOUT register. Alternately, Relay3 can be added at the expense of INTLK4 for each axis. Since relays are connected to specific GPIO pins, the bit in the PROGOUT register that can be configured to control a relay is restricted to the GPIO multiplex selection options. The options for each relay output is summarized in Table 8 below:

Relay #	GPIO PIN	Default PROGOUT Bit	Optional PROGOUT Bit Selection
1	3	0	0, 3, 6, 9, 12, 15
2	4	1	1, 4, 7, 10, 13
3*	5	-	2, 5, 8, 11, 14

Table 8. PROGOUT Bit Options

* See section 3.3.2 to configure relay.

The panel below is used to change the configuration of the GPIO pins. This panel was first presented in section 1.3 Configuration Features without the configuration controls visible. These controls are normally hidden from the User to avoid inadvertent changes and must be enabled to adjust the GPIO configuration. This is accomplished by logging on as the Configurer in the **Setup/System/Security Level** panel.

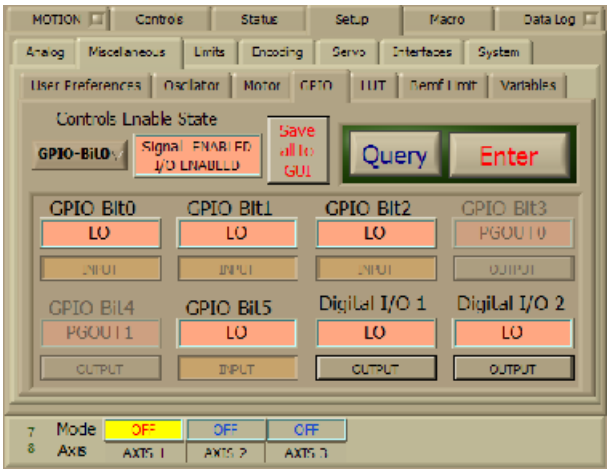


Figure 12.1 Setup/Miscellaneous/GPIO

If a grayed control needs to be changed, then it can be enabled for change by selecting the corresponding GPIO-BIT# and then selecting from the Enable pick box the Signal ENABLED I/O Enabled option. The controls associated with this GPIO pin should appear normal and allow the require modifications. In this example, GPIO-Bit4 (which is normally grayed) has been enabled for change.

Figure 12.1 Setup/Miscellaneous/GPIO

The multiplexed output of the direction of the GPIO pin can now be changed and Enter[ed] making the change in the RT configuration environment. Remember that configuration changes in the RT computer are made permanent by saving the RT system configuration in the Setup/System/SaveRestore panel.

The general rule for configuring the disabled state of the controls for the User profile is as follows: For GPIO-Bit0 through Bit5, the *direction control* should always be disabled and the *multiplex control* for pins configured as outputs should also be disabled. The multiplex signal selected on an input pin, is not used in the input process, thus it is available to be redirected by one of the Digital I/O pins to a front panel BNC.

After all configuration changes have been made, it is important to return controls to their original/appropriate disable state and to save the enabled state using the Save GUI control. To make the multiplex, direction, and enable/disable configuration permanent, enable the GUI Flash Update in the **Setup/System/SaveRestore System File Transfer** panel, and reboot the GUI computer. The GUI save and flash update procedure is not required if the current control enable configuration was not actually altered.

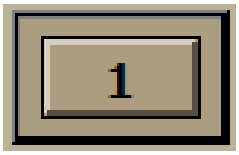
The default direction for the General Purpose Discrete I/O pins which is compatible with the default configuration of the Transition module is summarized in Table 9 below:

GPD [X] Pin	Default I/O Direction	Default MPX Selection
GPD0	IN*	LO
GPD1	IN*	LO
GPD2	IN*	LO
GPD3	OUT*	PGOUT0*
GPD4	OUT*	PGOUT1*
GPD5	IN*	LO
GPD6	OUT	LO
GPD7	OUT	LO

Table 9. GPD(X) Default Configuration

Table entries followed with a "*" are normally disabled in the User profile.

4.2 Discrete Output Control Panel Configuration



The **Controls/ Discrete Controls** panel provides the User with six (6) programmable **Function Buttons**, which are configured to control discrete functions in the system. Each button sets the desired state of the associated relay closure. The use of this panel for discrete control is very simple and provides the visual queues including Boolean text to clearly define the function and its current state. Refer to the Operator Interface User Guide TM-9388 for details of normal use.

The configuration process is very flexible in that any of the six buttons can be independently enabled and configured. Nominally one button is set to control one relay on a specific AIM board; however, a button can be configured to control the associated relay of “All” axes/AIMs present in the system.

Note that the control of a relay is done indirectly through the PROGOUT register as described in Section 1.1 System Level Overview. Each button can be configured to control the state of any of the 16 bits in the AIM PROGOUT register which in turn must be configured as the source for controlling the associated GPIO (output) pin and relay (see previous section).

The **Controls/Discrete Controls** panel as shown below has the configuration controls exposed so that changes can be made to the button configuration. These controls are normally hidden from the User to avoid inadvertent changes and must be enabled to adjust the Discrete Control configuration by logging on as the Configurer in the **Setup/System/Security Level** panel.

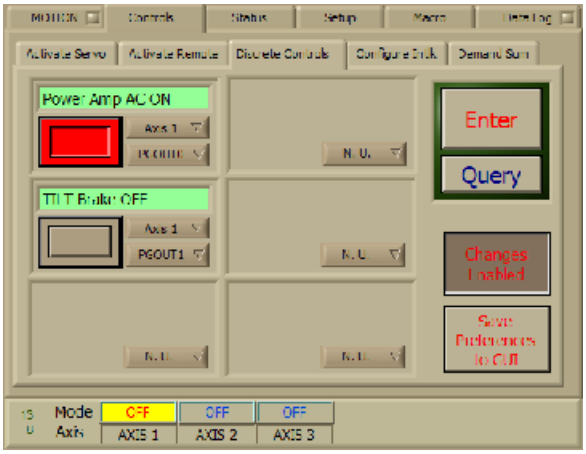
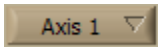


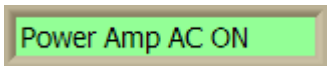
Figure 13. Controls/Discrete Controls

To change the configuration of a Discrete Control Button, ensure that the **Changes Enabled** control is selected. Controls that were grayed should become active. When a **PROGOUT** control is set to “N.U.” (Not Used), the discrete control button is disabled and the associated controls are hidden.

Select a bit in the **PGOUT** pick-box to enable/define an association between the Function Button and the PROGOUT register.



From the **Axis** control, select the Axis/AIM that is to control the Transition panel relay of interest. At this point it is appropriate to verify that toggling the Function Button changes the corresponding relay and the system function operates as expected.



The Descriptive Text indicator/control always displays the text that corresponds to the queried state of the associated PROGOUT register bit. When attempting to change the custom text, first ensure that the button is in the state that corresponds to the appropriate physical state of the controlled process. Do not change the text if the **Function Button** is flashing; this condition must be cleared by the **Query** or **Enter** operation. Next, select the GUI touch keyboard (**Kbd** button in the display toolbar at the top of the screen) and enter the appropriate text in the touch keyboard. Transfer this text to the (green) Descriptive Text control by touching the control. Toggle the **Function Button** then **Enter** to select the other discrete state. Edit the text for this function state and transfer it to the Descriptive Text control as before. A USB keyboard cannot be used for this text entry operation. Test the Function Button and verify that the correct text is indicated for the corresponding functional operation in the system.

After all configuration changes have been made, it is important to save the configuration of the **Axis** and **PGOUT** controls and the **Descriptive Text** indicator using the Save GUI control. To make these changes permanent, enable the GUI Flash Update found in the **Setup/System/SaveRestore** System File Transfer panel, and reboot the GUI computer.

Since the discrete control relays are connected to external hardware, it is important that the power on state be defined and applied whenever the system boots. The relays are inactive during the boot process and are guaranteed not to produce transient closures during this process. The power up state can be set to either “open” or “closed” contacts and are preserved by saving the real time configuration with the system in the default state; the preferred state is for a relay contact to default to the “open” contact state. Configuration changes in the RT computer are made permanent by saving the RT system configuration in the **Setup/System/SaveRestore** panel.

EXAMPLE: In the example panel above, the upper left button is used to remotely control the AC power of the power amplifier. The power is currently ON as indicated by the lighted button and Bit-0 of the PROGOUT register is active; the actual value of Bit-0 is a logic “0” because the relays in the Transition panel are powered from the +5 volt supply and are active when pulled to ground by a PGIO pin. From the default configuration of the GPIO pin, described in the previous section, GPIO-3 is connected to Relay1 on Axis1 and provides the closure on pins 7 and 26 of the Discrete Output connector J1 on the back of the Acutrol3000 chassis see Appendix.

The relays used in the Transition Panel provide a Form-A contact with a rating of 100 V DC at 0.5 Amps.

5 Discrete Status

5.1 Interlock (Fault) Status

The Interlock Fault Status (IFS) consists of one 16-bit status word per axis, which is dedicated to reporting the fail-safe servo operation of the hardware interlocks. Live status is reported whenever an axis is not servoed, and the Servo Fault (Abort) state has been reset. If an axis is servoed and a hardware fault is detected, the fault state is captured and reported in the Interlock (Fault) Status word.

Figure 14. Status/Interlock Fail

5.2 Discrete Output Status

5.3 System Status

System status is managed in the Acutrol3000 using the protocols of the IEEE488.2 Instrumentation Interface standard. The Top Level Status (STB) corresponds to the Status Byte register and summarizes the major sub-systems of the controller. These are indented at the first level in the illustration below and include System Interlock, Axis Control Processor, Supervisor, Remote Interface, and Standard Event sub-systems. Under each sub-system summary there are either lower level summary words or discrete status words. The size of all discrete status words is 16 bits and generally a bit defines a unique state or event in the system.

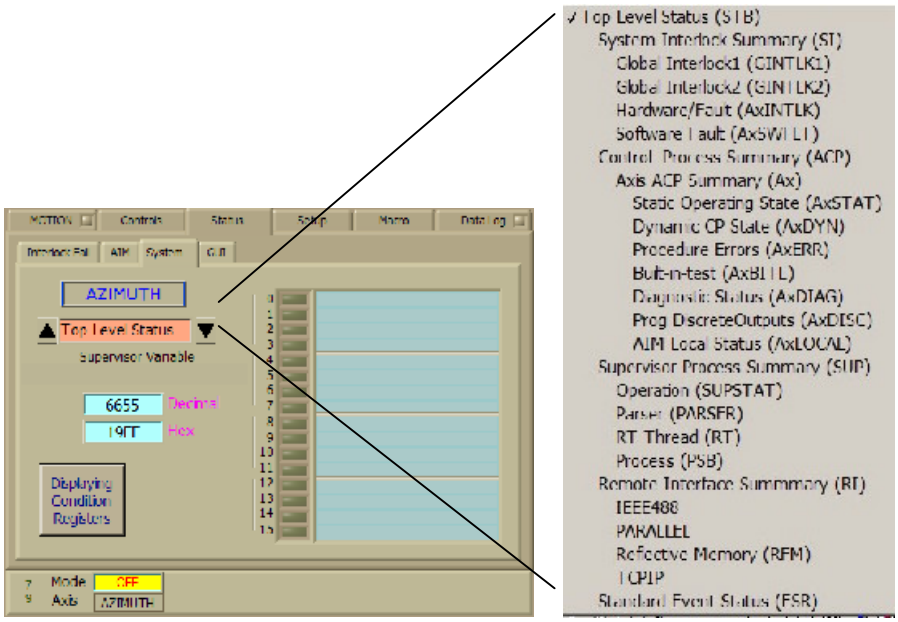


Figure 15. Status/System – Top Level

A detailed description of monitoring status via the IEEE interface is described in TM-8004 ACUTROL 3000 Command Language Programming Manual and in the IEEE488.2-1987 Instrumentation Interface Standard.

5.3.1 Status Monitor Operation

The Supervisor reviews the discrete status of the entire control system on each processing frame and updates Condition Registers that reflect the live status of the system. In the GUI **Status/System** panel, there is a control (visible in the figure above) that selects either the live status of the selected Condition Register or the latched status of the corresponding Event Register. The default mode in the GUI is to display the latched Event status and the associated controls. An Event Register records the occurrence of a change of state of any of the bits in the associated Condition Register.

The “Displaying Condition Registers” control is selected to view status bits that change dynamically/routinely such as the **AxDYN: +Rate Limit**. These status bits are of the type that come and go during the normal operation of the system, and do not usually include system states that are considered faults, which result in interrupting the servo.

Captured transient states are displayed by selecting the “Display Event Registers” control. An additional control is made visible on the GUI panel that permits resetting all of the Event Registers allowing future events to be captured.

When traversing through the status tree after the occurrence of a system fault, the Event Registers should be selected so that a transient fault can be identified. A typical example is a software detected Rate Trip fault whose live status is cleared when the velocity of the axis fall below the trip threshold.

Fig 16.1 Normal operation (live status)

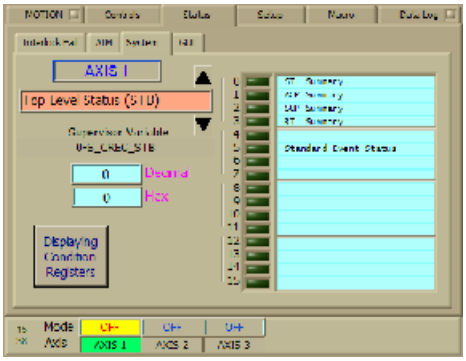


Fig 16.2 System Interlock Fault detected

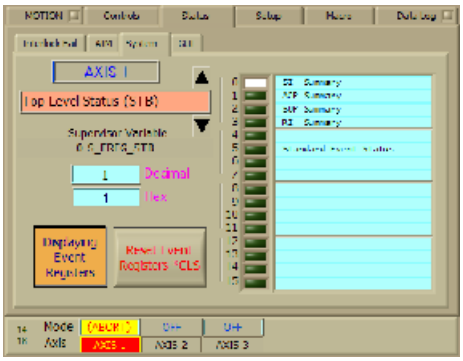


Fig 16.3 Software Fault detected on axis1

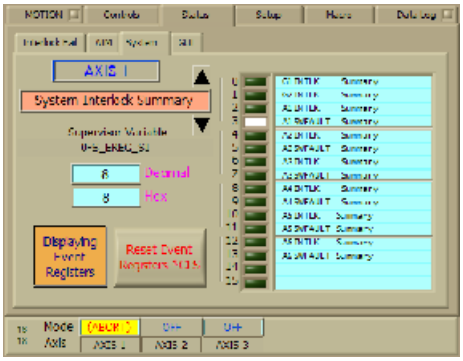
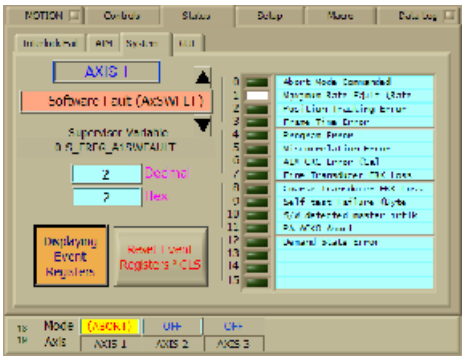


Fig 16.4 Rate Trip fault identified



5.3.2 Additional Status Access

The discrete status words and the associated bit functionality is described in detail in Appendix B of the Command Language Programming Manual TM-8004. The Condition Registers and the Event Registers can be read via the IEEE422.2 or any of the supported interfaces using the ACL command:

ACL :Status:ESR? *<register ID>,<bit #>*

Also, the status registers have supervisor variable numbers and can be read using the ACL command:

:Read:Variable? <variable>

or selecting and displaying a status variable in a readout window in the GUI (hexadecimal format).

5.4 AIM Status

The Axis Interface Module Status reports the state of the internal registers of the AIM. The registers provide an unaltered view-port into the operation of the FPGA logic. A set of 17 registers may be examined for each axis and the types of registers fall into (3) categories: status, configuration, and controls.

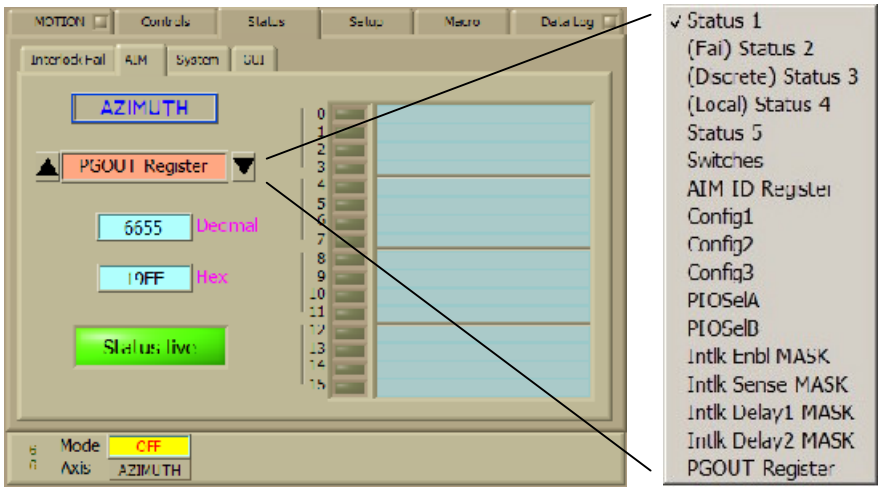


Figure 17. Status/AIM

This manual does not provide exhaustive explanations of the aim status because most of the relevant information from the AIM registers, necessary for setting up or operating a system, is processed into either the Fail Status or the System status. The principal use of these registers is for advanced system integration and/or as a development debug tool.

5.5 Identifying Faults using the Status Panel

The **Status** panel of the GUI provides a structured approach to identify the source of an operational fault.

5.5.1 GUI⇔RT Command/Communication Faults

If a fault occurs as a result of GUI-RT command/communication, the GUI will automatically switch to the **Status/GUI** panel to alert the operator and identify the nature of the fault. If the fault is the result of a RT parsing or execution error, then a message from the RT COMPUTER will be reported in the status window. If the error is detected in the GUI then a GUI error message will be reported in the status window identifying the reason for the error, and a program location number to facilitate debugging. Selecting Help on the top menu bar while the **Status/GUI** panel is selected will display a list of GUI error messages identifying the operation that caused the fault.

Figure 18. Status/GUI

Whenever a GUI error is detected, the communication with the RT computer is suspended. After the operator has had a chance to read the message, pressing the “Clear Error” control should clear the error; the GUI communication should resume.

If an error occurs immediately after returning to the panel that caused the error in the first place, and the cycle seems to repeat, it may be necessary to temporarily cancel the auto query feature. The **Status/GUI** panel provides a control to disable this feature; select “Auto Query OFF”, return to the suspect panel and fix bad data that caused the problem. Remember to return to the **Status/GUI** panel and re-enable the auto query feature.

5.5.2 Servo Fault Identification

While an axis is servoed, the Acutrol3000 performs software and fail-safe hardware safety test. If a fault is detected, the associated axis will be shut down and the GUI will indicate a failure by flashing the axis servo indicator at the bottom of the screen (also the Disable button on the front panel will be flashing). The **Status** panel is used to identify the source of the fault.

Select the **Status/Interlock Fail** panel, if a fault is indicated then it is likely that the indicated hardware interlock is the reason for the system shutdown. Resolving the hardware condition should enable normal operation. To servo the axis, reset the fault by pressing the “Reset Servo Faults” control and re-enabling the axis servo.

If there are no faults on the **Status/Interlock Fail** panel, then the fault was not detected by the fail-safe interlock hardware, but rather it was detected by a software safety test. To find the software-detected fault, switch to the **Status/System** panel, select the Top Level Status, and display the Event Status Registers. The active bit status indicators (bright red) will identify the sub-systems that have reported a fault. All sub-systems reporting a fault should be checked. Select a sub-system summary status and identify the next level down summary status or status word.

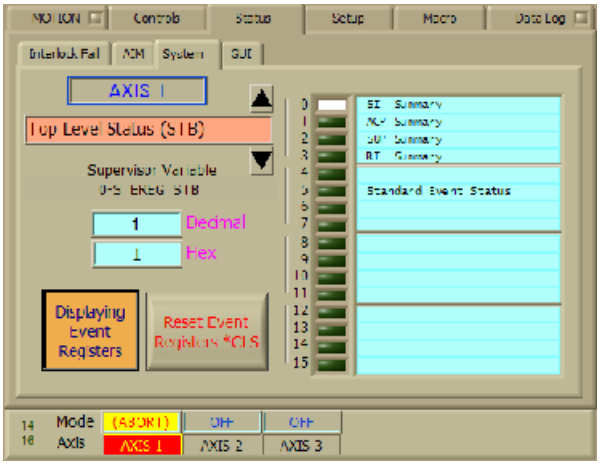


Figure 19.1 Status/System – SI Summary

Select the status word that indicates a fault and locate the source of the fault. In some cases more that one fault will be reported but usually one fault is the obvious source of a problem and the other faults are subordinate.

Figure 19.2 Status/System – SwFault

Keep following the fault indications until the reported status is at the bit level and the suspect source of the fault is indicated. If the indicated fault does not seem like the probable cause of the system shutdown, back up and follow another path of the status tree.

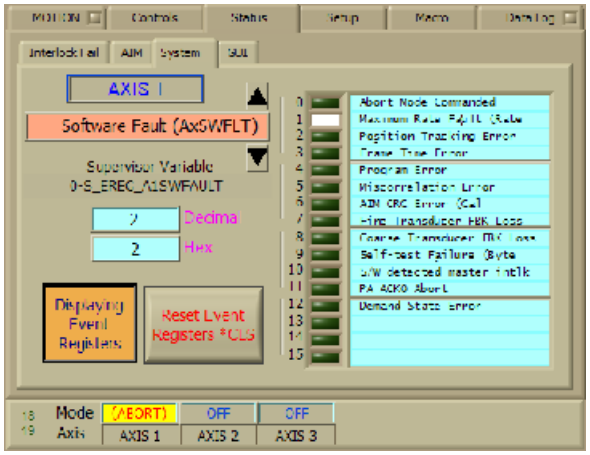


Figure 19.3 Status/System – Max Rate Fault

In this example, the Top Level status indicates a fault in the System Interlock Summary status, which in turn revels a fault in the Software Fault summary. Selecting the Software Fault (AxSWFAULT) status word indicated that a Maximum Rate Fault (Rate Trip) has occurred.

Note that the System Status panel above identifies the supervisor variable name as “0-S_EREG_A1SWFAULT”. The breakdown of this name is as follows:

- 0➔ axis 0 or Supervisor
- S ➔ Status
- EREG ➔ Event Register
- A1 ➔ Axis 1
- SWFAULT ➔ refers to the software detected servo fault register.

The Summary of Status registers is defined in detail in TM-8004 Acutrol3000 ACL Programming Manual.

6 Appendix A –Discrete Input Connector (Interlock Configuration Work Sheet)

Table 1 Acutrol3000 Digital Input Connector

Project_____

Transition Module Connector J-2 A2K counterpart is MIS-J5 (34 pins) Customer_____ DATE ___/___/____

User Interlock Name	Pin Number Ribbon	Pin Number "D-Sub"	Signal Name	Signal Source	Config[3] Jumpers	:	Comments
	1	1	GND	Gnd			
	2	20	GND	Gnd			
	3	2	AIM1-Intlk1-A	GPD0	JP100		
	4	21	AIM1-Intlk1-C	AIM(1) J8-Pin39	A B C		
	5	3	AIM1-Intlk2-A	GPD1	JP101		
	6	22	AIM1-Intlk2-C	AIM(1) J8-Pin40	A B C		
	7	4	AIM1-Intlk3-A	GPD2	JP102		
	8	23	AIM1-Intlk3-C	AIM(1) J8-Pin41	A B C		
	9	5	AIM1-Intlk4-A	GPD5	JP103	1	
	10	24	AIM1-Intlk4-C	AIM(1) J8-Pin44	A B C		
	11	6	AIM2-Intlk1-A	GPD0	JP200		
	12	25	AIM2-Intlk1-C	AIM(2) J8-Pin39	A B C		
	13	7	AIM2-Intlk2-A	GPD1	JP201		
	14	26	AIM2-Intlk2-C	AIM(2) J8-Pin40	A B C		
	15	8	AIM2-Intlk3-A	GPD2	JP202		
	16	27	AIM2-Intlk3-C	AIM(2) J8-Pin41	A B C		
	17	9	AIM2-Intlk4-A	GPD5	JP203	1	
	18	28	AIM2-Intlk4-C	AIM(2) J8-Pin44	A B C		
	19	10	AIM3-Intlk1-A	GPD0	JP300		
	20	29	AIM3-Intlk1-C	AIM(3) J8-Pin39	A B C		
	21	11	AIM3-Intlk2-A	GPD1	JP301		
	22	30	AIM3-Intlk2-C	AIM(3) J8-Pin40	A B C		
	23	12	AIM3-Intlk3-A	GPD2	JP302		
	24	31	AIM3-Intlk3-C	AIM(3) J8-Pin41	A B C		
	25	13	AIM3-Intlk4-A	GPD5	JP303	1	
	26	32	AIM3-Intlk4-C	AIM(3) J8-Pin44	A B C		
	27	14	Global INTLK1-A	Opto on AUX Servo	JP1	4	
	28	33	Global INTLK1-C	Intlk 1	A B C		
	29	15	Global INTLK2-A	Opto on AUX Servo	JP2	4	
	30	34	Global INTLK2-C	Intlk 2	A B C		
	31	16	Global INTLK3-A	GPD4	JP3	2	
	32	35	Global INTLK3-C	AIM J8-Pin43	A B C		
	33	17	Master INTLK -A	Input on Aux Servo	JP4		
	34	36	Master INTLK -C	Pin 20 (all axes)	A B C		
		18	+5 V (Fused)				
		37	HSP	Host Sync/Freeze			
		19	GND				

1. The default configuration for the GPD5 I/O pin is to input the INTLK4 signal for use as a discrete interlock for each axis. GPD5 can alternately be used as a Global interlock input or as an output to control the state of Relay closure #3.

2. The default configuration for GPD4 is as an output, which controlls the state of Relay 2. Optionally, GPD4 can input Global Interlock 3 on an axis by axis basis.

3. These Jumpers are used to configure the Opto isolated inputs for one of three cases: 24 volt logic, 5 volt logic, and floating closure (5 Volts supplied by Acutrol)

4. The default configuration for the Aux Servo Intlk1,2 opto isolated inputs is to be used as global interlocks. Current revision of the Transition Board requires that the aux-servo opto input be configured for 5 volt operation for these global inputs. Optionally, these inputs can be connected to the Servo B connector and used as classical power amplifier interlocks for a second drive/motor.

7 Appendix B – AIM Interlock Test Register (Axis Interlock Work Sheet)

AIM INTERLOCK Test Register						
REGISTER NAME: FAIL_STATUS2						
Project# _____ Axis _____ Date ____/____/____						
					INTERLOCK SOURCE	
Bit#	User Signal Name	Enable Mode*	Logic	Status Name	Local States	Multiplex
0				INTLK_STATUS0	GP_IN0	MIR0
1				INTLK_STATUS1	GP_IN1	MIR1
2				INTLK_STATUS2	GP_IN2	MIR2
3				INTLK_STATUS3	GP_IN3	MIR3
4				INTLK_STATUS4	GP_IN4	MIR4
5				INTLK_STATUS5	GP_IN5	MIR5
6				INTLK_STATUS6	PA_ACK0	MIR8
7				INTLK_STATUS7	INTLK1	MIR9
8				INTLK_STATUS8	INTLK2	MIR10
9				INTLK_STATUS9	MASTER_INTLK	MIR11
10	AIM - DMA Sync Fault	Immediate	NON-INV	INTLK_STATUS10	AIM - DMA_SYNC_ERROR	
11	AIM-RT Software Watchdog	Immediate	NON-INV	INTLK_STATUS11	AIM - SW_WD_FAULT	
12	AIM - 10 kHzCLK_WDOG	Immediate	NON-INV	INTLK_STATUS12	AIM - 10 kHzCLK_WDOG	
13	Serial Data Link	Disabled	NON-INV	INTLK_STATUS13	AIM - SDL_FAIL	
14	Servo Intlk Link	Disabled	NON-INV	INTLK_STATUS14	AIM - SIL Servo Intlk Link	
15	AIM - 10K_LOCK_FAULT	Immediate	NON-INV	INTLK_STATUS15	AIM - 10K_LOCK_FAULT	
* Enable mode options : Disabled, Immediate, Delay1, or Delay2						

8 Appendix C – GPD[X] Pin Default I/O Direction

GPD[X] Pin	Default I/O Direction	Axis 1	Axis 2	Axis 3
GPD0	IN			
GPD1	IN			
GPD2	IN			
GPD3	OUT			
GPD4	OUT			
GPD5	IN			
GPD6	OUT			
GPD7	OUT			

9 Appendix D – Transition Module Jumper Summary

Jumper Number	Default setting	Location	Function/Name	Options/Notes	Schematic Page
JP100	None	RAP-L	AIM1 - Opto Intlk1	A, B, C jumpers, see section 3.1	2
JP101	None	RAP-L	AIM1 - Opto Intlk2	A, B, C jumpers, see section 3.1	2
JP102	None	RAP-L	AIM1 - Opto Intlk3	A, B, C jumpers, see section 3.1	2
JP103	None	RAP-L	AIM1 - Opto Intlk4	A, B, C jumpers, see section 3.1	2
JP200	None	RAP-L	AIM2 - Opto Intlk1	A, B, C jumpers, see section 3.1	2
JP201	None	RAP-L	AIM2 - Opto Intlk2	A, B, C jumpers, see section 3.1	2
JP202	None	RAP-L	AIM2 - Opto Intlk3	A, B, C jumpers, see section 3.1	2
JP203	None	RAP-L	AIM2 - Opto Intlk4	A, B, C jumpers, see section 3.1	2
JP300	None	RAP-L	AIM3 - Opto Intlk1	A, B, C jumpers, see section 3.1	2
JP301	None	RAP-L	AIM3 - Opto Intlk2	A, B, C jumpers, see section 3.1	2
JP302	None	RAP-L	AIM3 - Opto Intlk3	A, B, C jumpers, see section 3.1	2
JP303	None	RAP-L	AIM3 - Opto Intlk4	A, B, C jumpers, see section 3.1	2
JP1	None	RAP-L	Global - Intlk1	A, B, C jumpers, see section 3.1	2
JP2	None	RAP-L	Global - Intlk2	A, B, C jumpers, see section 3.1	2
JP3	None	RAP-L	Global - Intlk3	A, B, C jumpers, see section 3.1	2
JP4	None	RAP-L	Master - Intlk4	A, B, C jumpers, see section 3.1	2
JP8	IN	INT		Interlock driver enable	2
JP12	None	INT	Host Sync Pulse	Header to Sync Connector (future use)	2
JP104	B	RAP-R	GPD4 Config	AIM1 GPD4, Global Intlk3, Relay2	3
JP204	B	RAP-R	GPD4 Config	AIM2 GPD4, Global Intlk3, Relay2	3
JP304	B	RAP-R	GPD4 Config	AIM3 GPD4, Global Intlk3, Relay2	3
JP105	A	RAP-R	GPD5 Config	AIM1 GPD5, Global Intlk3, Relay2	3
JP205	A	RAP-R	GPD5 Config	AIM2 GPD5, Global Intlk3, Relay3	3
JP305	A	RAP-R	GPD5 Config	AIM3 GPD5, Global Intlk3, Relay4	3
JP5	D	INT	CPLD Option Jumper	DE* (sel/mode), Master Invert, FP Fault Indication	4
JP6	A, B	INT	Power Option Header	+/- 12 Volts internal or external In/Out via Header	5
JP7	A	INT	CPLD Clock Enable	80.5 Hz clock to generate	4
JP9	A	INT	AIM Axis2 Enable	Spare1 I/O (required for auto axis enable)	4
JP10	A	INT	AIM Axis3 Enable	Spare3 I/O (required for auto axis enable)	4
JP11	None	INT	Spare2 I/O	No function at this time	4
JPx15	A	INT	INTLK1-Cathode	AIM1 Global INTLK1 or ServoB PA Fault	7, 9, 11
JPx16	A	INT	INTLK1-Anode	AIM1 Global INTLK1 or ServoB PA Fault	7, 9, 11
JPx17	A	INT	INTLK2-Cathode	AIM1 Global INTLK2 or ServoB PA Ack	7, 9, 11
JPx18	A	INT	INTLK2-Anode	AIM1 Global INTLK2 or ServoB PA Ack	7, 9, 11
JPx06	IN	INT	FRDL	Fine Resolver Drive High	8, 10, 12
JPx07	IN	INT	FRDH	Fine Resolver Drive Lo	8, 10, 12
JPx08	OUT	INT	GND	Fine Sine Feedback Shield	8, 10, 12
JPx09	OUT	INT	GND	Fine Cosine Feedback Shield	8, 10, 12
JPx10	OUT	INT		N.U.	8, 10, 12
JPx11	IN	INT	CSFS	Coarse Sine Feedback Shield	8, 10, 12
JPx12	IN	INT	GCCF	Ground Coarse Cosine Feedback	8, 10, 12
JPx13	IN	INT	GCSF	Ground Coarse Sine Feedback	8, 10, 12
JPx14	IN	INT	CCFS	Coarse Cosine Feedback Shield	8, 10, 12

10 Appendix E – Servo A Output Connector

Acutrol3000 Servo A Output Connector
Chassis Transition Module
Connector Axis1 - J12. Axis2 – J22, Axis3 – J32
ACT2000 counterpart is ECP J2

Ribbon	Sub "D"	Signal Name	Signal Source
1	1	GND	
2	14	GND	
3	2	ServoA Out 1 Hi	Aux Servo-Pin3 (AIM- AOC5)
4	15	ServoA Out1 Lo	GND
5	3	ServoA Out 2 Lo	GND
6	16	ServoA Out 2 Hi	Aux Servo-Pin6 (AIM-AOC6)
7	4	GND	
8	17	GND	
9	5	ServoA PA Fault0 (c)	Aux Servo-Pin9
10	18	ServoA PA Fault0 (a)	Aux Servo-Pin10
11	6°	(Aux) INTLK1 (c)	Aux Servo-Pin11 / ServoB-Pin5 / Global INTLK1
12	19°	(Aux) INTLK1 (a)	Aux Servo-Pin12 / ServoB-Pin18 / Global INTLK1
13	7	ServoA PA ACK0 (c)	Aux Servo-Pin13
14	20	ServoA PA ACK0 (a)	Aux Servo-Pin14
15	8°	(Aux) INTLK2 (c)	Aux Servo-Pin15 / ServoB-Pin7 / Global INTLK2
16	21°	(Aux) INTLK2 (a)	Aux Servo-Pin16 / ServoB-Pin20 / Global INTLK2
17	9*	PA ENBL0 (+)	Aux Servo-Pin17 / ServoB-Pin9
18	22*	PA ENBL0 (-)	Aux Servo-Pin18 / ServoB-Pin22
19	10*	PA ENBL1 (+)	AIM60-Pin58 / ServoB-Pin10
20	23*	PA ENBL1 (-)	AIM60-Pin58 / ServoB-Pin23
21	11	-	(Spare Pins)
22	24	-	(Spare Pins)
23	12	-	(Spare Pins)
24	25	-	(Spare Pins)
25	13	-	(Spare Pins)
26	-	-	(Spare Pins)

* Also being used/routed to the same Pin on Servo B connector.
° these signals are routed to:
- Servo B connector
- jumpers which allow them to be configured as axis or global Interlock input signals (Global INTLK 1 & 2)

11 Appendix F – Servo B Output Connector

Acutrol3000 Servo B Output Connector
Chassis Transition Module
Connector Axis1 - J13. Axis2 – J23, Axis3 – J33
ACT2000 counterpart is (none)

Ribbon	Sub "D"	Signal Name	Signal Source
1	1	GND	GND
2	14	GND	GND
3	2	ServoB Out 1 Hi	AIM60-Pin33 (AOC3)
4	15	ServoB Out1 Lo	GND
5	3	ServoB Out 2 Lo	GND
6	16	ServoB Out 2 Hi	AIM60-Pin34 (AOC4)
7	4	GND	GND
8	17	GND	GND
9	5°	ServoB PA FAULT0 (c)	Aux Servo-Pin11 /ServoA-Pin6 / Global INTLK1
10	18°	ServoB PA FAULT0 (a)	Aux Servo-Pin12 / ServoA-Pin19 / Global INTLK1
11	6		
12	19		
13	7°	ServoB PA ACK0 (c)	Aux Servo-Pin15 / ServoA-Pin8 / Global INTLK2
14	20°	ServoB PA ACK0 (a)	Aux Servo-Pin16 / ServoA-Pin21 / Global INTLK2
15	8		
16	21		
17	9	PA ENBL0 (+)	Aux Servo-Pin17 / ServoA-Pin9 (PA ENBL0)
18	22	PA ENBL0 (-)	Aux Servo-Pin18 / ServoA-Pin22 (PA ENBL0)
19	10	PA ENBL1 (+)	AIM60-Pin58 (DE1) / ServoA-Pin10 (PA ENBL1)
20	23	PA ENBL1 (-)	AIM60-Pin58 (DE1) / ServoA-Pin23 (PA ENBL1)
21	11		(Spare Pins)
22	24		(Spare Pins)
23	12		(Spare Pins)
24	25		(Spare Pins)
25	13		(Spare Pins)
26	-	-	-

° these signals are routed to jumpers which allows to configer them as axis or global Interlock input signals (DIC --> Global INTLK 1 & 2)

12 Appendix G – Discrete Output Connector

Acutrol3000 Digital Output Connector
Chassis Transition Module
Connector J1
ACT2000 counterpart is MIS-J1 (26 pins)

Pin Number		Signal Name	Signal Source
Ribbon	"D-Sub"		
1	1	GND	
2	20	GND	
3	2	AIM1 Servoed-A	AIM1-DE0
4	21	AIM1 Servoed-B	
5	3	AIM2 Servoed-A	AIM2-DE0
6	22	AIM2 Servoed-B	
7	4	AIM3 Servoed-A	AIM3-DE0
8	23	AIM3 Servoed-B	
9	5	Any AIM Servoed-A	DE0/DE1
10	24	Any AIM Servoed-B	
11	6	All AIM Servoed-A	AIM1-2-3-DE0/1
12	25	All AIM Servoed-B	
13	7	AIM1-Relay1-A	GPD3 (PGOUT3)
14	26	AIM1-Relay1-B	AIM(1)60-Pin42
15	8*	AIM1-Relay2-A	GPD4 (PGOUT4)
16	27*	AIM1-Relay2-B	AIM(1)60-Pin43
17	9**	AIM1-Relay3-A	GPD5 (PGOUT5)
18	28**	AIM1-Relay3-B	AIM(1)60-Pin44
19	10	AIM2-Relay1-A	GPD3 (PGOUT3)
20	29	AIM2-Relay1-B	AIM(2)60-Pin42
21	11*	AIM2-Relay2-A	GPD4 (PGOUT4)
22	30*	AIM2-Relay2-B	AIM(2)60-Pin43
23	12**	AIM2-Relay3-A	GPD5 (PGOUT5)
24	31**	AIM2-Relay3-B	AIM(2)60-Pin44
25	13	+5 V (Fused)	
26	32	GND	
27	14	AIM3-Relay1-A	GPD3 (PGOUT3)
28	33	AIM3-Relay1-B	AIM(3)60-Pin42
29	15*	AIM3-Relay2-A	GPD4 (PGOUT4)
30	34*	AIM3-Relay2-B	AIM(3)60-Pin43
31	16**	AIM3-Relay3-A	GPD5 (PGOUT5)
32	35**	AIM3-Relay3-B	AIM(3)60-Pin44
33	17	Master CNTL-Relay-A	Front Panel/
34	36	Master CNTL-Relay-B	Master Interlock
35	18		(Spare Pins)
36	37		(Spare Pins)
37	19		(Spare Pins)

* This relay output can be sacrificed to provide an additional optical Global input using Global INTLK3 as an input. This is a jumper option on the chassis transition module.

** This relay output can be sacrificed to provide an additional optical Global or single axis input using GPD5. This is a jumper option on the chassis transition module.

13 Appendix H – Transducer Drive and Feedback Connector

Acutrol3000 DRV - FBK
Chassis Transition Module
Connector Axis1 – J11, Axis2 – J21, Axis3 – J31
ACT2000 counterpart is ECP J1 (40 pin)

Pin Number		Signal Name	Description	Signal Source
Ribbon	"D-Sub"			
1	1	GND	Cable Shield (Drain)	
2	20	GND	Inductosyn Drive Shield	
3	2	INDH	Inductosyn Drive HI	AIM(1)60-Pin3
4	21	INDL	Inductosyn Drive LO	AIM(1)60-Pin4
5	3	FRDL	Fine Resolver Drive LO	AIM(1)60-Pin5
6	22	FRDH	Fine Resolver Drive HI	AIM(1)60-Pin6
7	4	GND	Fine Resolver Drive Shield	
8	23	GND	Analog Power common	
9	5	AV (+)	V+ Analog Power	AIM(1)60-Pin8 / exnternal
10	24	AV(-)	V- Analog Power	AIM(1)60-Pin9 / external
11	6	GND	Analog Power Shield	
12	25	GND (Jumper)	Fine Sind Feedback Shield (Open)	
13	7	FSFBKH	Fine Sine Feedback HI	AIM(1)60-Pin11
14	26	FSFBKL	Fine Sine Feedback LO	AIM(1)60-Pin12
15	8	GND	Control Line common	
16	27	GND (Jumper)	Fine Cosine Feedback Shield (Open)	
17	9	FCFBKH	Fine Cosine Feedback HI	AIM(1)60-Pin14
18	28	FCFBKL	Fine Cosine Feedback LO	AIM(1)60-Pin13
19	10			
20	29			
21	11	GND	Ground	
22	30	GND (Jumper)	coarse Sine Feedback Shield	
23	12	CSFBKH	Coars Sine Feedback HI	AIM(1)60-Pin17
24	31	CSFBL	Coarse Sine Feedback LO	AIM(1)60-Pin18
25	13	CCFBKL	Coarse Cosine Feedback LO	AIM(1)60-Pin19
26	32	CCFBKH	Coarse Cosine Feedback HI	AIM(1)60-Pin20
27	14	GND (Jumper)	Coarse Cosine Feedback Shield (installed)	
28	33	GND	Coarse Resolver Drive Shield	
29	15	CRDH	Coarse Resolver Drive HI	AIM(1)60-Pin5
30	34	CRDL	Coarse Resolver Drive LO	AIM(1)60-Pin6
31	16	ANALOGL0	Analog Input 0 LO	AIM(1)60-Pin22
32	35	ANALOGH0	Analog Input 0 HI	AIM(1)60-Pin21
33	17	GND	Analog Input 0 Shield	
34	36	GND	Analog Input 1 Shield	
	18	ANALOGH1	Analog Input 1 HI	AIM(1)60-Pin23
	37	ANALOGL1	Analog Input 1 LO	AIM(1)60-Pin24
	19			

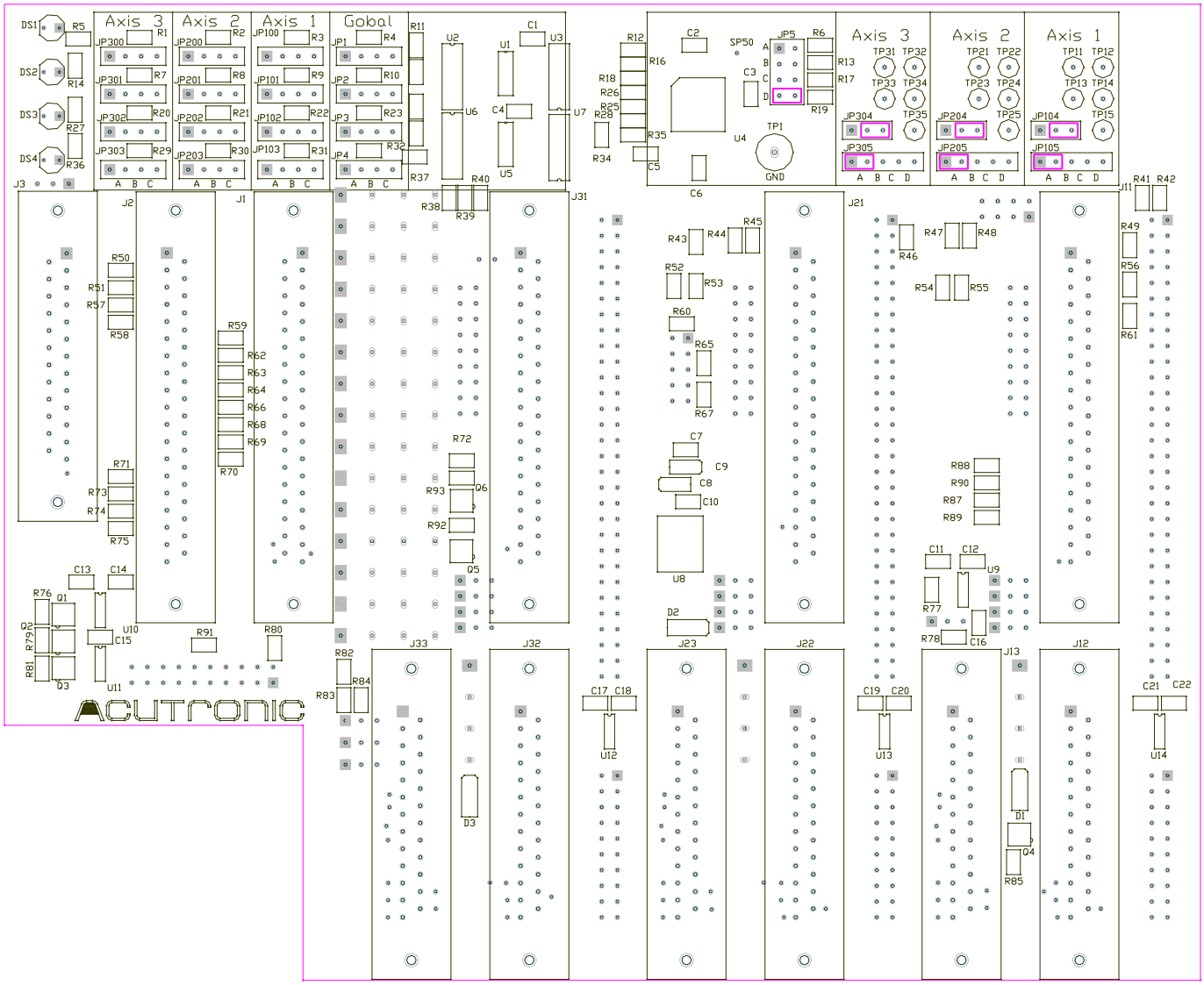
14 Appendix I – Optical Encoder/RS232 Connector

Optical Encoder/RS232 Connector
Acutrol3000 Chassis Transition Module
Connector J3

Ribbon	Sub "D"	Signal Name	Signal Source
1	1	GND	
2	14	+ 5 Volts	
3	2	AQuad	AIM(1)60-Pin49
4	15	Bquad	AIM(1)60-Pin50
5	3	Eref	AIM(1)60-Pin51
6	16	GND	
7	4	Rx	AIM(1)60-Pin59
8	17	Tx	AIM(1)60-Pin60
9	5	GND	
10	`8	+ 5 Volts	
11	6	AQuad	AIM(2)60-Pin49
12	19	Bquad	AIM(2)60-Pin50
13	7	Eref	AIM(2)60-Pin51
14	20	GND	
15	8	Rx	AIM(2)60-Pin59
16	21	Tx	AIM(2)60-Pin60
17	9	GND	
18	22	+ 5 Volts	
19	10	AQuad	AIM(3)60-Pin49
20	23	Bquad	AIM(3)60-Pin50
21	11	Eref	AIM(3)60-Pin51
22	24	GND	
23	12	Rx	AIM(3)60-Pin59
24	25	Tx	AIM(3)60-Pin60
25	13	HSP	Header to PP
26	-	-	-

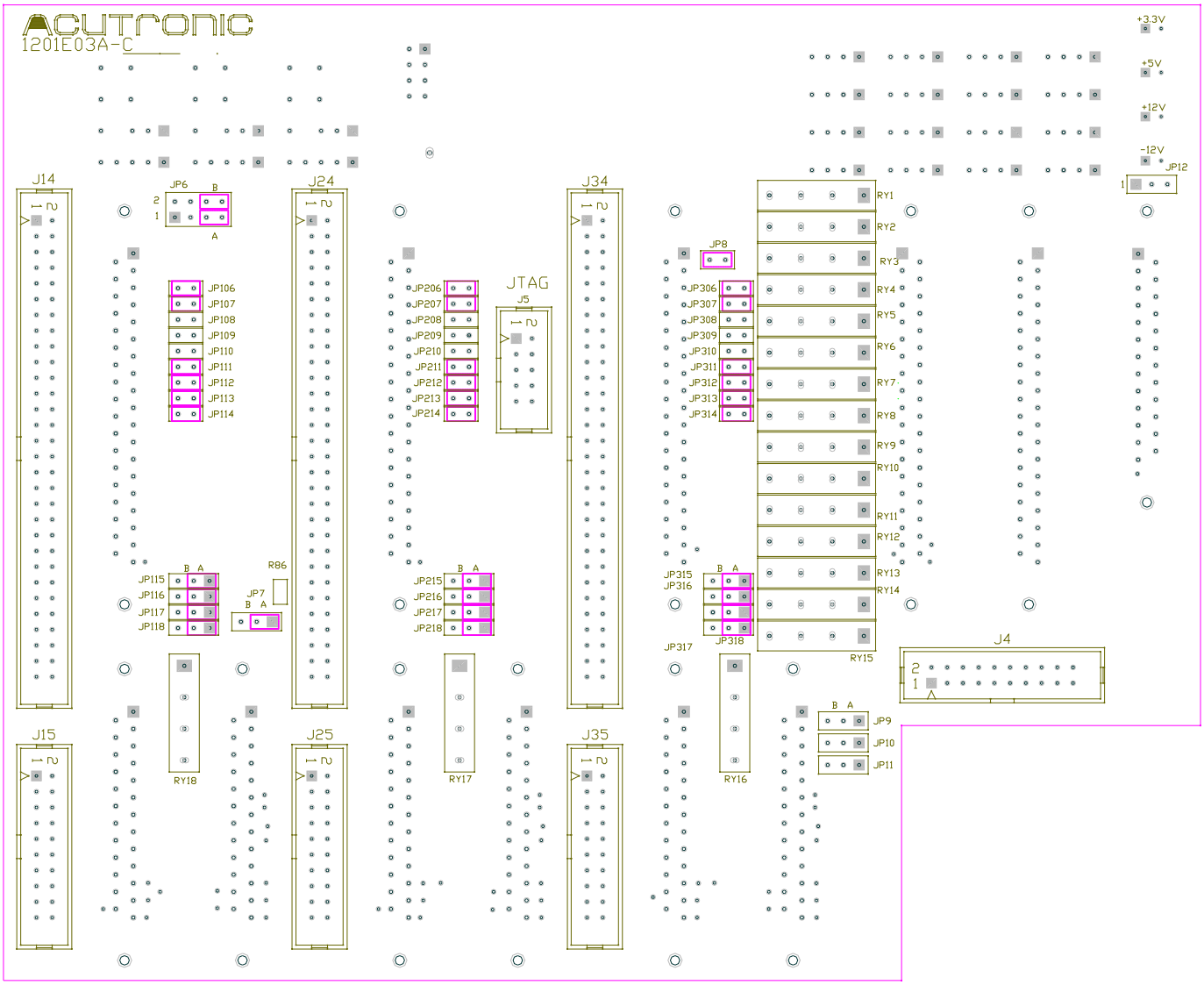
15 Appendix J - Component Side Transition Panel Assembly

This drawing shows the location and default position for the programming jumpers that that are accessible on the back panel of the Acutrol3000 chassis after removal of the jumper access cover.



16 Appendix K - Solder Side Transition Panel Assembly

This drawing shows the location and default position for the programming jumpers that that are accessible from the inside of the Acutrol3000 chassis after removal of the top cover.



17 Appendix L - Acutrol3000 Discrete I/O Overall Structure