Pontificia Universidad Católica de Chile
Escuela de Ingeniería
Departamento de Ingeniería Eléctrica
IEE2463 Sistema electrónicos programables

# Laboratorio 03

**ZYBO-Z7 Custom IP**

**Prof. Dr.-Ing. Félix Rojas - felix.rojas@uc.cl**

---

## 1. Laboratory Goals

After this laboratory, the student should:

- To understand all features and configurations of the *Create and Package New IP* wizard of Vivado.
- To create and package new IP based on a self-designed entity.
- To create and package new IP including an AXI coomunication port based on a self-designed entity.
- To integrate the self-created IP-Cores into a block design, connect the block inputs to switches and buttons and output to leds of the ZyboZ7 and validate the design.

## 2. Previous Requirements

These requirements are mandatory to perform the laboratory. Not accomplishing them count as missing the laboratory.

- You must have previously installed vitis/vivado version 2020.1.
- You must read the ZYbo Z7 Board Reference.

Note: **Version of the software 2020.1 is mandatory**. This is important to avoid compatibility problems.

# 3. Laboratory Activities

- Create a new Vivado project associated to ZyboZ7.
- Include ZyboZ7 constrains into the vivado project.
- Include a new source into the vivado project. Use the provided source for implementing this lab (LED_Controller.vhd).
- Create a new IP Core based on LED Controller Entity.
- Add the newly created IP-Core into a block design.
- Create a new IP-Core based on including AXI Lite communication protocol.
- Modify source files to properly declare and map the components (hardware) of AXI Protocol and LED Controller into the newly created IP-Core. item Add the newly created IP-Core into a block design. Verify that AXI protocol is present and that parameters available for modification in the IP-Core are the same that you selected into the design.

# 4. Complementary Homework

To fulfill this homework is mandatory, but not evaluated.

- Create a new IP-Core, namely IPCore2, with one input clock and one reset and a 32bits output. The last 4 bits of the output are randomly updated every one second. (This is IP-Core2).
- Run a *Post-Implementation Timing Simulation* for IP-Core2 and the IP-Core created in this lab (without AXI) to validate its performance. Makes changes that you consider correct to improve the design.
- Open a new vivado project and include the IP Cores created in this laboratory, and the one created by you) into the IP Catalog. For that, add the directory of the IPCores to the repository.(see image below).
- Open a new block design and incorporate the IP-Core created in this laboratory without AXI communication protocol. (IP-Core1)
- Incorporate the IP-Core2 created by yourself.
- In IP-Core1: Connect the clock to the clock pin of the zynq, the rst to a button, the cnt_disp to a switch.
- In IP-Core2: Connect the clock to the clock pin of the zynq, the rst to a button.

- Connect the output of IP-Core2 to the data_in of IP-Core1.
- validate the design in the zybo z7.

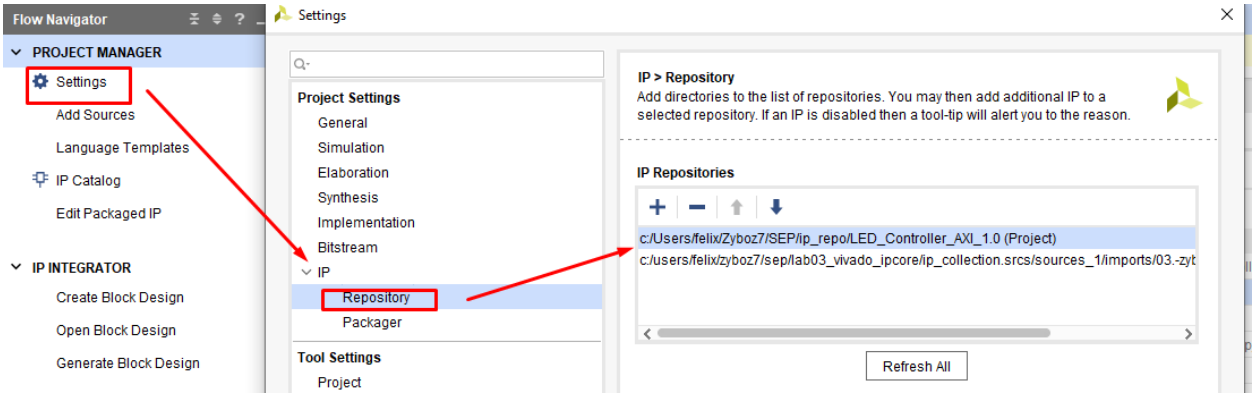


Figura 1: How to include new sources to the IP Core repository

.