Pontificia Universidad Católica de Chile
Escuela de Ingeniería
Departamento de Ingeniería Eléctrica
IEE2463 Sistema electrónicos programables

Laboratory 04

ZYBO-Z7 AXI4 Transactions

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1. Laboratory Goals

After this laboratory, the student should:

- To understand how AXI4 full and AXI4 Lite protocols work.
- How to create and understand the features of AXI Traffic Generator IP-Core.
- To understand in details the functions and mode of operation of ATG Custom profile, System Init/Test Mode.
- To understand in details the functions and mode of operation of ATG Custom profile, Advanced Mode.
- To create a simulation using 2 ATGs and one RAM memory to verify AXI4 full and AXI4-lite transactions.

2. Previous Requirements

These requirements are mandatory to perform the laboratory. Not accomplishing them count as missing the laboratory.

- You must have previously installed vitis/vivado version 2020.1.
- You must read the ZYbo Z7 Board Reference.
- You must have completed the complementary Homework proposed in LAB 03 guide.

Note: **Version of the software 2020.1 is mandatory**. This is important to avoid compatibility problems.

3. Laboratory Activities

- Create a new Vivado project associated to ZyboZ7.
- Include an ATG IP-Core from IP Catalog
- Create the example design from Vivado associated to ATG-IP Core.
- Configure the ATG components.
- Load the COE files and simulating files provided for this lab.
- Identify the Driver read and write transactions.
- Identify read and write transactions made by the Device Under Test (DUT).
- Analyze COE file and understand how we configure the transactions for the DUT and where is located the data when DUT perform a write operation and where is the data saved when it perform a read transaction.

It is very important that you complement the information given by this lab with the ATG IP COre Guide and the AMBA AXI Protocol specification guide.

4. Complementary Homework

To fulfill this homework is mandatory, but not evaluated.
Modify the COE files to:

- change the data written by the DUT.
- change the burst length to be written.
- change the burst length to be written.
- modify the number of write transactions by the DUT.
- modify the number of read transactions by the DUT.
- modify the moment of initialization of the DUT.