Pontificia Universidad Católica de Chile
Escuela de Ingeniería
Departamento de Ingeniería Eléctrica
IEE2463 Sistema electrónicos programables

Laboratory 05

ZYBO-Z7 Debugging Hardware with ILA and VIO

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1. Laboratory Goals

The goals of this laboratory are:

- To understand how to configure and set the Integrated Logic Analyzer (ILA) IP-Core.
- To understand how to configure and set the Virtual Input/Output (VIO) IP-Core.
- To run and configure ILA and VIO in Vivado.
- To understand thow to use of ILA and VIO in real time operation within Vivado.

2. Previous Requirements

These requirements are mandatory to perform the laboratory. Not accomplishing them count as missing the laboratory.

- You must have previously installed vitis/vivado version 2020.1.
- You must read the ZYbo Z7 Board Reference.

Note: **Version of the software 2020.1 is mandatory**. This is important to avoid compatibility problems.

3. Laboratory Activities

Create a new folder for this project and create a new project in vivado.

- Introduce a Binary counter. Enable the clock enable (CE) input and reset counter input (SCLR).

- Add clocking wizard and connect a 10MHz clock to the Binary counter.
- Use the slice Ip-Core to select the 4 MSB and connect them to the 4 outputs LEDs of the ZYBO Z7.
- Introduce a ILA IP-Core to watch 4 MSB connected to the LEDs and the binary counter output.
- Introduce a VIO to watch the 4 MSB connected to the LEDs and the binary counter output.
- Create three outputs of the VIO control the CR and SCRL of the binary counter and the reset of the clocking wizard.
- Use 10mHz as clock for the Binary Counter and 50Mhz for the VIO and ILA.

Generate bitstream, export hardware and program the FPGA. The Debug your design and have fun.

4. Complementary Homework

To fulfill this homework is mandatory, but not evaluated.

- Make use of trigger in and trigger out of the ILA IP Core.
- Incorporate any AXI IP Core that you have used from previous laboratories and use ILA in AXI Mode, to watch the AXI bus.