Pontificia Universidad Católica de Chile
Escuela de Ingeniería
Departamento de Ingeniería Eléctrica
IEE2463 Sistema electrónicos programables

Laboratory 06

ZYBO-Z7 Microblaze Configuration: AXI-GPIO and AXI-Timer

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1. Laboratory Goals

The goals of this laboratory are:

- To understand basic configuration of Microblaze.
- To integrate a soft-core processor into the PL part of the Zynq.
- To integrate local memory and cache memroy if needed.
- To integrate an AXI-GPIO IP-Core and connect it to switches, LEDS and/or buttons of the ZYboZ7.
- To integrate an AXI-TIMER IP-Core and understand its configuration.
- To implement a basic code into the microcontroller microblaze to tesxt the AXI-GPIO IP-Core.
- To implement a basic code into the microcontroller microblaze to tesxt the AXI-TIMER IP-Core.
- To understand main functions of libraries "xgpio.h"(associated to AXI-GPIO IPCore) and "xtmrctr.h"(associated to AXI-TIMER IPCore).
- To understand that ultimately, the only functions used to out or in information through the AXI Master port of the microblaze (or any procesor) are the *xil_out32(write_address, data)* and *xil_in32(read_address, data)* from the library"xil_io.h".

2. Previous Requirements

These requirements are mandatory to perform the laboratory. Not accomplishing them count as missing the laboratory.

- You must have previously installed vitis/vivado version 2020.1.
- You must read the ZYbo Z7 Board Reference.
- You must understand the design flow between vitis and vivado to program a microprocessor.

Note: **Version of the software 2020.1 is mandatory**. This is important to avoid compatibility problems.

3. Laboratory Activities

Part I:

- Create a new Vivado project associated to ZyboZ7.
- Include a Microblaze IP Core.
- Configure Microblaze with local memory and debug module.
- Include and AXI-GPIO IPCore with two channels of 4bits each.
- Associate the LEDs and switches to the AXI-GPIO-Core.
- Include constrain files to mapp reset, system clock, switches and leds.
- Make wrapper, run synthesis and implementation, create bitstream and export the hardware.
- Create a new platform project in Vitis with the designed hardware.
- Create a new application project in vitis,
- Program the Microblaze with the given file to blink the LEDs associated to the AXI-GPIO-Core.
- Validate your code into the Zybo Z7.

Part II:

- Go back to vivado and include an AXI-Timre IP Core.
- Validate the design and export this new hardware.

- Update the hardware in the Vitis platform Project.
- Program the Microblaze with the given file to test the AXI-Timer IP Core together with AXI GPIO-Core.
- Validate your code into the Zybo Z7.

It is very important that you complement the information given by this lab with the documents .AXI GPIO v2.0 LogiCORE IP Product Guide.and AXI "Timer v2.0 LogiCORE IP Product Guide", provided in the folder of this lab.

4. Complementary Homework

To fulfill this homework is mandatory, but not evaluated.

- Improve the code to make use of the switches connected to the AXi-GPIO IP-Core of the laboratory.
- Include a new AXI-GPIO IPCore and associate it to the buttons. Create a code taht make use of these buttons, leds and switches. Check carefully ohow the adress of this new IPCore differs from the address of the previously added AXI GPIO
- Configure the timer in cascade mode. Study this mode of operation and make use of it.
- Use the function *xil_out32(write_address, data)* to configure the timer. This exercise is very important to understand what you are really doing.