D Flip-flop

Symbol

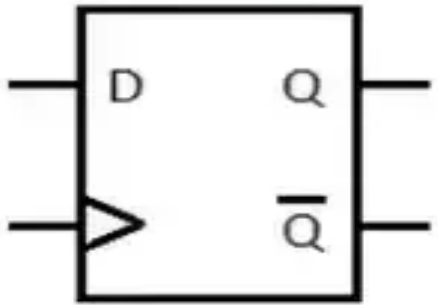
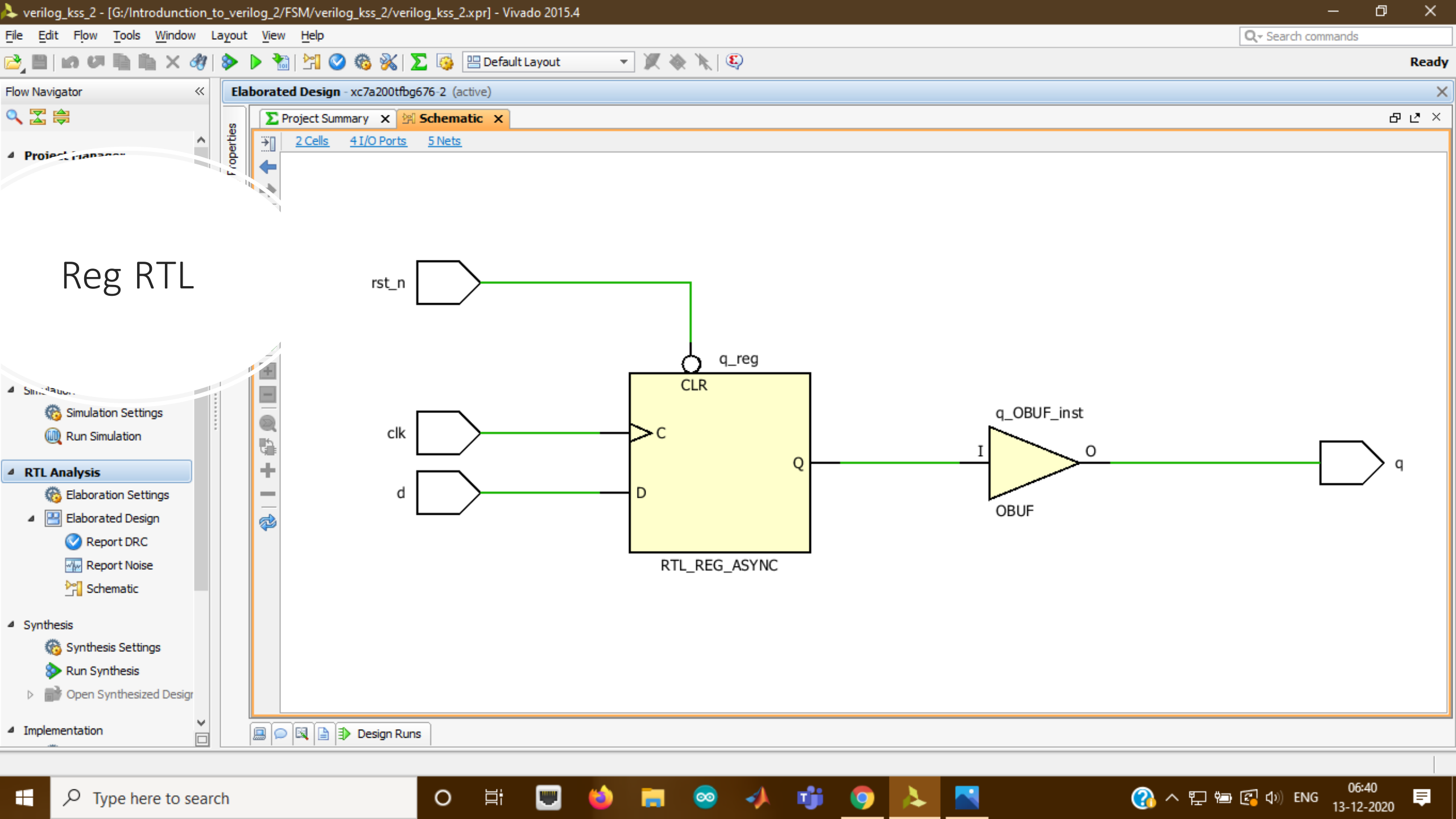


Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Reg RTL


verilog_kss_2 - [G:/Introdunction_to_verilog_2/FSM/verilog_kss_2/verilog_kss_2.xpr] - Vivado 2015.4
File Edit Flow Tools Window Layout View Help
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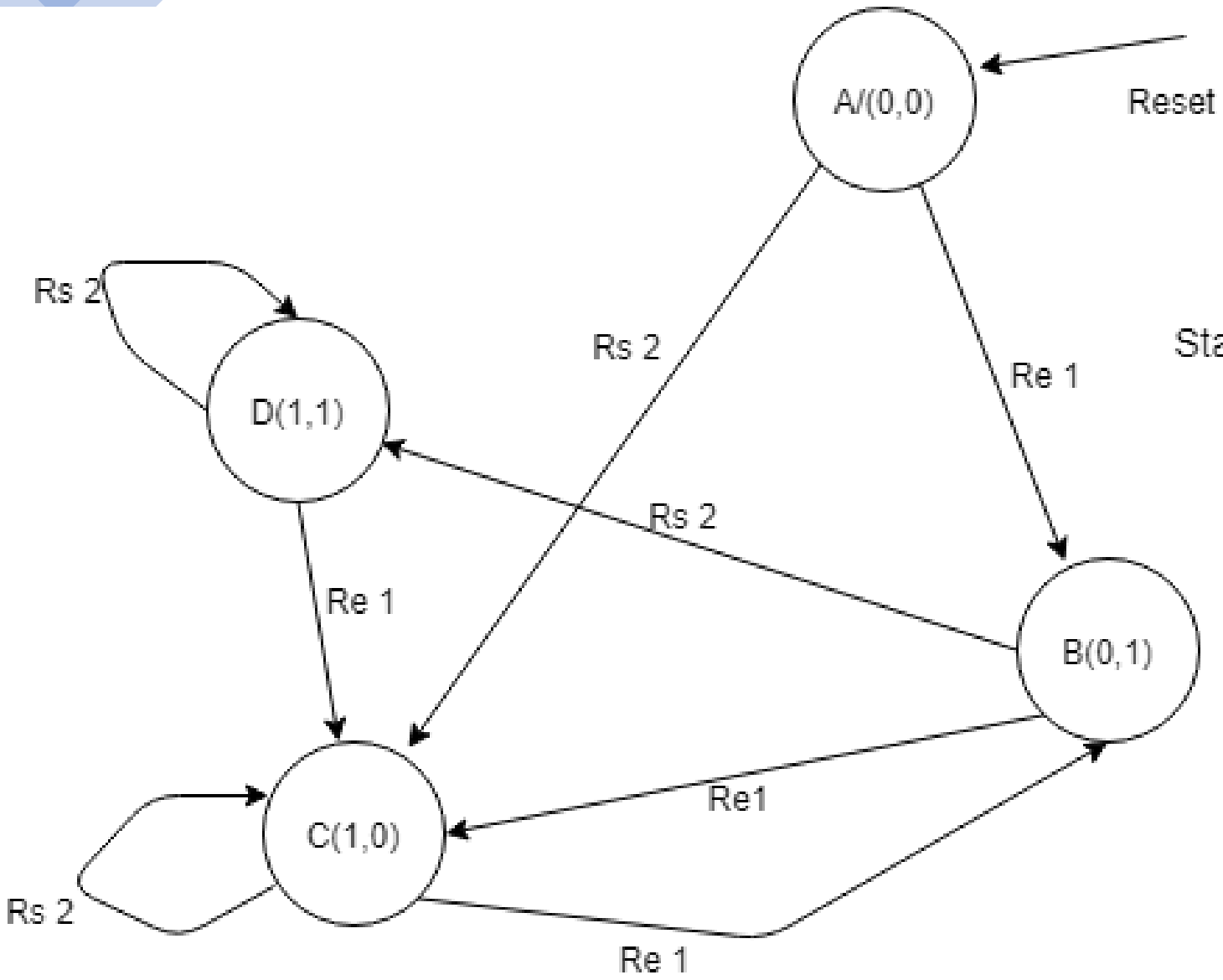
Default Layout
Ready
Flow Navigator
Elaborated Design - xc7a200tfbg676-2 (active)
Project Summary
Schematic
2 Cells
4 I/O Ports
5 Nets
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Elaborated Design
Report DRC
Report Noise
Schematic
Synthesis
Synthesis Settings
Run Synthesis
Implementation
rst_n
clk
d
q_reg
CLR
C
D
Q
RTL_REG_ASYNC
q_OBUF_inst
I
O
OBUF
q
Design Runs
Type here to search
ENG
06:40
13-12-2020

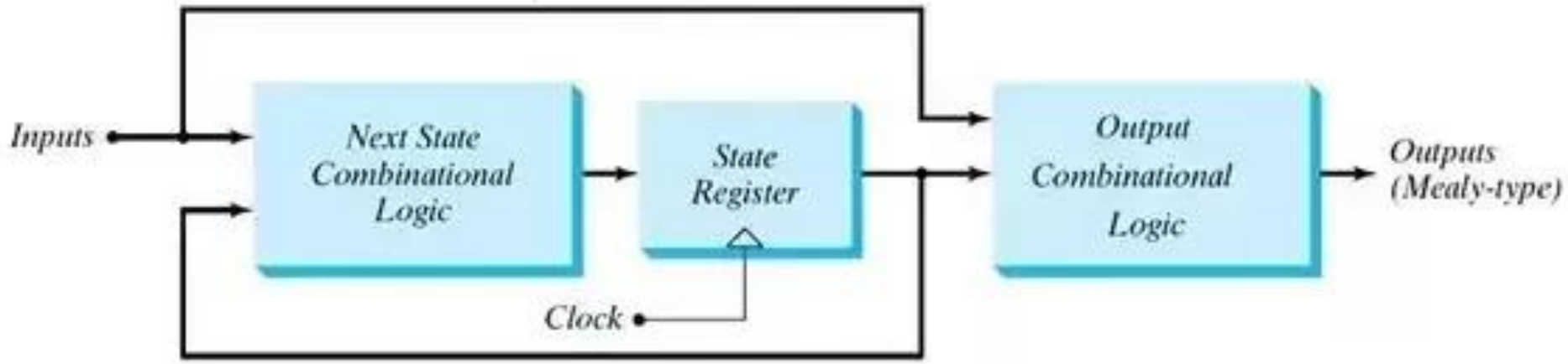


Nomenclature for state

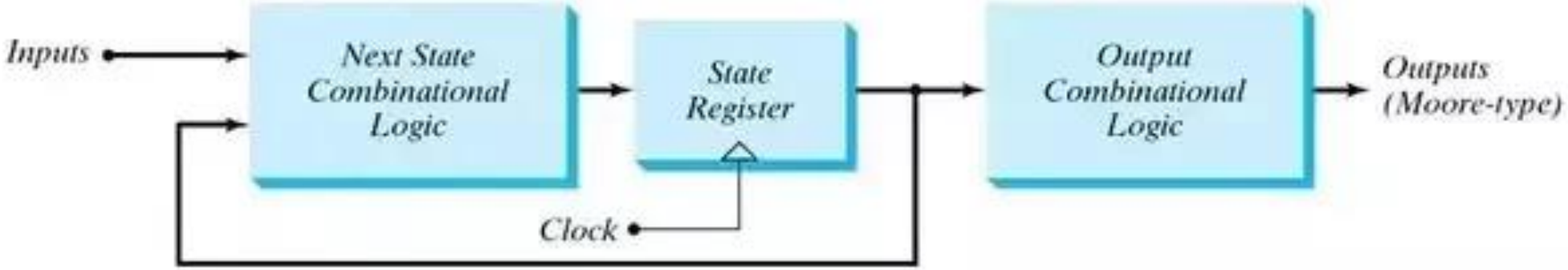
State_name (No.of candy dispatched, Change to be returned)

Candy Vending Machine

Mealy Machine



Moore Machine



verilog_kss_2 - [G:/Introdunction_to_verilog_2/FSM/verilog_kss_2/verilog_kss_2.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Help

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Default Layout

Ready

Flow Navigator

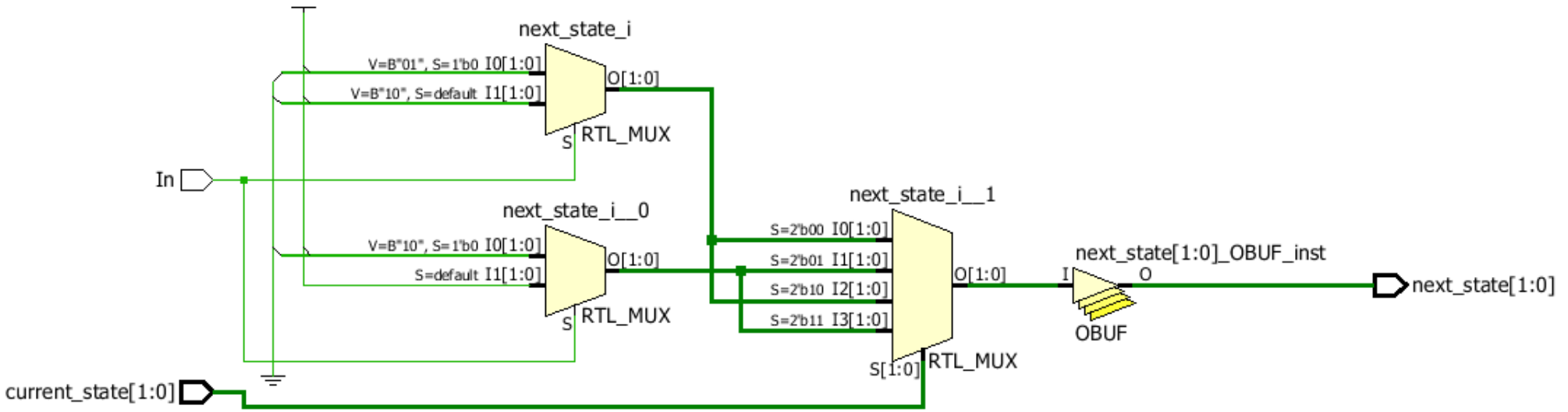
Elaborated Design - xc7a200tfbg676-2 (active)

Project Summary | Schematic

5 Cells | 5 I/O Ports | 13 Nets

Properties

Next state Logic



RTL Analysis
- Elaboration Settings
- Elaborated Design
  - Report DRC
  - Report Noise
  - Schematic

Synthesis
- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

Design Runs

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ENG 05:59 13-12-2020

verilog_kss_2 - [G:/Introdunction_to_verilog_2/FSM/verilog_kss_2/verilog_kss_2.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Help

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Ready

Flow Navigator

RTL Analysis
- Elaboration Settings
- Elaborated Design
  - Report DRC
  - Report Noise
  - Schematic

Synthesis
- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

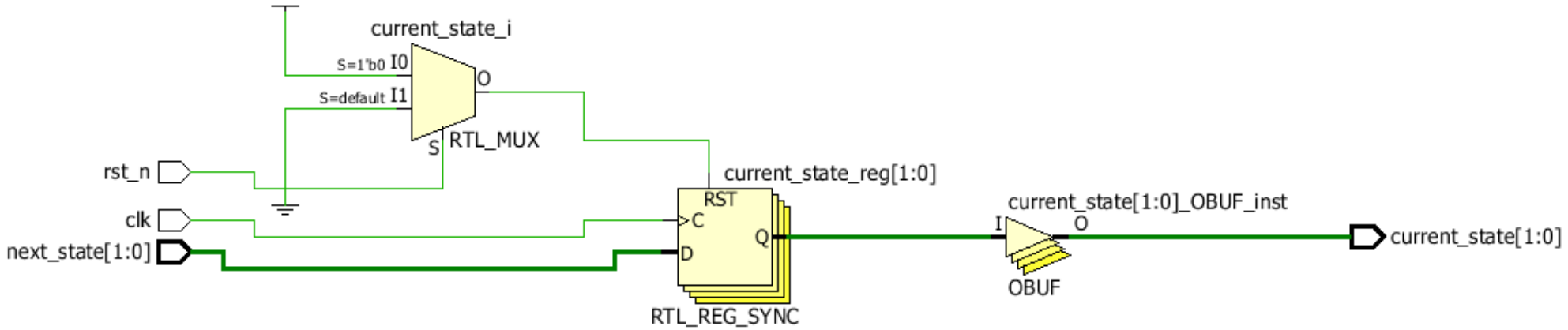
Elaborated Design - xc7a200tfbg676-2 (active)

Project Summary | Schematic

Properties

5 Cells | 6 I/O Ports | 11 Nets

Current state Reg



Design Runs

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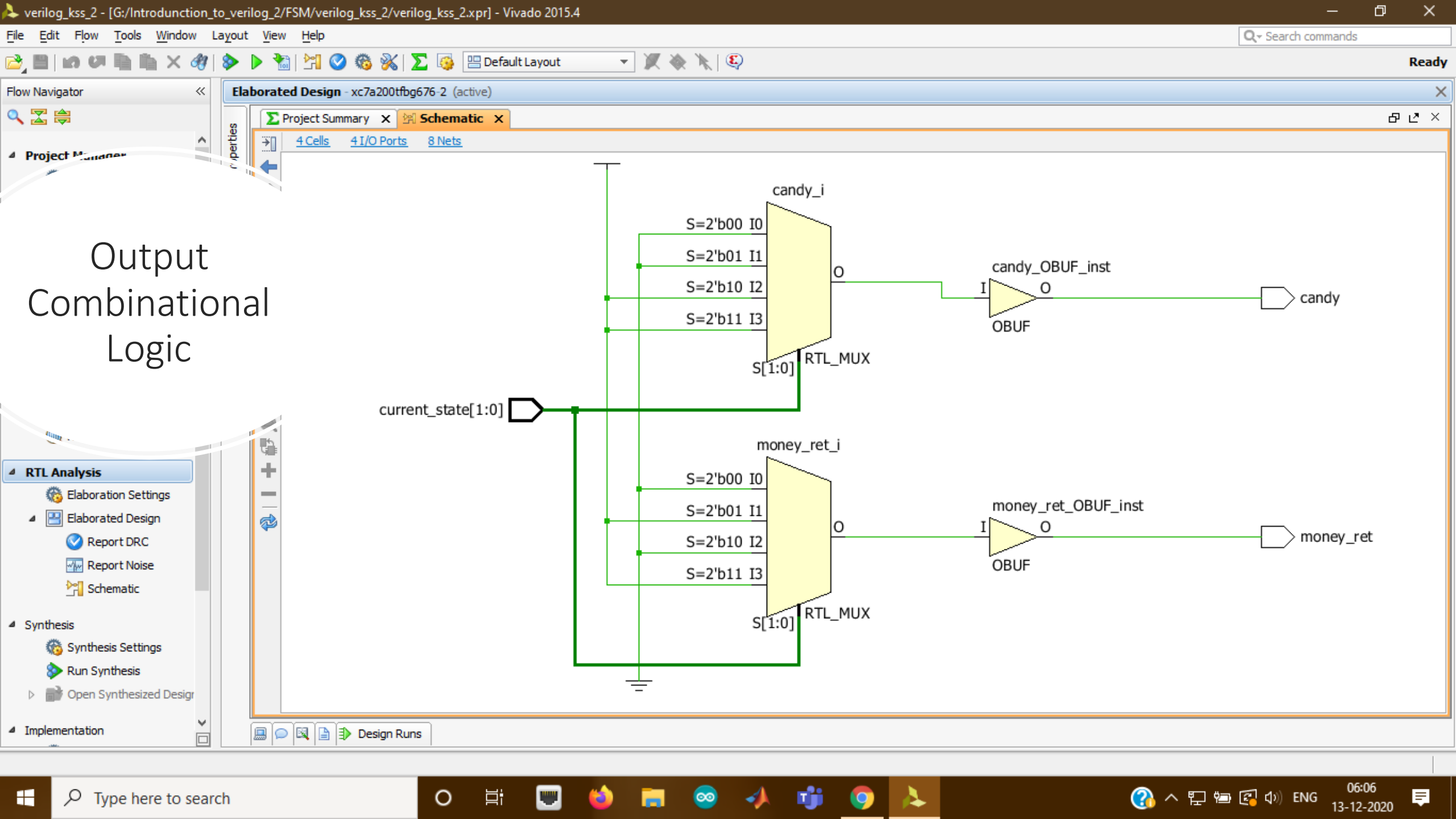
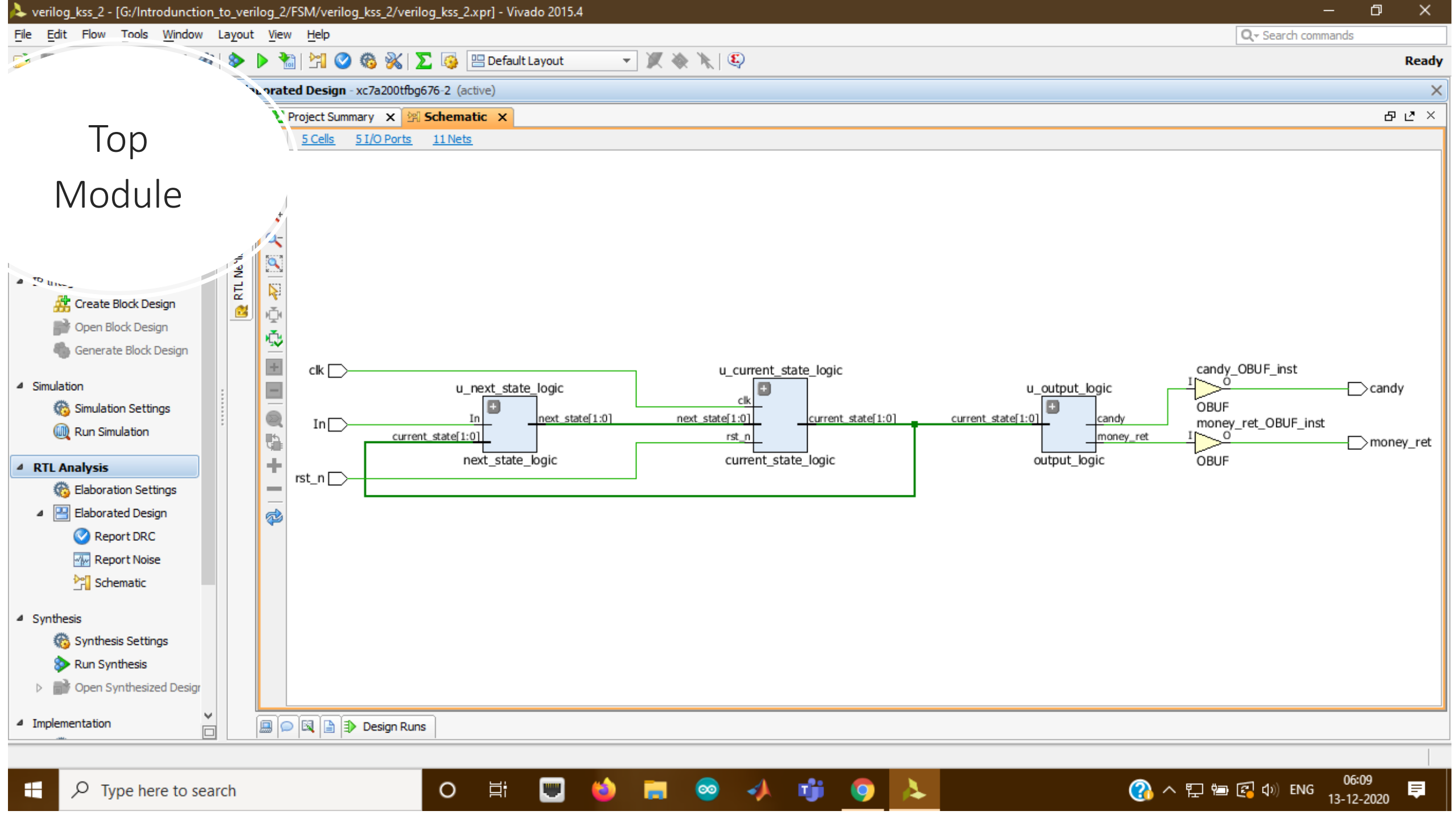
Output Combinational Logic



Top Module


verilog_kss_2 - [G:/Introdunction_to_verilog_2/FSM/verilog_kss_2/verilog_kss_2.xpr] - Vivado 2015.4
File Edit Flow Tools Window Layout View Help
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Default Layout
Ready
Project Summary
Schematic
5 Cells
5 I/O Ports
11 Nets
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Elaborated Design
Report DRC
Report Noise
Schematic
Synthesis
Synthesis Settings
Run Synthesis
Implementation
clk
In
rst_n
u_next_state_logic
next_state_logic
current_state[1:0]
u_current_state_logic
current_state_logic
u_output_logic
output_logic
candy_OBUF_inst
money_ret_OBUF_inst
OBUF
candy
money_ret
Design Runs
Type here to search
ENG
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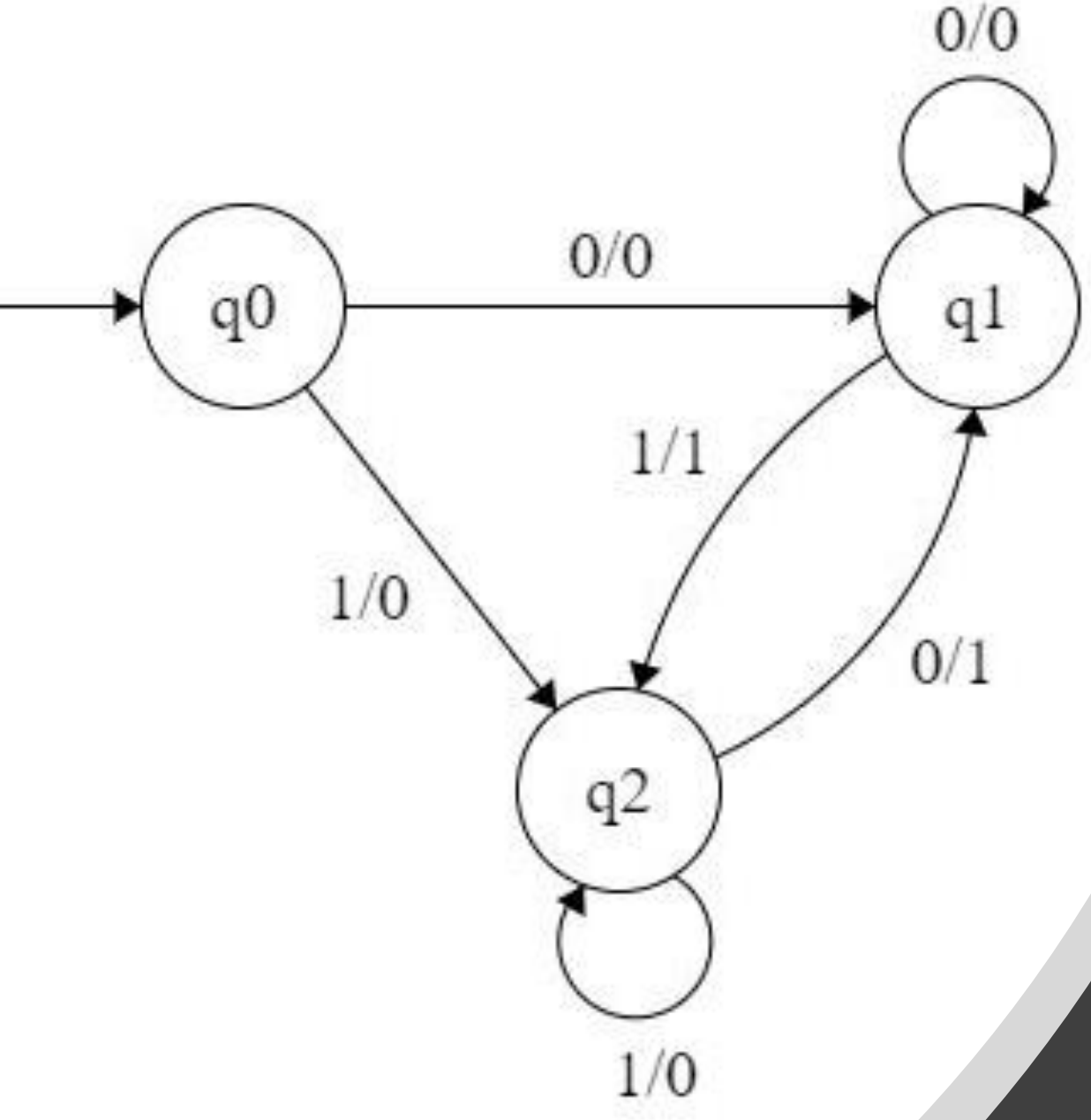
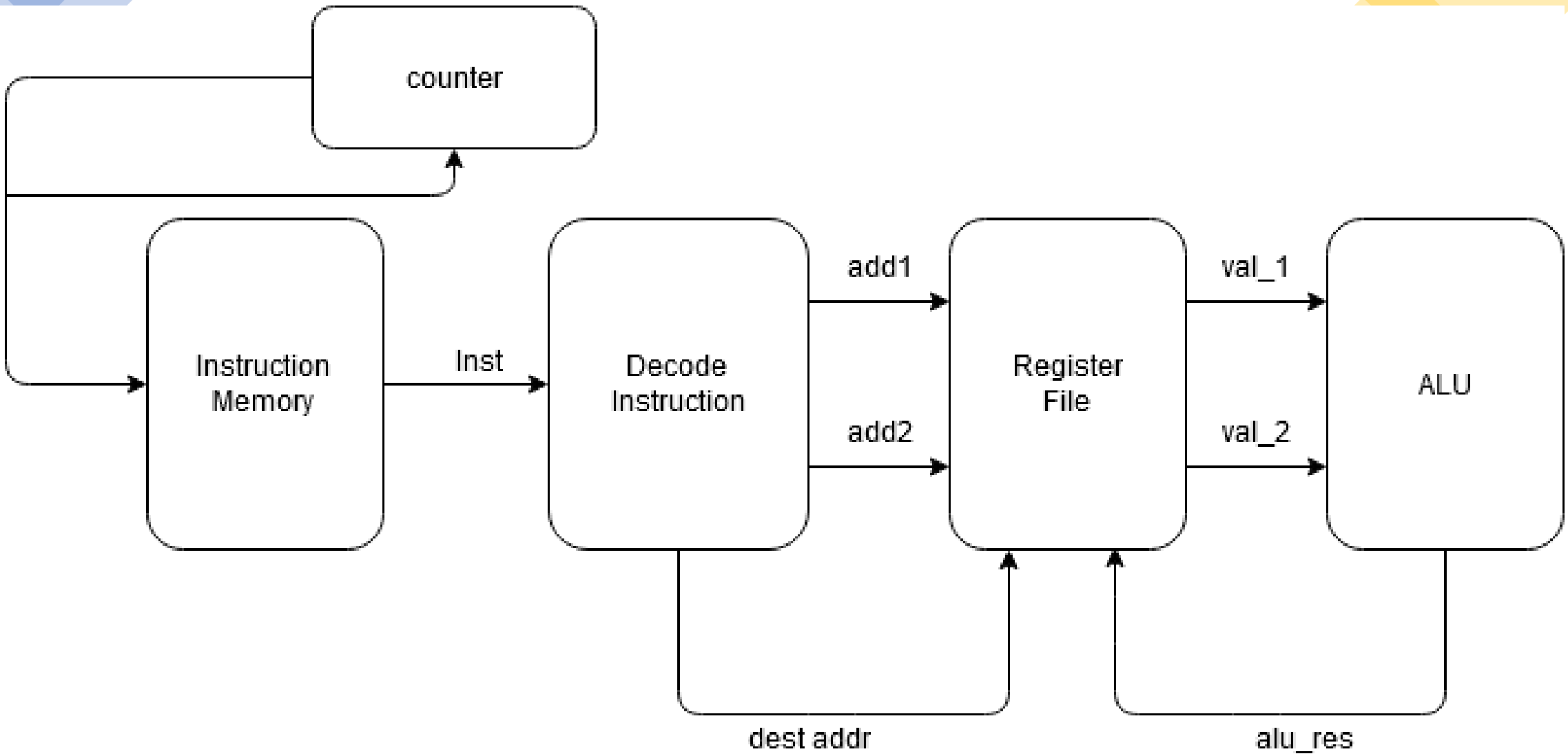
13-12-2020



Try This (Mealy Machine)


counter
Instruction Memory
Inst
Decode Instruction
add1
add2
Register File
val_1
val_2
ALU
dest addr
alu_res

Description for the processor

Perform ALU operations namely bitwise and, or, xor and negation

(00 -> AND , 01 -> OR , 10 -> XOR , 11-> Neg)

The instructions are 8 bit wide

Instruction encoding is as shown

1. AND R2,R1,R0 -----> 00100100

2. OR R3,R1,R0 ------> 01110100

verilog_kss_2 - [G:/Introdunction_to_verilog_2/FSM/verilog_kss_2/verilog_kss_2.xpr] - Vivado 2015.4

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RTL Analysis
- Elaboration Settings
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  - Report DRC
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  - Schematic

Synthesis
- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

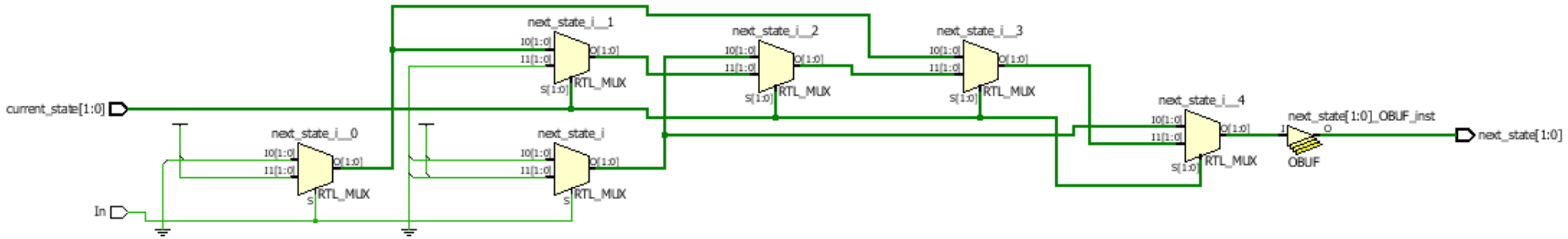
Elaborated Design - xc7a200tfbg676-2 (active)

Properties

Project Summary | Schematic

8 Cells | 5 I/O Ports | 19 Nets

Next state Logic using nested if else



Design Runs

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ENG 06:53 13-12-2020