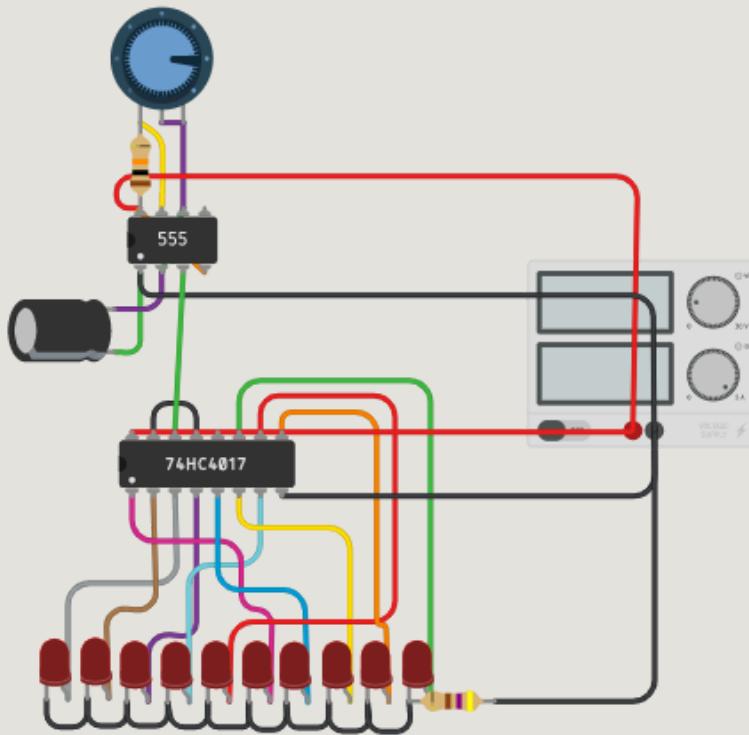


LED CHASER



This circuit is made using a **555 timer** and a **shift register**.

The 555 timer acts as a clock generator, producing a continuous wave of pulses that alternate between high and low voltages, at regular intervals. These pulses serve as a clock signal for the shift register, telling it when to shift the stored bits.

The shift register, specifically the 74HC595, is a Serial-In Parallel-Out (SIPO) device used to store and move binary data. Think of it like a row of buckets, each holding a bit (binary digit). Every time the shift register receives a clock pulse from the 555 timer, it moves each bit to the next bucket. The DS (Data Serial) pin receives one bit at a time. After 8 bits are loaded, the ST_CP (latch) pin is triggered to update the outputs. The 8 output pins (Q0-Q7) then light up the connected LEDs based on the stored bit pattern, creating the “LED chaser” effect.

The 555 provides the timing. The shift register passes the signal along. The LEDs do the show. Together, these chips demonstrate the building blocks of digital electronics: timing, logic, and output.

74HC595 SHIFT REGISTER

QB 1	16 Vcc
QC 2	15 QA
QD 3	14 SERIAL IN
QE 4	13 OE
QF 5	12 RCLK
QG 6	11 SRCLK
QH 7	10 SRCLR
GND 8	9 QH`

SUMMARY

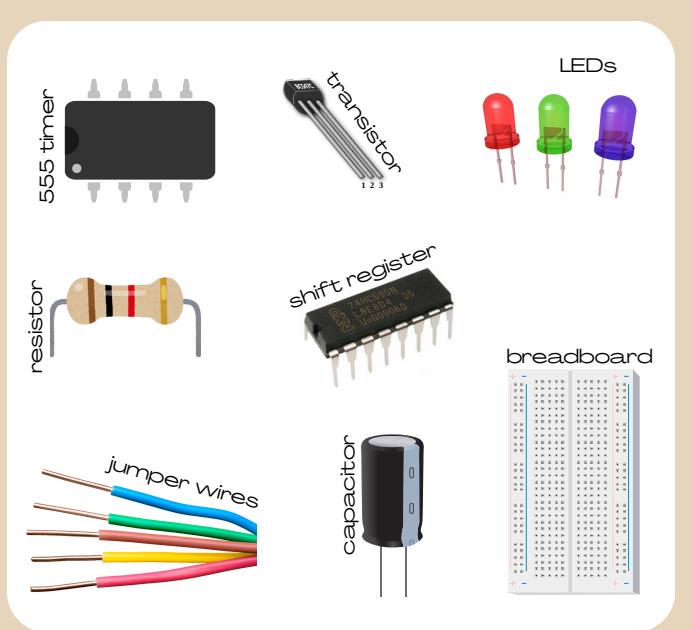
When the voltage at pin 11 is high, whatever voltage level is at pin 14 (1 OR 0) gets shifted into the internal storage controlled by pin 12. When the storage is full, pin 12 shifts those bits into the output pins (1-8 & 15). The voltage at pin 14 is determined by an external input (microcontroller, buttons, etc)

PINS 1-7, & 15	PARALLEL OUTPUTS	
PIN 8	GND	
PIN 9	QH`	Complement/Inverse of PIN 7. Used for daisy-chaining.
PIN 10	RESET	Pull LOW to clear all bits to 0 and pause functionality. Otherwise, HIGH.
PIN 11	SHIFT CLOCK	Pin where timing is provided by a clock
PIN 12	STORAGE CLOCK	Use to update data to the output pins.
PIN 13	OUTPUT ENABLE	Keep LOW. When LOW, Q0-Q7 outputs are active. When HIGH, outputs are disabled.
PIN 14	SERIAL INPUT	Data bits are sent here.
PIN 16	VCC	

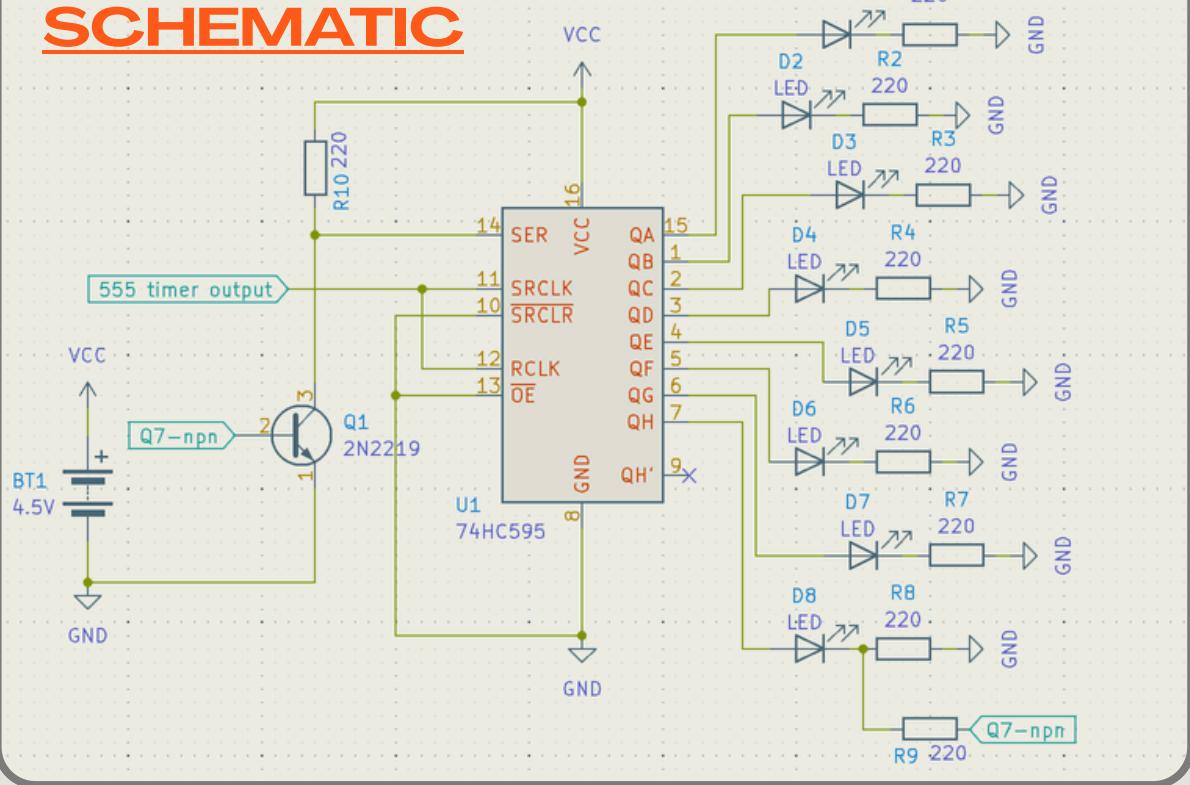
WIRE AN LED CHASER

MATERIALS:

- 74HC595N shift register
- 555 timer
- Breadboard and jumper wires
- [5V] power supply
- **8** LEDs
- **8** [220Ω] resistors
 - For LEDs
- **3** [10kΩ] resistors
- **1** [1kΩ] resistor
- **1** [10µF] capacitor
 - For 555 timer
- **1** transistor



SCHEMATIC



SIPO Shift Register

What is it?

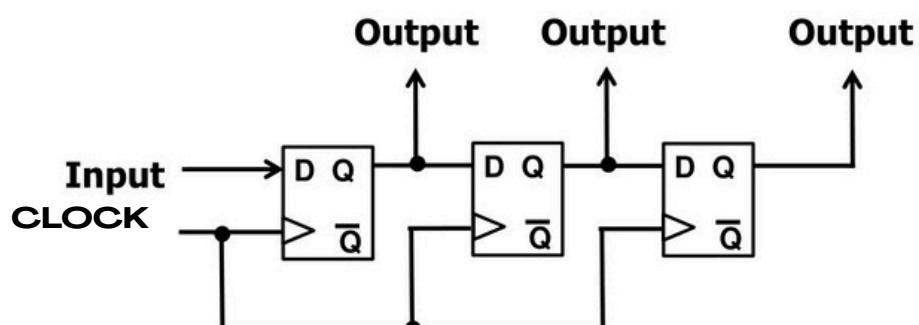
SIPO stands for **series-out-parallel-in**.

This shift register takes in **single inputs (series)** and gives the outputs on **many pins at once (parallel)**.

Inside, bits of data are being shifted across one by one. The frequency for how fast this shifting happens depends on the clock pulse/timing provided by an IC called a 555 timer.

- For a bunch of LEDs, light travel across the row — the register is literally handing off the signal step by step. It's a clever way to control a bunch of outputs using only a few inputs.

Internal Operation



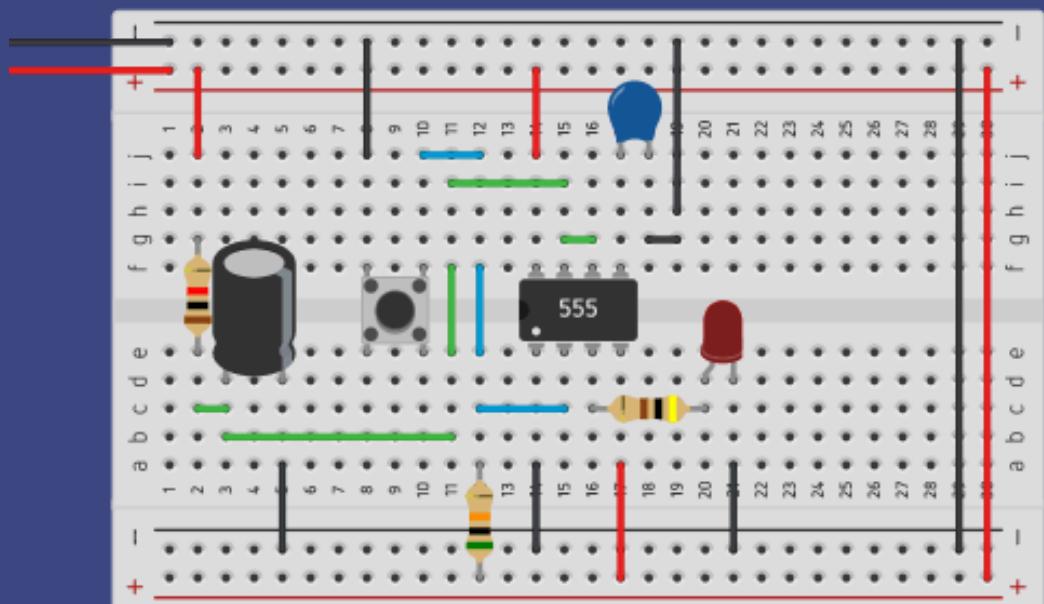
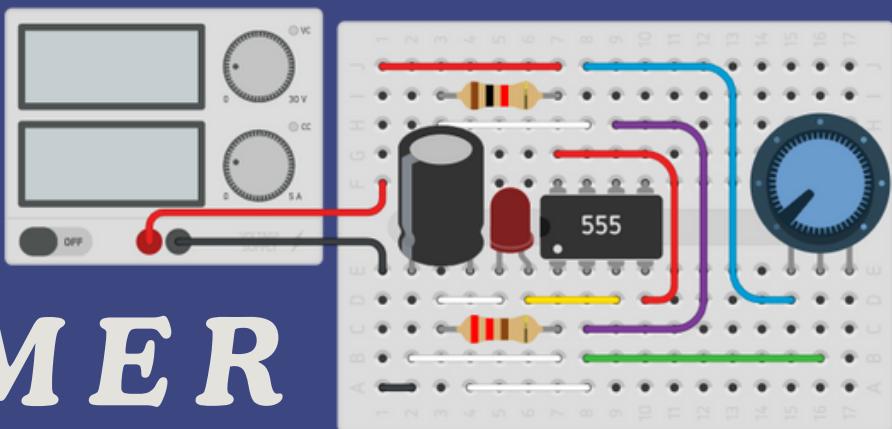
Input: The place in which you enter your input data into the shift register.

Outputs: Your data are distributed across each one.

Flip-flops: Acts as building blocks to store and move your input data.

Clock: Gives the timing for the shift register so that it can perform its operation (this is usually provided by a special IC called a 555 timer).

NE555 TIMER



monostable



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NE555 TIMER

The NE555 timer is one of the most iconic and widely used integrated circuits in electronics.

It contains two voltage comparators, a flip-flop, a discharge transistor, and a voltage divider made of three $5\text{k}\Omega$ resistors.

These internal components allow it to operate in multiple modes, most commonly astable and monostable, making it suitable for applications ranging from LED blinkers and tone generators to timers, pulse-width modulation, and frequency counters.

The Model

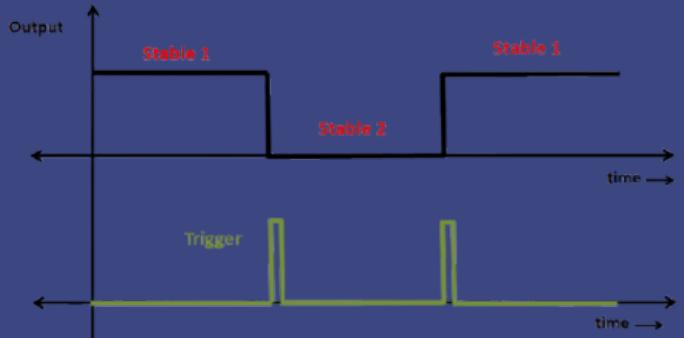
GND 1	■	8 VCC
Trigger 2	■	7 Discharge
Output 3	■	6 Threshold
Reset 4	■	5 CV

PIN 1	GND	
PIN 2	TRIGGER	Detects a LOW signal (below $\frac{1}{3} \text{Vcc}$) to begin timing cycle
PIN 3	OUTPUT	
PIN 4	RESET	Pull LOW to reset timer manually. Otherwise, HIGH.
PIN 5	Control Voltage	Smoothens Voltage (?)
PIN 6	THRESHOLD	Ends the timing cycle when capacitor voltage reaches $\frac{2}{3} \text{Vcc}$
PIN 7	Discharge	Discharges timing capacitor when output goes LOW
PIN 8	VCC	15V - 5V

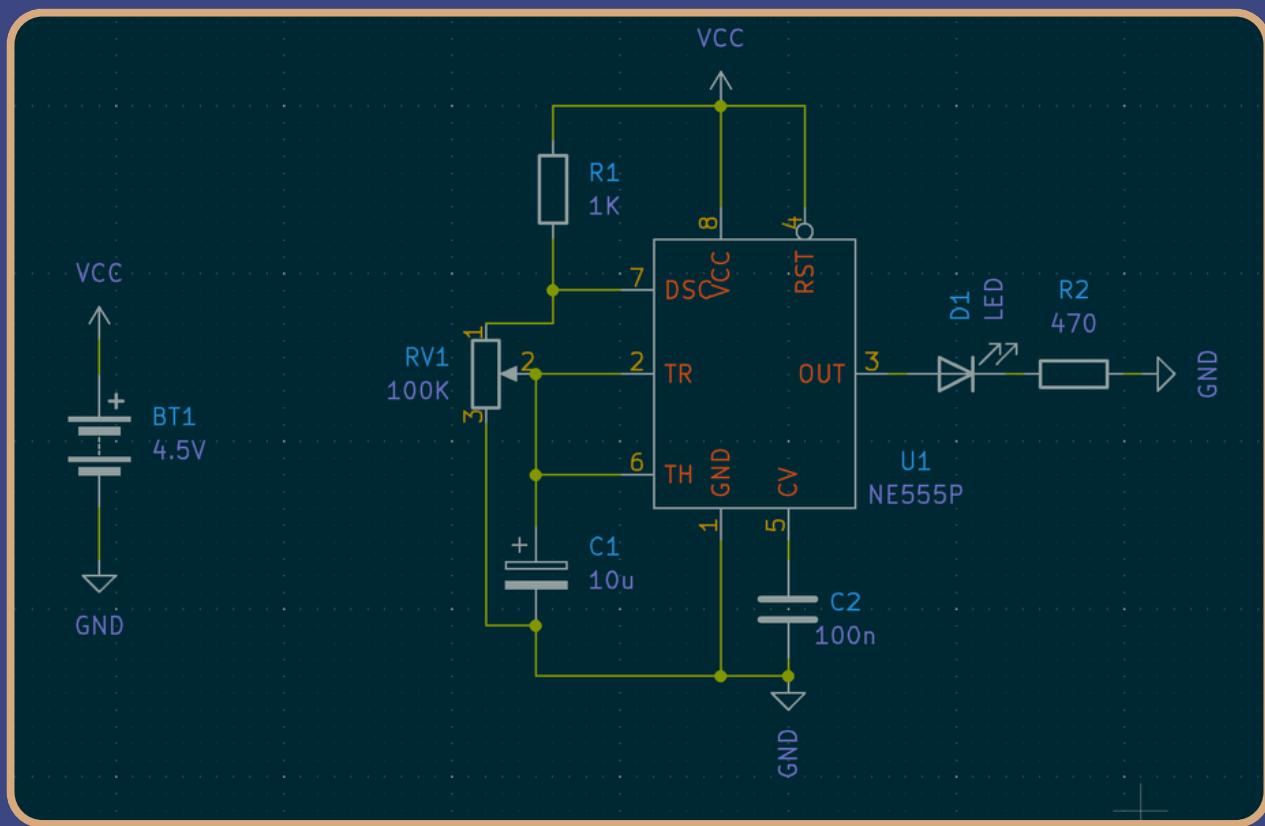
The Two Modes

Monostable mode: produces a single output pulse of fixed duration in response to a trigger. It's often called a one-shot timer because it generates one pulse per trigger event.

Astable mode: produces a continuous, oscillating output that looks like a square wave.



WIRING THE 555 TIMER IN ASTABLE MODE:

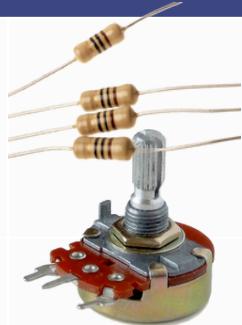


Resistors

limit current

Values: 1K Ohm & 470 Ohm

Connect $1k\Omega$ between VCC and PIN7;
 470Ω in series with the output LED



Potentiometers

are variable resistors

Values: 100K

1st terminal: PIN 7
 2nd terminal: 2,6, and 10 μF
 3rd terminal: GND



Capacitors

store charge

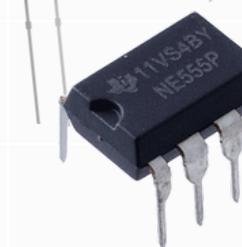
Values: 10 μF & 100 nF

100nF between PIN 5 and GND; 10uF @ RV1
 2nd Terminal and GND



LEDs emit light, but only in one direction.

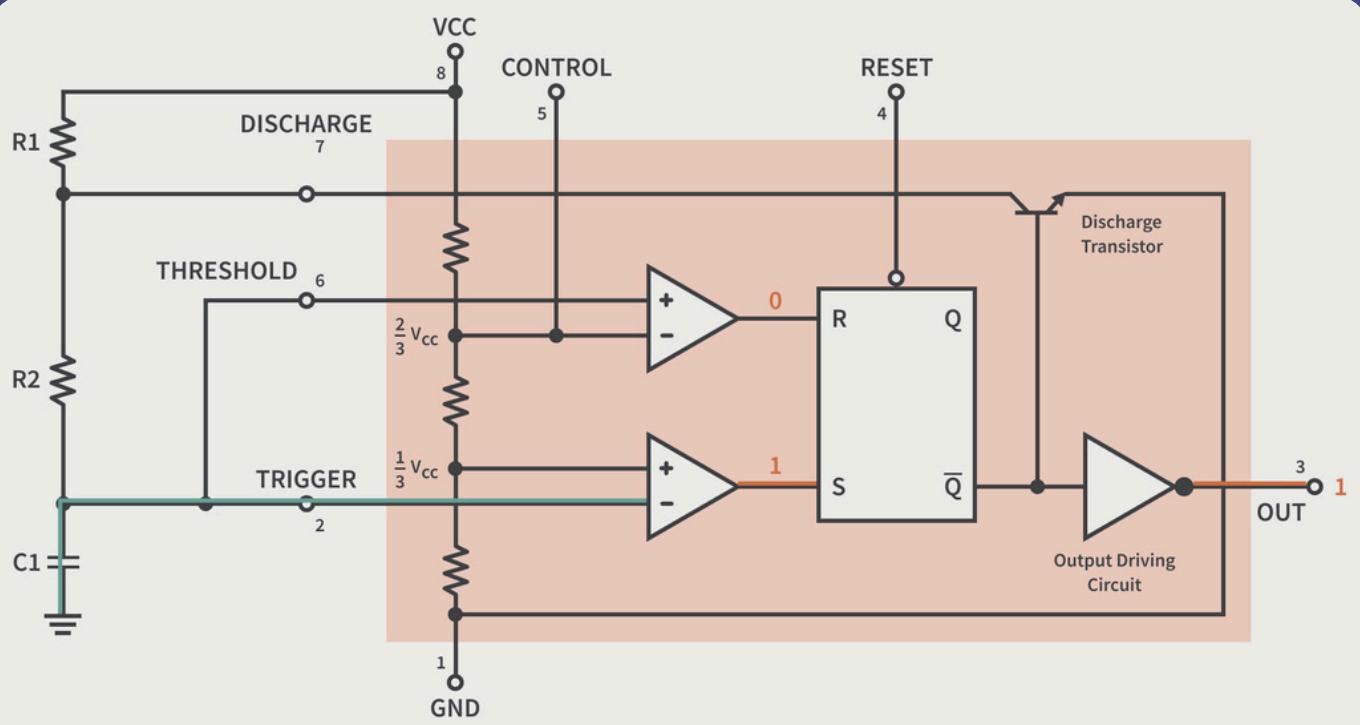
PIN 3 → LED → Resistor → GND



555 Timer

you got it

ASTABLE TIMER - INTERNAL OPERATION



Voltage Divider:

Three resistors split the supply into $\frac{1}{3} V_{CC}$ and $\frac{2}{3} V_{CC}$ reference levels for the comparators.

Comparators:

- Lower Comparator: Triggers the flip-flop when the **Trigger** pin voltage *drops* below $\frac{1}{3} V_{CC}$ (**SET** becomes HIGH, **OUTPUT** becomes)
- Upper Comparator: Resets the flip-flop when the **Threshold** pin voltage *rises* above $\frac{2}{3} V_{CC}$ (sets

Operation:

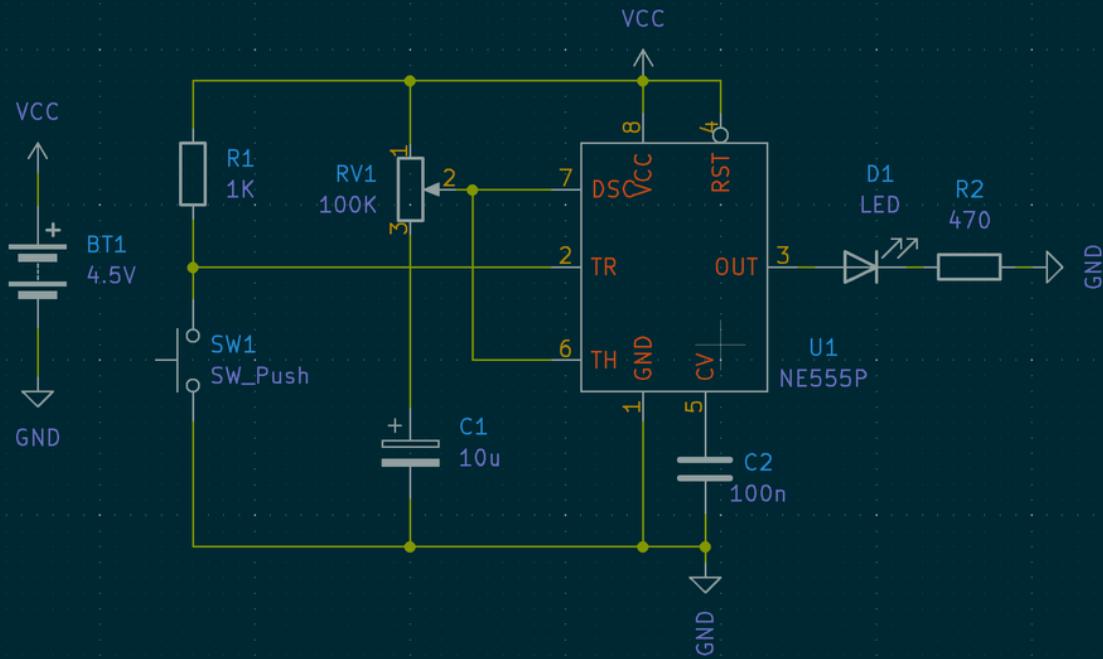
Output - LOW pulse:

- Base voltage is **not** applied to *discharge transistor*, so charge accumulates in C1. This affects the voltage at pins 2 and 6.
- Lower comparator output starts at HIGH. It goes LOW when C1 voltage exceeds $\frac{2}{3} V_{CC}$.
- Upper comparator output flips from LOW to HIGH when C1 voltage exceeds $\frac{2}{3} V_{CC}$. **OUT changes from 0 to 1**.

Output - HIGH pulse:

- Discharge transistor begins to *discharge* C1. When C1's voltage drops below $\frac{1}{3} V_{CC}$. **OUT changes from 1 to 0**.

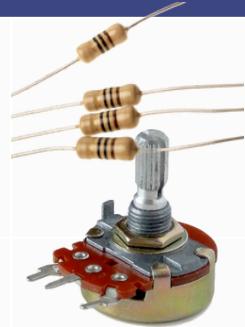
WIRING THE 555 TIMER IN MONOSTABLE MODE:



Resistors

limit current

Values: 1K Ohm & 470 Ohm



Potentiometers

are variable resistors

Values: 100K

Connect $1k\Omega$ between VCC and PIN7;
 470Ω in series with the output LED

1st terminal: PIN 7
2nd terminal: 2,6, and 10 μF
3rd terminal: GND

Capacitors

store charge

Values: 10 μF & 100 nF

100nF between PIN 5 and GND; 10μF @ RV1
2nd Terminal and GND



LEDs emit light, but only in one direction.

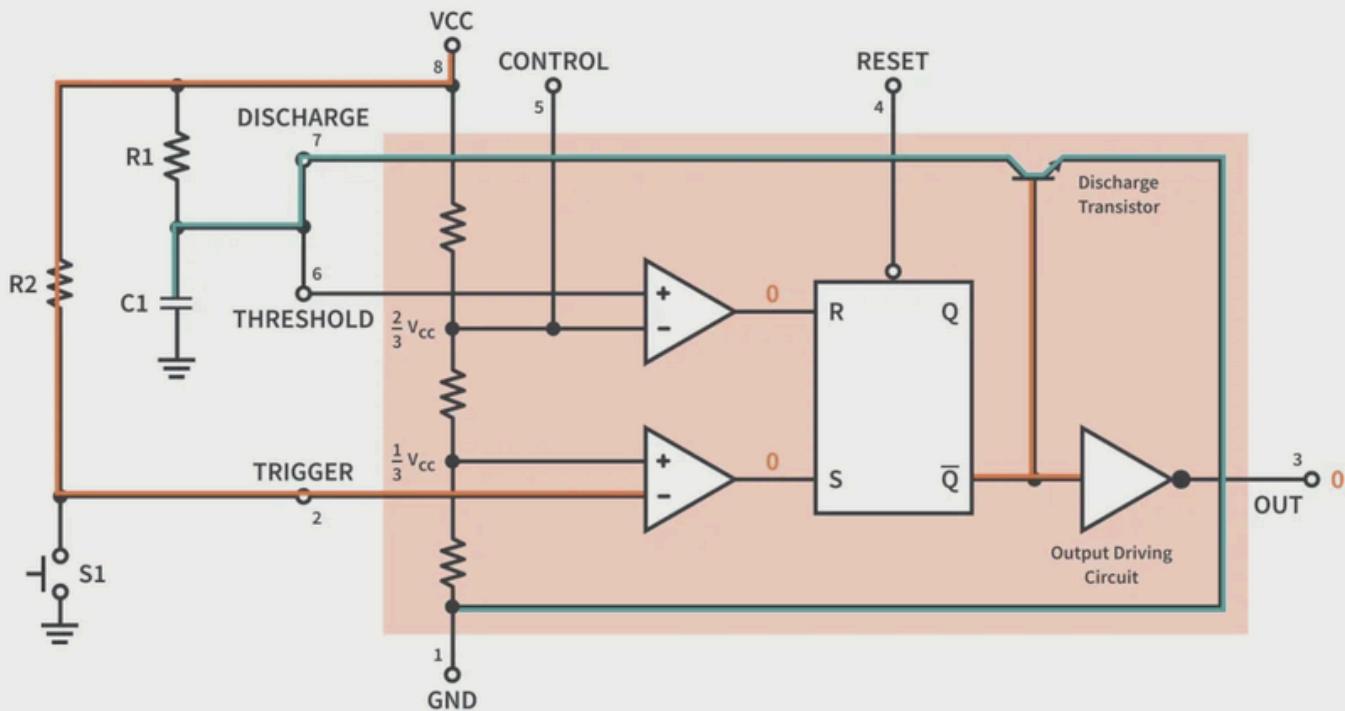
PIN 3 → LED → Resistor → GND



555 Timer

you got it

MONOSTABLE TIMER - INTERNAL OPERATION



Voltage Divider:

Three resistors split the supply into $\frac{1}{3} V_{CC}$ and $\frac{2}{3} V_{CC}$ reference levels for the comparators.

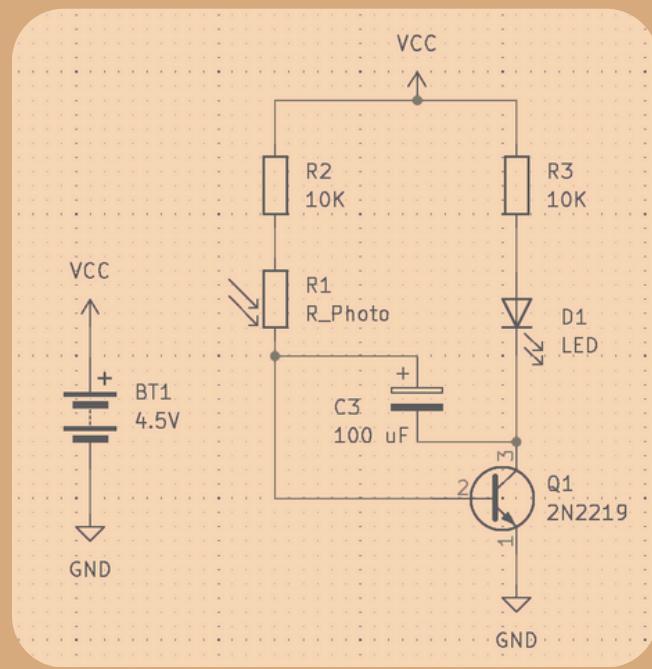
Comparators:

- Lower Comparator: Triggers the flip-flop when the Trigger pin voltage drops below $\frac{1}{3} V_{CC}$ (sets output HIGH).
- Upper Comparator: Resets the flip-flop when the Threshold pin voltage rises above $\frac{2}{3} V_{CC}$ (sets output LOW).
- **In Monostable:** Discharge and Threshold are tied together with C1.

Operation:

- Output- Stable (LOW)
 - C1 is constantly discharging due to the discharge transistor while **trigger** stays above $\frac{1}{3} V_{CC}$. When S1 is pressed, **trigger** turns off the gate across the discharge transistor. (**OUT: 0 → 1**)
- Output - Unstable Pulse (HIGH)
 - Since C1 can no longer discharge, voltage accumulates across C1 charges, until it rises above $\frac{2}{3} V_{CC}$. Rising above $\frac{2}{3} V_{CC}$ triggers the **threshold** comparator, activating the discharge transistor again.

REACTIVE TRANSISTOR

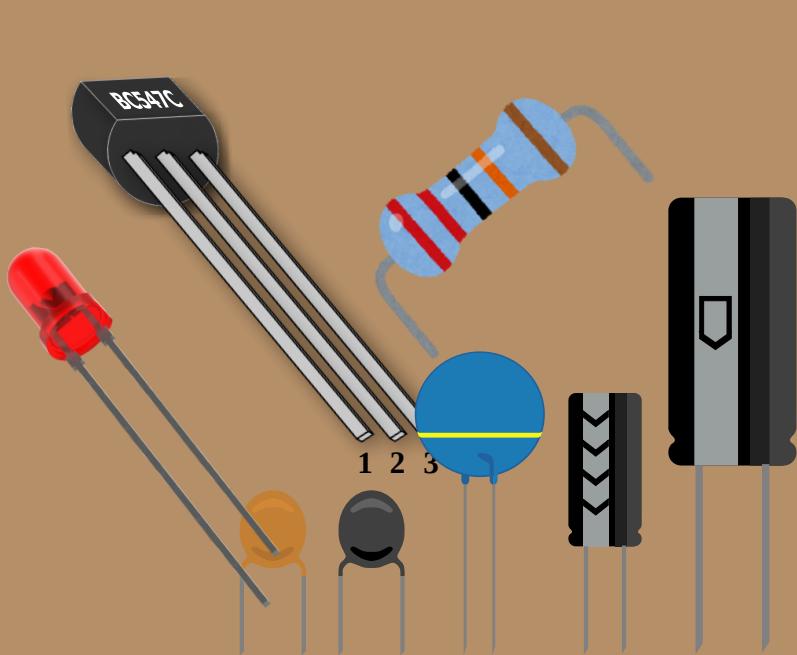


This circuit uses a **photo-resistor (LDR)** to detect light. The **resistance/voltage drop** across the LDR is inversely proportional to the light hitting the surface.

In this circuit, the transistor behaves as a **current amplifier**, with the current flowing through the LED being proportional to the **voltage applied at the base pin**.

Current also flows into a **capacitor**, which accumulates charge, so if the current supplied by the LDR drops, the capacitor continues to supply some power to the base pin. You'll be surprised at how quick the LED turns off once the capacitor is removed!

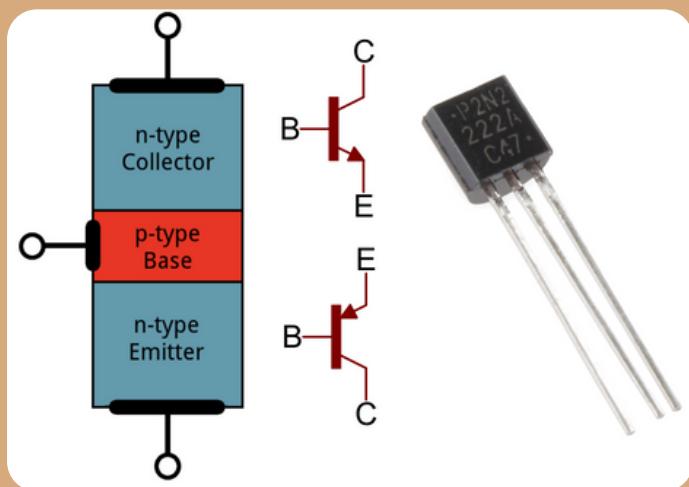
LET'S BUILD IT!



- 1 × NPN Transistor (e.g., BC547 or 2N2222)
- 1 × Photoresistor (LDR)
- 1 × Capacitor (100 μ F–470 μ F)
- 1 × LED, buzzer, or motor
- 2 × Resistor (for LED and LDR sensitivity)
- 1 × 9V battery + battery clip
- Breadboard and jumper wires

HOW THEY WORK

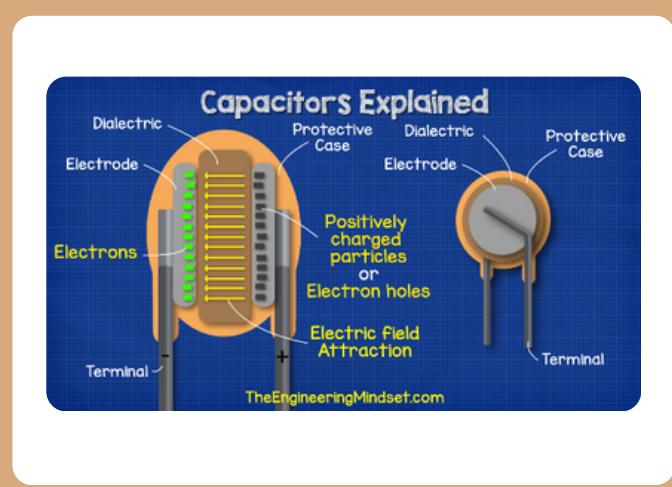
Transistors



An NPN transistor is made of two N-type layers with a thin P-type layer in between. The emitter releases electrons, the base controls how many get through, and the collector collects them. When a small voltage is applied to the base, it makes the base-emitter junction forward biased, letting electrons flow from the emitter (E) into the base (B). Most of these electrons are then pulled into the collector (C) by the higher voltage there.

Think of the transistor like a faucet: a tiny twist on the handle (base) controls how much water (current) flows through. The brighter the light, the more the faucet opens and the LED shines.

Capacitors

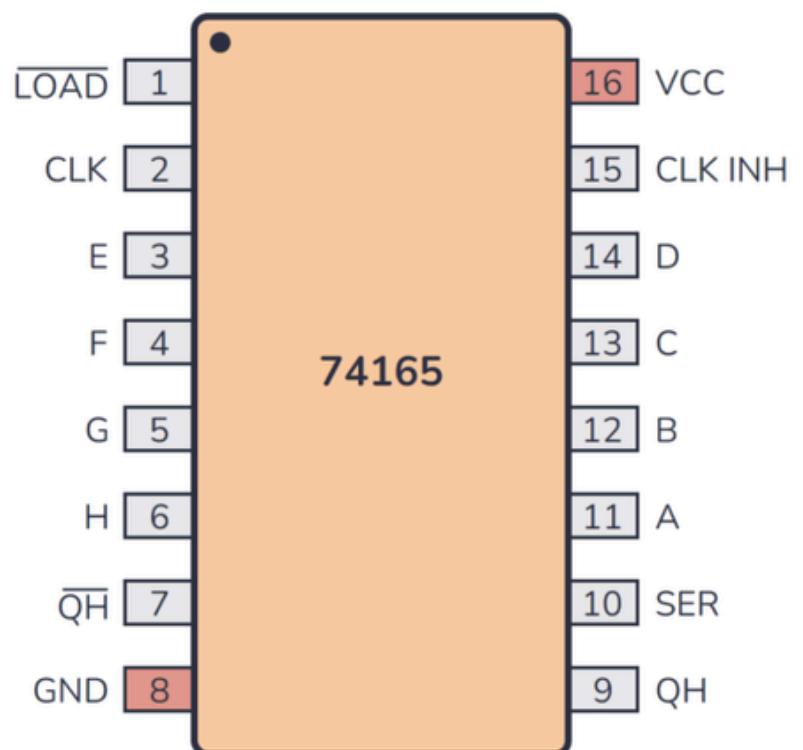
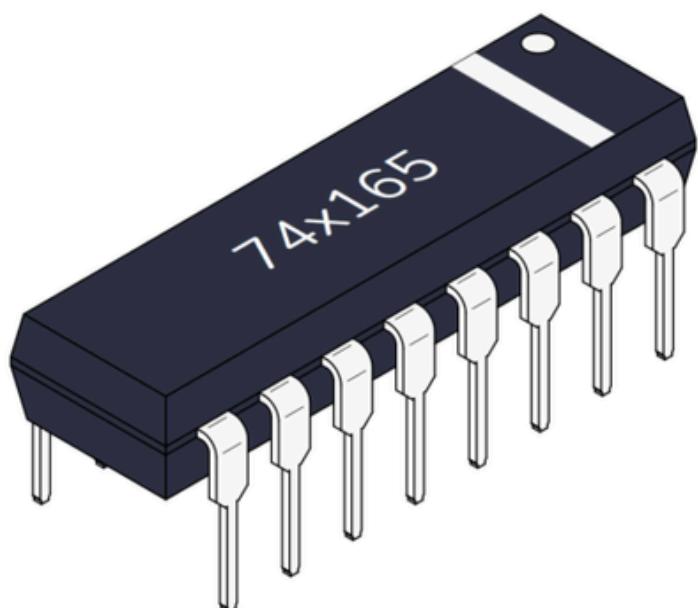


A capacitor has two metal plates separated by an insulator (called the dielectric). When voltage is applied, one plate gains electrons and the other loses them, building up an electric field between them. That field stores energy.

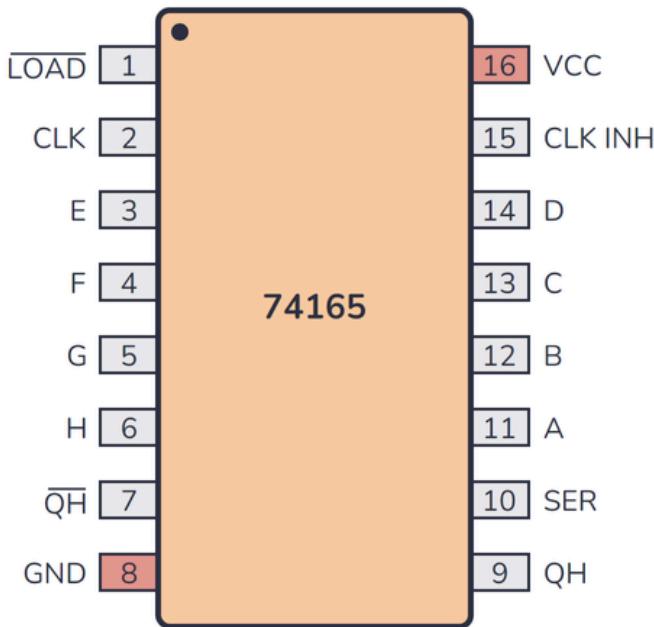
When the supply voltage drops, the field collapses and pushes electrons back into the circuit, releasing the stored charge.

The rate it charges and discharges depends on the resistor it's paired with (the RC time constant). Bigger capacitance or resistance = slower charge and discharge.

How To Work a PISO Shift Register (with LEDs and Switches)



Pinout Diagram



Pin 1 (LOAD): An active-low pin that controls the operation mode of the register.

- A **LOW** signal loads the 8-bit parallel data from pins A–H into the register.
- A **HIGH** signal enables serial shifting of the data out of the register.

Pin 2 (CLK): Clock for timing.

Pin 3 (E): Input

Pin 4 (F): Input

Pin 5 (G): Input

Pin 6 (H): Input

Pin 7: Serial out compliment.

Pin 8: Connected to Ground (GND).

Pin 16 (VCC): To power supply.

Pin 15: Clock inhibitor. Can stop change in output. Connected to Ground (GND) for now.

Pin 14 (D): Input

Pin 13 (C): Input

Pin 12 (B): Input

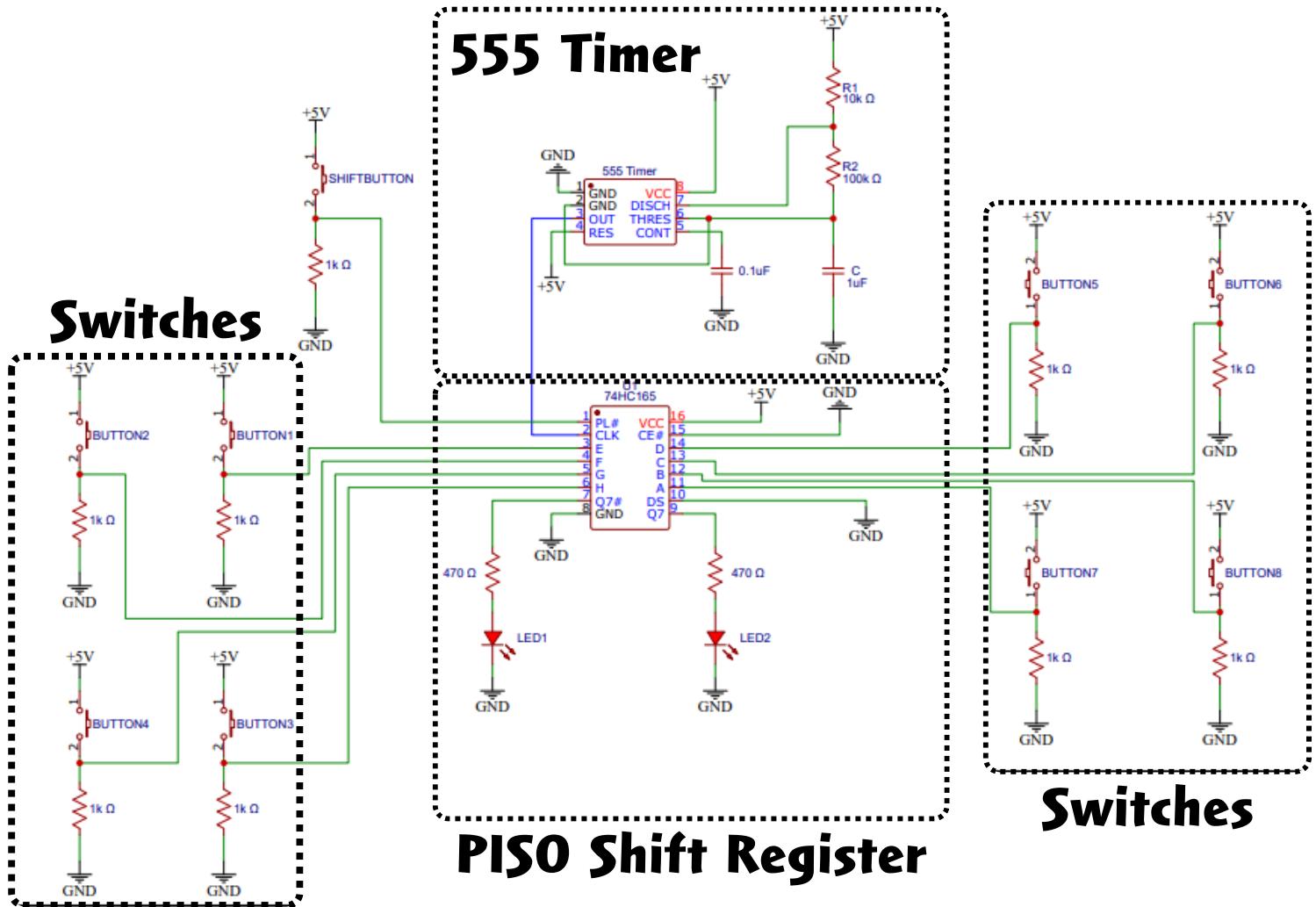
Pin 11 (A): Input

Pin 10: Serial in. Connected to Ground (GND) for now.

Pin 9: The main serial data output pin.

- The data that was loaded in parallel is shifted out one bit at a time.
- Synchronized with the clock signal.

Layouts of Schematic

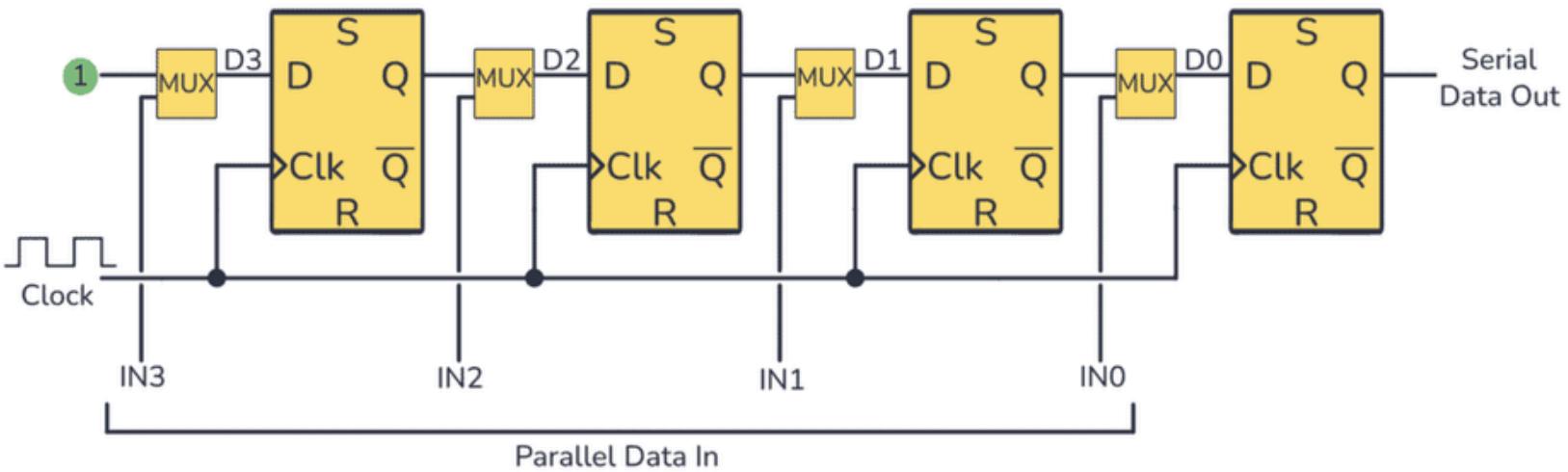


PISO Shift Register: The main chip that handles our inputs and give the output.

Switches: For us to give inputs (HIGH or LOW) to the shift register.

555 Timer: Acts a clock. Provides the timing for the shift register to move data bit to the output.

Inside the Chip



Parallel Data In: Data is loaded into the shift register in parallel, meaning all bits are input simultaneously. This is done through individual input lines connected to each flip-flop.

Clock: A clock signal is applied to the shift register, triggering the movement of data from one flip-flop to the next. Each clock pulse causes a bit to shift one position to the right.

Serial Data Out: The output of the shift register is serial, meaning the data is shifted out bit by bit. The output is read from the register serially, one bit at a time, in a sequence determined by the clock signal.