

# CHAPTER 1

## INTRODUCTION

1.1

An ADD/SUBTRACT logic circuit is shown below. It performs the ADD operation for  $P = 0$ , and SUBTRACT for  $P = 1$ .

- Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for transmission gate and XOR, are inverting. For example, AND gate is implemented with NAND followed by an inverter.
- By using the gate array platform given on page 47 , implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.

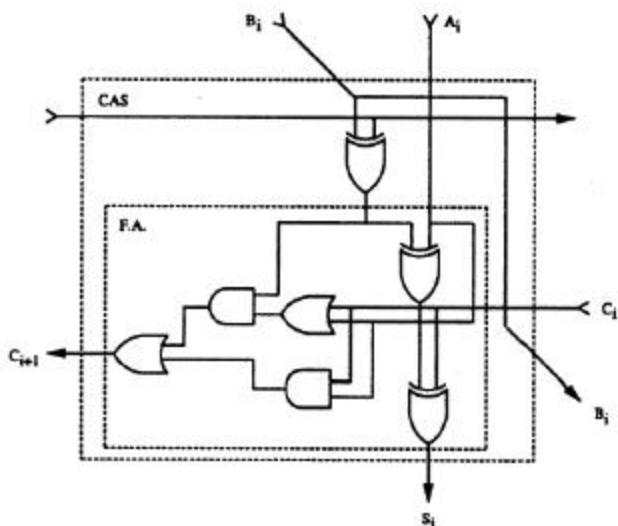
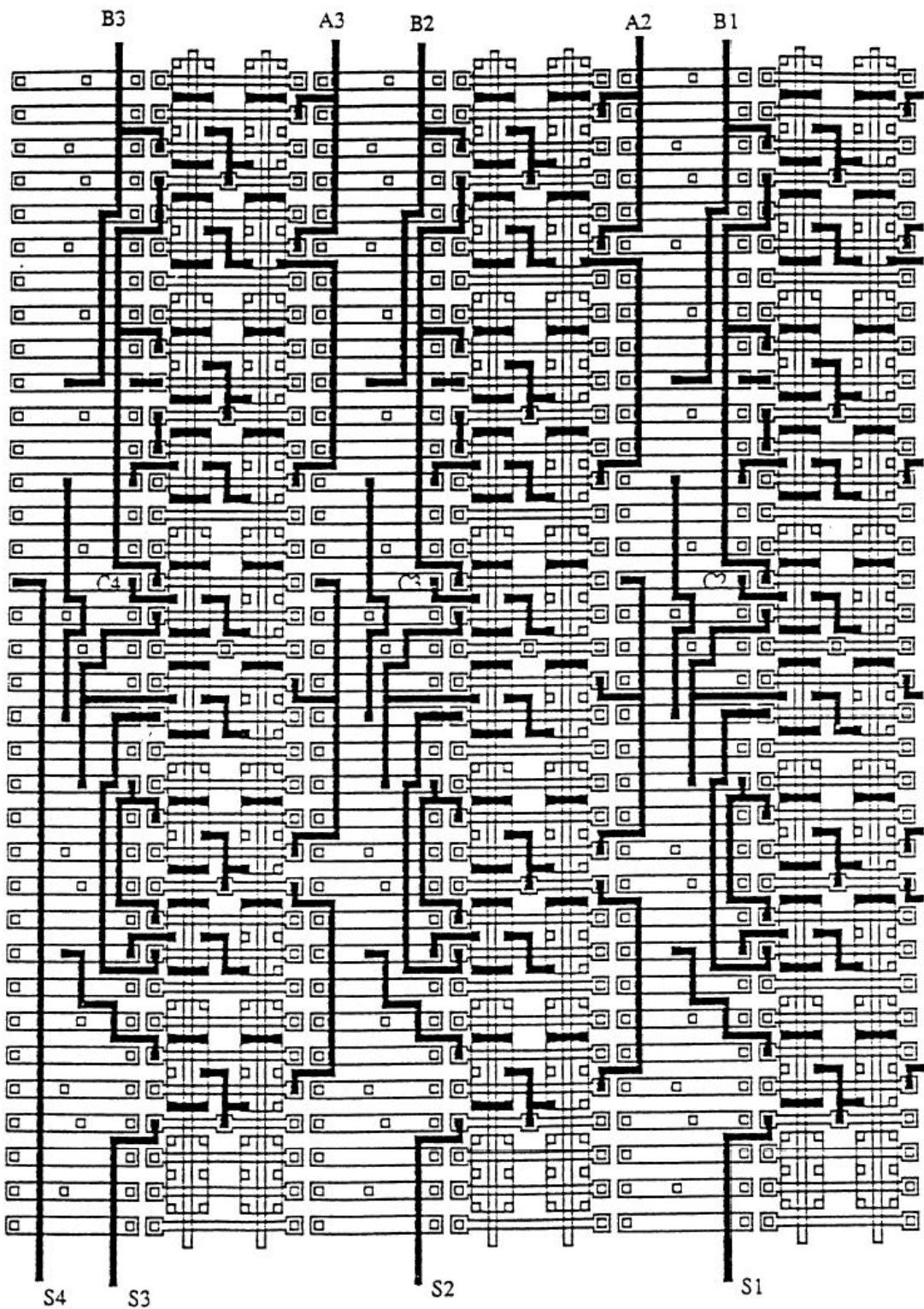


Figure P14.1(a)

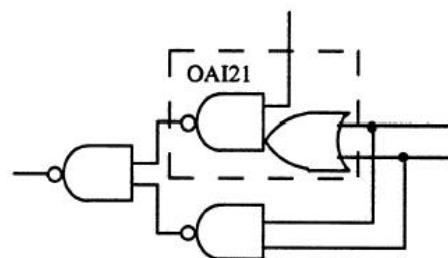
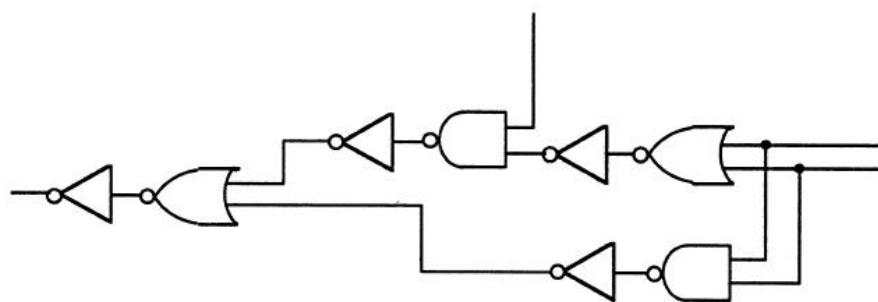
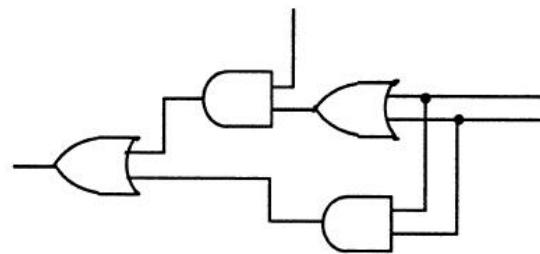
**SOLUTION:**

- The CMOS circuit implementation using the gate array platform:

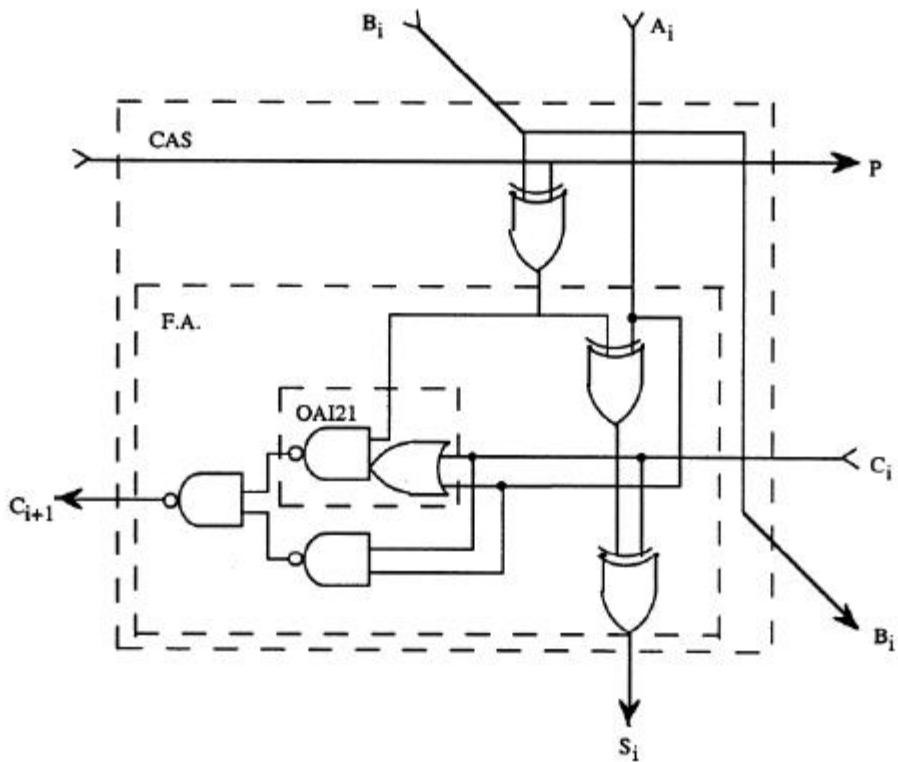


(a)

The AND and OR gates can be translated into CMOS circuit in the following steps:



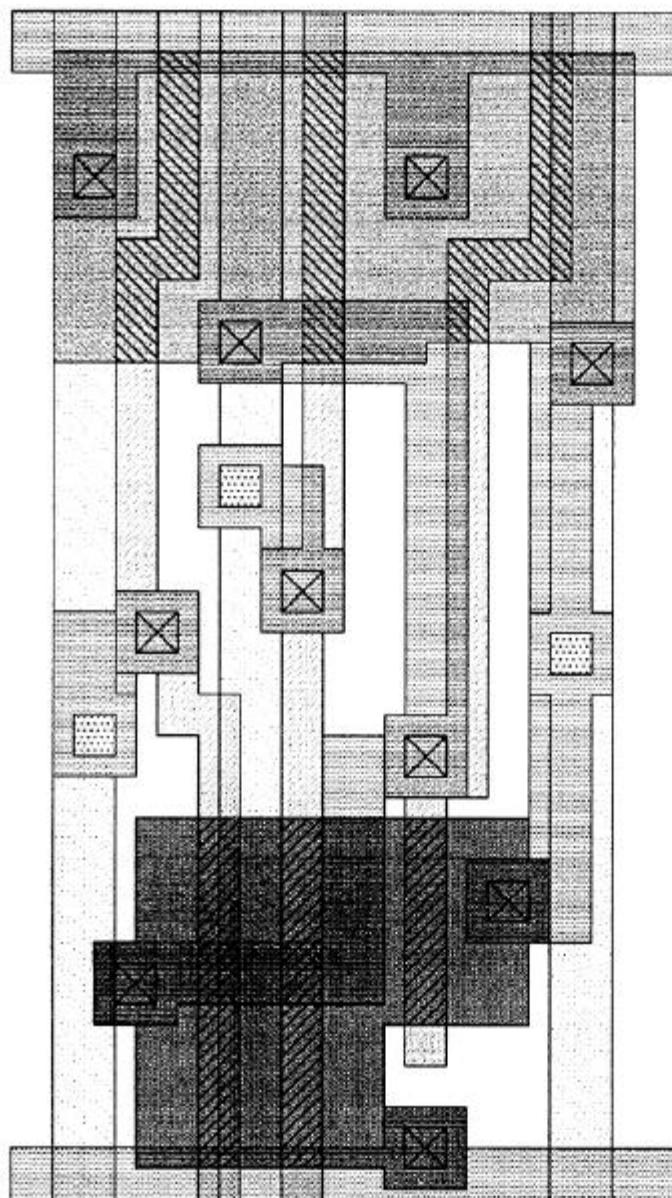
The equivalent CMOS logic gate is drawn:



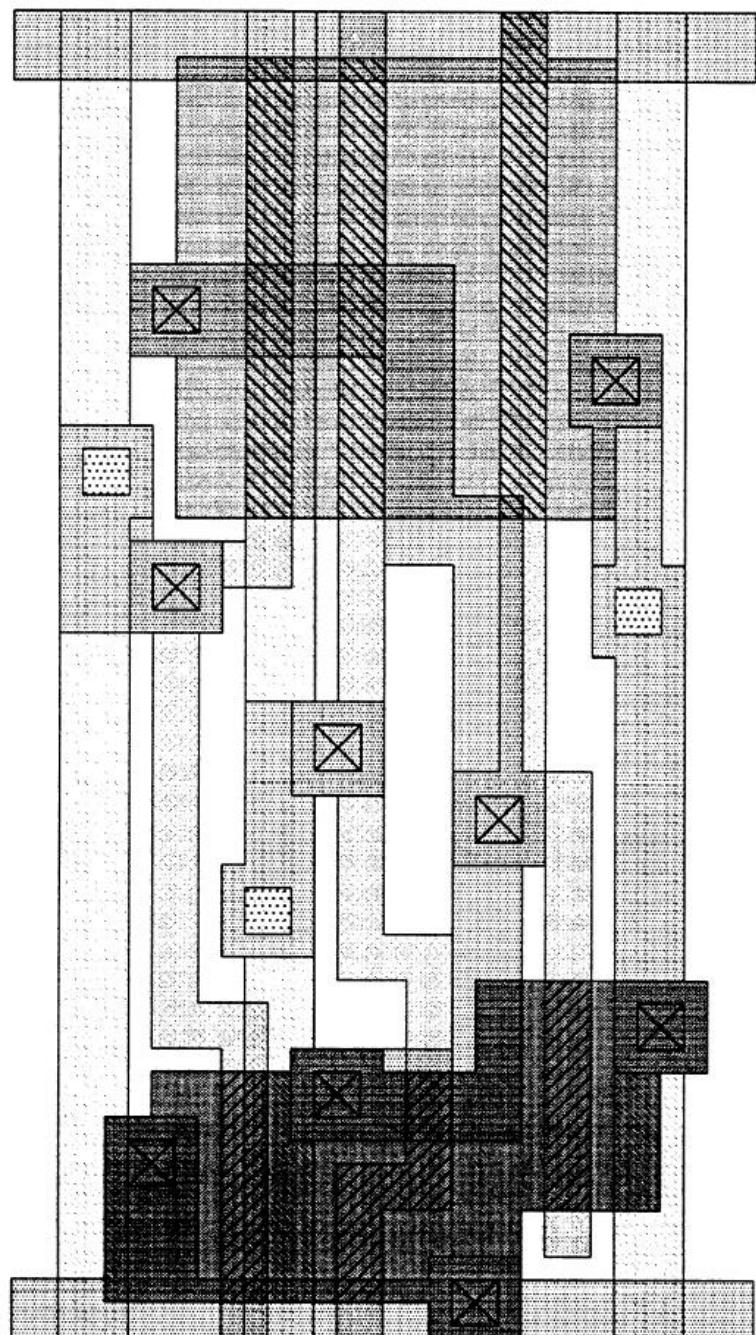
- 1.2 For the CMOS circuit in Problem 1.1
- First develop a small library of CMOS cells.
  - Place the cells into a single row and interconnect them with proper ordering such that the total interconnection wire length is minimized.

**SOLUTION:**

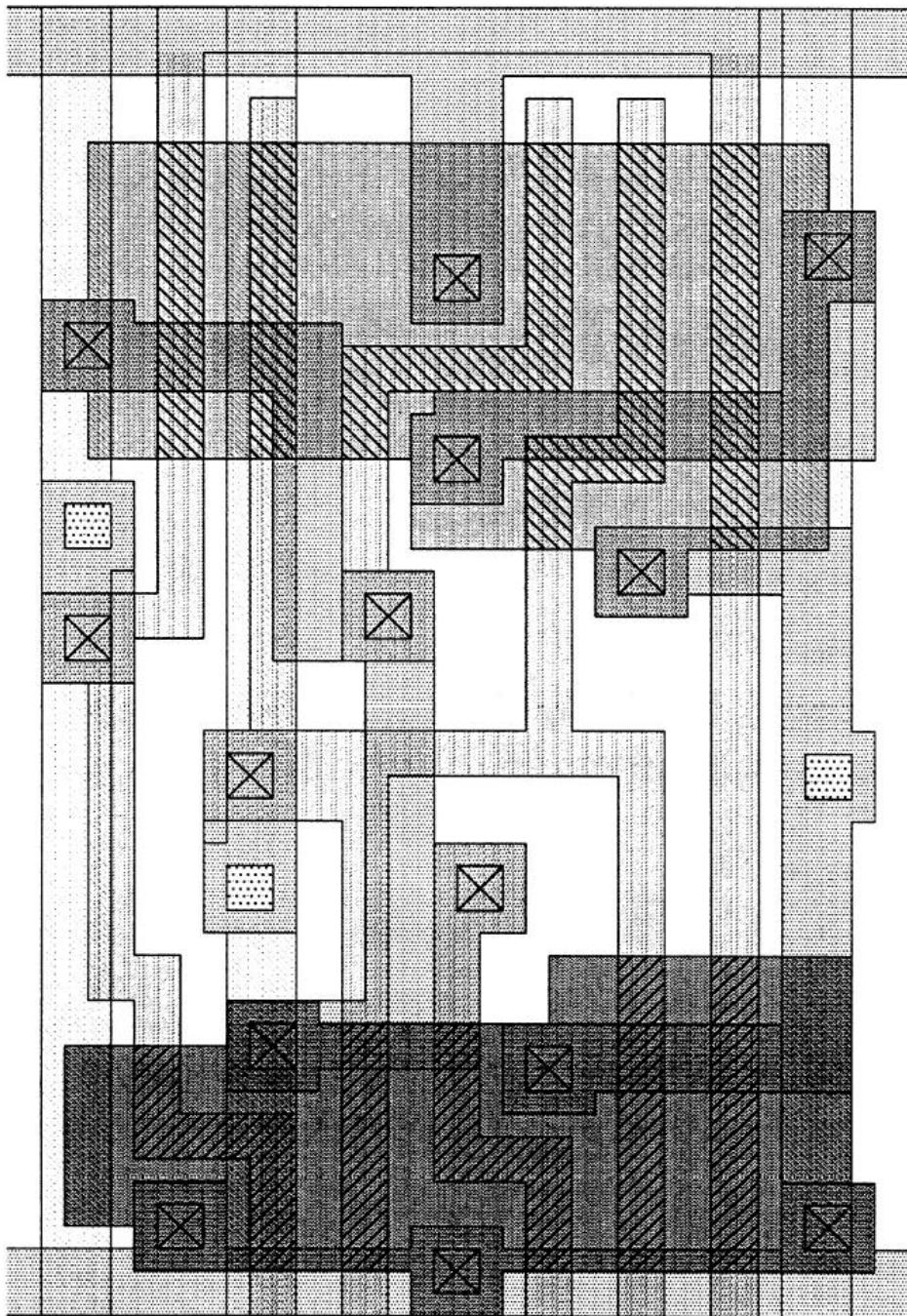
(a). CMOS cell library layout.  
AND cell:



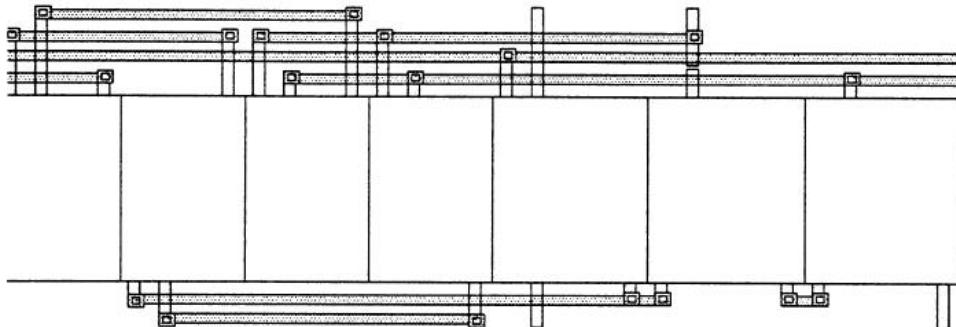
**OR cell:**



XOR cell:



Full adder:



- 1.3 A measure of design productivity predicts the required engineer-months in terms of design implementation styles, such as repeated transistors (RPT); non-repeatable unique transistors (UNQ); PLA, RAM, and ROM transistors; and the experience level of engineers (yr), the productivity improvement per year (D); and the design complexity (H). The formula proposed by Fey is

$$\text{Engineer - Months (EM)} = (1 + D)^{-\text{yr}} [A + Bk^H]$$

where the number of equivalent transistor count in the design is expressed by

$$k = \text{UNQ} + C \cdot \text{RPT} + E \cdot \text{PLA} + F \cdot \sqrt{\text{RAM}} + G \cdot \sqrt{\text{ROM}}$$

In this formula, the transistor count is in units of thousands and the coefficients A, B, C, D, E, F, G, and H are model parameters which depend on the designers' experience and CAD tool support. The parameter (yr) represents the number of years since the extraction time of the model parameters. A set of sample values for these parameters are A = 0, B = 12, C = 0.13, D = 0.02, E = 0.37, F = 0.65, G = 0.08, and H = 1.13.

- (a) Discuss how one would extract the model parameters within a design organization.
- (b) A 24-bit floating-point processor has been designed using 20,500 repeated transistors, 10,500 unique transistors, 105,500 RAM transistors, and 150,200 ROM transistors. Calculate the expected engineer-months (EM) by assuming the experience year value of yr = 3. Note that the transistor counts in the formula are in unit of thousands, for instance UNQ=10.5, not 10,500.

### SOLUTION:

(b)

$$\text{RPT} = 20.5$$

$$\text{UNQ} = 10.5$$

$$\text{RAM} = 105.5$$

$$\text{ROM} = 150.2$$

$$\begin{aligned} k &= \text{UNQ} + C \cdot \text{RPT} + E \cdot \text{PLA} + F \cdot \sqrt{\text{RAM}} + G \cdot \sqrt{\text{ROM}} \\ &= 10.5 + 0.13 \times 20.5 + 0.65 \times \sqrt{105.5} + 0.08 \times \sqrt{150.2} \\ &= 20.82 \end{aligned}$$

$$\text{EM} = (1 + D)^{-\text{yr}} [A + Bk^H] = (1 + 0.02)^{-3} [12 \times 20.08^{1.13}] = 349.35$$

- 1.4 A large-scale fast prototyping system has been produced by using a very large array of field programmable logic arrays (FPGAs).
- Discuss the pros and cons of such prototyping systems for proof of design concepts and verification in view of effort and speed performance of the design.
  - How would you compare the hardware prototyping method with the computer simulation method?

**SOLUTION:**

(a).

Pros:

- Rapid implementation.
- It is easy for hardware testing
- Functionality and timing problem can be resolved in short time.
- Hardware debugging can be done by reprogramming the chip.

Cons:

- FPGA chips operate at slower frequencies.
- FPGA chips are not dense, hence more chip area is required.
- Due to predetermined and restricted routing, some FPGA configurable blocks may not be utilized. This results in wasted chip area.

(b).

- Simulation systems may have bugs.
- Simulation algorithms are slow and they may miss some important application specific issues.
- FPGA implementation is a direct realization of the system. Hence it is a working chip.
- FPGA chip can be used as a final product if the time to market is short.

- 1.5 As the design complexity increases with increasing number of on-chip transistors, the on-chip noises have become more pronounced. Discuss the impact of packaging in suppressing on-chip noises in view of the numbers and strategic placement of ground and power pads, the numbers of ground and power planes.

**SOLUTION:**

The rule of thumb practiced in industry is to use one  $V_{DD}$  or  $V_{SS}$  pad for every two or three adjacent signal pads. The number of ground and power planes depends on the number of signal planes. It is good to put one  $V_{DD}$  at the top and one  $V_{SS}$  at the bottom of two signal planes.

- 1.6 The testing of VLSI chips at speed has become increasingly more difficult due to undesirable parasitic effects in testing environment. Also the cost of high-speed testing machines has become very high and hence in reality it has become difficult for smaller manufacturers to procure such equipment. Discuss what problems would the chip testing only at lower speed cause for systems houses which take such chips to develop systems

at speed. What alternative ways can be used to ease the problem in the absence of at-speed testers?

**SOLUTION:**

Testing a chip at lower speed would determine the functional yield of a chip design, identifying shorts, opens, and leakage current as well as circuit and logic faults. Parametric testing, however, can not be performed. Without this testing, there may be delay problems, unacceptable clock skew, etc. A company that can not afford high-speed testing machines could consider sending some of these chips to be tested elsewhere, developing delay models based on available data and relying more heavily on simulation for design validation in terms of speed, or intentionally designing chips more conservatively. A number of parametric failures are due to process variation. So the more familiar the designers are with the manufacturing limits, the safer the chips they can design without being overly conservative.

- 1.7 Draft plans for developing a chip as a function of design turnaround time and development cost. In particular, what particular design style would be chosen when the customer requires that the chip be delivered in one month, six months, and one year, respectively?

**SOLUTION:**

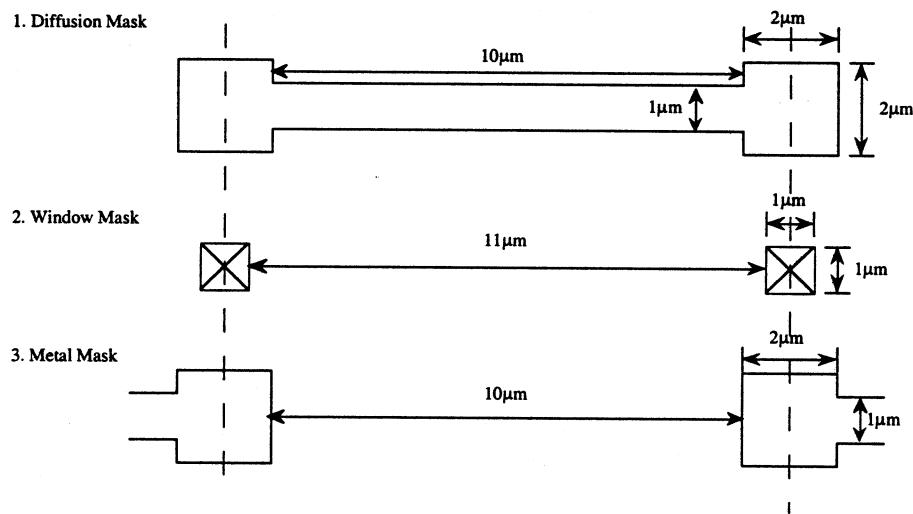
Development time and cost would obviously depend on the complexity and the size of the design, but the cheapest and fastest chip design would generally be done using FPGA's. This would be an appropriate design style for producing a chip in a month. If six months were available, a gate array or sea-of-gates style could be chosen. Patterning of the metal layers could be done in a few days on a few weeks. This is more expensive than FPGA, but will generally result in a smaller, faster chip. For a chip that must be produced in a year, a standard cells based design would be appropriate. This would be more expensive and time-consuming since a full custom mask set would be required, but the final product would be smaller and faster. Standard cell design is also appropriate for large-volume applications.

## CHAPTER 2

### FABRICATION OF MOSFETs

- 2.1** Design three masks for diffusion, window, and metal layers to realize  $1-k\Omega$  resistor with n-type diffusion with sheet resistance of  $100\Omega$  per square and lead metal lines. The minimum feature size allowed is  $1 \mu m$  for line width and window opening. Also  $0.5 \mu m$  extension of metal feature and diffusion feature over the window opening is required.

**SOLUTION:**



- 2.2** Discuss whether the mask set in Problem 2.1 will realize the resistance exactly. What would be the effect of window design on the resistance? Discuss at least two other mechanisms in the processing that can make the processed resistance deviate from the target value even if the effect of window is neglected.

**SOLUTION:**

The mask set will not realize the resistance exactly because of the number of squares contributed by the end configuration. In the above window design, 0.35 squares are added to each end, thus resulting a total of 10.7 squares. The realized resistor is thus  $1.07k\Omega$ .

The processed resistance can be deviated from the target value due to the resistivity variation on the wafer. Thus, the resistance on a die in the center of a wafer can be different from the resistance on a die at the edge of the wafer.

- 2.3** Let us now assume the variation in the resistance is affected only by the exact line feature

sizes. Discuss the pros and cons of having the line width at minimum as compared to making the width bigger than the minimum width.

**SOLUTION:**

Having the line width at minimum can save area while achieving the same functionality. But it is more sensitive to process variation.

- 2.4** A method for reducing interconnection resistance in the polysilicon lines is to use silicide material deposited on top to form polycide. This process can reduce the nominal sheet resistance from  $20\Omega$  to  $2\Omega$  or even less. For the same purpose, silicide material is also deposited on top of source and drain diffusions in MOS transistors. Thus, a single step deposition of silicide can be achieved on polysilicon gates and source and drain regions of MOS transistors. Discuss how such deposition can be achieved without causing electrical shorts between the gate and source or drain of an individual transistor.

**SOLUTION:**

The deposition can be achieved by using the oxide spacer.

- 2.5** In VLSI technologies with multiple layers of metallic interconnects, one of the most yield-limiting processes is the patterning of metal lines, especially when the surface features before metal deposition are not flat. To achieve flat surfaces, chemical mechanical polishing (CMP) has been introduced. Discuss the side effects of CMP on the circuit performance and the process steps following CMP.

**SOLUTION:**

After CMP, the metal lines become more close to each other such that the parasitic capacitances may increase. The process steps following CMP are as those from plain.

- 2.6** Discuss the difficulties in processing a window mask which contains a wide variation of window sizes, i.e., both very large rectangle and minimum size square shapes. In particular, what problem would you expect when the process control is based on the monitoring of smallest windows? How about the opposite case in which the process control is based on the largest window?

**SOLUTION:**

If the process control is based on monitoring the smallest windows, then during etching, the small windows may show complete etching but the big windows may not completely etched yet. If the process control is based on monitoring the largest window, then there could be misalignment for the smallest window.

- 2.7** The photolithography has been the driving force which enabled massive processing of MOS chips at low cost. Despite significant improvements in both photolithography and

photoresist materials, it has become increasingly more difficult to process very small, deep submicron feature sizes. Alternatives can be X-ray lithography or direct electron-beam writing. Discuss the difficulties inherent to such alternatives.

**SOLUTION:**

These alternatives turn out to be slow and expensive.

- 2.8 Consider a chip design using 10 mask levels. Suppose that each mask can be made with 98% yield. Determine the composite mask yield for the set of 10 masks. Would the processed chip yield be lower or higher than this composite yield? If your results are inconclusive, explain the reason.

**SOLUTION:**

The worst case composite mask yield would be

$$yield = 0.98^{10} = 0.817$$

81.7%. The processed chip yield could be higher than this composite yield, but could not be lower since this is the worst case situation.

## CHAPTER 3

### MOS TRANSISTOR

- 3.1** Consider a MOS system with the following parameters:

- $t_{ox} = 200 \text{ \AA}$
- $\phi_{GC} = -0.85 \text{ V}$
- $N_A = 2 \cdot 10^{15} \text{ cm}^{-3}$
- $Q_{ox} = q 2 \cdot 10^{11} \text{ C/cm}^2$

(a) Determine the threshold voltage  $V_{T0}$  under zero bias at room temperature ( $T=300\text{K}$ ).

Note that  $\epsilon_{ox} = 3.97\epsilon_0$  and  $\epsilon_{si} = 11.7\epsilon_0$ .

(b) Determine the type (p-type or n-type) and amount of channel implant ( $N_I/\text{cm}^2$ ) required to change the threshold voltage to 0.8V.

**SOLUTION:**

(a)

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$\phi_F = \frac{kT}{q} \ln \frac{n_i}{N_A} = 0.026 \ln \frac{1.45 \times 10^{10}}{2 \times 10^{15}} = -0.308 \text{ V}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.758 \times 10^{-7} \text{ F/cm}^2$$

$$\begin{aligned} Q_{B0} &= -\sqrt{2qN_A\epsilon_{si}|-2\phi_F|} \\ &= -\sqrt{2 \cdot 1.6 \times 10^{-19} \cdot 2 \times 10^{15} \cdot 11.7 \times 8.854 \times 10^{-14} \cdot |-2 \times 0.308|} \\ &= -2.01 \times 10^{-8} \end{aligned}$$

$$V_{T0} = -0.85 + 0.615 + \frac{2 \times 10^{-8}}{1.758 \times 10^{-7}} - \frac{1.6 \times 10^{-19} \cdot 2 \times 10^{11}}{1.758 \times 10^{-7}} = -0.303 \text{ V}$$

(b) p-type implanted needed in the amount of:

$$\Delta V = 0.8 - V_{T0} = 0.8 + 0.303 = 1.303 = \frac{qN_I}{C_{ox}}$$

$$N_I = \frac{1.303C_{ox}}{q} = \frac{1.303 \cdot 1.758 \times 10^{-7}}{1.6 \times 10^{-19}} = 1.21 \times 10^{12} \text{ cm}^{-2}$$

- 3.2** Consider a diffusion area which has the dimensions  $10\mu\text{m} \times 5\mu\text{m}$  and the abrupt junction depth is  $0.5\mu\text{m}$ . Its n-type impurity doping level is  $N_D = 1 \cdot 10^{20} \text{ cm}^{-3}$  and the surrounding p-type substrate doping level is  $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$ . Determine the capacitance when the diffusion area is biased at 5V and the substrate is biased at 0V. In this problem, assume that there is no channel-stop implant.

**SOLUTION:**

$$C_j(V) = A \cdot \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right)} \cdot \frac{1}{\sqrt{\phi_0 - V}}$$

$$\phi_0 = \frac{kT}{q} \ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 \ln \frac{1 \times 10^{16} \cdot 1 \times 10^{20}}{(1.45 \times 10^{10})^2} = 0.939$$

$$A = [5 \times 10 + 2(5 \times 0.5) + 2(10 \times 0.5)] = 65 \times 10^{-8}$$

$$C_j(V) = 65 \times 10^{-8} \sqrt{\frac{11.7 \cdot 8.854 \times 10^{-14} \cdot 1.6 \times 10^{-19}}{2} \left( \frac{1 \times 10^{36}}{1 \times 10^{20} + 1 \times 10^{16}} \right)} \frac{1}{\sqrt{0.939 + 5}} \\ = 7.678 \times 10^{-15} [F]$$

- 3.3** Describe the relationship between the mask channel length,  $L_M$ , and the electrical channel length,  $L$ . Are they identical? If not, how would you express  $L$  in terms of  $L_M$  and other parameters?

**SOLUTION:**

The electrical channel length is related to the mask channel length by:

$$L = L_M - 2L_D$$

where  $L_D$  is the lateral diffusion length.

- 3.4** How is the device junction temperature affected by the power dissipation of the chip and its package? Can you describe the relationship between the device junction temperature, ambient temperature, chip power dissipation and the packaging quality?

**SOLUTION:**

The device junction temperature at operating condition is given as  $T_j = T_a + \Theta P_{diss}$ , where  $T_a$  is the ambient temperature;  $P_{diss}$  is the power dissipated in the chip;  $\Theta$  is the thermal resistance of the packaging. A cheap package will have high  $\Theta$  which will result in large and possibly damaging junction temperature. Thus the choice of packaging must be such that it is both economic and protective of the device.

- 3.5** Describe the three components of the load capacitance  $C_{load}$ , when a logic gate is driving other fanout gates.

**SOLUTION:**

The three major components of the load capacitance are interconnect capacitance, the next stage input capacitance, i.e., the gate capacitance and the drain parasitic capacitances of the current stage.

**3.6** Consider a layout of an nMOS transistor shown in Fig.P3.6.

The process parameters are:

- $N_D = 2 \cdot 10^{20} \text{ cm}^{-3}$
- $N_A = 1 \cdot 10^{15} \text{ cm}^{-3}$
- $X_j = 0.5 \mu\text{m}$
- $L_D = 0.5 \mu\text{m}$
- $t_{ox} = 0.05 \mu\text{m}$
- $V_{T0} = 0.8 \text{ V}$
- Channel stop doping =  $16.0 \times (\text{p-type substrate doping})$

Find the effective drain parasitic capacitance when the drain node voltage changes from 5V to 2.5V.

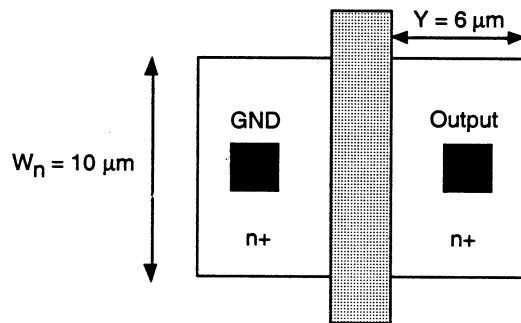


Figure P3.6

**SOLUTION:**

$$\phi_0 = \frac{kT}{q} \ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 \ln \left[ \frac{1 \times 10^{15} \cdot 2 \times 10^{20}}{(1.45 \times 10^{10})^2} \right] = 0.8967[V]$$

$$\phi_{osw} = \frac{kT}{q} \ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 \ln \left[ \frac{16 \times 10^{15} \cdot 2 \times 10^{20}}{(1.45 \times 10^{10})^2} \right] = 0.9688[V]$$

$$C_{jo} = \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\sqrt{\phi_o}}} \\ = \sqrt{\frac{11.7 \times 8.854 \times 10^{-14} \times 1.6 \times 10^{-19} \times 10^{15}}{2 \times 0.8967}} = 9.6 \times 10^{-9}[F/cm^2]$$

$$C_{josw} = \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\sqrt{\phi_{osw}}}}$$

$$= \sqrt{\frac{11.7 \times 8.854 \times 10^{-14} \times 1.6 \times 10^{-19} \times 16 \times 10^{15}}{2 \times 0.9688}} = 36.94 \times 10^{-9} [F/cm^2]$$

$$C_{jsw} = X_j C_{josw} = 0.5 \times 10^{-4} \times 36.94 \times 10^{-9} = 1.847 [pF/cm]$$

$$A = Y \times W = 6 \times 10 = 60 [\mu m^2]$$

$$P = 2(Y + W) = 2(6 + 10) = 32 [\mu m]$$

$$K_{eq} = 2\sqrt{\phi_0} \left( \frac{\sqrt{\phi_0 + 5} - \sqrt{\phi_0 + 2.5}}{5 - 2.5} \right)$$

$$= 2\sqrt{0.8967} \left( \frac{\sqrt{5.8967} - \sqrt{3.3967}}{2.5} \right) = 0.44$$

$$K_{eq'} = 2\sqrt{\phi_{osw}} \left( \frac{\sqrt{\phi_{osw} + 5} - \sqrt{\phi_{osw} + 2.5}}{5 - 2.5} \right)$$

$$= 2\sqrt{0.9688} \left( \frac{\sqrt{5.9688} - \sqrt{3.4688}}{2.5} \right) = 0.46$$

$$C_{drain} = K_{eq} \cdot C_{jo} \cdot A + K_{eq'} \cdot C_{jsw} \cdot P$$

$$= 0.44 \times 9.6 \times 10^{-9} \times 60 \times 10^{-8} + 0.46 \times 1.847 \times 10^{-12} \times 32 \times 10^{-4}$$

$$= 5.25 [fF]$$

**3.7** A set of *I-V* characteristics of an nMOS transistor at room temperature are shown in below for different biasing conditions. Figure P3.7 shows the measurement setup. Using the data, find

- (a) The threshold voltage  $V_{T0}$ ,
- (b) electron mobility  $\mu_n$ ,
- (c) body effect coefficient gamma( $\gamma$ ).

Some of the parameters are known to be:

- $W/L = 1.0$
- $t_{ox} = 345 \text{ \AA}$
- $|2\phi_F| = 0.64 \text{ V}$

$V_{GS}$	$V_{DS}$	$V_{SB}$	$I_D [\mu A]$
4V	4V	0.0V	256
5V	5V	0.0V	441
4V	4V	2.6V	144
5V	5V	2.6V	256

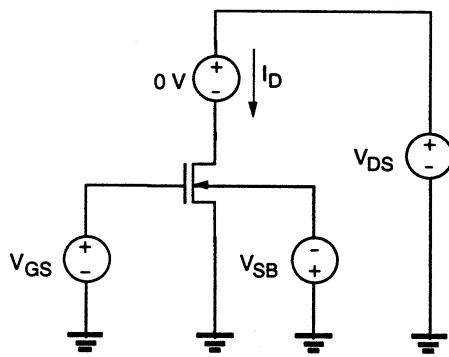


Figure P3.7

**SOLUTION:**

(a) Find  $V_{T0}$

For both case 1 (Row1) and case 2(Row2), the transistor operates in saturation region, using equation (3.62)

$$I_D(\text{sat}) = \frac{k_n}{2} (V_{GS} - V_{T0})^2$$

$$\frac{I_D(\text{Row1})}{I_D(\text{Row2})} = \frac{(4 - V_{T0})^2}{(5 - V_{T0})^2} = \frac{256}{441}.$$

$$\frac{4 - V_{T0}}{5 - V_{T0}} = \pm \frac{16}{21}$$

The correct solution is:

$$V_{T0} = 0.8[V]$$

(b) Find mobility

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{345 \times 10^{-8}} = 1.0 \times 10^{-7}[F/cm]$$

$$256 \times 10^{-6} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (4 - V_{T0})^2$$

$$\mu_n = \frac{2 \times 256 \times 10^{-6}}{1.0 \times 10^{-7} \times 1.0 \times 3.2^2} = 500 [cm^2/V \cdot s]$$

(c) Find body effect coefficient  $\gamma$

Using either Row 3 or Row4 data and equation (3.62), first find  $V_T$

$$144 \times 10^{-6} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (4 - V_T)^2$$

$$V_T = 1.6[V]$$

from equation (3.64)

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}} = \frac{1.6 - 0.8}{\sqrt{0.64 + 2.6} - \sqrt{0.64}} = 0.8[V^{1/2}]$$

- 3.8** Compare the two technology scaling methods, namely, (i) the constant electric field scaling and (ii) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay time, power dissipation, and power density are affected in terms of the scaling factor,  $S$ . To be more specific, what would happen if the design rules change from, say,  $1\mu\text{m}$  to  $1/S\mu\text{m}$  ( $S > 1$ )?

**SOLUTION:**

	<i>Const. E – field</i>	<i>Const. <math>V_{DD}</math></i>
$W, L, t_{ox}$	$1/S$	$1/S$
$V_{DD}$	$1/S$	1
$C_{ox}$	$S$	$S$
$C \propto C_{ox}WL$	$1/S$	$1/S$
$k_n, k_p$	$S$	$S$
$I_{DD}$	$1/S$	$S$
$t_{delay} \propto \frac{C\Delta V}{I_{DD}}$	$1/S$	$1/S^2$
$Power \propto I_{DD}V_{DD}$	$1/S^2$	$S$
$Power density \left( \frac{Power}{Area} \right)$	1	$S^3$

- 3.9** A pMOS transistor was fabricated on a n-type substrate with a bulk doping density of  $N_D = 10^{16}\text{cm}^{-3}$ , gate doping density(n-type poly) of  $N_{D,poly} = 10^{20}\text{cm}^{-3}$ ,  $Q_{ox}/q = 4 \cdot 10^{10}\text{cm}^{-2}$  and gate oxide thickness of  $t_{ox} = 0.1\mu\text{m}$ . Calculate the threshold voltage at room temperature for  $V_{SB} = 0$ . Use  $\epsilon_s = 11.7\epsilon_0$ .

**SOLUTION:**

$$\phi_F(\text{substrate}) = \frac{kT}{q} \ln \frac{N_{D,sub}}{n_i} = 0.026 \ln \frac{1 \times 10^{16}}{1.45 \times 10^{10}} = 0.348[V]$$

$$\phi_F(\text{gate}) = \frac{kT}{q} \ln \frac{N_{D,poly}}{n_i} = 0.026 \ln \frac{1 \times 10^{20}}{1.45 \times 10^{10}} = 0.587[V]$$

$$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = 0.348 - 0.587 = -0.239[V]$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-4}} = 3.45 \times 10^{-8}[F/cm^2]$$

$$\begin{aligned} Q_{B0} &= \sqrt{2qN_{D,sub}\epsilon_{si}|2\phi_F|} \\ &= \sqrt{2 \times 1.6 \times 10^{-19} \times 10^{16} \times 11.7 \times 8.85 \times 10^{-14} \times 2 \times 0.348} \\ &= 4.8 \times 10^{-8} [C/cm^2] \end{aligned}$$

$$\begin{aligned} V_{T0} &= \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\ &= -0.239 - 2 \times 0.348 - \frac{4.8 \times 10^{-8}}{3.45 \times 10^{-8}} - \frac{4 \times 10^{10} \times 1.6 \times 10^{-19}}{3.45 \times 10^{-8}} \\ &= -2.51 [V] \end{aligned}$$

**3.10** A depletion-type nMOS transistor has the following device parameters:

- $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{s}$
- $t_{ox} = 345 \text{ \AA}$
- $|2\phi_F| = 0.84 \text{ V}$
- $W/L = 1.0$

Some laboratory measurement results of terminal behavior of this device are shown in the table below. Using the data in the table, find the missing value of the gate voltage in the last entry. Show all of the details of your calculation.

$I_{DS} [\mu\text{A}]$	$V_D$	$V_S$	$V_B$	$V_g$
50.0	3V	0	0	0
40.0	5V	3V	0	?

### SOLUTION:

Assume at case 1 (Row1), the transistor is saturated, therefore

$$I_{ds} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{T0})^2 = \frac{1}{2} \times 500 \times \frac{3.9 \times 8.85 \times 10^{-14}}{345 \times 10^{-8}} (0 - V_{T0})^2$$

$$V_{T0} = -1.41 [V]$$

This is consistant with the assumption.

Now find  $\gamma$  in order to find  $V_T(V_{sb})$ .

Since

$$\begin{aligned} \phi_F &= \frac{kT}{q} \ln \frac{N_A}{n_i} \\ \frac{0.84}{2} &= 0.026 \ln \frac{N_A}{1.45 \times 10^{10}} \\ N_A &= 1.6 \times 10^{17} [cm^{-3}] \end{aligned}$$

From equation (3.24)

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{ox}} = \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 1.6 \times 10^{17} \times 11.7 \times 8.85 \times 10^{-14}}}{1.0 \times 10^{-7}} = 2.3$$

Note,  $\gamma$  is too large, this is a poorly designed device.

$$V_T(V_{sb}) = -1.41 + 2.3 \times (\sqrt{3+0.84} - \sqrt{0.84}) = 0.99[V]$$

Using case 2 data, again, assuming the transistor is saturated,

$$40 = \frac{1}{2} \times 50 \times (V_{gs} - 0.99)^2$$

$$V_{gs} = 2.25[V]$$

The assumption holds since,

$$V_{ds} = 2 > V_{gs} - V_T = 1.26$$

$$V_g = V_{gs} + V_s = 2.25 + 3 = 5.25[V]$$

- 3.11** Using the parameters given below, calculate the current through two nMOS transistors in series ( see Fig. P3.11), when the drain of the top transistor is tied to  $V_{DD}$ , the source of the bottom transistor is tied to  $V_{SS}=0$  and their gates are tied to  $V_{DD}$ . The substrate is also tied to  $V_{SS}=0V$ . Assume that  $W/L = 10$  for both transistors.

- $k' = 25 \mu\text{A}/\text{V}^2$
- $V_{T0} = 1.0 \text{ V}$
- $\gamma = 0.39 \text{ V}^{1/2}$
- $|2\phi_F| = 0.6 \text{ V}$

Hint: The solution requires some iterations and the body effect on threshold voltage has to be taken into account. Start with KCL equation.

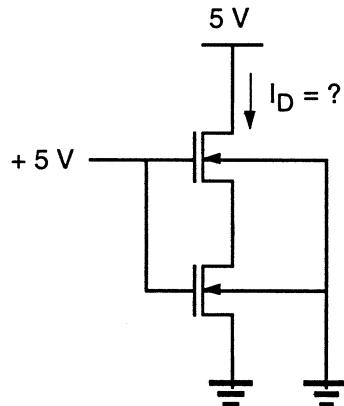


Figure P3.11

### SOLUTION:

Since gate voltage is high, the midpoint  $V_x$  is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

$$I_D = I_{D,driver} = I_{D,load}$$

$$\frac{1}{2}k' \frac{W}{L} (5 - V_x - V_{T,L}(V_x))^2 = \frac{1}{2}k' \frac{W}{L} (2(5 - V_{T0})V_x - V_x^2)$$

Using the following two equation to iteratively find the solution.

$$\begin{cases} (5 - V_x - V_{T,L}(V_x))^2 = 8V_x - V_x^2 \\ V_{T,L}(V_x) = 1 + 0.39(\sqrt{0.6 + V_x} - \sqrt{0.6}) \end{cases}$$

The intermediate values are listed in the table:

$V_{T,L}(V_x)$	$V_x$
1	2.83
1.42	0.97
1.19	1.08
1.20	1.07
1.20	1.07

$$I_D = \frac{1}{2} k' \frac{W}{L} (8V_x - V_x^2) = 0.5 \times 25 \times 10 \times (8 \times 1.07 - 1.07^2) = 927[\mu A]$$

**3.12** The following parameters are given for an nMOS process.

- $t_{ox} = 500\text{\AA}$
- substrate doping  $N_A = 1 \cdot 10^{16} \text{ cm}^{-3}$
- polysilicon gate doping  $N_D = 1 \cdot 10^{20} \text{ cm}^{-3}$
- oxide-interface fixed-charge density  $N_{ox} = 2 \cdot 10^{10} \text{ cm}^{-3}$
- (a) Calculate  $V_T$  for an unimplanted transistor.
- (b) What type and what concentration of impurities must be implanted to achieve  $V_T = +2V$  and  $V_T = -2V$ ?

### SOLUTION:

(a) For unimplanted transistor,

$$\phi_F(\text{substrate}) = \frac{kT}{q} \ln \frac{n_i}{N_A} = 0.026 \ln \frac{1.45 \times 10^{10}}{1.0 \times 10^{16}} = -0.35[V]$$

$$\phi_F(\text{gate}) = \frac{kT}{q} \ln \frac{N_{D,poly}}{n_i} = 0.026 \ln \frac{1 \times 10^{20}}{1.45 \times 10^{10}} = 0.59[V]$$

$$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.35 - 0.59 = -0.94[V]$$

$$\begin{aligned} Q_{B0} &= \sqrt{2qN_{A,sub}\epsilon_{si}|2\phi_F|} \\ &= \sqrt{2 \times 1.6 \times 10^{-19} \times 10^{16} \times 11.7 \times 8.85 \times 10^{-14} \times 2 \times 0.35} \\ &= -4.82 \times 10^{-8} [C/cm^2] \end{aligned}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{500 \times 10^{-8}} = 6.9 \times 10^{-8} [F/cm^2]$$

$$\begin{aligned}
V_{T0} &= \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\
&= -0.94 - 2 \times (-0.35) - \frac{(-4.82 \times 10^{-8})}{6.9 \times 10^{-8}} - \frac{2 \times 10^{10} \times 1.6 \times 10^{-19}}{6.9 \times 10^{-8}} \\
&= 0.41[V]
\end{aligned}$$

(b) For  $V_T = 2V$ :

$$V_T = 2 = V_{T0} - \frac{Q_{II}}{C_{ox}} = 0.412 - \frac{Q_{II}}{C_{ox}}$$

Negative charges needed in this case, so it must be p-type implant in the amount of  
 $Q_{II} = qN_I = (V_T - V_{T0})C_{ox}$

$$N_I = (2 - 0.41) \times \frac{6.9 \times 10^{-8}}{1.6 \times 10^{-19}} = 6.85 \times 10^{11} [cm^{-3}]$$

For  $V_T = -2V$ , positive charges need, must be n-type implant,

$$N_I = (2 + 0.41) \times \frac{6.9 \times 10^{-8}}{1.6 \times 10^{-19}} = 1.04 \times 10^{12} [cm^{-3}]$$

- 3.13** Using the measured data given below, determine the device parameters  $V_{T0}$ ,  $k$ ,  $\gamma$ , and  $\lambda$ , assuming  $2\phi_F = -0.6$  V.

$V_{GS}$	$V_{DS}$	$V_{BS}$	$I_D [\mu A]$
2	5	0	10
5	5	0	400
5	5	-3	280
5	8	0	480

### SOLUTION:

When  $V_{DS} \geq V_{GS}$ , the transistor operates in saturation region, therefore

$$I_{DSAT} = \frac{k}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

a) Find  $\lambda$ :

$$\begin{aligned}
\frac{I_{DSAT}(Row4)}{I_{DSAT}(Row2)} &= \frac{1 + \lambda V_{DS}(Row4)}{1 + \lambda V_{DS}(Row2)} = \frac{1 + 8\lambda}{1 + 5\lambda} = \frac{480}{400} \\
\lambda &= 0.1[V^{-1}]
\end{aligned}$$

b) Find  $V_{T0}$

$$\frac{I_{DSAT}(Row2)}{I_{DSAT}(Row1)} = \frac{(5 - V_{T0})^2}{(2 - V_{T0})^2}$$

$$V_{T0} = 1.44[V] \quad \text{and} \quad V_{T0} = 2.41[V] (\text{unreal})$$

c) Find  $k$ :

From Row2 data,

$$400 = \frac{k}{2} (5 - 1.44)^2 (1 + 0.1 \times 5)$$

$$k = 42 [\mu A/V^2]$$

d) Find  $\gamma$ :

From Row3 data,

$$280 = \frac{42}{2} (5 - V_T(V_{BS} = -3))^2 (1 + 0.1 \times 5)$$

$$V_T(V_{BS} = -3) = 2.02 [V]$$

$$2.02 = 1.44 + \gamma (\sqrt{3+0.6} - \sqrt{0.6})$$

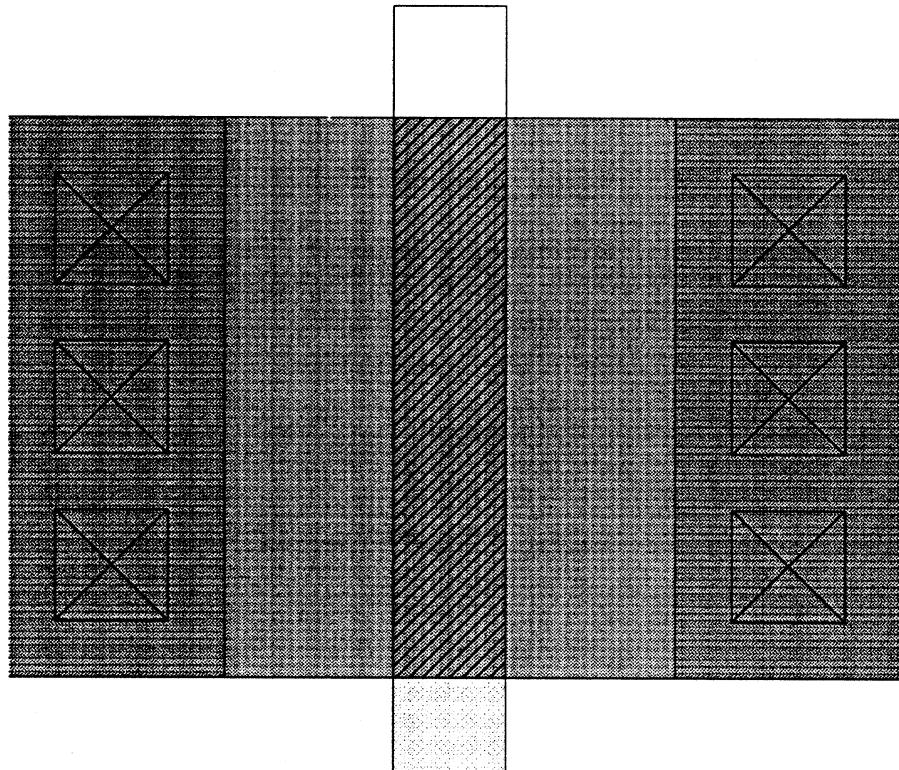
$$\gamma = 0.52 [V^{1/2}]$$

- 3.14 Using the design rules specified in Chapter 2, sketch a simple layout of an nMOS transistor on grid paper. Use a minimum feature size of  $3\mu m$ . Neglect the substrate connection. After you complete the layout, calculate approximate values for  $C_g$ ,  $C_{sb}$ , and  $C_{db}$ . The following parameters are given:

- Substrate doping  $N_A = 10^{16} \text{ cm}^{-3}$
- Drain/source doping  $N_D = 10^{19} \text{ cm}^{-3}$
- $W = 15 \mu m$
- $L = 3 \mu m$
- $t_{ox} = 0.05 \mu m$

#### SOLUTION:

The layout is shown in the following.



Calculate capacitances:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{500 \times 10^{-8}} = 6.9 \times 10^{-8} \text{ F/cm}^2$$

$$C_g = C_{ox} WL = 6.9 \times 10^{-8} \times 15 \times 3 \times 10^{-8} = 31.5 \text{ fF}$$

Since drain and source have the same geometry, the junction capacitance are the same.

$$\phi_0 = \frac{kT}{q} \ln \frac{N_A \cdot N_D}{n_i^2} = 0.026 \ln \left[ \frac{1 \times 10^{16} \cdot 1 \times 10^{19}}{(1.45 \times 10^{10})^2} \right] = 0.879 \text{ V}$$

$$\phi_{osw} = \frac{kT}{q} \ln \frac{N_A(sw) \cdot N_D}{n_i^2} = 0.026 \ln \left[ \frac{1 \times 10^{17} \cdot 1 \times 10^{19}}{(1.45 \times 10^{10})^2} \right] = 0.939 \text{ V}$$

$$C_{jo} = \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\sqrt{\phi_o}}} \\ = \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 10^{16}}{2 \times 0.879}} = 3.07 \times 10^{-8} \text{ F/cm}^2$$

$$C_{josw} = \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D} \right) \cdot \frac{1}{\sqrt{\phi_{osw}}}} \\ = \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 1 \times 10^{17}}{2 \times 1.01 \times 0.939}} = 9.35 \times 10^{-8} \text{ F/cm}^2$$

Assume junction depth is 0.5 μm,

$$C_{jsw} = X_j C_{josw} = 0.5 \times 10^{-4} \times 9.35 \times 10^{-8} = 4.67 \text{ pF/cm}$$

$$AD = AS = Y \cdot W = 10.5 \times 15 = 157.5 \text{ } \mu\text{m}^2$$

$$PD = PS = 2(Y + W) = 51 \text{ } \mu\text{m}$$

$$C_{db} = C_{sb} = AD \cdot C_{jo} + PD \cdot C_{jsw} \\ = 157.5 \times 10^{-8} \times 3.07 \times 10^{-8} + 51 \times 10^{-4} \times 4.67 \times 10^{-12} \\ = 72.2 \text{ fF}$$

- 3.15** Derive the current equation for a p-channel MOS transistor operating in the linear region, i.e., for  $V_{SG} + V_{TP} > V_{SD}$ .

### SOLUTION:

Following the analysis in the text, section 3.4, using gradual channel approximation:

$$Q_I(y) = C_{ox}(V_{SG} - V_C(y) - V_{TP})$$

$$dR = \frac{dy}{W \cdot \mu_p \cdot Q_I(y)}$$

$$dV_C = I_D \cdot dR = \frac{I_D}{W \cdot \mu_p \cdot Q_I(y)} dy$$

$$\int_0^L I_D dy = W \cdot \mu_p \int_0^{V_{SD}} Q_I \cdot dV_C$$

$$I_D \cdot L = W \cdot \mu_p \cdot C_{ox} \int_0^{V_{SD}} (V_{SG} - V_C(y) - V_{TP}) \cdot dV_C$$

$$I_D = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} [2(V_{SG} - V_{TP})V_{SD} - V_{SD}^2]$$

- 3.16** An enhancement-type nMOS transistor has the following parameters:

- $V_{T0} = 0.8V$
  - $\gamma = 0.2V^{1/2}$
  - $\lambda = 0.05V^{-1}$
  - $|2\phi_F| = 0.58V$
  - $k' = 20 \mu A/V^2$
- (a) When the transistor is biased with  $V_G = 2.8 V$ ,  $V_D = 5 V$ ,  $V_S = 1 V$ ,  $V_B = 0 V$ , the drain current  $I_D = 0.24 \text{ mA}$ . Determine  $W/L$ .
- (b) Calculate  $I_D$  for  $V_G = 5 V$ ,  $V_D = 4 V$ ,  $V_S = 2 V$  and  $V_B = 0 V$ .
- (c) If  $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{s}$  and  $C_g = C_{ox} \cdot W \cdot L = 1.0 \times 10^{-15} \text{ F}$ , find  $W$  and  $L$ .

### SOLUTION:

(a) For enhancement transistor and  $V_{T0} > 0$ , it must be nMOS.

$$V_T(V_{SB}) = V_{T0} + \gamma \left( \sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right)$$

$$= 0.8 + 0.2 \cdot \left( \sqrt{0.58 + 1} - \sqrt{0.58} \right) = 0.899[V]$$

$$\because V_{DS} = 4 > V_{GS} - V_T = 1.8 - 0.899 = 0.901$$

nMOS transistor is in saturation region.

$$\begin{aligned} \because I_D(\text{sat}) &= \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \\ \therefore \frac{W}{L} &= \frac{2 \cdot I_D(\text{sat})}{k' \cdot (V_{GS} - V_T)^2 (1 + \lambda V_{DS})} \\ &= \frac{2 \cdot 0.24 \times 10^{-3}}{20 \times 10^{-6} (1.8 - 0.899)^2 (1 + 0.05 \times 4)} = 24.64 \end{aligned}$$

(b)

$$V_T(V_{SB}) = V_{T0} + \gamma \left( \sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right)$$

$$= 0.8 + 0.2 \cdot \left( \sqrt{0.58 + 2} - \sqrt{0.58} \right) = 0.969[V]$$

$$\because V_{DS} = 2 < V_{GS} - V_T = 3 - 0.969 = 2.031$$

nMOS transistor is in linear region.

$$\begin{aligned} I_D(\text{lin}) &= \frac{k'}{2} \frac{W}{L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] [1 + \lambda V_{DS}] \\ &= 10 \times 10^{-6} \times 24.64 [2 \times (3 - 0.969) \times 2 - 4] [1 + 0.05 \times 2] \\ &= 1.12[\text{mA}] \end{aligned}$$

(c)

$$C_{ox} = \frac{k'}{\mu_n} = \frac{20 \times 10^{-6}}{500} = 4 \times 10^{-8} [\text{F/cm}^2]$$

$$\begin{cases} W \cdot L = \frac{C_g}{C_{ox}} = \frac{10^{-15}}{4 \times 10^{-8}} = 2.5 \times 10^{-8} [cm^2] \\ \frac{W}{L} = 24.64 \end{cases}$$

Solve for W and L,

$$\begin{cases} W = 7.85 [\mu m] \\ L = 0.32 [\mu m] \end{cases}$$

**3.17** An nMOS transistor is fabricated with the following physical parameters:

- $N_D = 10^{20} \text{ cm}^{-3}$
- $N_A(\text{substrate}) = 10^{16} \text{ cm}^{-3}$
- $N_A^+(\text{chanstop}) = 10^{19} \text{ cm}^{-3}$
- $W = 10 \mu\text{m}$
- $Y = 5 \mu\text{m}$
- $L = 1.5 \mu\text{m}$
- $L_D = 0.25 \mu\text{m}$
- $X_j = 0.4 \mu\text{m}$

(a) Determine the drain diffusion capacitance for  $V_{DB} = 5 \text{ V}$  and  $2.5 \text{ V}$ .

(b) Calculate the overlap capacitance between the gate and drain for an oxide thickness of  $t_{ox} = 200 \text{ \AA}$ .

**SOLUTION:**

(a)

$$\phi_o = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} = 0.026 \ln \frac{10^{16} \cdot 10^{20}}{(1.45 \times 10^{10})^2} = 0.94 [V]$$

$$\begin{aligned} C_{jo} &= \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_o}} \\ &= \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19}}{2} \cdot \frac{10^{20} \cdot 10^{16}}{10^{20} + 10^{16}} \cdot \frac{1}{0.94}} \\ &= 2.98 \times 10^{-8} [F/cm^2] \end{aligned}$$

$$A = W \cdot Y + W \cdot X_j = 10 \times 5 + 10 \times 0.4 = 54 [\mu m^2]$$

$$C_j(V) = \frac{A \cdot C_{jo}}{\sqrt{1 - \frac{V}{\phi_o}}}$$

$$C_j(-5) = \frac{54 \times 10^{-8} \cdot 2.98 \times 10^{-8}}{\sqrt{1 + \frac{5}{0.94}}} = 6.4 \times 10^{-15} [F]$$

$$C_j(-2.5) = \frac{54 \times 10^{-8} \cdot 2.98 \times 10^{-8}}{\sqrt{1 + \frac{2.5}{0.94}}} = 8.41 \times 10^{-15} [F]$$

For sidewall capacitance calculation,

$$\phi_{osw} = \frac{kT}{q} \ln \frac{N_A(sw) \cdot N_D}{n_i^2} = 0.026 \ln \frac{10^{19} \cdot 10^{20}}{(1.45 \times 10^{10})^2} = 1.118 [V]$$

$$\begin{aligned} C_{josw} &= \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D} \right) \cdot \frac{1}{\phi_{osw}}} \\ &= \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19}}{2} \cdot \frac{10^{20} \cdot 10^{19}}{10^{20} + 10^{19}} \cdot \frac{1}{1.118}} \\ &= 8.207 \times 10^{-7} [F/cm^2] \end{aligned}$$

$$\begin{aligned} C_{jsw}(V) &= \frac{P \cdot X_j \cdot C_{josw}}{\sqrt{1 - \frac{V}{\phi_{osw}}}} = \frac{(2 \times 5 + 10) \times 0.4 \times 8.207 \times 10^{-7}}{\sqrt{1 - \frac{V}{1.118}}} \\ &= \frac{6.566 \times 10^{-14}}{\sqrt{1 - \frac{V}{1.118}}} [F] \end{aligned}$$

$$C_{jsw}(-5V) = \frac{6.566 \times 10^{-14}}{\sqrt{1 + \frac{5}{1.118}}} = 28.07 \times 10^{-15} [F]$$

$$C_{jsw}(-2.5V) = \frac{6.566 \times 10^{-14}}{\sqrt{1 + \frac{2.5}{1.118}}} = 36.50 \times 10^{-15} [F]$$

$$\langle C_{db} \rangle (-5V) = C_j(-5V) + C_{jsw}(-5V) = 6.4 + 28.07 = 34.47 [fF]$$

$$\langle C_{db} \rangle (-2.5V) = C_j(-2.5V) + C_{jsw}(-2.5V) = 8.41 + 36.5 = 44.91 [fF]$$

(b)

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{200 \times 10^{-8}} = 1.726 \times 10^{-7} [F/cm^2]$$

$$C_{gd} = C_{ox} \cdot W \cdot L_D = 1.726 \times 10^{-7} \times 10 \times 10^{-4} \times 0.25 \times 10^{-4} = 4.31 [fF]$$

## CHAPTER 4

# MODELING OF MOS TRANSISTORS USING SPICE

- 4.1** Rewrite the SPICE code for the nMOS model in Example 4.1 for graded junction using the following parameters:

- $N_A = 2 \cdot 10^{15} \text{ cm}^{-3}$
- $N_A(\text{sidewall}) = 2.1 \cdot 10^{16} \text{ cm}^{-3}$
- $N_D = 10^{19} \text{ cm}^{-3}$
- $X_j = 0.5 \mu\text{m}$
- $t_{ox} = 200 \text{ Å}$
- $L_D = 0.2 \mu\text{m}$

**SOLUTION:**

Follow the steps in Example 4.1, calculate the parameter:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{200 \times 10^{-8}} = 1.73 \times 10^{-7} [\text{F/cm}^2]$$

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{ox}} = \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 2 \times 10^{15} \times 11.7 \times 8.85 \times 10^{-14}}}{1.73 \times 10^{-7}} = 0.15 [\text{V}^{1/2}]$$

$$|2\phi_F(\text{substrate})| = \left| 2 \frac{kT}{q} \ln \frac{n_i}{N_A} \right| = \left| 2 \times 0.026 \ln \frac{1.45 \times 10^{10}}{2.0 \times 10^{15}} \right| = 0.615 [\text{V}]$$

$$\phi_o = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} = 0.026 \ln \frac{2 \times 10^{15} \cdot 10^{19}}{(1.45 \times 10^{10})^2} = 0.837 [\text{V}]$$

$$\phi_{osw} = \frac{kT}{q} \ln \frac{N_A(\text{sw}) \cdot N_D}{n_i^2} = 0.026 \ln \frac{2.1 \times 10^{16} \cdot 10^{19}}{(1.45 \times 10^{10})^2} = 0.898 [\text{V}]$$

$$\begin{aligned} C_{jo} &= \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_o}} \\ &= \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19}}{2} \cdot \frac{2 \times 10^{15} \cdot 10^{19}}{2 \times 10^{15} + 10^{19}} \cdot \frac{1}{0.837}} \\ &= 1.41 \times 10^{-8} [\text{F/cm}^2] = 1.41 \times 10^{-4} [\text{F/m}^2] \end{aligned}$$

$$\begin{aligned} C_{jsw} &= X_j \cdot \sqrt{\frac{\epsilon_{si} \cdot q}{2} \left( \frac{N_A(\text{sw}) \cdot N_D}{N_A(\text{sw}) + N_D} \right) \cdot \frac{1}{\phi_{osw}}} \\ &= 0.5 \times 10^{-4} \cdot \sqrt{\frac{11.7 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19}}{2} \cdot \frac{2.1 \times 10^{16} \times 10^{19}}{2.1 \times 10^{16} + 10^{19}} \cdot \frac{1}{0.898}} \\ &= 2.2 \times 10^{-12} [\text{F/cm}] = 2.2 \times 10^{-10} [\text{F/m}] \end{aligned}$$

$$C_{GSO} = C_{GDO} = C_{ox} \cdot L_D = 1.73 \times 10^{-7} \times 0.2 \times 10^{-4} \\ = 3.46 \times 10^{-12} [F/cm] = 3.46 \times 10^{-10} [F/m]$$

Thus, the SPICE input file is as follows:

```
M1 6 12 4 7 NM1 W=5U L=3U LD=0.2U AS=36P PS=24.4U AD=93P
+ PD=42.4U
.MODEL NM1 NMOS (VTO=0.85 KP=45U LAMBDA=0.05 GAMMA=0.32
+ PHI=0.615 PB=0.837 CJ=1.41E-4 CJSW=2.2E-10
+ CGSO=3.46E-10 CGDO=3.46E-10 MJ=0.33 MJSW=0.5)
```

- 4.2 A layout of nMOS transistors in NAND2 gate is shown below. Write a SPICE description corresponding to the layout. The diffusion region between two polysilicon gates can be split equally between the two transistors.

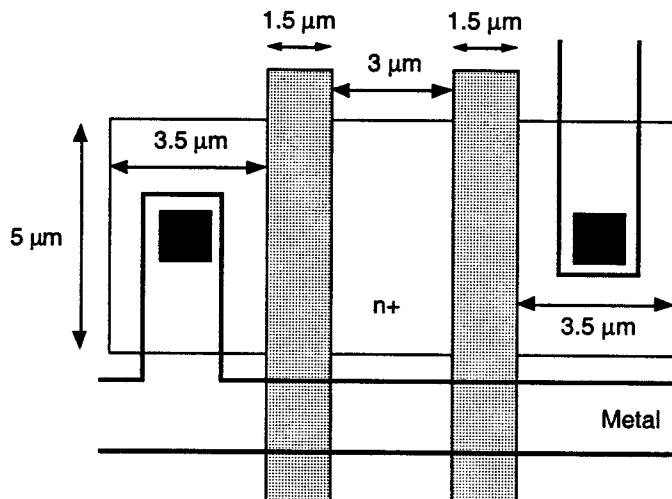


Figure P4.2

**SOLUTION:**

The SPICE input list could be as follows:

```
M1 2 1 0 0 NMOD W=5U L=1.5U AS=17.5P PS=17U AD=7.5P PD=8U
M2 4 3 2 0 NMOD W=5U L=1.5U AS=7.5P PS=8U AD=17.5P PD=17U
```

- 4.3 Using the SPICE LEVEL 1 MOSFET model equations, derive an expression for the sensitivity of the drain current  $I_D$  with respect to temperature. Calculate the sensitivity at room temperature  $T=300K$  by using the values in Example 4.1. For simplicity, assume that  $n_i$  is independent of temperature. Also verify your solution numerically by calculating  $I_D$  at 310K and then  $\Delta I_D / \Delta T$ .

**SOLUTION:**

The sensitivity of drain current with respect to temperature T can be expressed by:

$$\frac{\partial I_D}{\partial T} = \frac{\partial I_D}{\partial \mu_n} \cdot \frac{\partial \mu_n}{\partial T} + \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial T}$$

where in SPICE level 1 model,

$$\frac{\partial I_D}{\partial \mu_n} = \frac{I_D}{\mu_n}$$

The mobility temperature dependence is:

$$\mu_n(T) = \frac{\mu_n(300K)}{\left(\frac{T}{300}\right)^{3/2}}$$

$$\frac{\partial \mu_n}{\partial T} = -\frac{\mu_n(300K)}{200} \cdot \left(\frac{T}{300}\right)^{-5/2}$$

For simplicity, assume  $V_{SB} = 0$  V,

$$V_T = V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$\frac{\partial V_T}{\partial T} = \frac{\partial \Phi_{GC}}{\partial T} - 2\frac{\partial \phi_F}{\partial T} - \frac{1}{C_{ox}} \frac{\partial Q_{B0}}{\partial T}$$

$$\phi_F = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

$$\frac{\partial \phi_F}{\partial T} = \frac{\phi_F}{T}$$

$$\Phi_{GC} = \frac{kT}{q} \ln \frac{n_i^2}{N_A \cdot N_D}$$

$$\frac{\partial \Phi_{GC}}{\partial T} = \frac{\Phi_{GC}}{T}$$

$$Q_{B0} = \sqrt{2qN_A \epsilon_{si} |2\phi_F|}$$

$$\frac{\partial Q_{B0}}{\partial T} = -\frac{1}{2} \frac{Q_{B0}}{\phi_F} \frac{\partial \phi_F}{\partial T} = -\frac{1}{2} \frac{Q_{B0}}{T}$$

In linear region,

$$\frac{\partial I_D}{\partial V_T} = -\frac{\mu_n C_{ox}}{2} \frac{W}{L_{eff}} (1 + \lambda V_{DS}) (2V_{DS})$$

Therefore,

$$\begin{aligned} \frac{\partial I_D}{\partial V_T} &= -\frac{I_D}{\mu_n} \frac{\mu_n(300K)}{200} \left(\frac{T}{300}\right)^{-5/2} \\ &\quad - \frac{\mu_n C_{ox}}{2} \frac{W}{L_{eff}} (1 + \lambda V_{DS}) (2V_{DS}) \left[ \frac{\partial \Phi_{GC}}{\partial T} - 2\frac{\partial \phi_F}{\partial T} - \frac{1}{C_{ox}} \frac{\partial Q_{B0}}{\partial T} \right] \end{aligned}$$

In saturation region,

$$\frac{\partial I_D}{\partial V_T} = -\mu_n C_{ox} \frac{W}{L_{eff}} (1 + \lambda V_{DS}) (V_{GS} - V_T) V_T$$

$$\begin{aligned}\frac{\partial I_D}{\partial V_T} &= -\frac{I_D}{\mu_n} \frac{\mu_n(300K)}{200} \cdot \left(\frac{T}{300}\right)^{-5/2} \\ &\quad -\mu_n C_{ox} \frac{W}{L_{eff}} (1 + \lambda V_{DS}) (V_{GS} - V_T) V_T \left[ \frac{\partial \Phi_{GC}}{\partial T} - 2 \frac{\partial \phi_F}{\partial T} - \frac{1}{C_{ox}} \frac{\partial Q_{B0}}{\partial T} \right]\end{aligned}$$

At T = 300 K, when V<sub>DS</sub> = 5V, V<sub>BS</sub> = 0V, the transistor is saturated.

$$I_D = \frac{45 \times 10^{-6}}{2} \left(\frac{5}{2}\right) (5 - 0.85)^2 (1 + 0.05 \times 5) = 1.21 \text{ mA}$$

$$\frac{\partial I_D}{\partial V_T} = -2 \times 45 \times 10^{-6} \left(\frac{5}{2}\right) (1 + 0.25) (5 - 0.85) 0.85 = -0.992 \frac{\text{mA}}{\text{V}}$$

$$\mu_n = \frac{k'}{C_{ox}} = \frac{45 \times 10^{-6}}{5.75 \times 10^{-8}} = 783 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$$

$$\frac{\partial I_D}{\partial \mu_n} = \frac{I_D}{\mu_n} = \frac{1.21}{783} = 1.55 \times 10^{-3} \frac{\text{mA}}{\text{cm}^2 / \text{V} \cdot \text{s}}$$

$$\frac{\partial \mu_n}{\partial T} = -\frac{1}{200} (783) = -3.92 \frac{\text{cm}^2 / \text{V} \cdot \text{s}}{\text{K}}$$

$$\begin{aligned}\frac{\partial V_T}{\partial T} &= \frac{\Phi_{GC}}{T} - 2 \frac{\phi_F}{T} + \frac{1}{2C_{ox}} \frac{Q_{B0}}{T} \\ &= -\frac{0.875}{300} - 2 \frac{-0.289}{300} + \frac{1.38 \times 10^{-8}}{2 \times 5.75 \times 10^{-8} \times 300} = -5.9 \times 10^{-4} \frac{\text{V}}{\text{K}}\end{aligned}$$

$$\frac{\partial I_D}{\partial T} = 1.55 \times 10^{-3} (-3.92) + (-0.992) (-5.9 \times 10^{-4}) = -5.49 \times 10^{-3} \frac{\text{mA}}{\text{K}}$$

Calculate I<sub>D</sub> at T = 310K.

$$\phi_F = -2.76 \text{ V}$$

$$\Phi_{GC} = -0.861 \text{ V}$$

$$\frac{Q_{B0}}{C_{ox}} = 0.235 \text{ V}$$

$$V_{TO} = 0.846 \text{ V}$$

$$\mu_n = \frac{\mu_n(300K)}{\left(\frac{310}{300}\right)^{3/2}} = 745 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}$$

$$I_D = \frac{745 \times 5.75 \times 10^{-8}}{2} \left(\frac{5}{2}\right) (5 - 0.846)^2 (1 + 0.25) = 1.156 \text{ mA}$$

$$\frac{\Delta I_D}{\Delta T} = \frac{1.156 - 1.21}{310 - 300} = -5.5 \times 10^{-3} \frac{\text{mA}}{\text{K}}$$

The two results are very similar.

- 4.4** Explain why several versions of nMOS transistor models and pMOS transistor models coexist despite the fact that some models are more accurate than others.

**SOLUTION:**

Some models are more accurate especially for short channel devices, but they have a lot of model parameters and are thus very complicated. Some models are less accurate and much simpler. Therefore there is a need for different purposes, thus different models coexist.

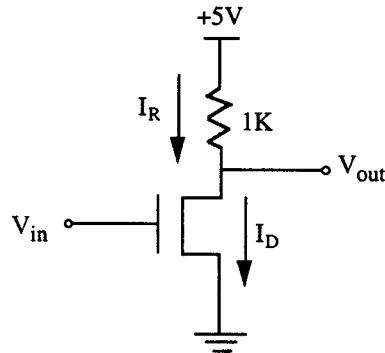
## CHAPTER 5

### MOS INVERTERS: STATIC CHARACTERISTICS

- 5.1** Design a resistive-load inverter with  $R = 1\text{k}\Omega$  such that  $V_{OL} = 0.6$  V when an enhancement-type nMOS driver transistor has the following parameters:
- $V_{DD} = 5.0$  V
  - $V_{T0} = 1.0$  V
  - $\gamma = 0.2 \text{ V}^{1/2}$
  - $\lambda = 0.0 \text{ V}^{-1}$
  - $k' = 22.0 \mu\text{A/V}^2$
- Determine the required aspect ratio,  $W/L$ .
  - Determine  $V_{IL}$  and  $V_{IH}$ .
  - Determine noise margins  $NM_L$  and  $NM_H$ .

**SOLUTION:**

(a)



When  $V_{out} = V_{OL}$ ,  $V_{in} = V_{DD} = 5.0$  V, the driver transistor operates in linear region. Using Eq.(5.12)

$$I_R = \frac{V_{DD} - V_{OL}}{1K} = \frac{k' W}{2 L} [2(V_{OH} - V_{T0})V_{OL} - V_{OL}^2]$$

$$\frac{5 - 0.6}{1000} = \frac{22 \times 10^{-6}}{2} \frac{W}{L} [2(5 - 1)0.6 - 0.6^2]$$

Solve for  $W/L$ ,

$$\frac{W}{L} = 90.1$$

(b) When  $V_{in} = V_{IL}$ , driver transistor operates in saturation region. Using Eq.(5.19)

$$\frac{V_{DD} - V_{out}}{R_L} = k' \frac{W}{L} \frac{(V_{in} - V_{T0})^2}{2}$$

Taking derivative with respect to  $V_{in}$  and set  $\left. \frac{dV_{out}}{dV_{in}} \right|_{V_{in}=V_{IL}} = -1$

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IL}} = k' \frac{W}{L} (V_{IL} - V_{T0}) = \frac{1}{R_L}$$

Thus,

$$V_{IL} = V_{T0} + \frac{1}{R_L \cdot k' \frac{W}{L}} = 1.0 + \frac{1}{1000 \cdot 22 \times 10^{-6} \cdot 90.1} = 1.5[V]$$

When  $V_{in} = V_{IH}$ , driver transistor operates in linear region. Using Eq.(5.24) repeated here:

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'}{2} \frac{W}{L} [2(V_{in} - V_{T0})V_{out} - V_{out}^2]$$

Differentiating both sides with respect to  $V_{in}$  and set  $\frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IH}} = -1$ ,

$$-\frac{1}{R_L} \frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IH}} = \frac{k'}{2} \frac{W}{L} \left[ 2(V_{in} - V_{T0}) \frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IH}} + 2V_{out} - 2V_{out} \frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IH}} \right]$$

$$\frac{1}{R_L} = k' \frac{W}{L} [(V_{IH} - V_{T0})(-1) + 2V_{out}]$$

$$V_{IH} = V_{T0} + 2V_{out} - \frac{1}{R_L k' \frac{W}{L}}$$

Plug in back to Eq.(5.24) repeated above to solve for  $V_{out}$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'}{2} \frac{W}{L} \left[ 2 \left( V_{T0} + 2V_{out} - \frac{1}{R_L k' \frac{W}{L}} - V_{T0} \right) V_{out} - V_{out}^2 \right]$$

$$V_{out} \Big|_{V_{in}=V_{IH}} = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{R_L k' \frac{W}{L}}}$$

$$\begin{aligned} V_{IH} &= V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{R_L k' \frac{W}{L}} - \frac{1}{R_L k' \frac{W}{L}}} \\ &= 1.0 + \sqrt{\frac{8}{3} \frac{5}{1000 \cdot 22 \times 10^{-6} \cdot 90.1} - \frac{1}{1000 \cdot 22 \times 10^{-6} \cdot 90.1}} = 3.09[V] \end{aligned}$$

(c)

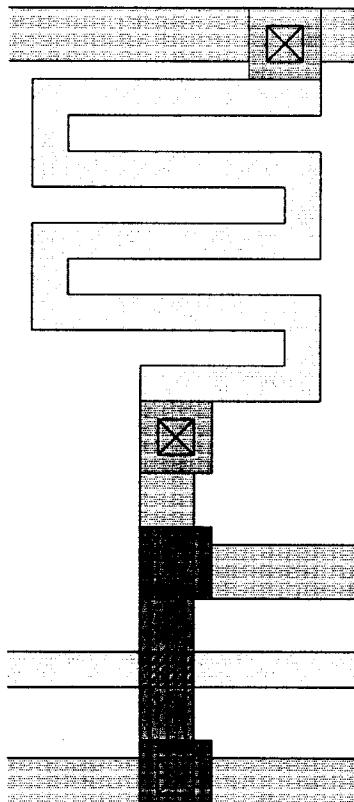
$$NM_L = V_{IL} - V_{OL} = 1.5 - 0.6 = 0.9 [V]$$
$$NM_H = V_{OH} - V_{IH} = 5.0 - 3.09 = 1.91 [V]$$

## 5.2 Layout of the resistive-load inverter design.

- (a) Draw the layout of the R-load inverter designed in excise problem (5.6) using a polysilicon resistor with sheet resistivity of  $25\Omega/\text{square}$  and the minimum feature size of  $2\mu\text{m}$ . It should be noted that  $L$  stands for the effective channel length which is related to the mask channel length as  $L=L_M + \delta - 2L_D$ , where  $\delta$  (process error) = 0 and  $L_D = 0.25 \mu\text{m}$ . To save the chip area, one should use the minimum sizes for  $L$  and  $W$ . Also, the resistor area can be reduced by using the folded layout (snake pattern) of the resistor.
- (b) Perform the circuit extraction to get the SPICE input list from the layout.
- (c) Run the SPICE program to obtain the DC voltage transfer characteristic (VTC) curve. Plot the VTC and check whether the calculated values in Problem 5.6 match with the SPICE results.

### SOLUTION:

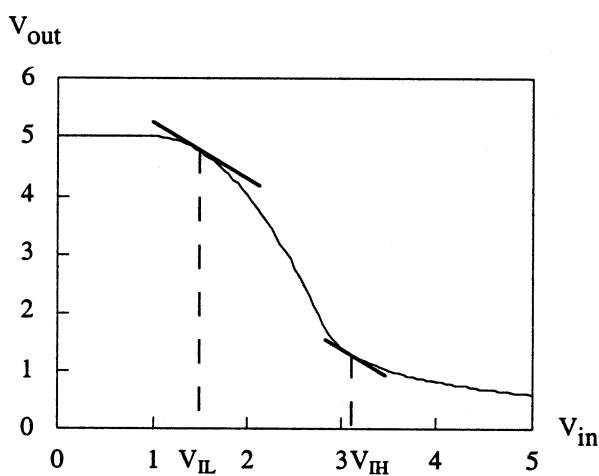
- (a) The layout is shown in the following.



(c). SPICE simulation for the parameters given in problem 5.6.  
SPICE input list:

```
R-load inverter DC analysis
m1 2 1 0 0 mn w=180u l=2u
r 3 2 1k
vdd 3 0 dc 5.0
vin 1 0 dc 0
.model mn nmos (vto=1.0 kp=22u gamma=0.2)
.dc vin 0 5 0.05
.print dc v(2)
.end
```

The VTC curve is shown in the following.  $V_{IL}$  and  $V_{IH}$  match the calculated values.



$$V_{IL} = 1.5 \text{ V}$$
$$V_{IH} = 3.1 \text{ V}$$

- 5.3 Refer to the CMOS process described in Chapter 2. Draw cross-sections of the following device along the lines A-A' and B-B'.

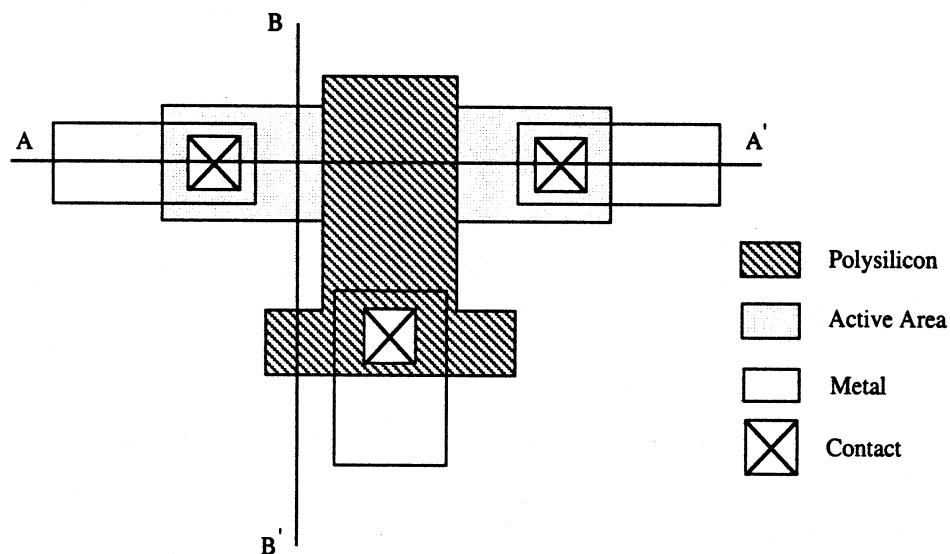
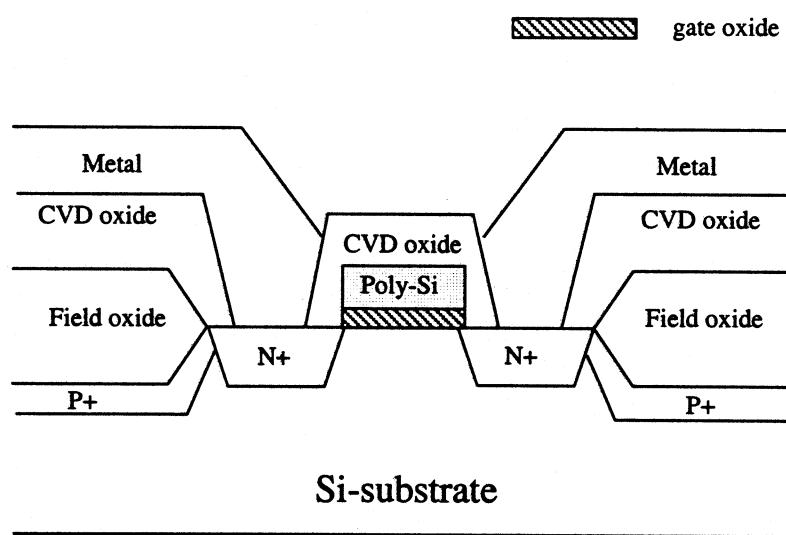


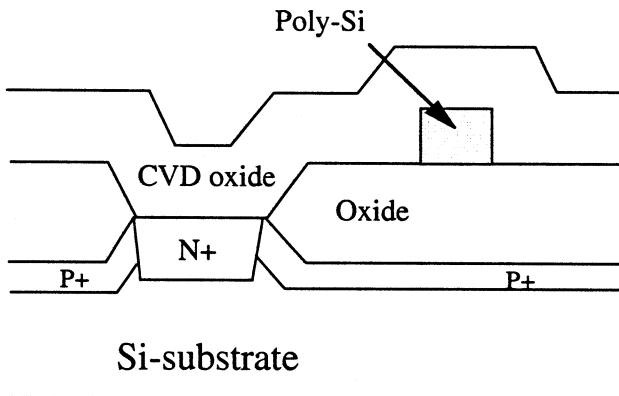
Figure P5.5

**SOLUTION:**

The cross section is not drawn to scale. For A-A',



The cross section for B-B':



#### 5.4 Calculation of $V_{OH}$ , $V_{OL}$ and the noise margins for the saturated enhancement-load nMOS inverter circuit.

##### SOLUTION:

In order to obtain  $NH_L$ ,  $V_{OL}$  and  $V_{IL}$  needs to be calculated. The value of  $V_{OH}$  must be found first to calculate  $V_{OL}$ .

$V_{OH}$ : load transistor in saturation, since  $\gamma=0$ ,  $V_T = V_{T0}$

$$\frac{k_{load}}{2} (V_{DD} - V_{OH} - V_{T0})^2 = 0$$

$$V_{OH} = V_{DD} - V_{T0} = 5 - 0.8 = 4.2V$$

$V_{OL}$ : load transistor in saturation, driver transistor in linear region, input is  $V_{OH}$

$$\frac{k_{load}}{2} (V_{DD} - V_{OL} - V_{T0})^2 = \frac{k_{driver}}{2} (2(V_{OH} - V_{T0})V_{OL} - V_{OL}^2)$$

$$(5 - V_{OL} - 0.8)^2 = 10(2(4.2 - 0.8)V_{OL} - V_{OL}^2)$$

$$11V_{OL}^2 - 76.4V_{OL} + 17.64 = 0$$

$$V_{OL} = 0.239V$$

$V_{IL}$ : load in saturation, driver in saturation.

$$\frac{k_{load}}{2} (V_{DD} - V_{out} - V_{T0})^2 = \frac{k_{driver}}{2} (V_{in} - V_{T0})^2$$

$$(5 - V_{out} - 0.8)^2 = 10(V_{in} - 0.8)^2 \quad (1)$$

take derivative with respect to  $V_{in}$  on both sides and use

$$\left. \frac{dV_{out}}{dV_{in}} \right|_{V_{IL}} = -1$$

$$2(4.2 - V_{out}) \left( \left. \frac{dV_{out}}{dV_{in}} \right|_{V_{IL}} \right) = 20(V_{IL} - 0.8)$$

$V_{out} = 12.2 - 10V_{IL}$  when  $V_{in} = V_{IL}$ . Thus plug these relationship back into (1)

$$(4.2 - 12.2 + 10V_{IL})^2 = 10(V_{IL} - 0.8)^2$$

$$90V_{IL}^2 - 144V_{IL} + 57.6 = 0$$

$$V_{IL} = 0.8V$$

$$NM_L = V_{IL} - V_{OL} = 0.8 - 0.239 = 0.561V$$

- 5.5** Please follow Example 5.3 and discussion of the design criteria for the depletion-load inverter circuit (pages 165 - 172).
- 5.6** Please follow Example 5.4 and discussion of the noise margins for the CMOS inverter circuit (pages 179 - 181).
- 5.7** Please follow the discussion of the inversion threshold for the CMOS inverter circuit (pages 181 - 182).
- 5.8** For Part (a), note that the nMOS transistor M3 operates in linear region, and that its drain current must be zero. Consequently, the drain-to-source voltage drop across M3 is also zero. Thus, the CMOS inverter operates at inversion threshold (by definition), and its output voltage is equal to  $V_{th}$ . The remaining parts (b and c) can be solved by straightforward use of the current-voltage equations.
- 5.9** For Part (a) and (b), the solution is very similar to Problem 5.7. For (c) and (d), note that the *slope* of the transition region of the voltage transfer curve (VTC) becomes smaller (i.e., less steep) for larger values of the channel length modulation factor  $\lambda$ . Consequently, CMOS inverters built with long-channel transistors can be expected to have steeper transfer characteristics, and hence, a higher gain in the transition region.
- 5.10** The solution can be obtained simply by solving the corresponding current-voltage equations for each stage.

## CHAPTER 7

### COMBINATIONAL MOS LOGIC CIRCUITS

- 7.1** A CMOS circuit was laid out based on a company X's 3  $\mu\text{m}$  design rules as shown in Fig. P7.1 with  $W_n=7\mu\text{m}$  and  $W_p=15\mu\text{m}$ .

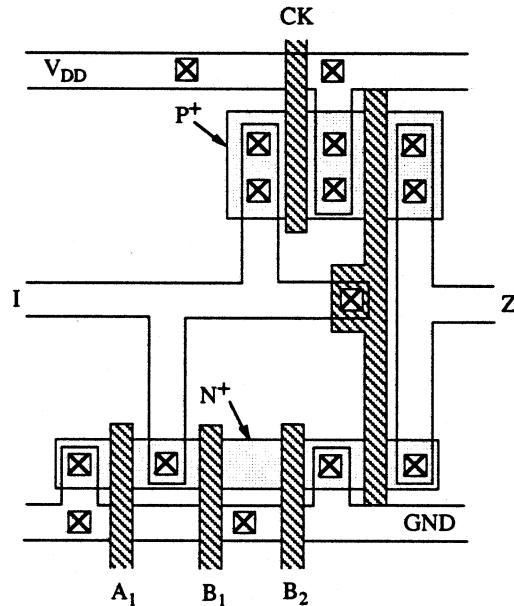


Fig. P7.1

- (a) From Fig. P7.1, determine the circuit configuration and draw the circuit diagram.
- (b) For simple hand analysis, make the following assumptions:
  - i) Wiring parasitic capacitances and resistances are negligible.
  - ii) Device parameters are

	<i>n</i> MOST	<i>p</i> MOST
$V_{T0}$	1.0 V	-1.0 V
$t_{ox}$	500 Å	500 Å
$k'$	$20\mu\text{A} / \text{V}^2$	$10\mu\text{A} / \text{V}^2$
$X_j$	$0.5\mu\text{m}$	$0.5\mu\text{m}$
$L_D$	$0.5\mu\text{m}$	$0.5\mu\text{m}$

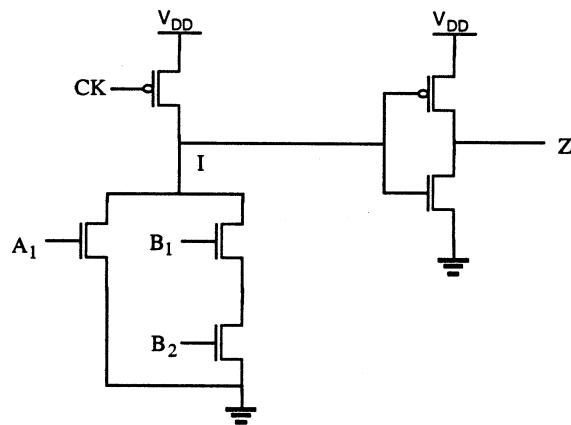
- iii) The total capacitance at node *I* is 0.6 pF.
- iv) An ideal step-pulse signal is applied to CK terminal such that

$$\begin{aligned}
 V_{CK} &= 5V, \quad t < 0 \\
 V_{CK} &= 0V, \quad 0 \leq t < T_w \\
 V_{CK} &= 5V, \quad t \geq T_w \\
 V_{DD} &= 5V
 \end{aligned}$$

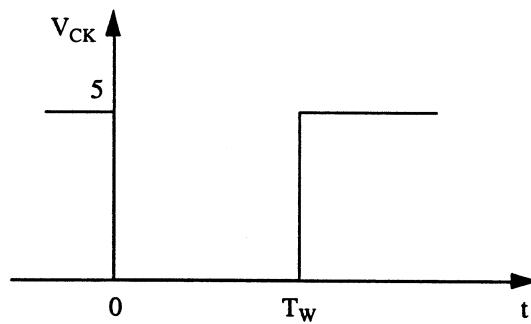
- v) At  $t = 0$ , the node voltage at  $I$  is zero.
- vi) The input voltages at  $A_1$ ,  $B_1$  and  $B_2$  are zero for  $0 \leq t \leq T_w$ . Find the minimum  $T_w$  that allows  $V_I$  to reach 2.5 V.

**SOLUTION:**

(a). The circuit diagram is drawn below:



(b). When the clock signal changes from high to low and  $A_1$ ,  $B_1$ , and  $B_2$  are low, node  $I$  is charged from 0 to 2.5V through the pMOS transistor.



The transistor first operates in saturation region and then in linear region. Thus,

$$T_w = t_{sat} + t_{lin}$$

When  $0 < V_I < 1V$ , the transistor is saturated.

$$I = -C \frac{dV_I}{dt}$$

$$I = \frac{1}{2} k'_p \cdot \frac{W}{L_{eff}} (V_{GS} - V_T)^2 = \frac{1}{2} \times 10 \times 10^{-6} \frac{15}{2} \times 16 = 0.6 \text{ mA}$$

$$\int_0^{t_{sat}} I dt = - \int_5^4 C dV_I$$

$$t_{sat} = \frac{0.6 \times 10^{-12}}{0.6 \times 10^{-3}} = 1.0 \text{ ns}$$

When  $1V < V_I < 2.5V$ , the transistor is in linear region.

$$I = \frac{1}{2} k'_p \frac{W}{L_{eff}} [2(-5+1)(V_I - 5) - (V_I - 5)^2] \\ = 37.5 \times 10^{-6} [-V_I^2 + 2V_I + 15]$$

$$\frac{37.5 \times 10^{-6}}{0.6 \times 10^{-12}} \int_0^{t_{lin}} dt = \int_4^{2.5} \frac{dV_I}{V_I^2 - 2V_I - 15} = \frac{1}{8} \int_4^{2.5} \left( \frac{1}{V_I - 5} - \frac{1}{V_I + 3} \right) dV_I$$

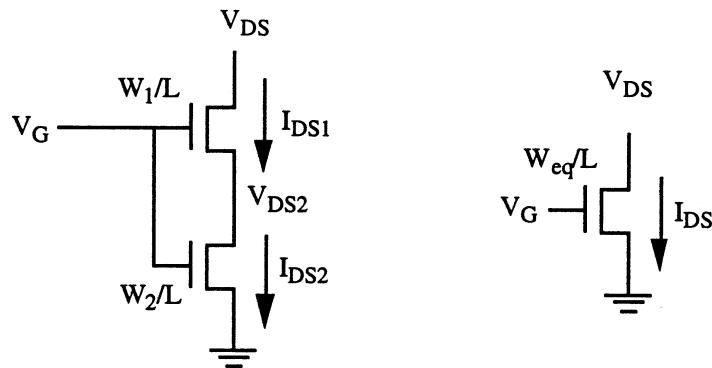
$$t_{lin} = \frac{0.6 \times 10^{-6}}{37.5} \frac{1}{8} \left[ \ln \frac{2.5 - 5}{4 - 5} - \ln \frac{2.5 + 3}{4 + 3} \right] = 2.31 \text{ ns}$$

The minimum  $T_W$  needed is thus

$$T_W = t_{sat} + t_{lin} = 1.0 + 2.31 = 3.31 \text{ ns}$$

- 7.2** Calculate the equivalent  $W/L$  of the two nMOSFs with  $W_1/L$  and  $W_2/L$  connected in series. For simplicity ,neglect the body effect, i.e., the threshold voltages of individual transistors are constant and do not depend on the source voltages. Although this is not true in reality, such an assumption is needed for simple analysis with a reasonably good approximation.

**SOLUTION:**



We know that  $I_{DS} = I_{DS1} = I_{DS2}$ , assuming all transistors are operating in linear region, neglecting body effect,

$$I_{DS} = I_{DS1} = k' \frac{W_1}{L} \left[ (V_{GS} - V_{DS2} - V_{T0})(V_{DS} - V_{DS2}) - \frac{1}{2}(V_{DS} - V_{DS2})^2 \right]$$

$$I_{DS} = I_{DS2} = k' \frac{W_2}{L} \left[ (V_{GS} - V_{T0})V_{DS2} - \frac{1}{2}V_{DS2}^2 \right]$$

Rewriting the first equation, we obtain

$$\begin{aligned} I_{DS} &= k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0} - V_{DS2})V_{DS} - (V_{GS} - V_{T0} - V_{DS2})V_{DS2} - \frac{1}{2}V_{DS}^2 + V_{DS}V_{DS2} - \frac{1}{2}V_{DS2}^2 \right] \\ &= k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2 \right] - k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0})V_{DS2} - \frac{1}{2}V_{DS2}^2 \right] \\ &= k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2 \right] - \frac{W_1}{W_2} I_{DS2} = k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2 \right] - \frac{W_1}{W_2} I_{DS} \end{aligned}$$

rearranging the above equation,

$$\left(1 + \frac{W_1}{W_2}\right) I_{DS} = k' \frac{W_1}{L} \left[ (V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

$$I_{DS} = k' \left( \frac{W_1 \cdot W_2}{W_1 + W} \right) \frac{1}{L} \left[ (V_{GS} - V_{T0})V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

Therefore, we find

$$W_{eq} = \frac{W_1 \cdot W_2}{W_1 + W} \quad \text{or} \quad \frac{1}{W_{eq}} = \frac{1}{W_1} + \frac{1}{W_2}$$

**7.3** Analytical expressions for  $V_{th}$ (logic) have been derived in Chapter 7 for the CMOS NOR2 gate. Now consider CMOS NAND2 gate for the following cases assuming  $k_p = k_n = 100 \mu\text{A/V}^2$ :

- two inputs switching simultaneously
  - top nMOS switching while the bottom NMOS's gate is tied to  $V_{DD}$
  - top nMOS gate is tied to  $V_{DD}$  and the gate input of the bottom nMOS is changing
- Derive an analytical expression for  $V_{th}$  corresponding to the first case. Also find the  $V_{th}$  value for the first case for  $V_{DD}=5$  V when the magnitudes of threshold voltages are same at 1V with  $\gamma=0$ .
  - Determine  $V_{th}$  for all three cases by using SPICE.
  - For  $C_{load}=0.2$  pF calculate 50% delays (low-to-high and high-to-low propagation delays) for ideal pulse input signal for each of the three cases by assuming that  $C_{load}$  includes all the internal parasitic capacitances. Verify the results using SPICE.

### SOLUTION:

- Considering Figure 7.15. When both transistors are switching simultaneously, transistor M1 is in saturation and M2 is in linear region. Let  $V_{D2}$  be the internal node voltage.

$$I_D = I_{M1} = \frac{1}{2} k_n (V_{th} - V_{TO,n} - V_{D2})^2$$

$$I_D = I_{M2} = \frac{1}{2} k_n (2(V_{th} - V_{TO,n})V_{D2} - V_{D2}^2)$$

From the first equation, we have

$$V_{D2} = V_{th} - V_{TO,n} - \sqrt{\frac{2I_D}{k_n}}$$

Plug into the second equation, the following can be found:

$$V_{th} - V_{TO,n} = 2\sqrt{\frac{I_D}{k_n}}$$

Both pMOS transistors are in saturation.

$$V_{GS3} = V_{GS4} = V_{th} - V_{DD}$$

$$I_D = I_{M3} + I_{M4} = k_p (V_{DD} - V_{th} - |V_{TO,p}|)^2$$

$$(V_{th} - V_{TO,n})^2 = 4 \frac{I_D}{k_n} = 4 \frac{k_p}{k_n} (V_{DD} - V_{th} - |V_{TO,p}|)^2$$

$$V_{th} = \frac{V_{TO,n} + 2\sqrt{\frac{k_p}{k_n} (V_{DD} - |V_{TO,p}|)}}{1 + 2\sqrt{\frac{k_p}{k_n}}}$$

$$V_{th} = \frac{1+2(5-1)}{1+2} = 3 \text{ V}$$

(b). SPICE simulation results.

Case1: SPICE input list for two transistors switching simultaneously.

```
CMOS NAND2 circuit DC analysis
m1 2 1 0 0 mn w=2u l=1u
m2 4 1 2 0 mn w=2u l=1u
m3 4 1 5 5 mp w=5u l=1u
m4 4 1 5 5 mp w=5u l=1u
vdd 5 0 dc 5.0
vin 1 0 dc 0
.model mn nmos (vto=1.0 kp=50u gamma=0.)
.model mp pmos (vto=-1.0 kp=20u gamma=0.)
.dc vin 0 5 0.05
.print dc v(4)
.end
```

Simulation result:  $V_{th} = 3.0 \text{ V}$

Case2: SPICE input list for top transistor switching.

```
CMOS NAND2 circuit DC analysis
m1 2 1 0 0 mn w=2u l=1u
m2 4 3 2 0 mn w=2u l=1u
m3 4 3 5 5 mp w=5u l=1u
m4 4 1 5 5 mp w=5u l=1u
vdd 5 0 dc 5.0
*case2 top transistor switching
vin 1 0 dc 5.0
vin1 3 0 dc 0
.model mn nmos (vto=1.0 kp=50u gamma=0.)
.model mp pmos (vto=-1.0 kp=20u gamma=0.)
.dc vin1 0 5 0.05
.print dc v(4)
.end
```

Simulation result:  $V_{th,top} = 2.62 \text{ V}$

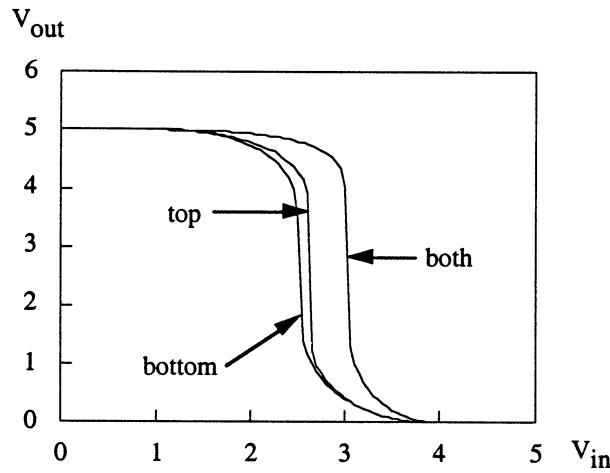
Case3: bottom transistor switching.

SPICE input list:

```
CMOS NAND2 circuit DC analysis
m1 2 1 0 0 mn w=2u l=1u
m2 4 3 2 0 mn w=2u l=1u
m3 4 3 5 5 mp w=5u l=1u
m4 4 1 5 5 mp w=5u l=1u
vdd 5 0 dc 5.0
*case3 bottom transistor switching
vin 1 0 dc 0
vin1 3 0 dc 5.0
.model mn nmos (vto=1.0 kp=50u gamma=0.)
.model mp pmos (vto=-1.0 kp=20u gamma=0.)
.dc vin 0 5 0.05
.print dc v(4)
.end
```

Simulation result:  $V_{th,bottom} = 2.53 \text{ V}$

The figure below shows the three simulation plotted on one graph.



(c). Calculate output from high to low.

Case1: both transistor switching simultaneously.

In this case, an equivalent nMOS transistor can be used with half the size. Thus,

$$I_D(V_{in} = 5, V_{out} = 5) = \frac{1}{2} \times \frac{100}{2} \times 10^{-6} (5 - 1)^2 = 0.4 \text{ mA}$$

$$I_D(V_{in} = 5, V_{out} = 2.5) = \frac{1}{2} \times \frac{100}{2} \times 10^{-6} (2(5 - 1)2.5 - 2.5^2) = 0.344 \text{ mA}$$

$$I_{avg, HL} = \frac{1}{2}(0.4 + 0.344) = 0.372 \text{ mA}$$

$$t_{PHL} = \frac{C_{load} \Delta V}{I_{avg, HL}} = \frac{0.2 \times 10^{-12} \times 2.5}{0.372 \times 10^{-3}} = 1.34 \text{ ns}$$

SPICE simulation gives 1.34ns.

Case2: top transistor switching, bottom transistor is tied to  $V_{DD}$ .

At  $V_{in} = 5\text{V}$ ,  $V_{out} = 5\text{V}$ , M1 in saturation M2 in linear,

$$I_D = I_{M1} = \frac{1}{2} k_n (V_G - V_{D2} - V_{T,n})^2$$

$$I_D = I_{M2} = \frac{1}{2} k_n [2(V_G - V_{T,n})V_{D2} - V_{D2}^2]$$

Solve for  $V_{D2}$ ,

$$V_{D2} = 1.17 \text{ V}$$

$$I_D(V_{in} = 5, V_{out} = 5) = \frac{1}{2} \times 100 \times 10^{-6} (5 - 1.17 - 1)^2 = 0.4 \text{ mA}$$

At  $V_{in} = 5\text{V}$ ,  $V_{out} = 2.5\text{V}$ , both transistors are in linear region, solve for  $V_{D2}$ ,

$$[2(V_G - V_{T,n})V_{D2} - V_{D2}^2] = [2(V_G - V_{D2} - V_{T,n})(2.5 - V_{D2}) - (2.5 - V_{D2})^2]$$

$$V_{D2} = 0.98 \text{ V}$$

$$I_D(V_{in} = 5, V_{out} = 2.5) = \frac{1}{2} \times 100 \times 10^{-6} (2(5-1)0.98 - 0.98^2) = 0.344 \text{ mA}$$

$$I_{avg,HL} = \frac{1}{2}(0.4 + 0.344) = 0.372 \text{ mA}$$

$$t_{PHL} = \frac{C_{load} \Delta V}{I_{avg,HL}} = \frac{0.2 \times 10^{-12} \times 2.5}{0.372 \times 10^{-3}} = 1.34 \text{ ns}$$

SPICE simulation gives high to low delay of 1.28 ns.

**Case3:** top transistor is tied to  $V_{DD}$ , bottom transistor is switching.

In this case, transistor M1 is in saturation at the edge of turn-on and the internal node voltage is 4V. Thus,

$$I_D(V_{in} = 5, V_{out} = 5) = \frac{1}{2} \times 100 \times (2(5-1)4 - 4^2) = 0.8 \text{ mA}$$

$$I_D(V_{in} = 5, V_{out} = 2.5) = 0.344 \text{ mA}$$

$$I_{avg,HL} = \frac{1}{2}(0.8 + 0.344) = 0.572 \text{ mA}$$

$$t_{PHL} = \frac{C_{load} \Delta V}{I_{avg,HL}} = \frac{0.2 \times 10^{-12} \times 2.5}{0.572 \times 10^{-3}} = 0.87 \text{ ns}$$

SPICE simulation gives 1.2ns.

For output low to high transition, in case 1 both pMOS transistors are on, in case 2 and 3, only one of the pMOS transistors is on, in either of the two cases, the delay is half that of case 1.

**Case1:**

$$I_D(V_{in} = 0, V_{out} = 0) = \frac{1}{2}(2k_p)(-5+1)^2 = 1.6 \text{ mA}$$

$$I_D(V_{in} = 0, V_{out} = 2.5) = \frac{1}{2}(2k_p)[2(-5+1)(-2.5) - 2.5^2] = 1.375 \text{ mA}$$

$$t_{PLH} = 0.34 \text{ ns}$$

SPICE simulation gives 0.4ns.

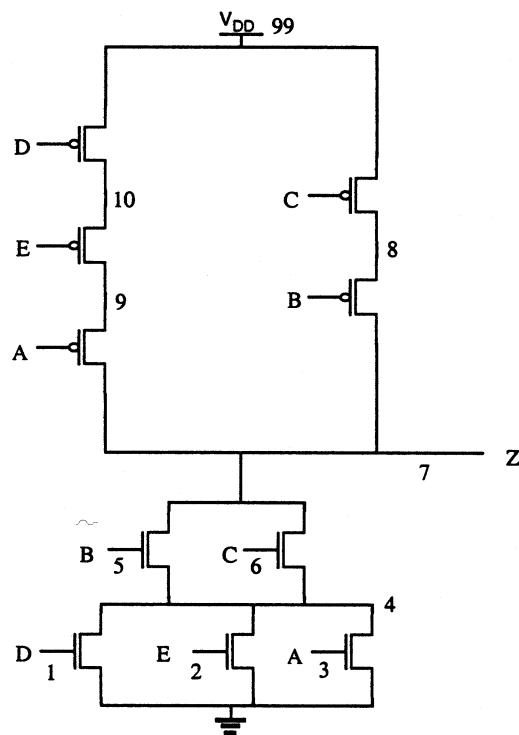
**Case 2 and Case 3**

$$t_{PLH} = 0.67 \text{ ns}$$

- 7.4 Write down the SPICE input description for transistor connections, source and drain parasitics in terms of areas, and perimeters for the layout shown in Example 7.2. Neglect the wiring capacitances in the polysilicon and metal runners. Default model names to be used for pMOS and nMOS are MODP and MODN. Assume  $L = 1 \mu\text{m}$  and  $Y = 10 \mu\text{m}$  for all transistors.

**SOLUTION:**

The circuit diagram is redrawn here with the node numbers.



The SPICE input description is:

```

Vdd 99 0 dc 5
nn1 4 1 0 0 rmod w=10u l=1u AS=100p AD=50p PS=40u PD=20u
nn2 4 2 0 0 rmod w=10u l=1u AS=50p AD=50p PS=20u PD=20u
nn3 4 3 0 0 rmod w=10u l=1u AS=50p AD=50p PS=20u PD=20u
nn4 7 5 4 0 rmod w=10u l=1u AS=50p AD=50p PS=20u PD=20u
nn5 7 6 4 0 rmod w=10u l=1u AS=100p AD=50p PS=40u PD=20u
np1 10 1 99 99 pmod w=15u l=1u AS=150p AD=75p PS=50u PD=25u
np2 9 2 10 99 pmod w=15u l=1u AS=75p AD=75p PS=25u PD=25u
np3 7 3 9 99 pmod w=15u l=1u AS=75p AD=75p PS=25u PD=25u
np4 7 5 8 99 pmod w=15u l=1u AS=75p AD=75p PS=25u PD=25u
np5 8 6 99 99 pmod w=15u l=1u AS=150p AD=75p PS=50u PD=25u

```

```
.model nmod MODN
.model pmod MODP
```

- 7.5 For the gate shown in Fig. P7.5,

- Pull-up transistor ratio is 5/5
  - pull-down transistor ratios are 100/5
  - $V_{TO} = 1.0 \text{ V}$
  - $\gamma = 0.4 \text{ V}^{1/2}$
  - $|2\phi_F| = 0.6 \text{ V}$
- (a) Identify the worst case input combination(s) for  $V_{OL}$ .
- (b) Calculate the worst case value of  $V_{OL}$ . (Assume that all pull-down transistors have the same body bias and initially, that  $V_{OL} \approx 5\% V_{DD}$ .)

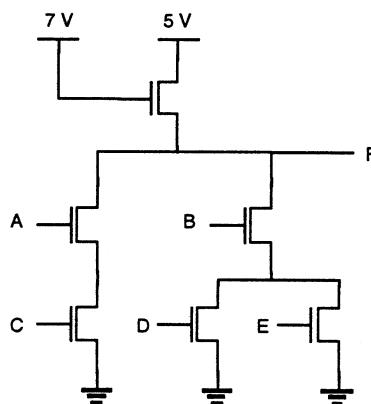


Figure P7.5

### SOLUTION:

- (a) The worst case input combinations are those that cause only one current path from output to ground. The combinations are listed in the following table.

$A = 1$	$C = 1$	$B = 0$
$A = 1$	$C = 1$	$C = 0 \quad E = 0$
$B = 1$	$D = 1$	$A = 0 \quad E = 0$
$B = 1$	$D = 1$	$C = 0 \quad E = 0$
$B = 1$	$E = 1$	$A = 0 \quad D = 0$
$B = 1$	$E = 1$	$C = 0 \quad D = 0$

- (b) The worst case equivalent circuit can be represented by a simple inverter, with the driver  $W/L=10$ , load  $W/L=1$ . Both transistors are operating in linear region in this case because:  
Driver:  $V_{GS} = 5, V_{DS} = 0.25$

Load:  $V_{GS} = 7 - 0.25 = 6.75$ ,  $V_{DS} = 5 - 0.25 = 4.75$

$$V_{T,load} \approx 1 + 0.4(\sqrt{0.25+0.6} - \sqrt{0.6}) = 1.06$$

$$V_{T,driver} = 1$$

$$\frac{k_{load}}{2} (2(7 - V_{OL} - 1.06)(5 - V_{OL}) - (5 - V_{OL})^2) = \frac{k_{load}}{2} 10(2(5 - 1)V_{OL} - V_{OL}^2)$$

Solve for  $V_{OL}$ , since  $V_{OL}$  is small, no iteration of  $V_{T,I}$  is needed in this case.

$$V_{OL} = 0.39V$$

- 7.6** A store has one express register and three regular ones. It is the store policy that the express register is open only when two or more of the other registers are busy. Assume that the boolean variables A, B, and C reflect the status of each of the regular registers (1 busy, 0 idle). Design the logic circuit, with A, B, and C as inputs and F as output, to automatically notify the manager (by setting F=1) to open the express register. Present two solutions, the first using only NAND gates, the second using only NOR gates.

### SOLUTION:

For NAND gate implementation,

$$F = AB + AC + BC = (\overline{AB}) \cdot (\overline{AC}) \cdot (\overline{BC})$$

For NOR gate implementation,

$$F = (A + B)(A + C)(B + C) = (\overline{A + B}) + (\overline{A + C}) + (\overline{B + C})$$

- 7.7** Calculate  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$ ,  $NM_L$  and  $NM_H$  for a two-input NOR gate fabricated in a CMOS technology.

- $(W/L)_p = 4$
- $(W/L)_n = 1$
- $V_{Tn} = 0.7V$
- $V_{Tp} = -0.7V$
- $k_n' = 40 \mu A/V^2$
- $k_p' = 20 \mu A/V^2$
- $V_{DD} = 5V$

Compare your answers with SPICE.

### SOLUTION:

First find the equivalent inverter for the NOR gate.

$$(W/L)_{eq,n} = 2(W/L)_n$$

$$(W/L)_{eq,p} = \frac{1}{2}(W/L)_p$$

therefore

$$k_{p,eq} = k_p \left( \frac{W}{L} \right)_{eq,p} = 40 \mu\text{A/V}^2$$

$$k_{n,eq} = k_n \left( \frac{W}{L} \right)_{eq,n} = 80 \mu\text{A/V}^2$$

$$\begin{aligned} V_{OH} &= V_{DD} = 5 \text{ V} \\ V_{OL} &= 0 \text{ V} \end{aligned}$$

Calculate  $V_{IL}$

$$V_{out} = \frac{1}{2} \left( \left( \frac{k_n}{k_p} + 1 \right) V_{IL} - \frac{k_n}{k_p} V_{TO,n} - V_{TO,p} + V_{DD} \right)$$

$$V_{out} = 1.5V_{IL} + 2.15$$

$$\frac{k_n}{2} (V_{IL} - V_{TO,n})^2 = k_p \left( V_{IL} - V_{DD} - V_{TO,p} - \frac{V_{out} - V_{DD}}{2} \right) (V_{out} - V_{DD})$$

$$V_{IL} = 1.65 \text{ V}$$

Calculating  $V_{IH}$

$$V_{out} = \frac{\left( 1 + \frac{k_p}{k_n} \right) V_{IH} - V_{TO,n} - \frac{k_p}{k_n} (V_{DD} + V_{TO,p})}{2}$$

$$V_{out} = 0.75V_{IH} - 1.425$$

$$k_n \left( V_{IH} - V_{TO,n} - \frac{V_{out}}{2} \right) V_{out} = \frac{k_p}{2} (V_{IH} - V_{DD} - V_{TO,p})^2$$

$$V_{IH} = 2.76 \text{ V}$$

$$NM_L = 1.65 - 0 = 1.65 \text{ V}$$

$$NM_H = 5 - 2.76 = 2.24 \text{ V}$$

SPICE input list:

```
CMOS NOR2 circuit DC analysis

m1 3 1 0 0 mn w=1u l=1u
m2 3 1 0 0 mn w=1u l=1u
m3 3 1 4 5 mp w=4u l=1u
m4 4 1 5 5 mp w=4u l=1u
vdd 5 0 dc 5.0
vin 1 0 dc 0
.model mn rmos (vto=0.7 kp=40u gamma=0.)
.model mp pmos (vto=-0.7 kp=20u gamma=0.)
.dc vin 0 5 0.05
.print dc v(3)
.end
```

SPICE results:

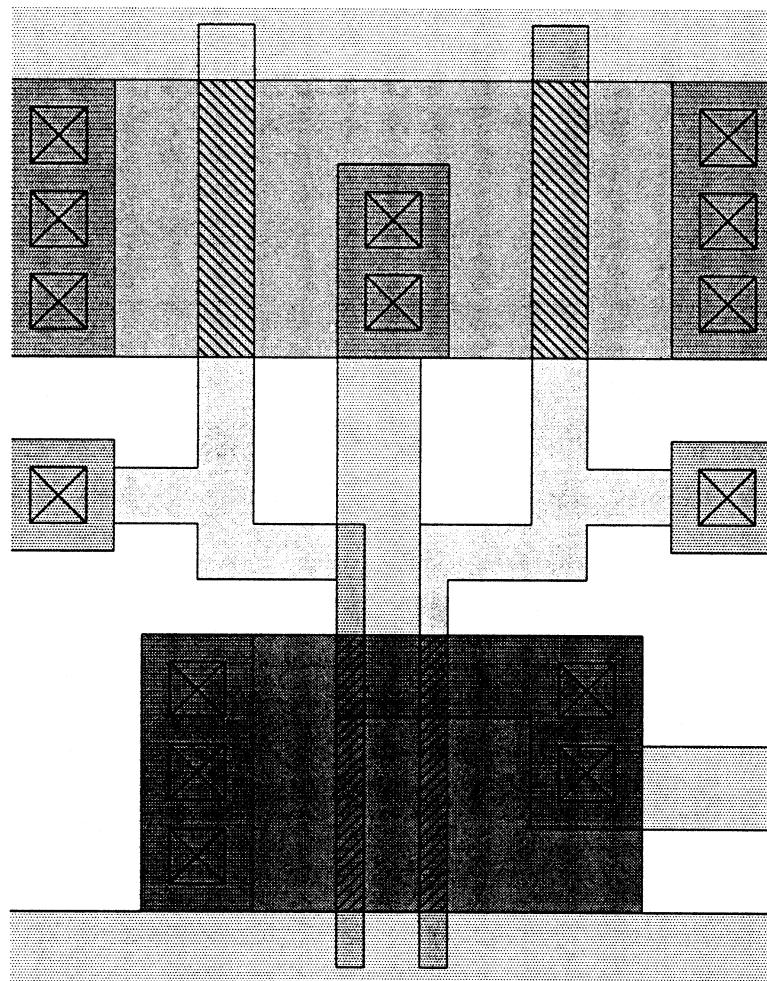
$$V_{IL} = 1.70 \text{ V}$$

$$V_{IH} = 2.70 \text{ V}$$

- 7.8 Use a layout editor (e.g., Magic) to lay out a two-input CMOS NAND gate. All devices have  $W = 10 \mu\text{m}$ . N-channel transistors have  $L_{eff} = 1 \mu\text{m}$  and p-channel transistors have  $L_{eff} = 2 \mu\text{m}$ . You can calculate the drawn channel lengths by assuming that  $L_d = 0.25 \mu\text{m}$ . After you lay out the gate use the design rule checker. Finally, you should have the layout editor perform parasitic capacitance extraction.

### SOLUTION:

The NAND gate layout is shown below:



- 7.9 Assume that the 2-input NAND gate in Problem 7.8 is driving a 0.01pF load. Use hand calculations to estimate  $t_{PLH}$  and  $t_{PHL}$ . Do not forget to add in the parasitic capacitances extracted from your layout! Check your answer with SPICE. Use:

- $k_n' = 20 \mu\text{A}/\text{V}^2$
- $k_p' = 10 \mu\text{A}/\text{V}^2$
- $V_{Tn} = |V_{Tp}| = 1.0 \text{ V}$

### SOLUTION:

The delay can be calculated using an equivalent inverter of the NAND gate. From equations (6.22b) and (6.23b), we obtain:

$$\begin{aligned}\tau_{PHL} &= \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left( \frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right] \\ &= \frac{0.01 \times 10^{-12}}{20 \times 10^{-6} \cdot 5/1 \cdot (5-1)} \left[ \frac{2}{4} + \ln \left( \frac{4 \times 4}{5} - 1 \right) \right] = 32.2 \text{ ps}\end{aligned}$$

$$\begin{aligned}\tau_{PLH} &= \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right] \\ &= \frac{0.01 \times 10^{-12}}{10 \mu\text{A} \cdot 10/1 \cdot (5-1)} \left[ \frac{2}{4} + \ln \left( \frac{4 \times 4}{5} - 1 \right) \right] = 32.2 \text{ ps}\end{aligned}$$

SPICE simulation results:

The extracted SPICE netlist is used for simulation, it's listed here.

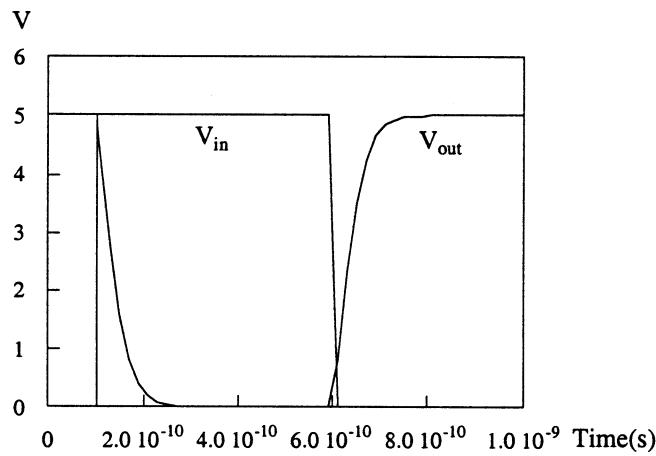
```
** SPICE file created for circuit 7.8
** Technology: scmos
**
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
Vdd! 1 0 5
VA 102 0 DC PULSE(0V 5V 0.1NS 0NS 0NS 0.5NS 1NS)
VB 104 0 DC PULSE(0V 5V 0.1NS 0NS 0NS 0.5NS 1NS)
RLJUMP0 100 101 50.0
RLJUMP1 102 103 311.0
M0 101 103 1 1 pfet L=2.0U W=10.0U
RLJUMP2 104 105 311.0
RLJUMP3 100 106 50.0
M1 1 105 106 1 pfet L=2.0U W=10.0U
RLJUMP4 107 108 68.0
RLJUMP5 102 109 311.0
M2 108 109 0 0 nfet L=1.0U W=10.0U
RLJUMP6 100 110 50.0
RLJUMP7 104 111 311.0
RLJUMP8 107 112 68.0
```

```

M3 110 111 112 0 nfet L=1.0U W=10.0U
.MODEL pfet PMOS(VTO=-1 KP=10E-6)
.MODEL nfet NMOS(VTO=1 KP=20E-6)
** NODE: 107 = 8_86_2#
** NODE: 0 = GND!
* This is the extracted capacitance
*C0 100 0 60FF
C0 100 0 0.01PF
** NODE: 100 = out
** NODE: 1 = Vdd!
** NODE: 104 = b
** NODE: 102 = a
.TRAN .001NS 1NS
.PRINT TRAN V(102) V(100)
.END

```

The simulation result is shown in the plot.



The delays are found out from the output which is very close to hand calculation.

$$\tau_{PLH} = 6.4 \times 10^{-10} - 6.05 \times 10^{-10} = 35 \text{ ps}$$

$$\tau_{PHL} = 1.4 \times 10^{-10} - 1.05 \times 10^{-10} = 35 \text{ ps}$$

- 7.10 Consider the circuit drawn in Fig. P7.10.
- Determine the logic function F.
  - Calculate  $W_L/L_L$  such that  $V_{OL}$  does not exceed 0.4 V.
  - Qualitatively, would  $W_L/L_L$  increase or decrease if the same conditions of (b) are to be achieved but  $\gamma = 0.4 \text{ V}^{1/2}$ ?
- $V_{T,load} = -3\text{V}$
  - $V_{T,driver} = 1\text{V}$

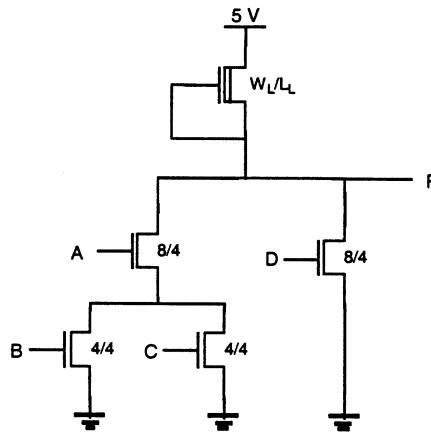


Figure P7.10

**SOLUTION:**

$$(a) F = \overline{A(B+C)+D}$$

(b)  $V_{OL}$  maximum occurs when  $A=1, D=0$  and either (but not both)  $B=1$  or  $C=1$ . Under these conditions, the circuit may be simplified as a depletion load inverter with the equivalent driver  $W/L$  given below.

$$\left. \frac{L}{W} \right|_{equiv} = \frac{4}{8} + \frac{4}{4} = \frac{3}{2}$$

$$\therefore \left. \frac{W}{L} \right|_{equiv} = \frac{2}{3}$$

When  $V_{OL}=0.4, V_{IN}=5$ , the load is saturated and the driver is in linear region.

$$\frac{k'}{2} \left( \frac{W}{L} \right)_{load} \left( V_{GS,load} - V_{T,load} \right)^2 = k' \frac{2}{3} \left[ (V_{IN} - V_{T,driver})V_{out} - \frac{1}{2} V_{out}^2 \right]$$

$$\frac{k'}{2} \left( \frac{W}{L} \right)_{load} (0+3)^2 = k' \frac{2}{3} \left[ (5-1) \times 0.4 - \frac{1}{2} \times 0.4^2 \right]$$

$$\left( \frac{W}{L} \right)_{load} = 0.225$$

$$\therefore \left( \frac{W}{L} \right)_{load} \leq 0.225 \quad \text{for} \quad V_{OL} \leq 0.4$$

(c) The load device suffers more from body effect than does the inverting transistor. Thus the absolute value of  $V_{T,load}$  decreases. An examination of the above equation shows that the equality will be satisfied for a larger  $W/L$  ratio.

7.11 Consider the circuit drawn in Fig. P7.11.

- Determine the logic function F.
- Design a circuit to implement the same logic function, but using NOR gates. Draw a transistor-level schematic and use NMOS E-D technology.
- Design a circuit to implement the same logic function, but using an AOI (AND-OR-INVERT) gate. Draw a transistor level schematic and use CMOS technology.

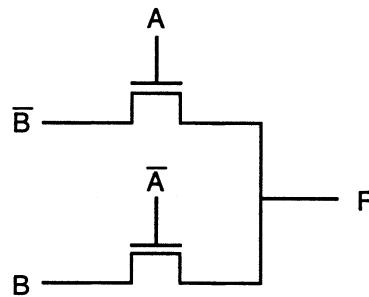


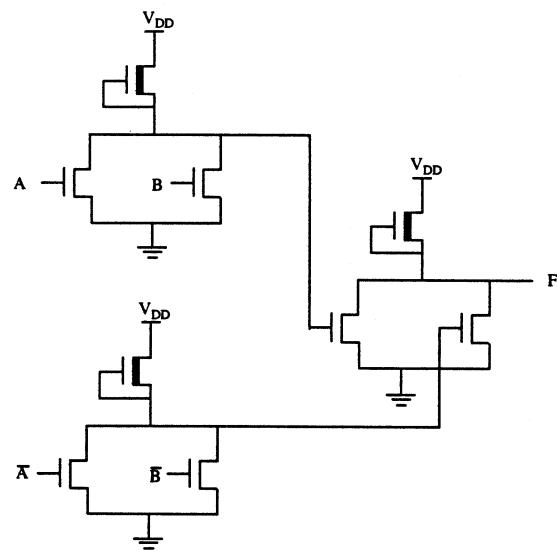
Figure P7.11

**SOLUTION:**

(a)  $F = A\bar{B} + \bar{A}B = A \oplus B$

(b) Using NOR gates,

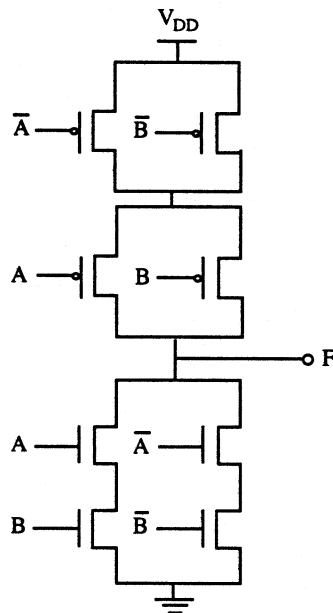
$$F = A\bar{B} + \bar{A}B = (A + B)(\bar{A} + \bar{B}) = \overline{(A + B)} + \overline{(\bar{A} + \bar{B})}$$



(c) Using AOI gates,

$$\bar{F} = AB + \bar{A}\bar{B}$$

$$F = \bar{\bar{F}} = \overline{AB + \bar{A}\bar{B}}$$



**7.12** The enhancement-type MOS transistor has the following parameters:

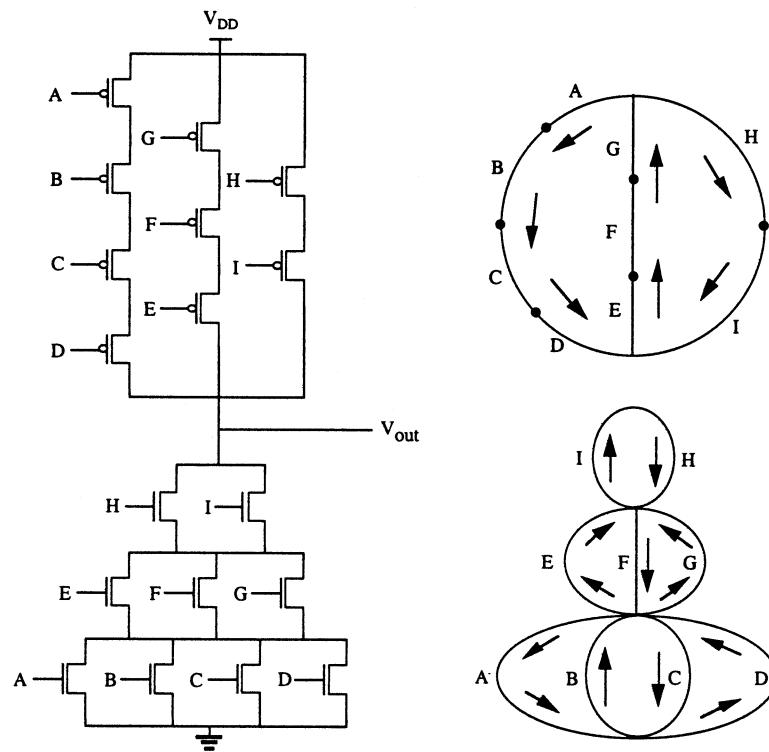
- $V_{DD} = 5$  V
- $|V_{T0}| = 1.0$  V for both nMOS and pMOS transistor
- $\lambda = 0.0$  V $^{-1}$
- $k'_p = 20$   $\mu\text{A}/\text{V}^2$
- $k'_n = 50$   $\mu\text{A}/\text{V}^2$

For a CMOS complex gate OAI432 with  $(W/L)_p = 30$  and  $(W/L)_n = 40$ ,

- (a) Calculate the  $W/L$  sizes of an equivalent inverter with the weakest pull-down and pull-up. Such an inverter can be used to calculate worst-case pull-up and pull-down delays, with proper incorporation of parasitic capacitances at internal nodes into the total load capacitance. In this problem, you are asked to calculate only  $(W/L)_{worse-case}$  for both p-channel and n-channel by neglecting the parasitic capacitances.
- (b) Do the layout of OAI432 with minimal diffusion breaks to reduce the number of polysilicon column pitches. With proper ordering of polysilicon gate columns, the number of diffusion breaks can be minimized. One way of achieving such a goal is to find an Euler path common to both p-channel and n-channel using graph models. Symbolic layout that shows source and drain connections is sufficient to answer this problem.

**SOLUTION:**

(a) The OAI432 circuit is drawn along with an Euler path in the following figure.



The weakest pull-up case is the A-B-C-D branch in pMOS network,

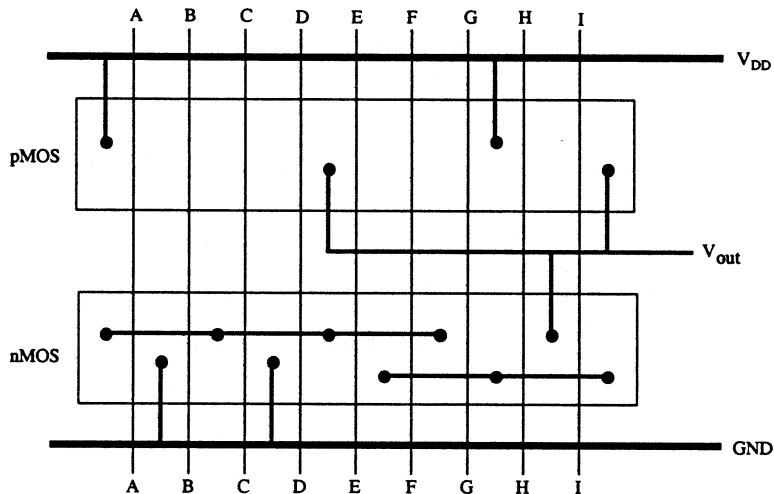
$$\left(\frac{W}{L}\right)_{eq,p} = \frac{1}{4} \left(\frac{W}{L}\right)_p = \frac{30}{4} = 7.5$$

The weakest pull-down case is one of the 24 listed below,

(H or I)--(E or F or G)--(A or B or C or D)

$$\left(\frac{W}{L}\right)_{eq,n} = \frac{1}{3} \left(\frac{W}{L}\right)_n = \frac{40}{3} = 13.3$$

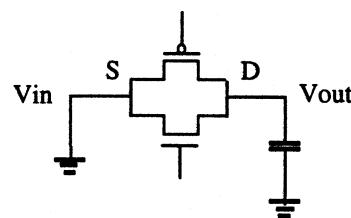
(b)



- 7.13** Consider a fully complementary CMOS transmission gate with its input terminal tied to ground (0 V) while the other non-gate terminal is tied to a 1pF load capacitor initially charged to 5 V. Use the  $V_{TO}$ ,  $k'_p$ , and  $k'_n$  values in Problem 7.12. At  $t=0$ , both transistors are fully turned on by clock signals to start the discharge of the capacitor.
- Plot the effective resistance of this transmission gate as a function of capacitor voltage when  $(W/L)_p = 50$  and  $(W/L)_n = 40$ . From the plot find the average value of the resistance. Then calculate the RC delay for the capacitor voltage to change from 5 V to 2.5 V. This can be found by solving the RC-circuit differential equation.
  - Verify your answer to part (a) by using SPICE simulation. The source/drain parasitic capacitances can be neglected.

**SOLUTION:**

(a).



At  $t=0$ , both transistors are saturated.

$$I_{D,n} = \frac{k'_n}{2} \left( \frac{W}{L} \right)_n (5 - 1)^2 = \frac{50\mu}{2} \times 40 \times 16 = 16 \text{ mA}$$

$$I_{D,p} = \frac{k'_n}{2} \left( \frac{W}{L} \right)_n (-V_{out} + 1)^2 = \frac{20\mu}{2} \times 50(V_{out} - 1)^2 = 0.5(V_{out} - 1)^2 \frac{\text{mA}}{\text{V}^2}$$

$$I_D = I_{D,n} + I_{D,p} = 16 \text{ mA} + 0.5(V_{out} - 1)^2 \frac{\text{mA}}{\text{V}^2}$$

For  $4 < V_{out} < 5$

$$R_{eff} = \frac{V_{out}}{I_D} = \frac{V_{out}}{16 \text{ mA} + 0.5(V_{out} - 1)^2 \frac{\text{mA}}{\text{V}^2}}$$

$$R_{eff}(5V) = 208 \Omega$$

$$R_{eff}(4V) = 195 \Omega$$

For  $1 < V_{out} < 4$ , nMOS transistor is linear, pMOS transistor is saturated,

$$I_{D,n} = 25\mu \times 40[2(5-1)V_{out} - V_{out}^2] = (8V_{out} - V_{out}^2) \frac{\text{mA}}{\text{V}^2}$$

$$I_D = (8V_{out} - V_{out}^2) \frac{\text{mA}}{\text{V}^2} + 0.5(V_{out} - 1)^2 \frac{\text{mA}}{\text{V}^2} = (-V_{out}^2 + 14V_{out} + 1)0.5 \frac{\text{mA}}{\text{V}^2}$$

The effective resistance is

$$R_{eff} = \left( \frac{V_{out}}{-V_{out}^2 + 14V_{out} + 1} \right) 2k\Omega$$

$$R_{eff}(1V) = 143\Omega$$

$$R_{eff}(2.5V) = 168\Omega$$

For  $0 < V_{out} < 1$

$$I_D = I_{D,n} = (8V_{out} - V_{out}^2) \frac{\text{mA}}{\text{V}^2}$$

$$R_{eff} = \frac{1k\Omega}{8 - V_{out}}$$

$$R_{eff}(0V) = 125\Omega$$

$$R_{avg} = \frac{1}{2}(R_{eff}(5V) + R_{eff}(2.5V)) = \frac{168 + 208}{2} = 188\Omega$$

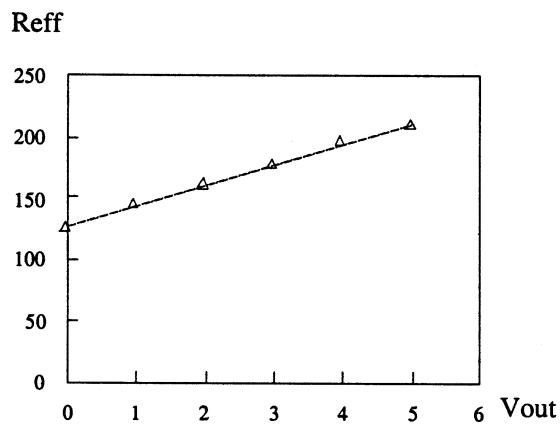
$$R_{avg} C_L = 188\Omega \times 10^{-12} F = 1.88 \text{ s}$$

The current through the capacitance is thus,

$$i_C = \frac{V_{out}}{R_{avg}} = -C_L \frac{dV_{out}}{dt}$$

Integrate  $V_{out}$  from 5V to 2.5V,

$$t = 1.3 \times 10^{-10} \text{ s}$$



(b). SPICE simulation.

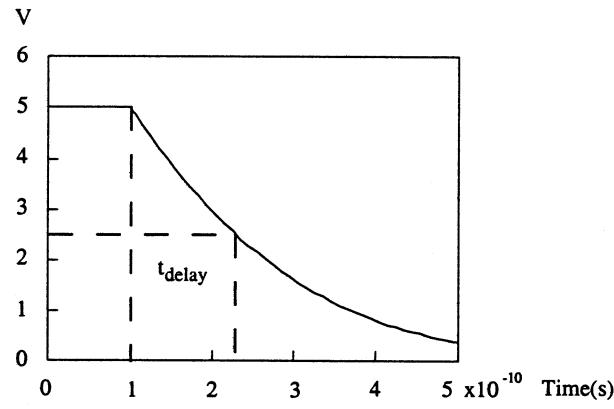
SPICE input list:

```

CMOS transmission gate
mn1 1 3 0 0 mm w=40u l=1u
mp1 0 2 1 1 mp w=50u l=1u
c1 1 0 1.0p ic=5.0
.model mn nmos (vto=1 kp=50u gamma=0)
.model mp pmos (vto=-1 kp=20u gamma=0)
vp 2 0 dc pulse (5 0 0.1n 0 0 10n 20n)
vn 3 0 dc pulse (0 5 0.1n 0 0 10n 20n)
.tran 0.01n .5n uic
.end

```

SPICE simulation result:



The delay time is:

$$t_{delay} = (2.3 - 1) \times 10^{-10} = 1.3 \times 10^{-10} \text{ s}$$

## CHAPTER 8

### SEQUENTIAL MOS LOGIC CIRCUITS

- 8.1** Figure P8.1 is a schematic for a positive edge triggered D flip-flop. Use a layout editor (e.g., Magic) to design a layout of the circuit. Use CMOS technology, and assume that you have n-type substrate. On the printout of your layout, clearly indicate the location of each logic gate in the figure below. Also, calculate the parasitic capacitances of your layout.

- $W_n = 4 \mu\text{m}$  and  $W_p = 8 \mu\text{m}$  for all gates
- $L_M = 4 \mu\text{m}$
- $L_D = 1 \mu\text{m}$
- $V_{T0,n} = 1 \text{ V}$
- $V_{T0,p} = -1 \text{ V}$
- $k'_n = 25 \mu\text{A/V}^2$
- $k'_p = 10 \mu\text{A/V}^2$
- $t_{ox} = 20 \text{ nm}$

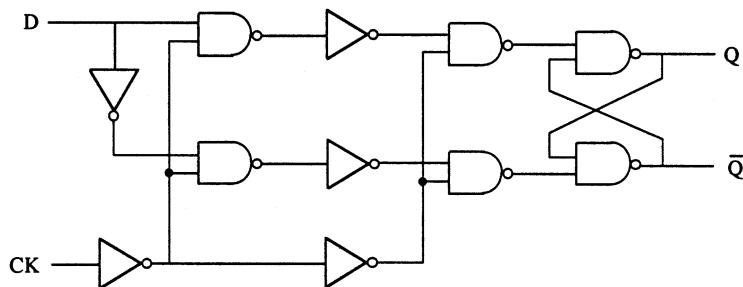
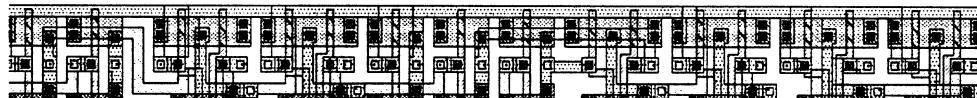


Figure P8.1

**SOLUTION:**



- 8.2** For the layout in Problem 8.1, find the minimum set-up time ( $t_{\text{setup}}$ ) and hold time ( $t_{\text{hold}}$ ) for the flip-flop using SPICE simulation. This will require you to obtain four plots.
- A plot of the output using the minimum setup time of ( $t_{\text{setup}}$ )
  - A plot of the output using a setup time of  $0.8t_{\text{setup}}$
  - A plot of the output using the minimum hold time  $t_{\text{hold}}$
  - A plot of the output using a hold time of  $0.8t_{\text{hold}}$

**SOLUTION:**

The following is the SPICE input file extracted from the layout in Problem 8.1.

```

** SPICE file created for circuit 8.2
** Technology: scmos
**
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 1 1 pfet L=4.0U W=8.0U
M1 102 103 1 1 pfet L=4.0U W=8.0U
M2 104 101 1 1 pfet L=4.0U W=8.0U
M3 1 102 104 1 pfet L=4.0U W=8.0U
M4 105 100 1 1 pfet L=4.0U W=8.0U
M5 1 102 105 1 pfet L=4.0U W=8.0U
M6 106 104 1 1 pfet L=4.0U W=8.0U
M7 107 105 1 1 pfet L=4.0U W=8.0U
M8 108 102 1 1 pfet L=4.0U W=8.0U
M9 109 108 1 1 pfet L=4.0U W=8.0U
M10 1 107 109 1 pfet L=4.0U W=8.0U
M11 110 106 1 1 pfet L=4.0U W=8.0U
M12 1 108 110 1 pfet L=4.0U W=8.0U
M13 111 109 1 1 pfet L=4.0U W=8.0U
M14 1 112 111 1 pfet L=4.0U W=8.0U
M15 112 110 1 1 pfet L=4.0U W=8.0U
M16 1 111 112 1 pfet L=4.0U W=8.0U
M17 100 101 0 0 nfet L=4.0U W=4.0U
M18 102 103 0 0 nfet L=4.0U W=4.0U
M19 113 101 0 0 nfet L=4.0U W=4.0U
M20 104 102 113 0 nfet L=4.0U W=4.0U
M21 114 100 0 0 nfet L=4.0U W=4.0U
M22 105 102 114 0 nfet L=4.0U W=4.0U
M23 106 104 0 0 nfet L=4.0U W=4.0U
M24 107 105 0 0 nfet L=4.0U W=4.0U
M25 108 102 0 0 nfet L=4.0U W=4.0U
M26 115 108 0 0 nfet L=4.0U W=4.0U
M27 109 107 115 0 nfet L=4.0U W=4.0U
M28 116 106 0 0 nfet L=4.0U W=4.0U
M29 110 108 116 0 nfet L=4.0U W=4.0U
M30 117 109 0 0 nfet L=4.0U W=4.0U
M31 111 112 117 0 nfet L=4.0U W=4.0U
M32 118 110 0 0 nfet L=4.0U W=4.0U
M33 112 111 118 0 nfet L=4.0U W=4.0U
*
VDD 1 0 dc 5
*For setup time simulation
*This pulse for minimum setup time
VD 101 0 dc pulse(0 5 6.8n 2n 2n 73.2n 84n)
*This pulse for 0.8 times minimum setup time
*VD 101 0 dc pulse(0 5 9.68n 2n 2n 70.32n 84n)
VCK 103 0 dc pulse(0 5 20n 2n 2n 60n 84n)
*For setup time simulation

```

```

*For hold time simulation
*This pulse for minimum hold time
VD 101 0 dc pulse(0 5 0n 2n 2n 13.55n 84n)
*This pulse for 0.8 times minimum hold time
*VD 101 0 dc pulse(0 5 0n 2n 2n 13.44n 84n)
VCK 103 0 dc pulse(0 5 15n 2n 2n 65n 84n)
*For hold time simulation

** NODE: 118 = 8_532_6#
** NODE: 117 = 8_470_6#
** NODE: 116 = 8_408_6#
** NODE: 115 = 8_346_6#
** NODE: 114 = 8_170_6#
** NODE: 113 = 8_108_6#
** NODE: 0 = GND!
C0 1 0 435F
** NODE: 1 = Vdd!
C1 111 0 62F ic=5
** NODE: 111 = QB
C2 110 0 65F
** NODE: 110 = 8_398_40#
C3 112 0 68F ic=0
** NODE: 112 = Q
C4 109 0 63F
** NODE: 109 = 8_336_40#
C5 106 0 1p
** NODE: 106 = 8_222_6#
C6 107 0 1p
** NODE: 107 = 8_260_6#
C7 108 0 71F
** NODE: 108 = 8_298_6#
C8 105 0 61F
** NODE: 105 = 8_160_40#
C9 104 0 62F
** NODE: 104 = 8_98_40#
C10 100 0 59F
** NODE: 100 = 8_10_6#
C11 102 0 86F
** NODE: 102 = 8_48_6#
** NODE: 103 = CK
C12 101 0 14F
** NODE: 101 = D
*
.model pfet pmos (vto=-1 kp=10e-6 ld=1u)
.MODEL nfet nmos (vto=1 kp=25e-6 ld=1u)
.tran 1n 50n uic
.print tran v(112)
.end

```

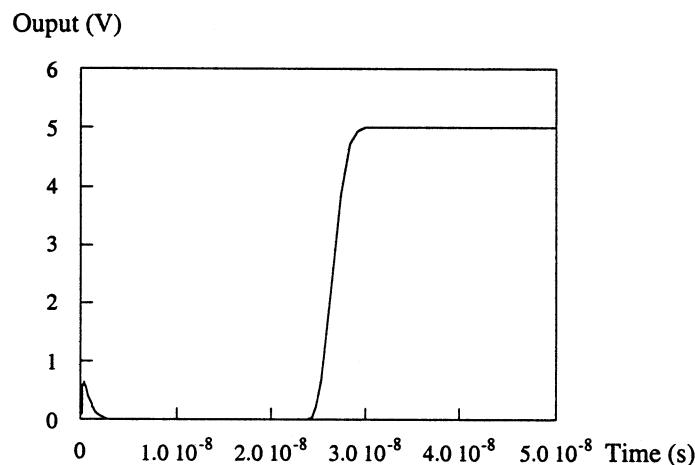
The minimum setup time is found to be:

$$t_{\text{setup}} = 14.4 \text{ ns}$$

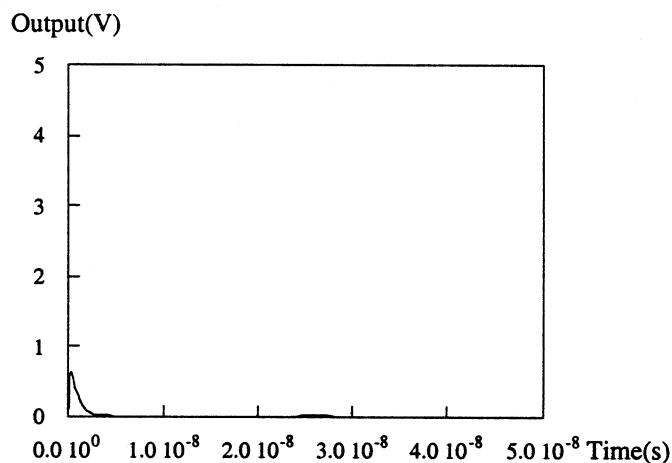
The minimum hold time is found to be:

$$t_{\text{hold}} = 0.55 \text{ ns}$$

(a). A plot of the output using the minimum setup time  $t_{\text{setup}}$ .

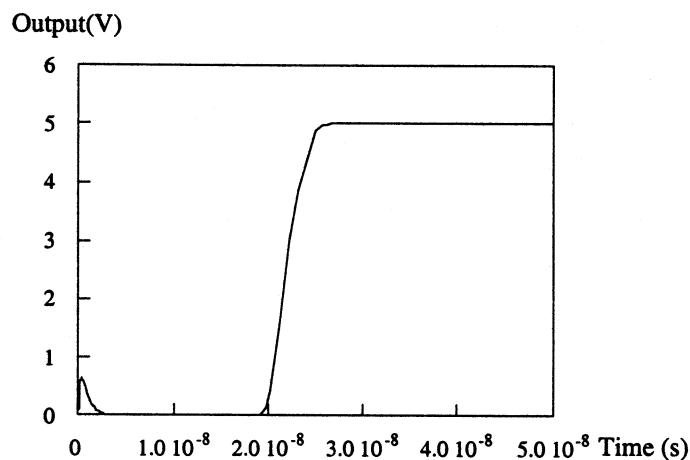


(b). A plot of the output using a setup time of  $0.8t_{\text{setup}}$ .

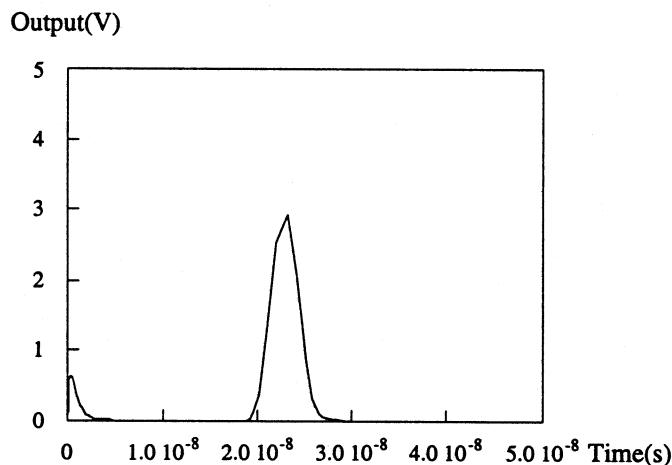


If the setup time is not satisfied, the circuit doesn't work properly.

(c). A plot of the output using the minimum hold time  $t_{\text{hold}}$ .



(d). A plot of the output using a hold time of  $0.8t_{\text{hold}}$ .



If the input was not held long enough, the output is not right.

- 8.3** We have discussed the features of CMOS Schmitt trigger. It has been pointed out a useful application lies in the receiver circuit design to filter out noises. However, in terms of speed performance it delays the switching activity. In view of speed alone, it would be useful to reverse the switching directions. In particular, we want to have the negative going (high to low transition) edge to occur at an input voltage smaller than the typical inverter's saturation voltage and also the positive going (low to high transition) edge to occur at an input voltage larger than the inverter's saturation voltage. Complete the circuit connection in Fig. P8.3 to realize such a circuit block for the assembly of the following components. Justify your answer by using SPICE circuit analysis. You can make some approximation technique to simulate the circuit. For instance, the different VTC curves can be simulated by using inverters of different  $\beta$  ratios. To be more specific, for larger

saturation voltage, you can use an inverter with strong pull-up transistor, and for smaller saturation voltage use an inverter with strong pull-down transistor.

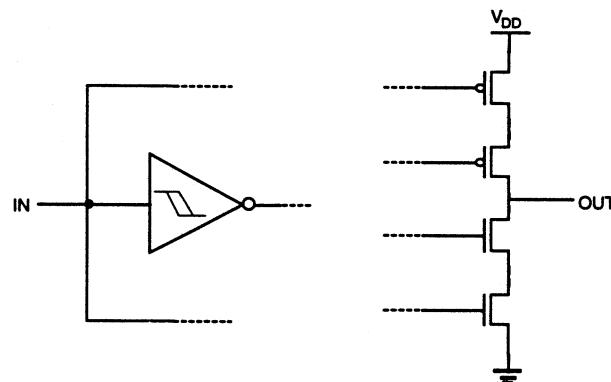


Figure P8.3

### SOLUTION:

The new Schmitt trigger is shown below along with its VTC. Assume that the Schmitt Trigger has threshold voltages such that  $V_L < V_{TN}$  and  $V_H > V_{DD} - |V_{TP}|$ .

Qualitative Explanation:

#### (a) High to low transition

- Assume that  $V_{out}$  is High and  $V_{in}$  is low (1). The Schmitt Trigger output  $V_x$  is High, therefore MP1 is off; MN2 is on; MN1 is off, so  $V_{out}$  is at high impedance state.
- When  $V_{in}$  is larger than  $V_{TN}$ , MN1 turns on, the output node is discharged since  $V_x$  is still high. Therefore  $V_{out}$  goes to 0V. (2)
- Further increase in  $V_{in}$  turns off MP1. pMOS path remains off while nMOS path remains on.  $V_{out}$  stays at 0V. (3)
- When  $V_{in} > V_H$ ,  $V_x$  is 0V and MN2 is turned off. Since pMOS path is still off,  $V_{out}$  is at high impedance state. (4)

#### (b) Low to high transition

- Assume that  $V_{out}$  is low and  $V_{in}$  is high (4).  $V_x$  is low,  $V_{out}$  is at high impedance state.
- As  $V_{in}$  decreases below  $V_{DD} - |V_{TP}|$ , MP1 turns on. MP2 is on since  $V_x$  is still at 0V. Therefore pMOS path turns on,  $V_{out}$  is charged quickly to  $V_{DD}$  as MN2 remains off (5)
- As  $V_{in}$  decreases further, MN2 remains off, vout is high (6).
- High impedance state. (1)

SPICE Simulation input list:

```
CMOS SCHMITT TRIGGER
VDD 3 0 5
VS 1 0 DC PULSE (0 5 2NS 2NS 2NS 6NS )
CLOAD 2 0 3.0E-14
```

```

.MODEL NMOS NMOS VT0=1.0 GAMMA=0.37 KP=2.5E-5
.MODEL PMOS PMOS VT0=-1 GAMMA=0.4 KP=1.0E-5

***Classical Schmitt Trigger

.subckt schmitt 1 2 3
MP1 4 2 1 1 PMOD W=1.2U L=1.2U
MP2 3 2 4 1 PMOD W=12.0U L=1.2U
MP3 4 3 0 1 PMOD W=12.0U L=1.2U
MN1 3 2 5 0 NMOD W=4.0U L=1.2U
MN2 5 2 0 0 NMOD W=1.2U L=1.2U
MN3 5 3 1 0 NMOD W=4.0U L=1.2U
.ends

***New CMOS Schmitt Trigger

.subckt trig 1 2 4
X1 1 2 3 schmitt
C1 3 0 50F
MP1 5 2 1 1 PMOD W=18.0U L=1.2U
MP2 4 3 5 1 PMOD W=18.0U L=1.2U
MN1 4 3 6 0 NMOD W=6.0U L=1.2U
MN2 6 2 0 0 NMOD W=6.0U L=1.2U
.ends

X1 3 1 2 TRIG
.IC V(2)=5
.TRAN 0.5NS 25NS
.PRINT TRAN V(2)
.PRINT TRAN V(1)
.END

```

- 8.4 Consider the monostable multivibrator circuit drawn in Fig.P8.4. Calculate the output pulse width.

- $V_T(\text{dep}) = -2 \text{ V}$
- $V_T(\text{enh}) = 1 \text{ V}$
- $k' = 20 \mu\text{A}/\text{V}^2$
- $\gamma = 0$

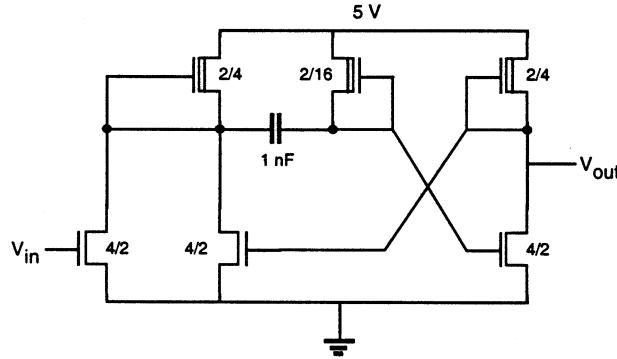


Figure P8.4

**SOLUTION:**

When  $V_{out}$  is high, the current through the capacitor can be calculated by

$$I_{cap} = \frac{1}{2} k(V_{GS} - V_{T,dep})^2 = \frac{1}{2} \cdot \frac{2}{16} \cdot 20 \frac{\mu A}{V^2} (0+2)^2 = 5 \mu A$$

The output pulse width  $t_{pw}$  can be expressed

$$t_{pw} = \frac{C \cdot \Delta V}{I_{cap}}$$

where,

$$\Delta V = V_{TH} - V_{OL}$$

$V_{OL}$  is found when the inverter driver operates in linear region while the load operates in saturation region. Thus,

$$k' \cdot \frac{4}{2} \cdot \left( 5 - 1 - \frac{V_{OL}}{2} \right) \cdot V_{OL} = \frac{k'}{2} \cdot \frac{2}{4} \cdot (0+2)^2$$

$$V_{OL} = 0.13 \text{ V}$$

For  $V_{TH}$ , any of  $V_{IL}$ ,  $V_{IH}$ , and  $V_T(\text{enh})$  are valid assumptions, here we use  $V_{IL}$ .

From equation (5.55) in the text and neglect body effect, we have

$$\frac{k_{driver}}{2} (V_{in} - V_{T,enh})^2 = \frac{k_{load}}{2} \left( 2(0 - V_{T,dep})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right) \quad (1)$$

Differentiate both sides of the above equation with respect to  $V_{in}$  and using the condition for  $V_{IL}$ , i.e.,

$$\left. \frac{dV_{out}}{dV_{in}} \right|_{V_{in}=V_{IL}} = -1$$

we obtain

$$k_{driver} (V_{in} - V_{T,enh}) = k_{load} [V_{T,dep} - (V_{DD} - V_{out})]$$

$$V_{DD} - V_{out} = V_{T,dep} - k_R (V_{in} - V_{T,enh})$$

Plug the above equation into equation (1) and  $V_{IL}$  can be found as:

$$V_{IL} = V_{T,enh} + \frac{|V_{T,dep}|}{\sqrt{k_R(1+k_R)}}$$

$$V_{IL} = 1 + \frac{2}{\sqrt{4(1+4)}} = 1.45 \text{ V}$$

$$t_{pw} = \frac{1 \times 10^{-9} \cdot (1.45 - 0.13)}{5 \times 10^{-6}} = 0.26 \text{ ms}$$

- 8.5** Shown in Fig. P8.5 is an nMOS Schmitt trigger. Draw the voltage transfer characteristic. Include values for all important points on the graph. Use parameters in Problem 8.4 and  $\lambda=0$ . W/L ratios for the transistors are given below.

	M1	M2	M3	M4
W / L	1	0.5	10	1

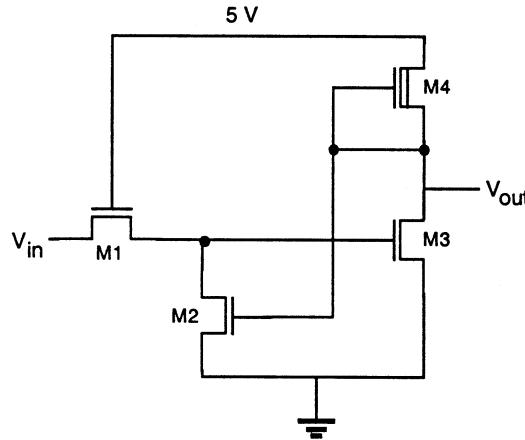


Figure P8.5

### SOLUTION:

The nMOS Schmitt trigger VTC curve goes from high to low in the forward direction when the input of M3 is  $V_{IL}$ , and goes from low to high in the reverse direction when the input of M3 is  $V_{IH}$ . Thus we need to calculate these two points for the given circuit configuration.

$V_{IL}$  of M3 and M4 depletion load inverter:

When  $V_{in} = V_{IL}$ , M3 in saturation and M4 in linear region,

$$\frac{k_{M3}}{2}(V_{in} - V_{T0})^2 = \frac{k_{M4}}{2} \left( 2(0 - V_{T,4})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right) \quad (1)$$

we also know that  $\frac{dV_{out}}{dV_{in}} \Big|_{V_{in}=V_{IL}} = -1$ , thus we obtain another equation

$$V_{IL} = V_{T0} + \frac{k_{M4}}{k_{M3}} [V_{out} - V_{DD} - V_{T,4}] \quad (2)$$

Using the result obtained in Problem 8.4,

$$V_{IL} = V_{T0} - V_{T,4} \left[ \frac{1}{\sqrt{k_R(1+k_R)}} \right]$$

Thus,

$$V_{out} = V_{DD} + V_{T,4} \left[ 1 - \sqrt{\frac{k_R}{1+k_R}} \right]$$

where

$$k_R = \frac{k_{M3}}{k_{M4}} = 10$$

$$V_{out} = 5 + (-2) \left[ 1 - \sqrt{\frac{10}{1+10}} \right] = 4.91V$$

$$V_{IL} = 1 - (-2) \left[ \frac{1}{\sqrt{10(1+10)}} \right] = 1.19V$$

Find  $V_{in}$  of M1:  $I_{D,M1} = I_{D,M2}$ , both M1 and M2 operates in linear region.

$$\begin{aligned} \frac{k_{M2}}{2} (2(V_{GS2} - V_{T0})V_{DS2} - V_{DS2}^2) &= \frac{k_{M1}}{2} (2(V_{GS1} - V_{T0})V_{DS1} - V_{DS1}^2) \\ \frac{1}{2} (2(4.91 - 1)1.19 - 1.19^2) &= \frac{2}{2} (2(5 - 1.19 - 1)(V_{in} - 1.19) - (V_{in} - 1.19)^2) \\ V_{in}^2 - 8V_{in} + 12.04 &= 0 \\ V^+ = V_{in} &= 2.01V \end{aligned}$$

$V_{IH}$  of depletion load inverter (M3 and M4):

M3 in linear and M4 in saturation region. Following the same steps in calculating  $V_{IL}$ , we found the two equations to solve  $V_{IH}$  and  $V_{out}$ :

$$\begin{cases} \frac{k_{M3}}{2} [2(V_{IH} - V_{T0})V_{out} - V_{out}^2] = \frac{k_{M4}}{2} [0 - V_{T,4}]^2 \\ V_{IH} = V_{T0} + 2V_{out} \end{cases}$$

$$\begin{cases} V_{IH} = V_{T0} - \frac{2V_{T,4}}{\sqrt{3k_R}} = 1 + \frac{4}{\sqrt{30}} = 1.73V \\ V_{out} = -\frac{V_{T,4}}{\sqrt{3k_R}} = 0.37V \end{cases}$$

Since  $V_{G2} = V_{out} = 0.37V < 1V$ , M2 is off, M1 is also off, thus

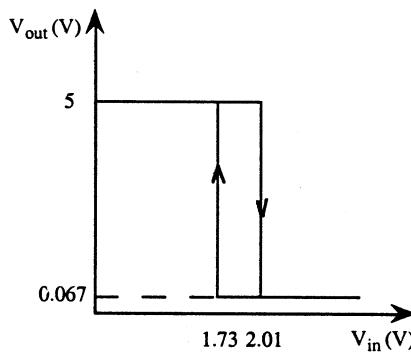
$$V^- = V_{IH} = 1.73V$$

Find out  $V_{OL}$  for the VTC curve:

When  $V_{in} = 5V$  for the nMOS trigger,  $V_{out} = V_{OL}$ , M1 and M2 are off, M3 in linear region and M4 is saturated.

$$\frac{k_{M3}}{2} [2(4 - V_{T0})V_{OL} - V_{OL}^2] = \frac{k_{M4}}{2}(0 - V_{T,4})^2$$

$$V_{OL} = 0.067V$$



- 8.6 Design a circuit to implement the truth table shown in Fig. P8.6. A gate-level design is sufficient.

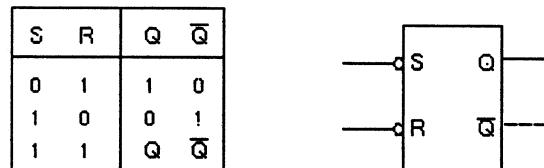
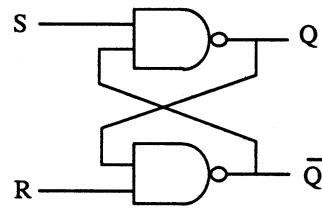


Figure P 8.6

**SOLUTION:**



- 8.7 The circuit you have designed in Problem 8.6 is embedded in the larger circuit shown in Fig.P8.7. Complete the timing diagram for the output.

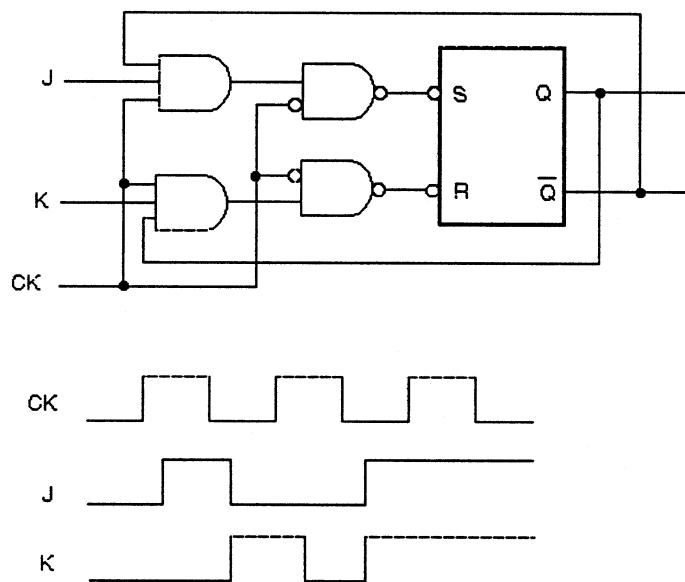
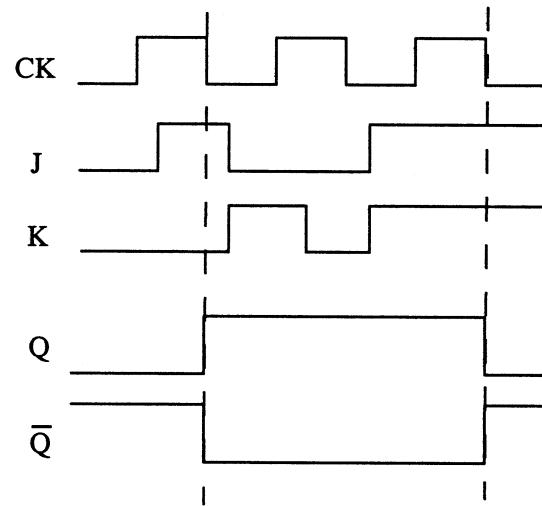


Figure P8.7

**SOLUTION:**



- 8.8 The voltage waveform shown below are applied to the nMOS JK master-slave flip-flop shown in Figure 8.23 in chapter 8. With the flip-flop initially reset, show the resulting waveforms at nodes  $Q_M$  (master flip-flop output) and  $Q_S$  (slave flip-flop output).

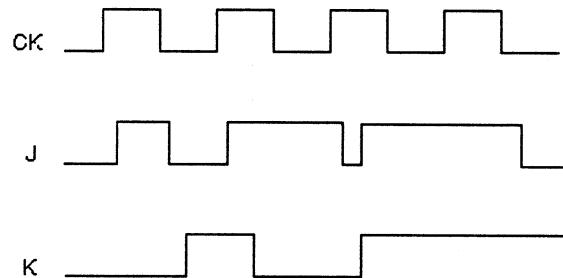


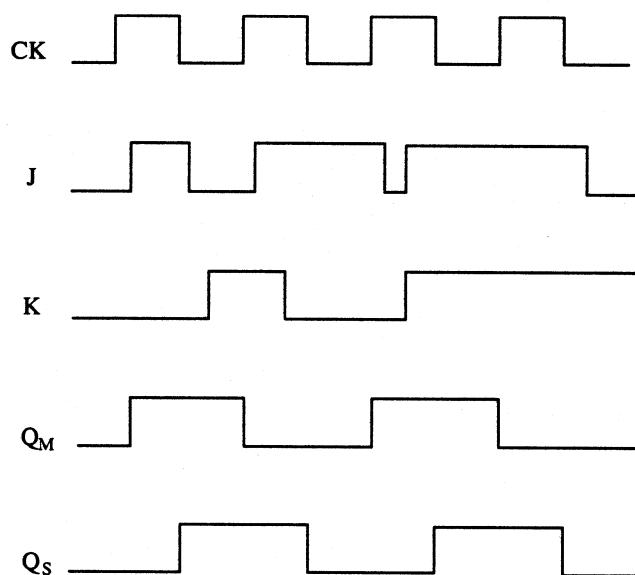
Figure P8.8

**SOLUTION:**

When the clock is "0",  $Q_M$  remains unchanged. When the clock is "1" the following truth table is shown here:

$J$	$K$	$Q_S(n+1)$	$Q_M(n+1)$
0	0	0/1	$Q_M(n)$
0	1	0	$Q_M(n)$
0	1	1	0
1	0	0	1
1	0	1	$Q_M(n)$
1	1	0	1
1	1	1	0

Thus, the corresponding output of  $Q_M$  and  $Q_S$  can be obtained.



## CHAPTER 9

### DYNAMIC LOGIC CIRCUITS

- 9.1** Consider the CMOS circuit shown in Fig. P9.1 that was designed to drive a total capacitive load of  $C_L = 0.2 \text{ pF}$ . For the n-channel devices, assume zero bias threshold voltage  $V_{T0} = 1.0 \text{ V}$  and transconductance parameter  $k'_n = 50 \mu\text{A/V}^2$ . For the p-channel devices, assume  $V_{T0} = -1.0 \text{ V}$  and  $k'_p = 25 \mu\text{A/V}^2$ . For all the devices, assume the  $W/L$  ratios for each device is shown in the figure. The initial voltage across the load capacitor  $C_L$  is 0 V. The waveform at input  $E$  is identically 0V for all time. For the clock  $CK$  and the rest of the inputs, the waveforms are also shown in the figure. Sketch the voltage waveform across the load capacitor  $C_L$  and provide clear marking of the 50% crossings along the time axis in nanoseconds for both rise and fall transitions. [Hint: The n-channel transistor group can be approximated by a single equivalent n-channel transistor and either an average current method or a state equation method may be used to compute the required delay times.

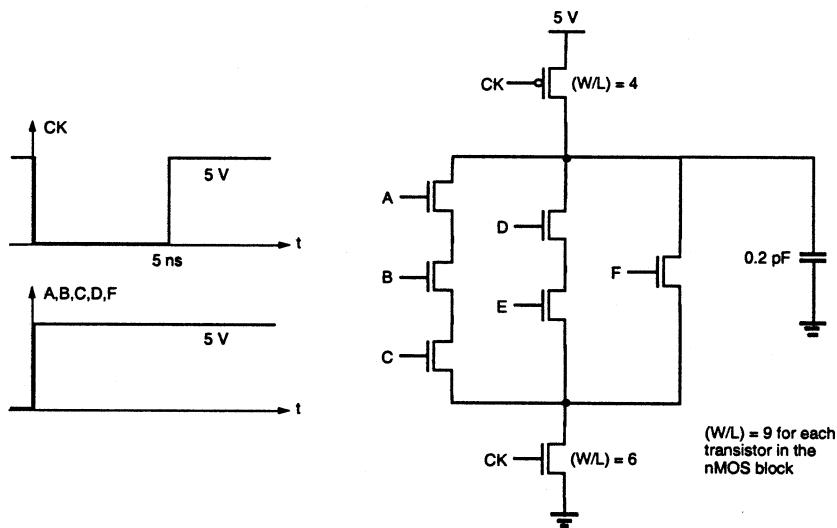


Figure P9.1

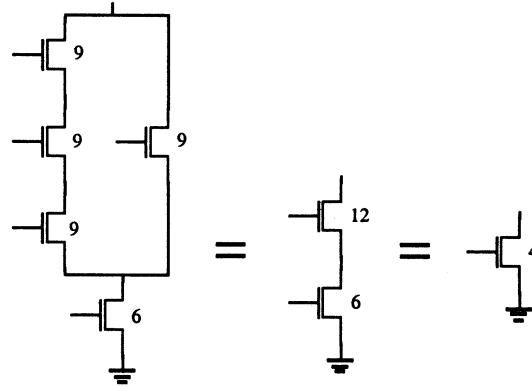
#### SOLUTION:

Since the input  $E$  is kept low all the time, only  $A, B, C$  and  $F$  branches are conducting, thus, the equivalent transistor of nMOS block has

$$\left(\frac{W}{L}\right)_{n-block} = \frac{1}{\frac{1}{9} + \frac{1}{9} + \frac{1}{9}} + 9 = 12$$

Thus, the circuit can be reduced to an inverter circuit with

$$\left(\frac{W}{L}\right)_{n-eq} = \frac{1}{\frac{1}{12} + \frac{1}{6}} = 4$$



(i) Charge up phase:

Assume the time it takes for the transistor to stay in saturation region is  $\tau_s$  then,

$$\tau_s = \frac{C_L \cdot \Delta V}{I_{P,SAT}} = \frac{C_L \cdot \Delta V}{\frac{1}{2} k'_p \left(\frac{W}{L}\right)_p (V_{GS} - V_T)^2} = \frac{0.2 \text{ pF} \cdot 1}{\frac{1}{2} \cdot 25 \mu A \cdot 4 \cdot (-5+1)^2} = 0.25 \text{ ns}$$

The time it takes from saturation region to 50%  $V_{DD}$  is

$$\begin{aligned} \tau_{50\%} - \tau_s &= \frac{C_L \cdot \Delta V}{I_{AVG}} = \frac{C_L \cdot \Delta V}{\frac{1}{2} (I_{P,SAT} + I_{P,LIN})} \\ &= \frac{0.2 \text{ pF} \cdot (4 - 2.5)}{\frac{1}{2} \cdot \left( 0.8 + 4 \times 25 \left( -(-5+1) \times 2.5 - \frac{1}{2} \times 2.5^2 \right) \times 10^{-3} \right) \text{ mA}} = 0.4 \text{ ns} \end{aligned}$$

$$\tau_{50\%} = 0.65 \text{ ns}$$

(ii) Falling phase:

The equations are the same except the nMOS transconductance is twice that of pMOS.

$$\tau_s = \frac{C_L \cdot \Delta V}{I_{N,SAT}} = \frac{0.2 \text{ pF} \cdot 1}{\frac{1}{2} \cdot 50 \mu A \cdot 4 \cdot (5-1)^2} = 0.125 \text{ ns}$$

$$\begin{aligned} \tau_{50\%} - \tau_s &= \frac{C_L \cdot \Delta V}{I_{AVG}} \\ &= \frac{0.2 \text{ pF} \cdot (4 - 2.5)}{\frac{1}{2} \cdot \left( 1.6 + 4 \times 50 \left( (5-1) \times 2.5 - \frac{1}{2} \times 2.5^2 \right) \times 10^{-3} \right) \text{ mA}} = 0.2 \text{ ns} \end{aligned}$$

$$\tau_{50\%} = 0.125 + 0.2 = 0.325 \text{ ns}$$

The plot is shown in the following.

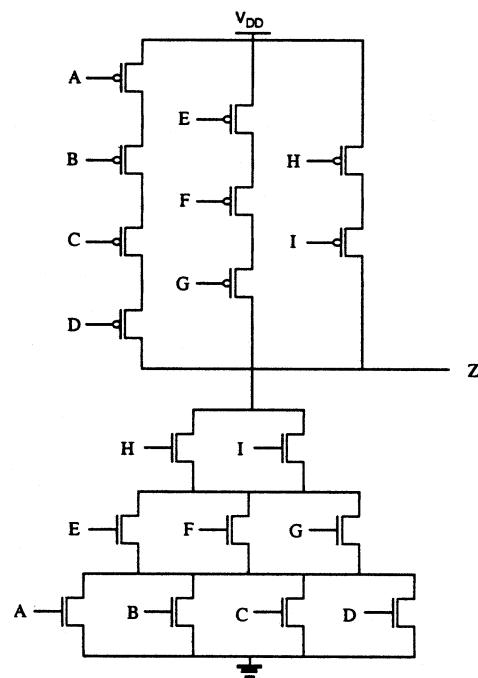
- 9.2 In logic design, complex gates such as AOI or OAI gates are often used to combine the functions of several gates into a single gate, thus reducing the chip area and parasitics of the circuit. Let us consider an OAI432 whose logic function is  $Z = \overline{(A + B + C + D)(E + F + G)(H + I)}$ . Assume that only A, E, H inputs are high and other inputs are low. The device parameters are:

- $C_{jsw} = 250 \text{ pF/m}$
- $C_{jo} = 80 \mu\text{F/m}^2$
- $C_{ox} = 350 \mu\text{F/m}^2$
- $L_D = 0.5 \mu\text{m}$
- $K_{eq} = 1.0$  for worst-case capacitance
- $C_{metal} = 2.0 \text{ pF/cm}$
- $C_{poly} = 2.2 \text{ pF/cm}$
- $R_{poly} = 25 \Omega/\text{sq.}$
- $R_{metal} = 0.2 \Omega/\text{sq.}$
- Polysilicon line width =  $2\mu\text{m}$ , metal line width =  $2\mu\text{m}$
- $k'_n = 20 \mu\text{A/V}^2$
- $k'_p = 10 \mu\text{A/V}^2$
- $|V_{T0}| = 1.0 \text{ V}$

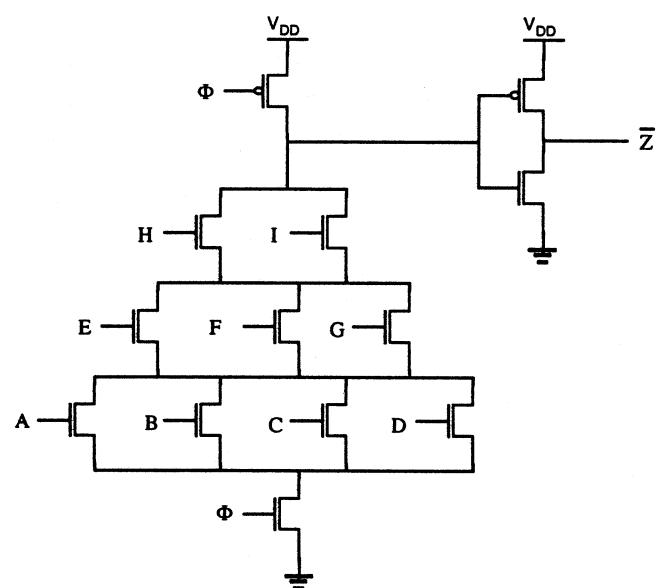
- (a) Draw a full CMOS circuit diagram for this OAI432.
- (b) Draw a domino CMOS circuit implementation whose output is  $\overline{Z}$ .
- (c). Draw an equivalent circuit for this case by using equivalent transistor sizes with  $W/L=30/2$  (both for NMOS and PMOS).
- (d). By assuming that the total parasitic capacitances at the precharging node and the output nodes are  $0.2 \text{ pF}$ , calculate the delay from the end of precharging (clock signal is a rectangular pulse) to the time point at which output voltage reaches  $2.5 \text{ V}$ . For simple analysis, neglect the body effect. For approximate solution of this problem, first calculate the delay for the precharging node to fall to  $2.5 \text{ V}$ . Then use a rectangular pulse at that time point which falls from  $5 \text{ V}$  to  $0 \text{ V}$  to calculate the delay of the inverter gate. The total delay can be found by adding the two delay components. (A more accurate method is to approximate the precharging node voltage by a falling ramp function.)

**SOLUTION:**

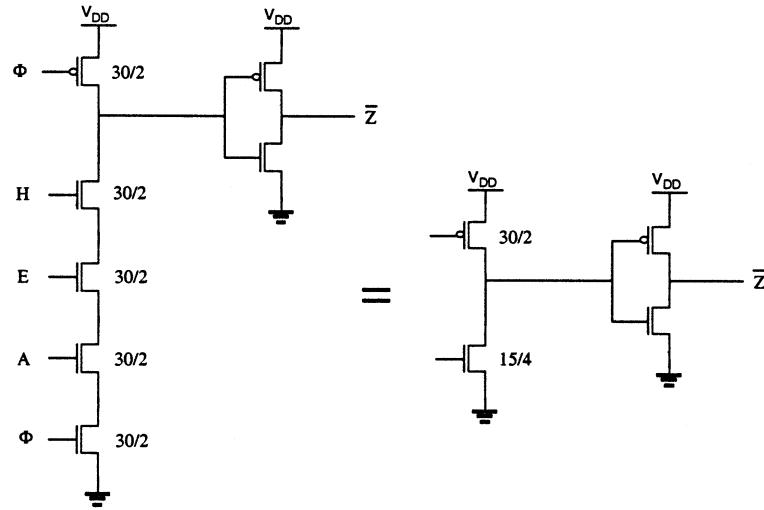
(a) Full CMOS:



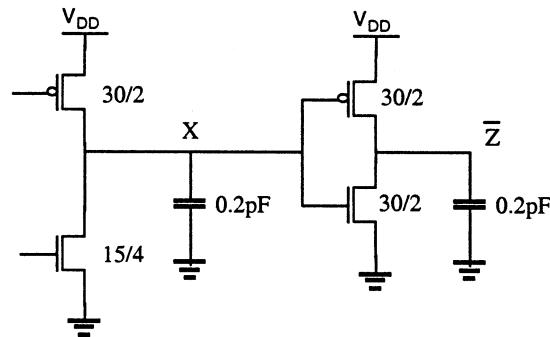
(b) Domino Circuit:



(c) Equivalent Circuit:



(d) The following circuit is used for delay calculation:



(i) Delay calculation for node X to fall to 2.5V. Using equation (6.22b) and  $V_{OH} = V_{DD}$  and  $V_{OL} = 0$ ,

$$t_1 = \tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left( \frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$= \frac{0.2 \mu F}{20 \mu A \cdot 15/4 \cdot (5-1)} \left[ \frac{2}{4} + \ln \left( \frac{4 \times 4}{5} - 1 \right) \right] = 0.86 \text{ ns}$$

(ii) Delay calculation for output node to rise from 0 to 2.5V. Using equation (6.23b)

$$t_2 = \tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

$$= \frac{0.2 \mu F}{10 \mu A \cdot 15 \cdot (5-1)} \left[ \frac{2}{4} + \ln \left( \frac{4 \times 4}{5} - 1 \right) \right] = 0.43 \text{ ns}$$

Thus, the total delay is

$$t_{delay} = t_1 + t_2 = 0.86 + 0.43 = 1.29 \text{ ns}$$

- 9.3** Discuss the charge sharing problems in VLSI circuits. Explain various circuit techniques used in domino CMOS circuits for solving charge-sharing problems. State as many as you know.

**SOLUTION:**

Charge sharing between the output capacitance and an intermediate node capacitance during the evaluation cycle in domino CMOS circuit may reduce the output voltage level or cause the output to go wrong. Several measures can be taken in order to prevent this. One way is to use a weak pMOS pull-up transistor to force the node to remain high. Another method is to use a separate pMOS transistor to precharge intermediate node.

- 9.4** Bootstrapping circuits are used to increase the gate voltages of transistors such that the drain node voltage can be pulled high (despite the threshold voltage drop). The circuit shown in Fig. P9.4 can be used for such purposes and can indeed increase the node voltage at X well beyond  $V_{DD}=5$  V. Determine the maximum achievable voltage at node X using the following parameters:

- $V_{TO} = 1.0$  V
- $\gamma = 0.3$  V $^{1/2}$
- $|2\phi_F| = 0.6$  V
- $V_{OL} = 0.2$  V
- $C_{sub} = 12$  fF
- $C_{boot} = 20$  fF

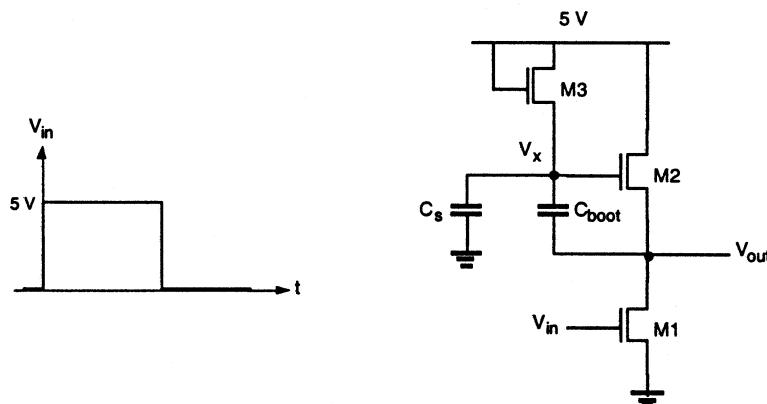


Figure P9.4

**SOLUTION:**

From equation (9.31), we have,

$$V_x = (V_{DD} - V_{T3}(V_x)) + \frac{C_{boot}}{C_{sub} + C_{boot}} (V_{DD} - V_{OL})$$

where  $V_{T3}$  is a function of  $V_x$  and can be expressed as:

$$V_{T3}(V_x) = V_{T3,0} + \gamma \left( \sqrt{|2\phi_F| + V_x} - \sqrt{|2\phi_F|} \right)$$

Solving the two equations using iteration starting at  $V_{T3}=1V$ ,

$V_x$	7	6.405	6.438	6.437
$V_{T3}(V_x)$	1.595	1.562	1.563	1.563

$$V_{x,MAX} = 6.437V$$

- 9.5 A CMOS circuit is shown in Fig. P9.5. Suppose that the precharge transistor was chosen such that the node X is guaranteed to be charged to  $V_{DD}$ . All nMOS transistors have  $W/L = 20$ . Determine how long it takes for the node voltage at X to decrease to  $0.8V_{DD}$  after the clock signal pulse goes to high (with zero rise time) when input voltages at A,B,D are 5 V and the input voltage at C is zero. Assume the following parameter values:

- $\gamma = 0.0 \text{ V}^{1/2}$
- $V_m = 1.0 \text{ V}$
- $k'_n = 10 \mu\text{A/V}^2$

Hint: The NMOS transistor tree between the node X and the ground can be approximated by an equivalent transistor with an effective W/L.

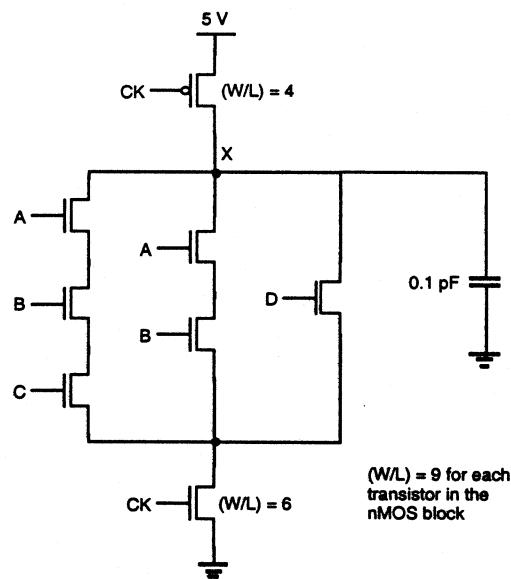
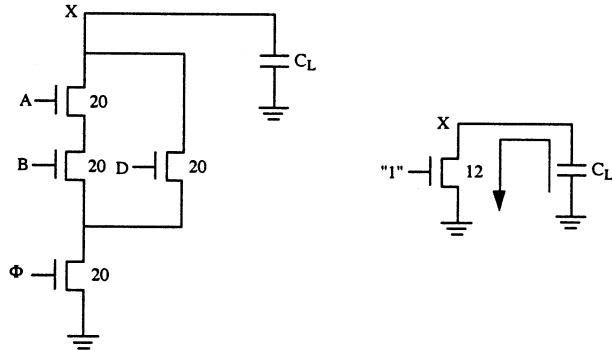


Figure P9.5

### SOLUTION:

The equivalent circuit after clock  $\Phi$  goes high is shown below along with single transistor equivalent circuit.



The equivalent nMOS transistor  $(W/L)_{eq}$

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{20 \cdot 20}{20+20} + 20\right) \cdot 20}{\left(\frac{20 \cdot 20}{20+20} + 20\right) + 20} = 12$$

The discharging current can be found

$$C_L \frac{dV_{out}}{dt} = -I_D$$

Between  $V_{DD}$  and  $0.8V_{DD}$ , the transistor operates in saturation region, thus

$$\int_0^t dt = -C_L \int_{V_{DD}}^{0.8V_{DD}} \frac{dV_{out}}{k'_n \left(\frac{W}{L}\right)_{eq} (V_{DD} - V_{T0})^2}$$

$$t = 0.1pF \frac{2}{10\mu A \cdot 12 \cdot (5-1)^2} = 0.104[ns]$$

- 9.6** The inputs to a domino logic gate are always LO during precharge ( $\phi = \text{LO}$ ) and may undergo a LO-to-HI transition during evaluate ( $\phi = \text{HI}$ ). Consider the domino 3-input AND gate shown in Fig. P9.6 below. If, during evaluate,  $A = \text{HI}$ ,  $B = \text{LO}$ , and  $C = \text{LO}$ , charge sharing will cause the voltage at the input of the inverter to drop. Given that the switching threshold of the inverter is 3V, calculate the maximum ratio  $C_p/C_L$  needed to ensure that charge sharing does not corrupt the value of F for the given case.

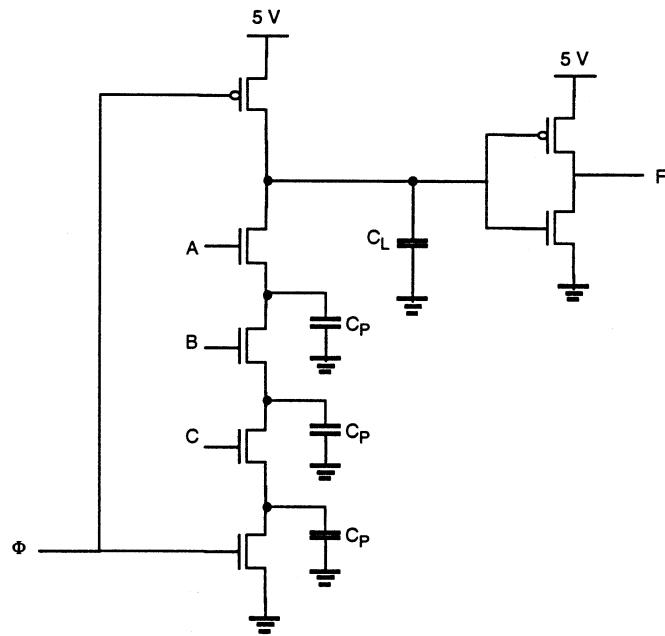


Figure P9.6

**SOLUTION:**

The total charge at node  $C_L$  before charge sharing is

$$Q_L = V_{in} \cdot C_L = 5C_L$$

After charge sharing, suppose the node voltage is  $V_{final}$ , then

$$Q_L = 5C_L = V_{final} \cdot C_L + V_{final} \cdot C_P$$

To prevent the inverter from switching,

$$V_{final} = \frac{5C_L}{C_L + C_P} > 3$$

The maximum ratio is:

$$\frac{C_P}{C_L} < \frac{2}{3}$$

- 9.7 Consider the following CMOS logic circuit which is a simple domino circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the domino circuit.
- (a) Explain how the voltage level at node X, after it is precharged to 5 V, can be affected by the charge sharing between node X and node Y if their node capacitances are the same. Express the final voltage at node X in terms of the initial voltage at node Y when the charge sharing is completed following the full precharge operation when the gate terminal of M2 transistor is fixed at 0 V.

- (b) Determine the ratio between device transconductance parameters,  $k_p$  and  $k_n$ , of the inverter to prevent any logic error due to charge sharing between nodes X and Y under all circumstances. Assume that the magnitudes of threshold voltages in the inverter are equal to 1.0 V. The use of Level 1 transistor current equations is deemed adequate.

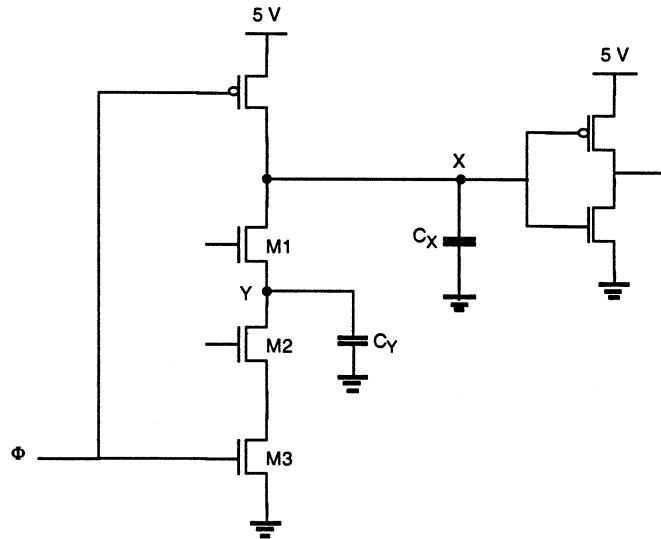


Figure P9.7

**SOLUTION:**

- (a). Before charge sharing, the total charge at node X is

$$Q_{total} = C_X V_X + C_Y V_Y$$

After charge sharing,

$$Q_{total} = (C_X + C_Y) V_{final}$$

The final voltage at node X is then

$$V_{final} = \frac{5C_X + C_Y V_Y}{C_X + C_Y}$$

- (b). In order to prevent logic error, the final voltage after charge sharing must be higher than the inverter threshold voltage, that is,

$$V_{final} \geq V_{th} = \frac{V_{T,n} + \sqrt{\frac{k_p}{k_n} (V_{DD} - |V_{T,p}|)}}{1 + \sqrt{\frac{k_p}{k_n}}}$$

The worst case charge sharing is when the initial voltage at Y is 0. Thus,

$$\frac{5C_X}{C_X + C_Y} \left( 1 + \sqrt{\frac{k_p}{k_n}} \right) \geq 1 + 4\sqrt{\frac{k_p}{k_n}}$$

$$\frac{k_p}{k_n} \geq \left( \frac{C_Y - 4C_X}{C_X - 4C_Y} \right)^2$$

- 9.8** Consider the domino CMOS circuit shown in Fig. P9.6. Using the input voltage waveforms illustrated in Fig. P9.8 determine the output voltage waveform.

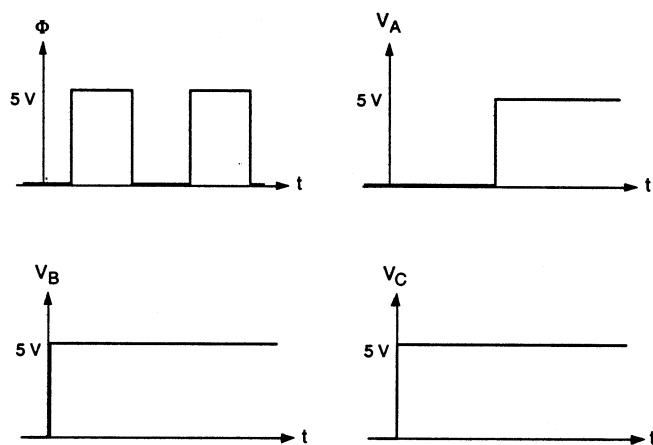


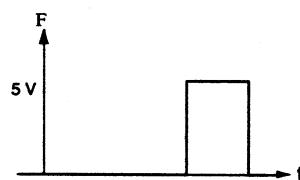
Figure P9.8

**SOLUTION:**

When the clock signal is high, the following function is achieved:

$$F = ABC$$

When the clock signal is low, precharging occurs and F is held low.  
The waveform of F is shown:



## CHAPTER 10

### SEMICONDUCTOR MEMORIES

- 10.1** Consider the DRAM circuit shown in Figure 10.45 in the text. The threshold voltage of the two precharge transistors is 2V. Calculate the steady-state voltages of  $V_D$  in region I and region II of Fig.P10.1 by assuming the following:
- $C = 50 \text{ fF}$
  - $C_D = 400 \text{ fF}$
  - $V(C) = V(C/2) = V_y = 0 \text{ V}$  in region I
  - while PC is high, no other transistor connected to  $D$  or  $\bar{D}$  is on.

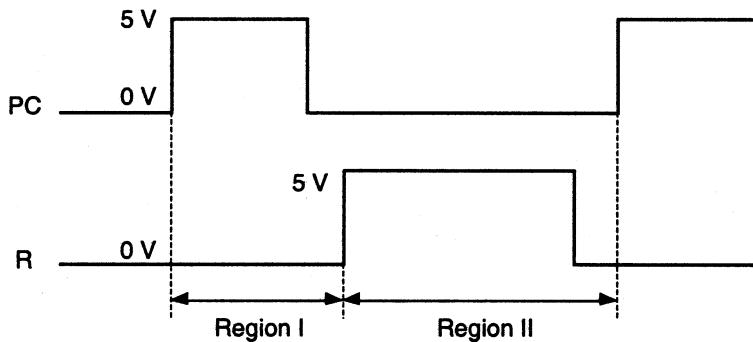


Figure P10.1

**SOLUTION:**

At steady state, there is no current flow through the precharging transistors. Therefore, in Region I:

$$I = \frac{k}{2} (V_G - V_D - V_T)^2 = 0$$

$$V_D = V_{DD} - V_T = 5 - 2 = 3 \text{ V}$$

In Region II, charge sharing occurs,

$$C_D V_D + CV(C) = C_D V_{final} + CV_{final}$$

$$V_{final} = \frac{C_D V_D + 0}{C_D + C} = \frac{400 \times 3}{400 + 50} = 2.67 \text{ V}$$

- 10.2** A single-transistor DRAM cell is represented by the following circuit diagram. The bitline can be precharged to  $V_{DD}/2$  by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bitline to  $V_{DD}$  or 0 V during the WRITE operation with wordline at  $V_{DD}$ . Using the parameter given:
- $V_m = 1.0 \text{ V}$
  - $\gamma = 0.3 \text{ V}^{1/2}$
  - $|2\phi_F| = 0.6 \text{ V}$

- (a) Find the maximum voltage across the storage capacitor  $C_s$  after WRITE-1 operation, i.e., when the bitline is driven to  $V_{DD} = 5$  V.
- (b) Assuming zero leakage current in the circuit, find the voltage at the bitline during READ-1 operation after bitline is first precharged to  $V_{DD}/2$ .

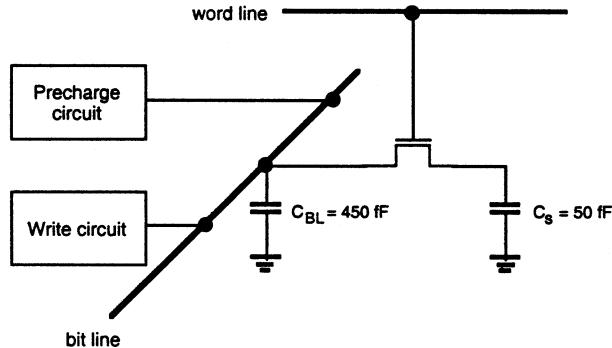


Figure P10.2

**SOLUTION:**

- (a) When the bitline is driven to  $V_{DD}$ , the transistor operates in saturation region, the maximum voltage is achieved across the storage capacitor when steady state is reached. That is:

$$I_S = \frac{1}{2} k_n (V_G - V_S - V_T)^2 = 0$$

$$V_S = 4 \text{ V}$$

- (b). During READ 1 operation, charge sharing occurs between  $C_s$  and  $C_{BL}$ .

$$C_s V_s + C_{BL} V_{BL} = (C_s + C_{BL}) V_{final}$$

$$V_{final} = \frac{C_s V_s + C_{BL} V_{BL}}{C_s + C_{BL}} = \frac{50 \times 4 + 450 \times 2.5}{50 + 450} = 2.65 \text{ V}$$

- 10.3** A dynamic CMOS Read Only Memory (ROM) has been designed with a core array consisting of 64 rows with a pitch of  $12\mu\text{m}$  and 64 columns with a pitch of  $10\mu\text{m}$  as shown below. Each column is precharged to 5 V by a PMOS transistor during the interval of zero clock phase and then gets pulled down after the clock signal switches to 5 V by one or more nMOS transistors ( i.e., NOR implementation) with high gate inputs on the appropriate rows. All of the nMOS transistors have channel width  $W = 4 \mu\text{m}$  and the source/drain length  $Y = 5 \mu\text{m}$ . Now as a designer, you are to determine the propagation delay time from a particular input (on row 64) going high to a particular bit-line output (on column 64) going low  $t_{PHL}$  between 50% points. Assume that the input signal to row 64 becomes valid high only after the precharge operation is finished as shown in the timing diagram. Also, assume that row 64 is running over 30 nMOS transistors and

column 64 has 20 nMOS transistors connected to it. For delay calculation, assume that only one nMOS transistor is pulling down. Also assume that pMOS is strong enough to fully charge the precharging node during the precharge phase of the clock signal and neglect its drain parasitic capacitance. Device parameters are given:

- $C_{jw} = 250 \text{ pF/m}$
- $C_{jo} = 80 \mu\text{F/m}^2$
- $C_{ox} = 350 \mu\text{F/m}^2$
- $L_D = 0.5 \mu\text{m}$
- $K_{eq} = 1.0$  for worst-case capacitance
- $C_{metal} = 2.0 \text{ pF/cm}$  and  $R_{metal} = 0.03 \Omega/\text{sq}$ .
- $C_{poly} = 2.2 \text{ pF/cm}$  and  $R_{poly} = 25 \Omega/\text{sq}$ .
- Polysilicon line width =  $2\mu\text{m}$
- Metal line width =  $2\mu\text{m}$
- $k'_n = 20 \mu\text{A/V}^2$
- $k'_p = 10 \mu\text{A/V}^2$
- $V_{Tn} = -V_{Tp} = 1.0 \text{ V}$

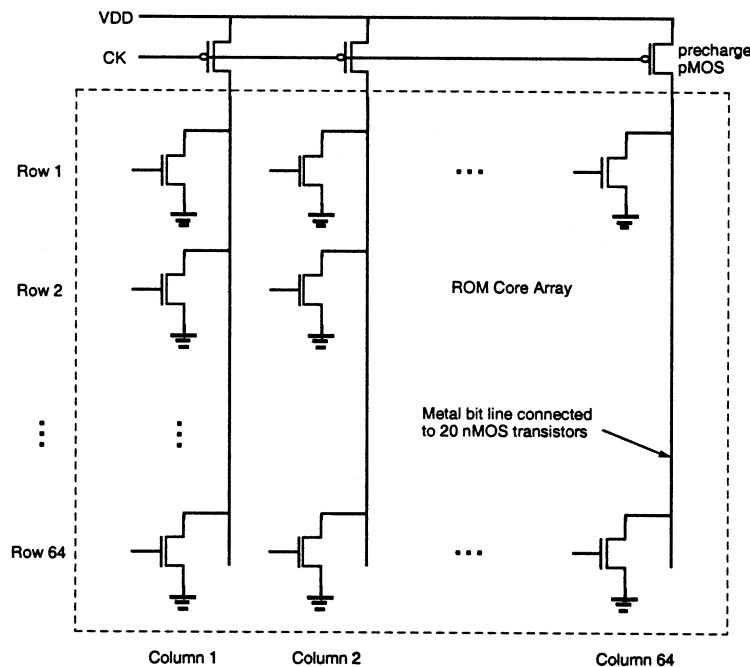


Figure P10.3

### SOLUTION:

First calculate the row delay:

$$R_{row} = R_{poly} \times \frac{\text{column pitch}}{\text{poly width}} \times 64 = 25 \times \frac{10}{2} \times 64 = 8000 \Omega$$

$$C_{row} = C_{poly} \times 10 \times 64 = 640 \times 10^{-4} \times 2.2 = 0.14 \text{ pF}$$

$$t_{row} = 0.38 R_{row} C_{row} = 0.38 \times 8 \times 10^3 \times 0.14 \times 10^{-12} = 3.4 \text{ ns}$$

Calculate the column delay:

Consider the interconnect capacitance, junction capacitance and overlap capacitance.

$$C_{int} = C_{metal} \times 12 \times 64 = 2.0 \times 12 \times 10^{-4} \times 64 = 0.154 \text{ pF}$$

$$\begin{aligned} C_{db} &= AD \cdot C_{jo} + PD \cdot C_{jsw} \\ &= 4 \times 5 \times 80 \times 10^{-6} \times 10^{-12} + 14 \times 250 \times 10^{-12} \times 10^{-6} = 5100 \times 10^{-18} \text{ F} \end{aligned}$$

$$C_{gd} = C_{ox} \cdot W \cdot L_D = 350 \times 10^{-18} \times 4 \times 0.5 = 700 \times 10^{-18} \text{ F}$$

The total load capacitance is:

$$C_L = C_{int} + 20(C_{db} + C_{gd}) = 0.154 + 0.116 = 0.27 \text{ pF}$$

Using the average current method to calculate the high to low delay.

$$\begin{aligned} I(V_{in} = 5, V_{out} = 5) &= \frac{1}{2} k'_n \left( \frac{W}{L_{eff}} \right) (V_{GS} - V_T)^2 \\ &= \frac{1}{2} \times 20 \times 10^{-6} \frac{4}{2-2 \times 0.5} (5-1)^2 = 0.64 \text{ mA} \end{aligned}$$

$$\begin{aligned} I(V_{in} = 5, V_{out} = 2.55) &= \frac{1}{2} k'_n \left( \frac{W}{L_{eff}} \right) (2(V_{GS} - V_T)V_{DS} - V_{DS}^2) \\ &= \frac{1}{2} \times 20 \times 10^{-6} \times 4 \times (2 \times 4 \times 2.5 - 2.5^2) = 0.55 \text{ mA} \end{aligned}$$

$$I_{avg} = \frac{1}{2}(0.55 + 0.64) = 0.595 \text{ mA}$$

The 50% delay at column is:

$$t_{PHL}' = \frac{C_L \Delta V}{I_{avg}} = \frac{0.27 \times 2.5}{0.595} = 1.13 \text{ ns}$$

The total delay is thus,

$$t_{PHL} = t_{row} + t_{PHL}' = 3.4 + 1.13 = 4.53 \text{ ns}$$

- 10.4** Consider the CMOS SRAM cell drawn in Fig. P10.4. Transistors M1 and M2 have  $W/L$  values of 4/4. Transistors M3 and M4 have  $W/L$  values of 2/4. M5 and M6 are to be sized such that the state of the cell can be changed for  $V_C \leq 0.5 \text{ V}$ . Assuming that M5 and M6 are the same size, calculate the required  $W/L$ . Use the following parameter:

- $V_{T0,n} = 0.7 \text{ V}$
- $V_{T0,p} = -0.7 \text{ V}$
- $k'_n = 20 \mu\text{A}/\text{V}^2$
- $k'_p = 10 \mu\text{A}/\text{V}^2$
- $\gamma = 0.4 \text{ V}^{1/2}$
- $|2\phi_F| = 0.6 \text{ V}$

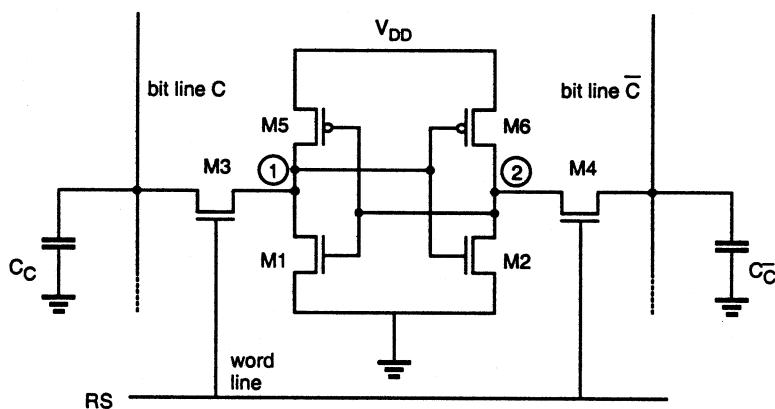


Figure P10.4

**SOLUTION:**

Assume during this operation, the storage bit changes from 1 to 0. Also assume the cell will change state for  $V_b = V_{T,n} = 1V$ . ( $V_b = V_{DD}/2$  is also a good assumption.) A better assumption would be  $V_{IH}$ , but we don't know it until M5 and M6 have been sized. The initial condition is  $V_b = 5 V$ , M1 is off. At the transition point, For M5:

$$V_{GS} = 0 - 5 = -5 \text{ V}$$

$$V_{DS} = 0.7 - 5 = -4.3 \text{ V}$$

Thus, M5 is saturated. For M3:

$$V_{GS} = 5 - 0.5 = 4.5 \text{ V}$$

$$V_{DS} = 0.7 - 0.5 = 0.2 \text{ V}$$

$$V_{T,n} = 0.7 + 0.4(\sqrt{0.6+0.5} - \sqrt{0.6}) = 0.81 \text{ V}$$

Thus, M3 is in linear region.

$$I_{D,M5} = I_{D,M3}$$

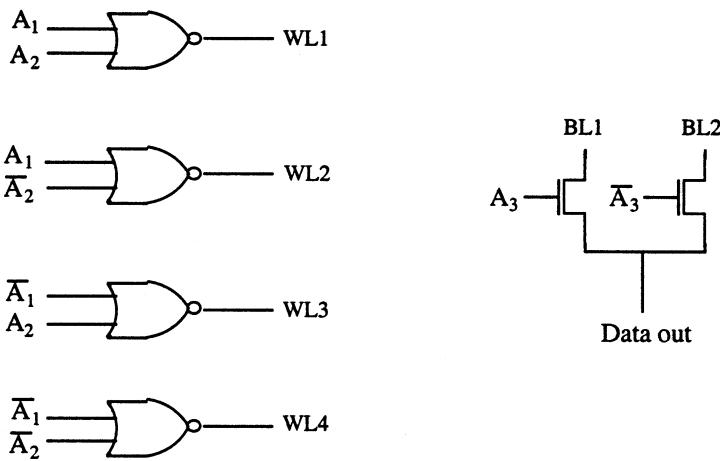
The transistor W/L for M5 and M6 are thus:

$$\frac{10}{2} \left( \frac{W}{L} \right)_p (-5 + 0.7)^2 = 20 \left( \frac{2}{4} \right) \left( 4.5 - 0.81 - \frac{0.2}{2} \right) 0.2$$

$$\left( \frac{W}{L} \right)_p = 0.078$$

- 10.5** Draw circuit diagrams of the row decoder and the column decoder for an EPROM with 4 rows and 2 columns. Use nMOS technology. Develop formulas for the row and column delays in the EPROM. Define any terms in your formulas which are not obvious.

## SOLUTIONS:



Row Decoder

Column Decoder

(1) Row delay:

$$t_{ROW} = 0.38 R_{ROW} \cdot C_{ROW}$$

where,

$$\begin{aligned} R_{ROW} &= 2 \times R_{ROW/BIT} \\ C_{ROW} &= 2 \times C_{ROW/BIT} \end{aligned}$$

$$R_{ROW/BIT} = \text{Poly sheet resistance} \cdot \frac{L_{col}}{W_{poly}}$$

$L_{col}$  is the distance from the center of one column to the next,  $W_{poly}$  is the poly line width which is equal to drawn channel length.

$$C_{ROW/BIT} = C_g = C_{cg} // C_{fg} = \frac{C_{cg} \cdot C_{fg}}{C_{cg} + C_{fg}}$$

The control gate capacitance per bit is

$$C_{cg} = \frac{\epsilon_{ox2}}{T_{ox2}} \cdot W \cdot L$$

The floating gate capacitance per bit is

$$C_{fg} = \frac{\epsilon_{ox1}}{T_{ox1}} \cdot W \cdot L$$

(2) Column delay:

$$t_{COL} = \frac{C_{col} \cdot \Delta V}{I_{AVG}}$$

$$C_{COL} = 4 \times C_{COL/BIT}$$

$$C_{COL/BIT} = C_{gd} + C_{db}$$

$$C_{db} = K_{eq} (A_{drian} \cdot C_{jo} + P_{drian} \cdot C_{jsw})$$

where  $K_{eq}$  can be calculated for a voltage swing of 2.5V.

$$C_{gd} = C_{fgd} // C_{cg}$$

$$C_{cg} = \frac{\epsilon_{ox2}}{T_{ox2}} \cdot W \cdot L$$

$$C_{fgd} = \frac{\epsilon_{ox1}}{T_{ox1}} \cdot W \cdot L_D$$

$$I_{AVG} = \frac{I_{init} + I_{final}}{2}$$

$$I_{final} = k \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) \times V_{DS} = k \left( 5 - V_{T,enh} - \frac{2.5}{2} \right) \times 2.5$$

- 10.6** Consider an 8K x 8K SRAM. An 8K x 8K SRAM has 64K (=65536) memory cells and 8 output lines. In the particular SRAM under discussion, 7 address bits go to the row decoder and 6 address bits go to the column decoder. Bit lines are precharged to  $V_{DD} = 5$  V before each read operation. A read operation is complete when the bit line has discharged by 0.5 V. A memory cell can provide 1.0 mA of pull-down current to discharge the bit line.
- (a) Word line resistance is  $390 \Omega$  per memory cell. What formula was used to calculate this resistance?
  - (b) Word line capacitance is 22 fF per memory cell. What formula was used to calculate this capacitance?
  - (c) Bit line capacitance is 6 fF per memory cell. What formula was used to calculate this capacitance?
  - (d) Calculate the access time (row delay + column delay) for this SRAM.
  - (e) Describe the operation and design of the word line decoder and the bit line decoder.

#### SOLUTION:

(a).  $R_{WL}$  calculation:

$$R_{WL} = (\# \text{ of squares}) \times (\text{Poly sheet resistance})$$

(b).  $C_{WL}$  calculation:

Consider a full CMOS cell implementation, neglecting poly capacitance:

$$C_{WL} = 2C_{ox} \cdot W \cdot L = 2 \frac{\epsilon_{ox}}{T_{ox}} \cdot W \cdot L$$

(c). Bit line capacitance:

$$\begin{aligned}C_{BL} &= C_{db} + C_{gd} + C_{metal/cell} \\C_{db} &= K_{eq} (A \cdot C_{jo} + P \cdot C_{jsw}) \\C_{gd} &= C_{ox} \cdot W \cdot L_D\end{aligned}$$

(d). Access time calculation:

$$\begin{aligned}t_{ROW} &= 0.38 \cdot R_{WL/cell} \cdot C_{WL/cell} \cdot (\# \text{ of cells})^2 \\&= 0.38 \cdot 390\Omega \cdot 22fF \cdot (2^6 \cdot 8)^2 = 854.7ns \\t_{COL} &= \frac{C_{WL/cell} \cdot (\# \text{ of cells}) \cdot \Delta V}{I} = \frac{6fF \cdot 2^7 \cdot 0.5}{10^{-3}} = 0.38ns \\t_{TOTAL} &= t_{ROW} + t_{COL} = 854.7 + 0.38 = 855ns\end{aligned}$$

(e).

Word line---Each Word line driven by gate which has function equal to a 7 input NOR gate. One word line HI for any combination of inputs.

Bit line --- 8 BL/BL\_bar are passed to sense amplifier and output for 1 address. Bitline functionality equal to a 6-input NOR driving a pass gate. Tree decoder can be used to reduce number of gates.

## CHAPTER 11

### LOW-POWER CMOS LOGIC CIRCUITS

- 11.1** For Part (a), please note that the voltage across the pMOS transistor will be equal to  $(V_{DD} - V_{out})$ . Knowing the output voltage variation as a function of time, the drain-to-source voltage waveform of the pMOS transistor can be easily found. At the beginning of the transition, the voltage drop is equal to  $V_{DD}$ . It drops to zero when the output voltage attains its final value, at the end of the transition. For Part (b), please refer to the discussion in Section 6.7 (pages 242 - 249).
- 11.2** Note that in this case, the voltage drop across the pMOS transistor will be much smaller than the full  $V_{DD}$  level, at any time during the low-to-high transition. Hence, the power dissipation is also less (you may use power-meter simulation described in Chapter 6).
- 11.3** Please refer to the discussion on adiabatic logic gates (pages 484 - 486).
- 11.4** Please refer to the discussion on adiabatic logic gates (pages 484 - 486).

*Extra question not contained in the textbook:*

- 11.5** The nMOS and pMOS transistors in a CMOS inverter have the following parameters:
- $|V_{to}| = 1.0 \text{ V}$  for both nMOS and pMOS transistors
  - $\lambda = 0.0 \text{ V}^{-1}$
  - $k'_n = 50.0 \mu\text{A/V}^2$
  - $k'_p = 20.0 \mu\text{A/V}^2$

The CMOS inverter is designed with  $(W/L)_p = 20$  and  $(W/L)_n = 10$ , and its capacitive load is 2pF. It is assumed that the load capacitance includes all parasitic capacitances connected to the drain node.

- (a) Calculate the average power dissipation in the inverter when its input signal is a rectangular pulse with 100 ns period which swings between 5 V and 0 V.
- (b) Repeat Part (a) for the case when each transistor channel width is exactly twice as that used in (a), but the load capacitance and input signal remain the same.
- (c) What observations can you make from the results of part (b) ?  
Can you explain why the results should be same or different.
- (d) Verify your answer using the power meter with SPICE simulation. For SPICE simulation, you can set the parasitic capacitances in drain and source regions to zero by setting AD, AS, PD, PS to zero.

**SOLUTION:**

(a)

$$f = \frac{1}{T} = \frac{1}{100\text{ns}} = 10[\text{MHz}]$$

$$P_{avg} = C_L \cdot V_{DD}^2 \cdot f = 2 \times 10^{-12} \times 25 \times 10 \times 10^6 = 0.5[\text{mW}]$$

(b)

Since the load capacitance and input signal remain the same, the power dissipation will be the same.

(c)

The power dissipation does not depend on the transistor width and length. In CMOS circuits, there is always a full voltage swing from 0 to  $V_{DD}$  at the output regardless of the transistor sizes. Thus, the average power depends only on  $V_{DD}$ , the load capacitance and the operating frequency. Increasing width would increase the drain and source capacitance of the transistors' load and will increase the power consumption slightly, this however is not taken into consideration in this problem.

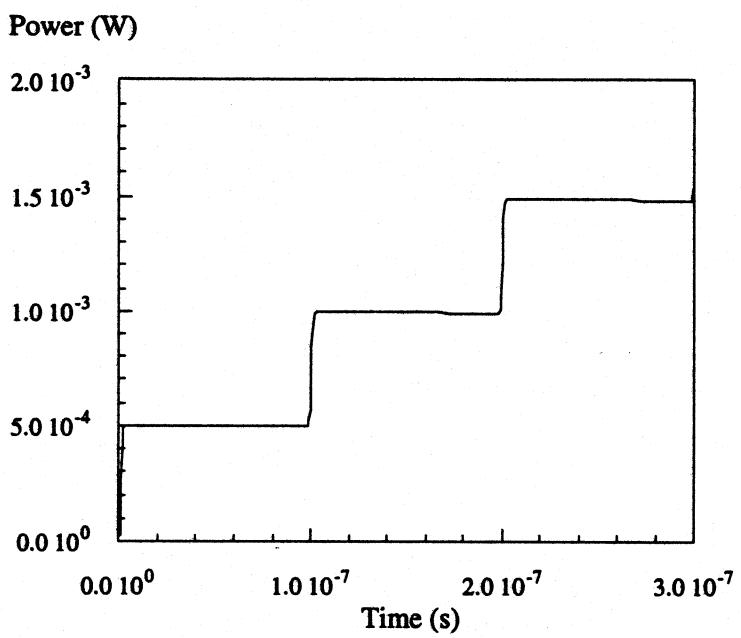
(d)

The SPICE simulation results show that the power dissipation is 0.5 mW.

SPICE input list:

```
Power meter simulation:  
mn 3 2 4 0 nmod w=10u l=1u  
mp 3 2 5 1 pmod w=20u l=1u  
vdd 1 0 5  
vtstp 1 5 0  
vtstn 4 0 0  
.model nmod nmos(vto=1 kp=50u)  
.model pmod pmos(vto=-1 kp=20u)  
vin 2 0 pulse(0 5 8n 2n 2n 88n 100n)  
cl 3 0 2p  
fp 0 9 vtstp 0.005  
fn 0 10 vtstn 0.005  
rn 10 0 100k  
rp 9 0 100k  
cn 10 0 100p  
cp 9 0 100p  
.tran 1n 300n uic  
.print tran v(9)  
.end
```

Plot of SPICE output:



## CHAPTER 12

### BiCMOS LOGIC CIRCUITS

- 12.1** A BJT transistor has  $\alpha_F = 0.99$  and  $\alpha_R = 0.2$ . Calculate the collector junction reverse saturation current when its emitter junction reverse saturation current is  $10^{-14}$  A. Determine the area of the collector junction compared to the area of the emitter junction.

**SOLUTION:**

From equation (12.25)

$$\alpha_F I_{ES} = \alpha_R I_{CS}$$

$$I_{CS} = \frac{\alpha_F I_{ES}}{\alpha_R} = \frac{0.99 \times 10^{-14}}{0.2} = 4.95 \times 10^{-14} \text{ A}$$

The ratio of the two areas are:

$$\frac{A_{\text{collector}}}{A_{\text{emitter}}} = \frac{I_{CS}}{I_{ES}} = 4.95$$

- 12.2** A circuit for generating a reference voltage  $V_R$  is shown below. Find the value of  $V_R$  by assuming that the voltage drop across each diode and base-emitter junction in  $Q_1$  is 0.7V.

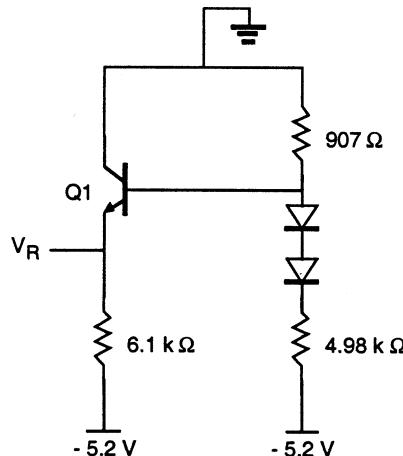


Figure P12.2

**SOLUTION:**

The current through the two diodes can be found

$$I_D = \frac{0 - (-5.2) - 2 \times 0.7}{4.98 + 0.907} = 0.645 \text{ mA}$$

thus the voltage at base node of  $Q_1$  is

$$V_B = 0 - I_D R_2 = -0.645 \times 0.907 = -0.585 \text{ V}$$

$$V_R = V_B - 0.7 = -0.585 - 0.7 = -1.285V$$

**12.3** Derive the expression for  $\tau_s$  in equation (12.64) in the text.

**SOLUTION:**

In saturation,

$$\frac{dQ_{jE}}{dt} = \frac{dQ_{jC}}{dt} = 0$$

From equation (12.58), we have

$$i_C = \frac{Q_F}{\tau_F} - Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right) - \frac{dQ_R}{dt}$$

$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{d}{dt}(Q_F + Q_R)$$

knowing the fact that

$$Q_F = Q_A + Q_S - Q_R$$

$$\frac{dQ_A}{dt} = 0$$

$i_{BS}$  can then be expressed as

$$i_{BS} = i_B - i_{B(EOS)} = i_B - \frac{Q_A}{\tau_{BF}}$$

$$= \frac{Q_A + Q_S - Q_R}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{d}{dt}(Q_A + Q_S) - \frac{Q_A}{\tau_{BF}}$$

$$= \frac{Q_S - Q_R}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{dQ_S}{dt}$$

Next, we find the relationship between QR and QS. From

$$i_C = \frac{Q_F}{\tau_F} - Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right) - \frac{dQ_R}{dt}$$

and at the edge of saturation (EOS),

$$\frac{dQ_R}{dt} = 0$$

we know  $i_{C(EOS)}$  is:

$$i_{C(EOS)} = \frac{Q_F}{\tau_F} - Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right) = \frac{Q_A}{\tau_F}$$

Thus,

$$\frac{Q_A - Q_F}{\tau_F} = \frac{Q_R - Q_S}{\tau_F} = -Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right)$$

Solving for  $Q_R$ , we obtain

$$Q_R = \frac{Q_S}{1 + \tau_F \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right)} = \frac{Q_S}{1 + \frac{\tau_F}{\tau_R} \frac{1}{\alpha_R}}$$

Rewrite  $i_{BS}$ ,

$$\begin{aligned} i_{BS} &= \frac{Q_S - Q_R}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{dQ_S}{dt} \\ &= \frac{Q_S}{\tau_{BF}} + Q_R \left( \frac{1}{\tau_{BR}} - \frac{1}{\tau_{BF}} \right) + \frac{dQ_S}{dt} \\ &= \frac{Q_S}{\tau_{BF}} + \frac{Q_S}{1 + \frac{\tau_F}{\tau_R} \frac{1}{\alpha_R}} \left( \frac{1}{\tau_{BR}} - \frac{1}{\tau_{BF}} \right) + \frac{dQ_S}{dt} = \frac{Q_S}{\tau_s} + \frac{dQ_S}{dt} \\ \frac{1}{\tau_s} &= \frac{1}{\tau_{BF}} + \frac{1}{1 + \frac{\tau_F}{\tau_R} \frac{1}{\alpha_R}} \left( \frac{1}{\tau_{BR}} - \frac{1}{\tau_{BF}} \right) \\ \tau_s &= \frac{\beta_F (\alpha_R \tau_R + \tau_F)}{1 + \beta_F (1 - \alpha_R)} = \frac{\alpha_F (\alpha_R \tau_R + \tau_F)}{1 - \alpha_F \alpha_R} \end{aligned}$$

**12.4** For the BJT inverter circuit in Figure 12.12 with the following parameters:

- $V_{CC} = 5 \text{ V}$
- $R_B = 10 \text{ k}\Omega$
- $R_C = 1 \text{ k}\Omega$
- $\beta_F = 100$
- $V_{BE(on)} = 0.7 \text{ V}$
- $V_{BE(sat)} = 0.8 \text{ V}$
- $V_{CE(sat)} = 0.1 \text{ V}$

Calculate  $V_{IL}$ ,  $V_{IH}$  and noise margins  $NM_L$ ,  $NM_H$ .

**SOLUTION:**

$$V_{IL} = V_{BE(on)} = 0.7 \text{ V}$$

$$V_{OH} = V_{DD} = 5 \text{ V}$$

$$\begin{aligned} V_{IH} &= V_{BE(sat)} + I_{B(sat)} \cdot R_B = V_{BE(sat)} + \frac{R_B}{R_C \cdot \beta_F} (V_{CC} - V_{CE(sat)}) \\ &= 0.8 + \frac{10}{1 \cdot 100} (5 - 0.1) = 1.29 \text{ V} \end{aligned}$$

$$V_{OL} = V_{CE(sat)} = 0.1 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.7 - 0.1 = 0.6 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5 - 1.29 = 3.71 \text{ V}$$

**12.5** Derive equation (12.65) for the equivalent circuit in Figure 12.26.

**SOLUTION:**

The bipolar transistor is in cut-off region. Let the base node of Q1 be node X.  
The total effective capacitance at node X is:

$$C_X = \frac{C_{BE1} \cdot C_{load}}{C_{BE1} + C_{load}} + C_{B1} + C_{BC1}$$

$$\frac{dV_X}{dt} = \frac{I_{D,p}}{C_X}$$

Consider  $C_{BE1}$ ,  $C_{load}$  branch,

$$i = C_{BE1} \cdot \frac{dV_{BE1}}{dt} = \frac{C_{BE1} \cdot C_{load}}{C_{BE1} + C_{load}} \cdot \frac{dV_x}{dt}$$

$$\frac{dV_{BE1}}{dt} = \frac{C_{load}}{C_{BE1} + C_{load}} \cdot \frac{dV_X}{dt}$$

$$\frac{dV_{BE1}}{dt} = I_{D,p} \cdot \frac{C_{load}}{C_{BE1} + C_{load}} \cdot \frac{1}{\frac{C_{BE1} \cdot C_{load}}{C_{BE1} + C_{load}} + C_{B1} + C_{BC1}}$$

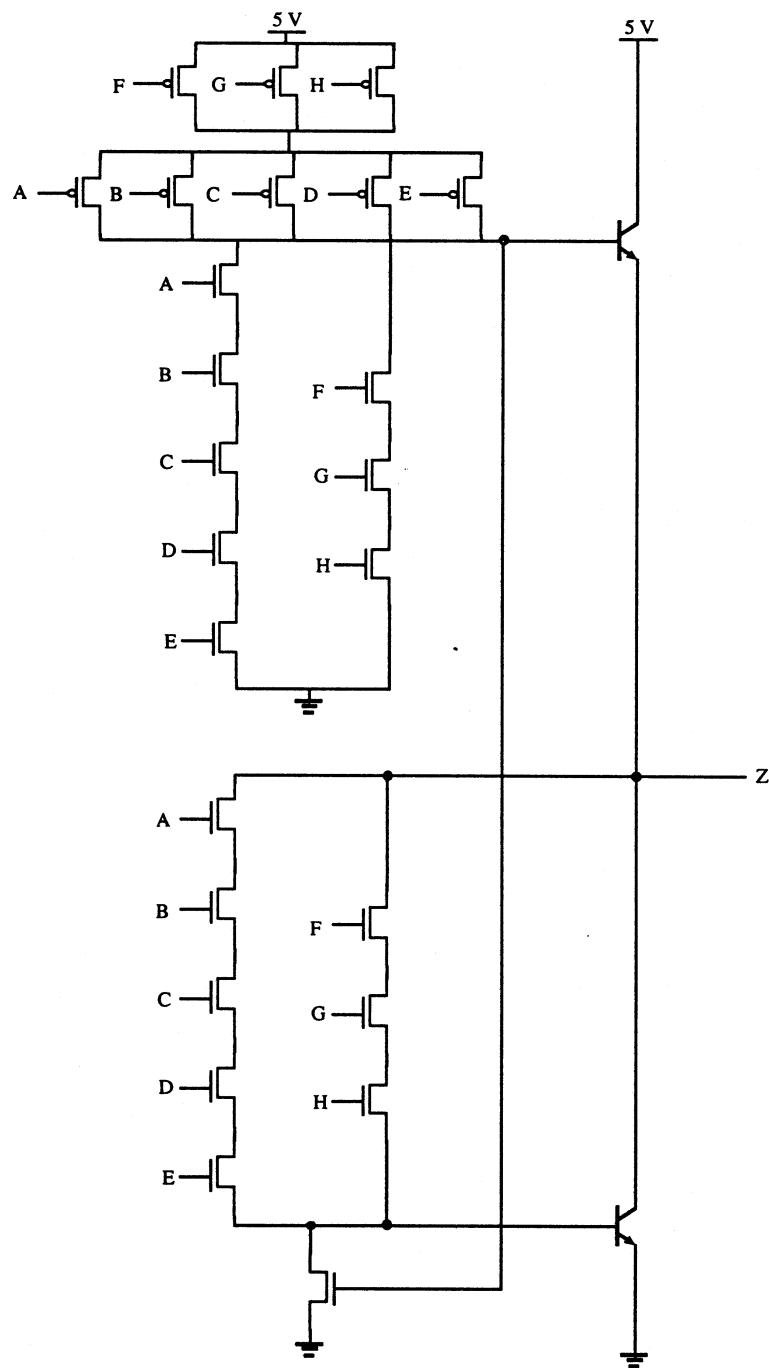
$$\frac{dV_{BE1}}{dt} = I_{D,p} \cdot \frac{C_{load}}{C_{load} \cdot C_{BE1} + (C_{B1} + C_{BC1})(C_{BE1} + C_{load})}$$

**12.6** Consider a logic gate for the following boolean function  $Z = \overline{ABCDE + FGH}$ .

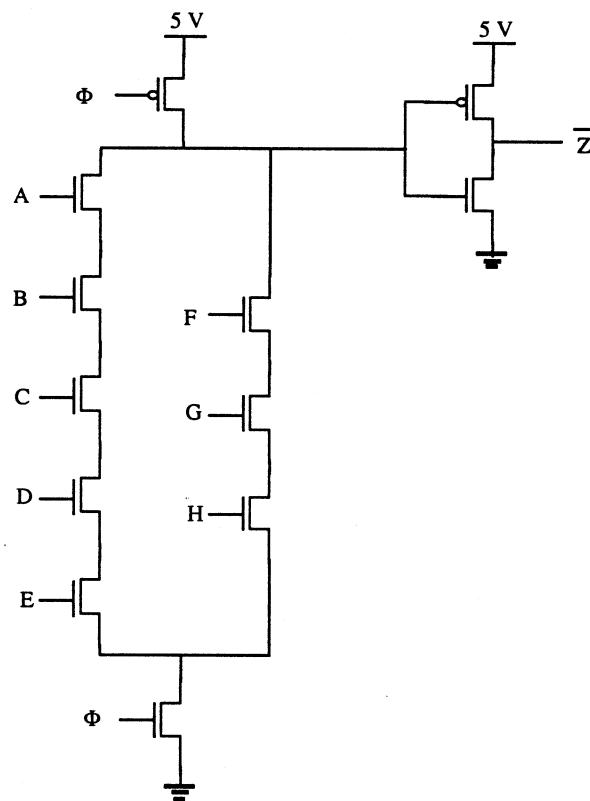
- (a) Design a BiCMOS circuit to implement the boolean function Z.
- (b) Design a domino CMOS circuit to implement the boolean function  $\overline{Z}$ .
- (c) Compare the pros and cons of the BiCMOS over the domino CMOS implementation.

**SOLUTION:**

- (a). BiCMOS circuit implementation:



(b). domino CMOS implementation:



(c). BiCMOS circuit is faster but uses more area. Domino circuit saves area but is slower.

**12.7** For the bipolar transistor shown in Fig.P12.7, use the following parameters and neglect any junction capacitances.

- $I_{ES} = 10^{-16} \text{ A}$
- $I_{CS} = 2 \times 10^{-16} \text{ A}$
- $\alpha_F = 0.98$
- $\alpha_R = 0.49$
- $\tau_F = 0.2 \text{ ns}$
- $\tau_R = 20 \text{ ns}$

- Use the Ebers-Moll equations to find  $I_B$ ,  $I_E$ , and  $I_C$  before and (long) after the transition.
- Use the simplified charge-control equations to sketch  $V_B$  as a function of time. Include values for all important voltages and time intervals on the graph.

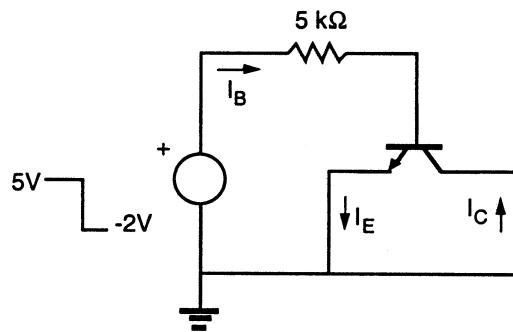


Figure P12.7

**SOLUTION:**

(a). Since  $V_{CE}=0$ ,

$$V_{BC} = V_{BE} = V_B$$

From equations (12.5), (12.6) and the circuit configuration, we have:

$$\begin{aligned} I_B &= I_E - I_C \\ &= I_{ES}(e^{V_B/V_T} - 1) - \alpha_R I_{CS}(e^{V_B/V_T} - 1) - \alpha_F I_{ES}(e^{V_B/V_T} - 1) + I_{CS}(e^{V_B/V_T} - 1) \\ I_B &= \frac{V_{in} - V_B}{5k\Omega} = I_{ES}(e^{V_B/V_T} - 1)(1 - \alpha_F) + I_{CS}(e^{V_B/V_T} - 1)(1 - \alpha_R) \end{aligned}$$

When  $V_{in}=+5V$ , the transistor is saturated, using given data,

$$\frac{5 - V_B}{5k\Omega} = 1.04 \times 10^{-16} e^{V_B/V_T}$$

iterate and find,

$$V_B = 0.7729V$$

Using the above equations, we obtain:

$$\begin{aligned} I_B &= 0.845mA \\ I_E &= 0.016mA \\ I_C &= -0.829mA \end{aligned}$$

When  $V_{in}=-2V$ , the transistor is cut-off,

$$\begin{aligned} I_E &= -I_{ES} + \alpha_R I_{CS} = -2 \times 10^{-18} A \\ I_C &= -\alpha_F I_{ES} + I_{CS} = 1.02 \times 10^{-16} A \\ I_B &= I_E - I_C = -1.04 \times 10^{-16} A \\ I_B &= \frac{-2 - V_B}{5000} = -1.04 \times 10^{-16} A \\ V_B &= -2 V \end{aligned}$$

(b). Since  $V_{BE}=V_{BC}$ , the transistor operates in saturation region and cut-off region. In saturation region, from equation (12.58)

$$i_B = \frac{Q_F}{\tau_{BF}} + \frac{Q_R}{\tau_{BR}} + \frac{d}{dt}(Q_F + Q_R)$$

$$i_C = \frac{Q_F}{\tau_F} - Q_R \left( \frac{1}{\tau_R} + \frac{1}{\tau_{BR}} \right) - \frac{dQ_R}{dt}$$

$$\tau_{BF} = \beta_F \cdot \tau_F = \frac{\alpha_F}{1 - \alpha_F} \cdot \tau_F = \frac{0.98}{1 - 0.98} \cdot 0.2 = 9.8 \text{ ns}$$

$$\tau_{BR} = \beta_R \cdot \tau_R = \frac{\alpha_R}{1 - \alpha_R} \cdot \tau_R = \frac{0.49}{1 - 0.49} \cdot 20 = 19.2 \text{ ns}$$

at steady state,

$$\frac{dQ_F}{dt} = 0$$

$$\frac{dQ_R}{dt} = 0$$

$$0.845 \times 10^{-3} = \frac{Q_F}{9.8 \times 10^{-9}} + \frac{Q_R}{19.2 \times 10^{-9}}$$

$$-0.829 \times 10^{-3} = \frac{Q_F}{0.2 \times 10^{-9}} - Q_R \left( \frac{1}{20 \times 10^{-9}} + \frac{1}{19.2 \times 10^{-9}} \right)$$

Solve for  $Q_F$  and  $Q_R$ ,

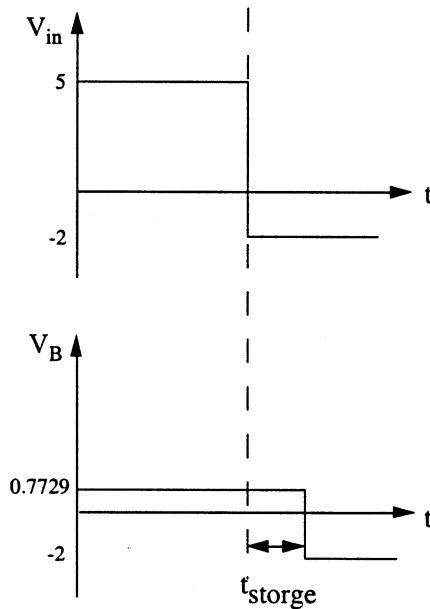
$$Q_F = 0.159 \times 10^{-12} \text{ Coulomb}$$

$$Q_R = 15.9 \times 10^{-12} \text{ Coulomb}$$

After transition, the base current is:

$$i_B = \frac{-2 - 0.7729}{5000} = -0.55 \text{ mA}$$

$$t_{storage} = -\frac{Q_B}{i_B} = -\frac{(Q_F + Q_R)}{i_B} = -\frac{0.159 + 15.9}{-0.55} \cdot \frac{10^{-12}}{10^{-3}} = 29.2 \text{ ns}$$



- 12.8** Compare the basic BiCMOS inverter and the basic BiNMOS inverter. Specifically, address voltage swing and propagation delay.

**SOLUTION:**

In basic BiCMOS inverter circuit, the voltage swing is from  $V_{DD} - V_{BE}$  to  $V_{BE}$ , but in basic BiNMOS inverter, the voltage swing is from  $V_{DD} - V_{BE}$  to 0 because there is no bipolar transistor in the pull-down path. Pull-up delay should be the same, while the BiCMOS pull-down is faster.

- 12.9** Use the following parameters for your calculations, assuming the emitter junction is an abrupt junction and the collector junction is a gradual junction:

- $V_{BE(on)} = 0.7 \text{ V}$
- $V_{BE(sat)} = 0.8 \text{ V}$
- $V_{CE(sat)} = 0.1 \text{ V}$
- $\tau_F = 0.2 \text{ ns}$
- $\tau_{BF} = 15 \text{ ns}$
- $\tau_S = 20 \text{ ns}$
- $C_{je0} = 0.5 \text{ pF}$  (emitter junction capacitance at zero bias)
- $C_{jc0} = 0.25 \text{ pF}$  (collector junction capacitance at zero bias)
- $\phi_e = 0.9 \text{ V}$
- $\phi_c = 0.7 \text{ V}$

- (a) For the bipolar inverter shown in Fig.P12.9a, calculate the DC transfer characteristics (*i.e.*,  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ ,  $V_{IL}$ ,  $NM_H$ ,  $NM_L$ ). Repeat for the circuit shown in Fig. P12.9b.
- (b) For the circuit shown in Fig. P12.9a, use hand calculations to solve for  $t_{PLH}$  and  $t_{PHL}$ . Repeat for the circuit shown in Fig.P12.9b. Describe how the pull-down resistor at the base affects propagation delay.
- (c) Compare your calculations for both circuits with SPICE results. Note: run SPICE to simulate both DC and transient responses.
- (d) For the circuit shown in Fig.P12.9a, let  $R_C = 0$ . Calculate the size of the optimum speed-up capacitor to be placed in parallel with  $R_B$  to minimize the propagation delay (neglect charge due to junction capacitance). Repeat for the circuit shown in Fig.P 12.9b.

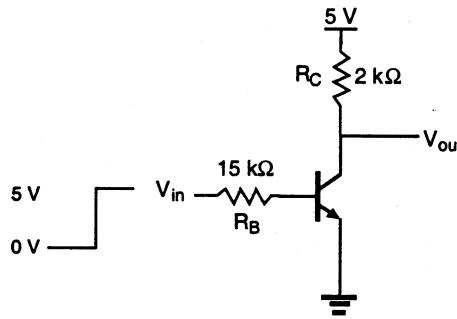


Figure P12.9a

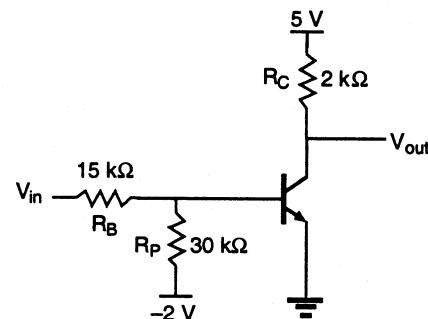


Figure P12.9b

### SOLUTION:

(a)

(i) Circuit of Figure P12.9a:

At  $V_{IL}$ , the transistor is cut-off,

$$V_{IL} = V_{BE(on)} = 0.7 \text{ V}$$

$$V_{OL} = V_{CE(sat)} = 0.1 \text{ V}$$

$$V_{OH} = 5 \text{ V}$$

At  $V_{IH}$ , the transistor is at the edge of saturation and forward active region, therefore,

$$I_C = \frac{V_{DD} - V_{CE(sat)}}{R_C} = \frac{5 - 0.1}{2k} = 2.45 \text{ mA}$$

$$\beta_F = \frac{\tau_{BF}}{\tau_F} = \frac{15}{0.2} = 75$$

$$I_B = \frac{I_C}{\beta_F} = \frac{2.45 \text{ mA}}{75} = 32.67 \mu\text{A}$$

$$V_{IH} = I_{RB} \cdot R_B + V_{BE(sat)} = 32.67 \times 10^{-6} \cdot 15 \times 10^3 + 0.8 = 1.29 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.7 - 0.1 = 0.6 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5 - 1.29 = 3.71 \text{ V}$$

(ii) Circuit of Figure P12.9b:

First, we need to find out whether  $V_B$  is limited by resistor or transistor. Supposed the transistor does not exist, then,

$$V_{B,max} = \frac{5 - (-2)}{R_B + R_P} \cdot R_P - 2 = \frac{7}{45} \cdot 30 - 2 = 2.67 \text{ V}$$

With the transistor present,

$$V_{B,max} = V_{BE(sat)} = 0.8 \text{ V}$$

which means that the transistor can saturate. Let  $I_{RP}$  be the current through resistor  $R_p$ ,  $I_{RB}$  be the current through resistor  $R_B$ .  $V_{IL}$  is found when the transistor is at the edge of turning on and that,

$$V_B = 0.7 \text{ V}$$

$$I_{RB} = I_{RP} = \frac{0.7 - (-2)}{30k\Omega} = 90 \mu\text{A}$$

$$V_{IL} = V_{BE(on)} + I_{RB} \cdot R_B = 0.7 + 90 \times 10^{-3} \cdot 15 = 2.05 \text{ V}$$

$$V_{OL} = V_{CE(sat)} = 0.1 \text{ V}$$

At the edge of saturation,  $I_C$  and  $I_B$  are the same as in case (i),

$$I_{RP} = \frac{0.8 - (-2)}{R_p} = \frac{2.8}{30k\Omega} = 93.3 \mu\text{A}$$

$$I_{RB} = I_B + I_{RP} = 32.67 + 93.3 = 126 \mu\text{A}$$

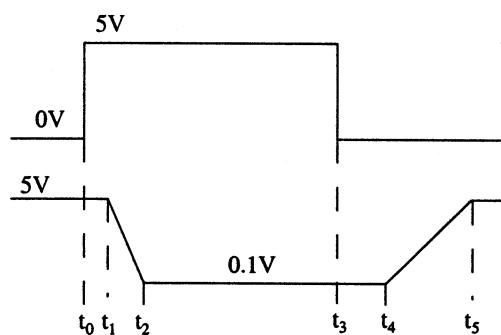
$$V_{IH} = I_{RB} \cdot R_B + V_{BE(sat)} = 126 \times 10^{-3} \times 15 + 0.8 = 2.69 \text{ V}$$

$$V_{OH} = 5 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 2.05 - 0.1 = 1.95 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 5 - 2.69 = 2.31 \text{ V}$$

(b). Circuit a:



The above figure shows the input and output waveforms.

(1) Region  $\tau_1$ :

In this region, the junction capacitances  $C_{je}$  and  $C_{jc}$  are charged from 0V to 0.7V. The average base current during this period is found as:

$$i_{B,avg} = \frac{1}{2} \left( \frac{5-0}{R_B} + \frac{5-0.7}{R_B} \right) = \frac{1}{2} \left( \frac{5+5-0.7}{15k} \right) = 0.31 \text{ mA}$$

The total charge change in emitter and collector region can be represented by:

$$\begin{aligned}\Delta Q_{BE} &= \Delta V_{BE} \cdot C_{je,eq} \\ \Delta Q_{BC} &= \Delta V_{BC} \cdot C_{jc,eq}\end{aligned}$$

the equivalent capacitances can be calculated using the same method as in MOSFETs.

$$\begin{aligned}C_{je,eq} &= -\frac{C_{jeo} \cdot \phi_e}{\Delta V_{BE}(1-m_e)} \left\{ \left( 1 - \frac{V_{BE}(t_1)}{\phi_e} \right)^{1-m_e} - \left( 1 - \frac{V_{BE}(t_0)}{\phi_e} \right)^{1-m_e} \right\} \\ &= -\frac{0.5 \text{ pF} \cdot 0.9}{0.7(1-0.5)} \left\{ \left( 1 - \frac{0.7}{0.9} \right)^{0.5} - 1 \right\} = 0.68 \text{ pF}\end{aligned}$$

$$\begin{aligned}C_{jc,eq} &= -\frac{C_{jco} \cdot \phi_c}{\Delta V_{BC}(1-m_c)} \left\{ \left( 1 - \frac{V_{BC}(t_1)}{\phi_c} \right)^{1-m_c} - \left( 1 - \frac{V_{BC}(t_0)}{\phi_c} \right)^{1-m_c} \right\} \\ &= -\frac{0.25 \text{ pF} \cdot 0.7}{0.7(1-0.33)} \left\{ \left( 1 - \frac{-4.3}{0.7} \right)^{2/3} - \left( 1 - \frac{-5}{0.7} \right)^{2/3} \right\} = 0.127 \text{ pF}\end{aligned}$$

The total charge change due to junction capacitance charging is

$$\begin{aligned}\Delta Q_{jct} &= \Delta Q_{BE} + \Delta Q_{BC} = \Delta V_{BE} \cdot C_{je,eq} + \Delta V_{BC} \cdot C_{jc,eq} \\ &= 0.7 \cdot (0.68 + 0.127) = 0.565 \text{ pC}\end{aligned}$$

$$\tau_1 = \frac{\Delta Q_{jct}}{i_{B,avg}} = \frac{0.565}{0.31} = 1.82 \text{ ns}$$

(2) Transistor turns on and reaches the edge of saturation.

$$\begin{aligned}V_B(t_1) &= 0.7 \text{ V}, \quad V_C(t_1) = 5 \text{ V} \\ V_B(t_2) &= 0.8 \text{ V}, \quad V_C(t_2) = 0.1 \text{ V}\end{aligned}$$

$$\Delta Q_F = Q_F(t_2) - Q_F(t_1)$$

$$\because I_C(t_1) = 0$$

$$\therefore Q_F(t_1) = 0$$

$$Q_F(t_2) = I_C(t_2) \cdot \tau_F = \frac{5-0.1}{2k} \cdot 0.2 = 0.49 \text{ pC}$$

$$\begin{aligned}\Delta Q_{jE} &= C_{je,eq} \cdot \Delta V_{BE} = -\frac{0.5 \times 0.9}{(0.8-0.7) \times 0.5} \times \left\{ \left( 1 - \frac{0.8}{0.9} \right)^{1/2} - \left( 1 - \frac{0.7}{0.9} \right)^{1/2} \right\} \times 0.1 \\ &= 0.1243 \text{ pC}\end{aligned}$$

$$\Delta Q_{jc} = C_{jc, eq} \cdot \Delta V_{BC} = -\frac{0.25 \times 0.7}{(0.7 - (0.7 - 5)) \times 2/3} \times \left\{ \left(1 - \frac{0.7}{0.7}\right)^{2/3} - \left(1 + \frac{4.3}{0.7}\right)^{2/3} \right\} \times 5 \\ = 0.975 \text{ pC}$$

$$\Delta Q = \Delta Q_F + \Delta Q_{jE} + \Delta Q_{jC} = 0.49 + 0.1243 + 0.975 = 1.589 \text{ pC}$$

Integrate equation (12.57) base current equation, we reach

$$\int_{t_1}^{t_2} i_{B, avg} dt = \frac{1}{\tau_{BF}} \int_{t_1}^{t_2} Q_F(t) dt + \Delta Q \\ i_{B, avg} = \frac{i_B(t_2) + i_B(t_1)}{2} = \frac{1}{2} \left( \frac{5 - 0.8}{2k} + \frac{5 - 0.7}{2k} \right) = 0.2833 \text{ mA} \\ \frac{1}{\tau_{BF}} \int_{t_1}^{t_2} Q_F(t) dt = (t_2 - t_1) \frac{1}{2\tau_{BF}} (Q_F(t_1) + Q_F(t_2)) \\ = (t_2 - t_1) \frac{1}{2 \times 15} 0.49 = 0.0163 \text{ mA} \\ t_2 - t_1 = \frac{1.589}{0.2833 - 0.0163} = 5.95 \text{ ns} \\ \tau_{PHL} = t_1 + \frac{t_2 - t_1}{2} = 4.795 \text{ ns}$$

(3) Time to remove excess charge QS from the base. Transistor goes from saturation to edge of saturation.

$$t_4 - t_3 = t_s = \tau_s \ln \frac{i_{BF} - i_{BR}}{\frac{i_{C(EOS)}}{\beta_F} - i_{BR}} \\ i_{BF} = \frac{5 - 0.8}{15k} = 0.296 \text{ mA} \\ i_{BR} = \frac{0 - 0.8}{15k} = -0.053 \text{ mA} \\ I_{C(EOS)} = \frac{5 - 0.1}{2k} = 2.45 \text{ mA} \\ t_s = 20 \times 1.355 = 27.1 \text{ ns}$$

(4) Transistor turns off. It goes from edge of saturation to edge of forward active and then to edge of cut-off. The situation is analogous to that during turn-on.

$$i_B(t_4) = \frac{0 - 0.8}{15k} = -0.053 \text{ mA} \\ i_B(t_5) = \frac{0 - 0.7}{15k} = -0.0467 \text{ mA} \\ i_{B, avg} = \frac{1}{2} (i_B(t_4) + i_B(t_5)) = -50 \mu\text{A}$$

$$\int_{t_4}^{t_5} i_{B,avg} dt = \frac{1}{\tau_{BF}} \int_{t_4}^{t_5} Q_F(t) dt + \Delta Q_F + \Delta Q_{jE} + \Delta Q_{jC}$$

$$t_5 - t_4 = \frac{1.589}{0.05 + \frac{0.49}{2\tau_{BF}}} = 23.95 \text{ ns}$$

$$\tau_{PLH} = t_s + \frac{t_5 - t_4}{2} = 39.1 \text{ ns}$$

(b). Circuit b:

(1) Time t0 to time t1: charging junction capacitance:

$$I_{RB} = I_B + I_{RP}$$

$$V_{in} = I_{RB} \cdot R_B + I_{RP} \cdot R_P - 2$$

therefore, when  $V_{in} = 5 \text{ V}$

$$I_B = \frac{5 - (-2) - 45k \cdot I_{RP}}{15k}$$

$$I_{RP} = \frac{V_B + 2}{R_P}$$

The voltages are listed here:

$$V_B(t_0) = \frac{-2}{15k + 30k} \cdot 15k = -0.667 \text{ V}$$

$$V_B(t_1) = 0.7 \text{ V}$$

$$V_C(t_1) = V_C(t_0) = 5 \text{ V}$$

$$\Delta V_{BE} = \Delta V_{BC} = 0.7 + 0.667 = 1.37 \text{ V}$$

$$I_{RP}(t_0) = \frac{-0.667 + 2}{30k} = 44.4 \mu\text{A}$$

$$I_B(t_0) = \frac{7 - 45k \cdot 44.4 \mu}{15k} = 333 \mu\text{A}$$

$$I_{RP}(t_1) = \frac{0.7 + 2}{30k} = 90 \mu\text{A}$$

$$I_B(t_0) = \frac{7 - 45k \cdot 90 \mu}{15k} = 196.67 \mu\text{A}$$

$$I_{B,avg} = 265 \mu\text{A}$$

Using the same equations for Figure (a),

$$\begin{aligned} C_{je,eq} &= -\frac{C_{jeo} \cdot \phi_e}{\Delta V_{BE}(1-m_e)} \left\{ \left( 1 - \frac{V_{BE}(t_1)}{\phi_e} \right)^{1-m_e} - \left( 1 - \frac{V_{BE}(t_0)}{\phi_e} \right)^{1-m_e} \right\} \\ &= -\frac{0.5 \text{ pF} \cdot 0.9}{1.37(1-0.5)} \left\{ \left( 1 - \frac{0.7}{0.9} \right)^{0.5} - \left( 1 + \frac{0.67}{0.9} \right)^{0.5} \right\} = 0.56 \text{ pF} \end{aligned}$$

$$C_{jc,eq} = -\frac{C_{jco} \cdot \phi_c}{\Delta V_{BC}(1-m_c)} \left\{ \left(1 - \frac{V_{BC}(t_1)}{\phi_c}\right)^{1-m_c} - \left(1 - \frac{V_{BC}(t_0)}{\phi_c}\right)^{1-m_c} \right\}$$

$$= -\frac{0.25 \text{ pF} \cdot 0.7}{1.37(1-0.33)} \left\{ \left(1 - \frac{-4.3}{0.7}\right)^{2/3} - \left(1 - \frac{-5.67}{0.7}\right)^{2/3} \right\} = 0.12 \text{ pF}$$

$$\Delta Q_j = \Delta V_{BE} \cdot C_{je,eq} + \Delta V_{BC} \cdot C_{jc,eq} = 1.37(0.56 + 0.12) = 0.93 \text{ pC}$$

(2) From t1 to t2, the transistor goes from EOC to EOS.

$$\Delta Q_F = Q_F(t_2) - Q_F(t_1)$$

$$Q_F(t_1) = 0, \quad Q_F(t_2) = \frac{5 - 0.1}{2k} = 0.49 \text{ pC}$$

$$V_B(t_1) = 0.7 \text{ V}, \quad V_B(t_2) = 0.8 \text{ V}$$

$$V_C(t_1) = 5 \text{ V}, \quad V_C(t_2) = 0.1 \text{ V}$$

$$\Delta V_{BE} = 0.1 \text{ V}, \quad \Delta V_{BC} = 5 \text{ V}$$

Since the conditions are the same as in the other case,

$$\Delta Q_{jE} = 0.1243 \text{ pC}, \quad \Delta Q_{jC} = 0.975 \text{ pC}$$

Using the same IB equations as in case (1)

$$I_{B,avg} = \frac{I_B(t_1) + I_B(t_2)}{2} = 191.67 \mu\text{A}$$

$$\Delta t = t_2 - t_1 = \frac{0.49 + 0.124 + 0.975}{(191.67 - 16.33)} \cdot \frac{\text{pC}}{\mu\text{A}} = 9.06 \text{ ns}$$

so,

$$\tau_{PHL} = t_1 + \frac{t_2 - t_1}{2} = 3.5 + 4.5 = 8 \text{ ns}$$

(3) Time t3 to time t4, transistor goes from saturation to EOS:

$$i_{BF} = i_B(t_2) = 186.67 \mu\text{A}$$

$$i_{BR} = -\left(\frac{0.8}{15k} + \frac{2.8}{30k}\right) = -146.67 \mu\text{A}$$

$$t_s = 12.4 \text{ ns}$$

(4) From time t3 to time t4, EOS to EOC,

$$i_B(t_4) = -\left(\frac{0.8}{15k} + \frac{2.8}{30k}\right) = -146.67 \mu\text{A}$$

$$i_B(t_5) = -\left(\frac{0.7}{15k} + \frac{2.7}{30k}\right) = -136.67 \mu\text{A}$$

$$i_{B,avg} = -141.67 \mu\text{A}$$

$$t_5 - t_4 = -\frac{1.589}{141.67 + 16.33} = 10.06 \text{ ns}$$

$$\tau_{PLH} = t_S + \frac{t_5 - t_4}{2} = 17.4 \text{ ns}$$

$R_p$  speeds up  $\tau_{PLH}$  considerably though  $\tau_{PLH}$  is degraded.

d)

(i) Circuit (a).

$$i_C = \frac{Q_F}{\tau_F} = \frac{C(V - V_{BE, on})}{\tau_F}$$

$$i_C = \beta \cdot i_B = \beta \frac{V - V_{BE, on}}{R_B} = \frac{\tau_{BF}}{\tau_F} \left( \frac{V - V_{BE, on}}{R_B} \right)$$

$$C = \frac{\tau_{BF}}{R_B} = \frac{15}{15} = 1 \text{ pF}$$

(ii) Circuit (b)

$$Q_F = C(V_2 - V_1) = C\Delta V$$

$$V_1 = 0 - (-0.667) = 0.667 \text{ V}$$

$$V_1 = 5 - V_{BE, on} = 4.3 \text{ V}$$

$$i_C = \frac{Q_F}{\tau_F} = \beta \cdot I_B = \frac{\tau_{BF}}{\tau_F} I_B = \frac{C\Delta V}{\tau_F}$$

$$C = \frac{\tau_{BF} \cdot I_B}{\Delta V}$$

$$I_{RB} = I_{RP} + I_B$$

$$I_{RP} = \frac{2.7}{30k} = 90 \mu\text{A}$$

$$5 = I_{RB} R_B + V_{BE, on} = (I_B + 90 \mu\text{A}) R_B + V_{BE, on}$$

$$I_B = \frac{4.3}{15k} - 90 \mu\text{A} = 196.67 \mu\text{A}$$

$$C = \frac{15 \text{ ns} \cdot 196.67 \mu\text{A}}{4.3 - 0.667} = 0.81 \text{ pF}$$

- 12.10 Calculate the  $t_{PLH}$  and  $t_{PHL}$  for the BiCMOS gate shown in Figure 12.20. Assume that charging of the MOSFET's parasitic capacitances can be neglected. Use the following parameters for MOSFETs and BJTs. Ignore the bias dependencies of the capacitances. Explain any simplifying assumptions that you make.

- $V_{CC} = 5 \text{ V}$
- $V_{BE(on)} = 0.7 \text{ V}$
- $V_{TO} = 0.8 \text{ V}$
- $k'_n = 200 \mu\text{A/V}^2$
- $k'_p = 100 \mu\text{A/V}^2$
- $\beta_F = 100$
- $C_{je} = 20 \text{ fF}$
- $C_{jc} = 22 \text{ fF}$
- $C_L = 0.5 \text{ pF}$
- $(W/L)_p = 6$
- $(W/L)_n = 3$
- $r_C = 75 \Omega$

### SOLUTION:

Assume that the delay is only due to the turn-on of one BJT not the turn-off of the other BJT. That is to select transistor MB1 and MB2, assume they only act to quickly shut off a BJT.

$$t_{PLH} = t_{d,Q1} + \frac{C_L(V_{CC}/2 + V_{BE(on)})}{I_{avg}}$$

$$t_{d,Q1} = \frac{\Delta Q_{jE} + \Delta Q_{jC}}{i_{B,avg}}$$

$$i_{B,avg} = I_{MP} = \frac{6 \cdot 100 \mu}{2} (-5 + 0.8)^2 = 5.3 \text{ mA}$$

$$\Delta Q_{jE} = 0.7 \times 20 f = 14 \text{ fC}$$

$$\Delta Q_{jC} = 0.7 \times 22 f = 15.4 \text{ fC}$$

$$t_{d,Q1} = \frac{14 + 15.4}{5.3} = 5.5 \text{ ps}$$

For capacitor charging,

$$I_{B,avg} = [5.3 \text{ mA} + 6 \times 100 \mu \text{A} \times (-5 + 0.8 + 1.25)(-2.5)]/2 = 4.86 \text{ mA}$$

Since the BJT operates in saturation region,

$$I_{C,max} = \frac{5 - 0.1 - (V_{CC}/2 - V_{BE(on)})}{r_C} = \frac{5 - 0.1 - 1.8}{75} = 41.33 \text{ mA}$$

$$I_E = I_{avg} = I_B + I_C = 4.86 + 41.33 = 46.2 \text{ mA}$$

$$t_{PLH} = 5.5 + \frac{C_L \cdot \Delta V}{I_{avg}} = 5.5 \text{ pS} + \frac{0.5 \text{ pF} \times 1.8}{46.2 \text{ mA}} = 25 \text{ pS}$$

We notice that the delay is very small. It was designed to operate in the GHz region.

(ii) High to low delay calculation:

$$t_{d,Q2} = \frac{\Delta Q_{jE} + \Delta Q_{jC}}{i_{B,avg}}$$

$$i_{B,avg} = \frac{3 \times 200\mu}{2} (5 - 0.8)^2 = 5.3 \text{ mA}$$

For capacitance charging,,

$$I_{avg} = I_{C2} = I_{C,sat} = 41.33 \text{ mA}$$

$$t_{PLH} = 5.5 + \frac{C_L \cdot \Delta V}{I_{avg}} = 5.5 \text{ pS} + \frac{0.5 \text{ pF} \times 1.8}{41.33 \text{ mA}} = 27.3 \text{ pS}$$

## CHAPTER 13

### INPUT/OUTPUT CIRCUITS

- 13.1** For low-power design, multiple power supply voltages may be used on a chip by using on-chip voltage converters. A chip may take in 5-V power supply and then in turn generate and use 3.3-V power rails besides 5-V power rails. Design a level shifter which can interface 3.3-V logic with 5-V logic circuit. Use  $|V_{T0}| = 1.0$  V,  $\mu_n/\mu_p = 3$  in your calculation.

**SOLUTION:**

The worst case output signal levels are:

$$V_{OL} = 0 \text{ V}$$

$$V_{OH} = 3.3 \text{ V}$$

Therefore the inverter threshold voltage should be set at 1.65V.

From equation (13.4), assume channel lengths are the same for both pMOS and nMOS.

$$\frac{W_n}{W_p} = \frac{\mu_p}{\mu_n} \left[ \frac{V_{DD} + V_{T,p} - V_{th}}{V_{th} - V_{T,n}} \right]^2 = 3 \left[ \frac{5 - 1 - 1.65}{1.65 - 1} \right]^2 \approx 40$$

- 13.2** The distribution of clock signals without clock skew is usually desirable in order to lessen the design complexity. However, in some cases, clock skews can be utilized to resolve very tight timing budget problems. Find an example wherein clock skews can be utilized.

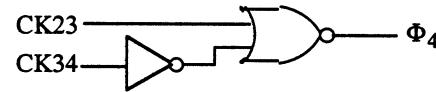
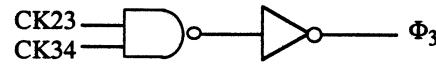
**SOLUTION:**

Clock skew can be used for setup time. In a tight timing budget, if there is no clock skew, then setup requirement may not be met.

- 13.3** Design a clock decoder circuit which generates four clock phases from two primary clock signals.

**SOLUTION:**

Using the primary clock signals given in Figure 13.20, the following decoder circuits can generate four clock phases  $\Phi_1$ ,  $\Phi_2$ ,  $\Phi_3$  and  $\Phi_4$ .



**13.4** Since the fanout count of a typical clock signal is very high, it is important to size the interconnection wire dimensions properly. The parasitic interconnection resistance and capacitance are discussed in Chapter 6 using formulas in (6.34), (6.36), and (6.37). The parasitic resistance in metallic wire is assumed to be  $0.03\Omega/\text{square}$ .

- For  $t = 0.4 \mu\text{m}$ ,  $h = 1 \mu\text{m}$ ,  $l(\text{length}) = 1000 \mu\text{m}$  and  $w(\text{width}) = 2 \mu\text{m}$ . Calculate the interconnection delay for fanout capacitance load of  $5 \text{ pF}$  by using the Elmore delay formula. For consideration of distributed parasitic effect, the total length can be divided into 10 segments of  $100\text{-}\mu\text{m}$  length.
- Verify the answer in part (a) using SPICE simulation.

#### SOLUTION:

Assume the total parasitic capacitance is  $C_{\text{total}}$  and the total parasitic resistance is  $R_{\text{total}}$ , the capacitance in each segment is  $C$  and the resistance in each segment is  $R$ , then the Elmore delay formula is:

$$\tau_{\text{delay}} = C_L \cdot R_{\text{total}} + C \cdot 10R + C \cdot 9R + C \cdot 8R + \dots + C \cdot R$$

$$\tau_{\text{delay}} = C_L \cdot R_{\text{total}} + C \cdot 55R = C_L \cdot R_{\text{total}} + \frac{55}{100} C_{\text{total}} \cdot R_{\text{total}}$$

From equation (6.34)

$$R_{\text{total}} = R_{\text{sheet}} \left( \frac{l}{w} \right) = 0.03 \times \frac{1000}{2} = 15 \Omega$$

From equation (6.36)

$$C_{total} = \epsilon \cdot l \cdot \left[ \frac{w - \frac{t}{2}}{h} + \frac{2\pi}{\ln \left( 1 + \frac{2h}{t} + \sqrt{\frac{2h}{t} \left( \frac{2h}{t} + 2 \right)} \right)} \right]$$

Thus the total delay is:

$$\tau_{delay} = R_{sheet} \frac{l}{w} \left( C_L + \frac{55}{100} \epsilon \cdot l \cdot \left[ \frac{w - \frac{t}{2}}{h} + \frac{2\pi}{\ln \left( 1 + \frac{2h}{t} + \sqrt{\frac{2h}{t} \left( \frac{2h}{t} + 2 \right)} \right)} \right] \right)$$

$$\tau_{delay} = 15 \left( 0.5p + \frac{55}{100} \times \epsilon_0 \times 3.9 \times 0.1 \left[ \frac{2 - 0.2}{1} + \frac{2\pi}{\ln(1 + 5 + \sqrt{35})} \right] \right) = 8.73 \text{ ps}$$

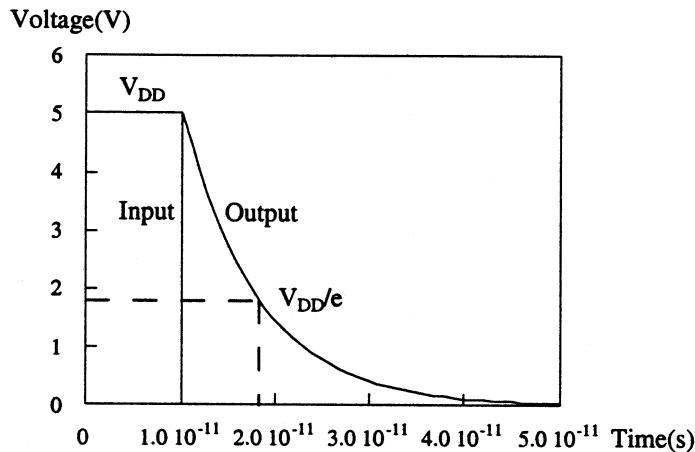
(b). SPICE Simulation.

Input list of a 10 segments RC network is shown below.

```
RC network delay calculation:
.subckt net 1 2
r 1 2 1.5
c 2 0 8.23f
.ends net
x1 1 2 net
x2 2 3 net
x3 3 4 net
x4 4 5 net
x5 5 6 net
x6 6 7 net
x7 7 8 net
x8 8 9 net
x9 9 10 net
x10 10 11 net
c1 11 0 0.5p
vin 1 0 dc pulse (5 0 10p 0 0 50p 100p)
.tran 0.01p 50p
.print tran v(1) v(11)
.end
```

SPICE simulation results:

$$t_{delay} = (1.88 - 1.0) \times 10^{-11} = 8.8 \text{ ps}$$



- 13.5** The bonding pads in I/O circuits are implemented in topmost metal layer with a dimension of  $75\mu\text{m} \times 75\mu\text{m}$ . If the separation of the topmost metal layer with  $\text{SiO}_2$  from the common substrate layer (ground plane) is  $1\mu\text{m}$ ,

- (a) What is the parasitic capacitance of the bonding pad?
- (b) What is the total parasitic capacitance of the bonding pad node if it is connected to a CMOS inverter gate ( $W_p = 10\ \mu\text{m}$ ,  $W_n = 5\ \mu\text{m}$ ,  $L_M = 1\ \mu\text{m}$ ,  $t_{ox} = 500\ \text{\AA}$ ) and also to the output of a tristatable buffer ( $W_p = 1000\ \mu\text{m}$ ,  $W_n = 500\ \mu\text{m}$ ,  $L_M = 1\ \mu\text{m}$ ).

The other dimension of the drains is  $3\mu\text{m}$  and the parasitic capacitance in the drain is  $C_{jo} = 0.3\ \text{fF}/\mu\text{m}^2$ ,  $C_{jsw} = 0.5\ \text{fF}/\mu\text{m}$ .

#### SOLUTION:

- (a). The bonding pad parasitic capacitance is:

$$C_{pad} = \frac{\epsilon_{ox}}{t_{sep}} Area = \frac{3.9 \times 8.85 \cdot 10^{-14}}{1.0 \times 10^{-4}} (75 \times 10^{-4})^2 = 0.19\ \text{pF}$$

where  $t_{sep}$  is the separation of the topmost metal layer from the common substrate layer.

- (b). The total capacitance would be the three kind of capacitances in parallel, thus

$$C_{total} = C_{pad} + C_{gate} + C_{buf}$$

where  $C_{pad}$  is calculated in (a),  $C_{gate}$  is the gate to substrate capacitance and  $C_{buf}$  is the junction capacitance of the tristate buffer.

$$C_{gate} = C_{gate,n} + C_{gate,p} = C_{ox}(W_n L_M + W_p L_M)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$C_{gate} = \frac{\epsilon_{ox}}{t_{ox}} L_M (W_n + W_p) = \frac{3.9 \cdot 8.85 \times 10^{-14}}{500 \cdot 10^{-8}} 1 \times 10^{-4} \cdot (5 + 10) \times 10^{-4} = 10.35\ \text{fF}$$

$$C_{buf} = C_{buf,n} + C_{buf,p} = C_{j0}(AD_p + AD_n)K_{eq} + C_{jsw}(PD_p + PD_n)K_{eq,sw}$$

note, this is the worst case estimation of the junction capacitance, so  $K_{eq} = K_{eq,sw} = 1$ .

$$\begin{aligned} C_{buf} &= C_{j0}(AD_p + AD_n) + C_{jsw}(PD_p + PD_n) \\ &= 0.3 \times 10^{-15}(1000 \times 3 + 500 \times 3) + 0.5 \times 10^{-15}(2006 + 1006) \\ &= 2.856 \text{ pF} \end{aligned}$$

$$C_{total} = 0.19 + 2.856 + 0.010 = 3.056 \text{ pF}$$

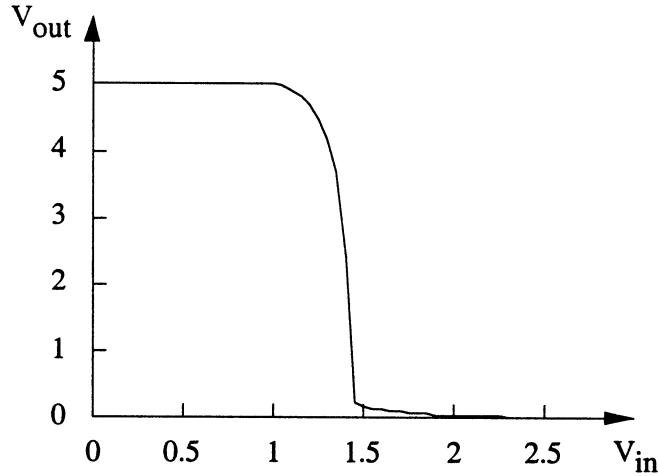
**13.6 Verify the correctness of the TTL to CMOS level shifter by SPICE simulation.**

**SOLUTION:**

The SPICE input list is as follows:

```
TTL to CMOS level shifter DC analysis
m1 2 1 0 0 mn w=169u l=1u
m2 2 1 5 5 mp w=12u l=1u
c1 2 0 0.01p
vdd 5 0 dc 5.0
vin 1 0 dc 0
.model mn nmos (vto=1.0 kp=60u gamma=0.)
.model mp pmos (vto=-1.0 kp=20u gamma=0.)
.dc vin 0 5 0.05
.print dc v(2)
.end
```

The resulting voltage transfer curve is:



The SPICE simulation gives:

$$\begin{aligned} V_{IL} &= 1.08 \text{ V} \\ V_{IH} &= 1.45 \text{ V} \end{aligned}$$

- 13.7** The transistors in the final stage of the chip output buffer are usually chosen to be huge in order to provide sufficient current driving capability. Discuss the layout strategy for implementing such huge transistors in the bonding pad area.

**SOLUTION:**

Usually, the multi-finger structure is used for these huge transistors. The multi-finger nMOS transistors also provide ESD/EOS protection.

- 13.8** The switching noise in the power and ground rails of the chip output driver circuit can be very large to the extent that it may upset the logic level of nearby internal circuits due to coupled noise. Discuss whether this problem can be avoided with use of separate power and ground rails for I/O circuits (noisy) and internal circuits (quiet).

**SOLUTION:**

Decoupling the power supply lines to I/O and internal circuits may not completely eliminate the ringing and noise on the power supply lines. The problem may still occur if there is sufficient coupling capacitance between the dirty and clean  $V_{DD}$  and  $V_{SS}$  lines. This is specially true for very high speed futuristic technologies.

- 13.9** The bonding wire inductance is 2 nH, load capacitance is 100 pF, and the 50% switching delay time is 5 ns.
- Estimate the maximum  $L(di/dt)$  noise.
  - Explain how this noise would change at lower operating temperature and higher power supply voltage.
  - Calculate the total noise voltage peaks when 32 such output pads are switching simultaneously and when 32 output pads are switching with 3.2 ns skew from the first bit to the last bit.
  - Verify your results using proper models and SPICE simulation.

**SOLUTION:**

(a). Assume the output circuit current peaks at 50% delay point. Therefore,

$$t_s = 10 \text{ ns}$$

From equation (12.7)

$$L \left[ \frac{di}{dt} \right]_{max} \geq \frac{4C_{load}V_{DD}}{t_s^2}$$

The maximum noise is

$$L \left[ \frac{di}{dt} \right]_{max} = \frac{4C_{load}V_{DD}}{t_s^2} L = \frac{4 \times 100 \times 10^{-12} \times 5 \times 2 \times 10^{-9}}{(10 \times 10^{-9})^2} = 40 \text{ mV}$$

(b). At very low operating temperature, the device mobility increase, therefore the noise voltage increases. It's obvious from the equation that higher power supply voltages cause higher noise.

(c).

(1).Simultaneous switching:

The total noise voltage would be the sum of 32 of the above.

$$L \left[ \frac{di}{dt} \right]_{max} \times 32 = 40 \times 32 = 1.28 \text{ V}$$

(2). Switching with 3.2ns skew.

Since the total delay from the first bit to the last bit is 3.2ns, the delay between each bit is therefore 0.1ns. Assume the noise voltage for each bit is represented by 'a'. Due to delay of 0.1ns between each bit, the total noise voltage can be calculated as:

$$\begin{aligned} V_{total} &= a + \left( a - \frac{0.1}{5}a \right) + \left( a - 2 \times \frac{0.1}{5}a \right) + \dots + \left( [n+1]a - [1+2+\dots+n] \frac{0.1}{5}a \right) \\ &= (n+1)a - \frac{n(n+1)}{2} \frac{0.1}{5}a \end{aligned}$$

For n=32 and a=40 mV

$$V_{total} = 33 \times 40 - \frac{32 \times 33}{2} \frac{0.1}{5} \times 40 = 897.6 \text{ mV}$$

- 13.10** Discuss how the sensitivity of the level shifting I/O circuit to process variations, especially the variation in the channel length, can be reduced by mask design of particular W/L values. Would you choose minimum L allowed ?

#### SOLUTION:

Choosing larger L value can reduce the sensitivity. For example, suppose that process variation is  $0.2\mu\text{m}$ . For  $W/L=10$ , if  $L=1\mu\text{m}$  and  $W=10\mu\text{m}$ , the sensitivity is 25% in the lower shift and 17% in the higher shift. However, if  $L=2\mu\text{m}$  and  $W=20\mu\text{m}$ , then the sensitivity is 11%.

- 13.11** Discuss the pros and cons of having pull-up and pull-down resistors connected to I/O pads in view of impedance matching in high-speed circuits.

#### SOLUTION:

Pros:

- Impedance matching is essential to prevent unwanted ringing due to reflections caused by transmission line effect with load mismatch.
- Impedance matching corresponds to maximum power transfer to the line by the driver.

Cons:

- The high impedance may slow down a high speed circuit unnecessarily.
- A direct path between  $V_{DD}$  and  $V_{SS}$  leads to increased power dissipation in the I/O circuit making it more susceptible to damage and reliability problems.

## Chapter 14

# DESIGN FOR MANUFACTURABILITY

**NOTE:** All solutions numbered **15.x** ( $x = 1$  through 15) on the following pages apply to exercise problems numbered **14.x** in the 3<sup>rd</sup> edition.

There are no changes in the content and ordering.

## CHAPTER 15

### DESIGN FOR MANUFACTURABILITY

- 15.1** Consider a simple RC circuit model for a point-to-point interconnect in CMOS chips. The 50% delay time for a step input pulse is

$$\tau_{50\%} = 0.38 R C$$

Both R and C values are subject to random fluctuations due to process variations.

- (a). Express the sensitivities of  $\tau_{50\%}$  with respect to R and C.
- (b). Express the percentage change in the delay in terms of percentage changes in both R and C values under the assumption that their values can vary independently.
- (c). Determine the largest delay increase possible due to  $\pm 10\%$  fluctuations in both R and C values.

**SOLUTION:**

- (a).The sensitivities can be found:

$$S_R^{\tau_{50\%}} = \frac{\partial \tau_{50\%}}{\partial R} = 0.38C$$

$$S_C^{\tau_{50\%}} = \frac{\partial \tau_{50\%}}{\partial C} = 0.38R$$

- (b).The percentage change:

$$\frac{\Delta \tau_{50\%}}{\tau_{50\%}} = \frac{\frac{\partial \tau_{50\%}}{\partial R} \Delta R + \frac{\partial \tau_{50\%}}{\partial C} \Delta C}{\tau_{50\%}} = \frac{0.38C\Delta R + 0.38R\Delta C}{0.38RC} = \frac{\Delta R}{R} + \frac{\Delta C}{C}$$

- (c).The largest delay increase is

$$\left. \frac{\Delta \tau_{50\%}}{\tau_{50\%}} \right|_{max} = \left| \frac{\Delta R}{R} \right| + \left| \frac{\Delta C}{C} \right| = 10\% + 10\% = 20\%$$

- 15.2** An empirically determined relationship between the bulk mobility of majority carriers and the doping level is

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left( \frac{N}{N_0} \right)^\alpha} [cm^2 / V.sec]$$

where  $\mu_{max} = 1360$ ,  $\mu_{min} = 92$ ,  $N_0 = 1.3 \times 10^{17} / cm^3$ ,  $\alpha = 0.91$  for electrons and the corresponding numbers for holes are 495, 48,  $6.3 \times 10^{16}$  and 0.76.

- (a). Express the sensitivity of the mobility  $\mu$  with respect to the doping level N.

- (b). Determine the percentage change in  $\mu$  for 10% change in doping level from the nominal value for electrons and holes, respectively.

**SOLUTION:**

(a).

$$S_N^\mu = \frac{d\mu}{dN} = -\frac{\alpha(\mu_{max} - \mu_{min})}{N_0^\alpha} \frac{N^{\alpha-1}}{\left(1 + \left(\frac{N}{N_0}\right)^\alpha\right)^2}$$

(b). The nominal value for N is  $N_0$ , thus

$$\frac{\Delta\mu}{\mu} = \left| \frac{\frac{d\mu}{dN} \Big|_{N=N_0} \Delta N}{\mu_{N_0}} \right| = \frac{\frac{\alpha(\mu_{max} - \mu_{min})}{N_0^\alpha} \frac{N_0^{\alpha-1}}{\left(1 + \left(\frac{N_0}{N_0}\right)^\alpha\right)^2} \Delta N}{\mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_0}{N_0}\right)^\alpha}} = \frac{\mu_{max} - \mu_{min}}{\mu_{max} + \mu_{min}} \frac{\alpha}{2} \frac{\Delta N}{N_0}$$

$$\left( \frac{\Delta\mu}{\mu} \right)_e = \frac{1360 - 92}{1360 + 92} \times \frac{0.91}{2} \times 10\% = 3.97\%$$

$$\left( \frac{\Delta\mu}{\mu} \right)_h = \frac{495 - 48}{495 + 48} \times \frac{0.76}{2} \times 10\% = 1.565\%$$

**15.3** The dependence of the mobility on temperature is determined empirically as

$$\mu(T) = \frac{\mu(300K)}{\left(\frac{T}{300}\right)^{1.5}}$$

- (a). Derive an expression for  $\Delta\mu/\mu$  in terms of  $\Delta T/T$ .  
 (b). Calculate the percentage change in  $\mu$  due to 5% increase in temperature from 300°K for  $\mu(300K) = 980 \text{ cm}^2/\text{V}\cdot\text{sec}$ .

**SOLUTION:**

(a).

$$\frac{\Delta\mu}{\mu} = \frac{\frac{d\mu}{dT} \Delta T}{\mu} = \frac{\mu(300K) \cdot \left(-\frac{3}{2}\right) \cdot \left(\frac{T}{300}\right)^{-5/2} \cdot \frac{1}{300} \cdot \Delta T}{\mu(300K) \cdot \left(\frac{T}{300}\right)^{-3/2}} = -\frac{3}{2} \cdot \frac{\Delta T}{T}$$

(b).

$$\left| \frac{\Delta\mu}{\mu} \right| = \left| -\frac{3}{2} \cdot \frac{\Delta T}{T} \right| = 1.5 \times 5\% = 7.5\%$$

**15.4** Let us consider the device conductance parameter

$$k = \mu C_{ox} \frac{W}{L}$$

It is known that all four variables  $\mu$ ,  $C_{ox}$ ,  $W$  and  $L$  are random variables due to process variations.

- (a). Derive an expression for the percentage change in  $k$  due to percentage changes in  $\mu$ ,  $C_{ox}$ ,  $W$  and  $L$ .
- (b). If you assume that all four parameters change independently (corners technique), what would be the maximum percentage change expected due to 5% changes in all four parameters for nominal values of  $(\mu^o, C_{ox}^o, W^o, L^o) = (980 \text{ cm}^2/\text{V}\cdot\text{sec}, 35 \times 10^{-8} \text{ F/cm}^2, 5 \mu\text{m}, 1.0 \mu\text{m})$ ?

**SOLUTION:**

(a).

$$\begin{aligned} \frac{\Delta k}{k} &= \frac{\frac{\partial k}{\partial \mu} \Delta \mu + \frac{\partial k}{\partial C_{ox}} \Delta C_{ox} + \frac{\partial k}{\partial W} \Delta W + \frac{\partial k}{\partial L} \Delta L}{k} \\ \frac{\Delta k}{k} &= \frac{C_{ox} \frac{W}{L} \Delta \mu + \mu \frac{W}{L} \Delta C_{ox} + \mu C_{ox} \frac{1}{L} \Delta W + \mu C_{ox} W \left( -\frac{\Delta L}{L^2} \right)}{\mu C_{ox} \frac{W}{L}} \\ \frac{\Delta k}{k} &= \frac{\Delta \mu}{\mu} + \frac{\Delta C_{ox}}{C_{ox}} + \frac{\Delta W}{W} - \frac{\Delta L}{L} \end{aligned}$$

(b). The maximum percentage change would be:

$$\left| \frac{\Delta k}{k} \right| = \left| \frac{\Delta \mu}{\mu} \right| + \left| \frac{\Delta C_{ox}}{C_{ox}} \right| + \left| \frac{\Delta W}{W} \right| + \left| -\frac{\Delta L}{L} \right| = 4 \times 5\% = 20\%$$

**14.5** The logic threshold voltage  $V_{th}$  of a CMOS inverter from (5.87) is

$$V_{th} = \frac{V_{TO,n} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{1}{k_R}}}$$

where

$$k_R = \frac{k_n}{k_p} = \frac{\mu_n C_{ox} \frac{W_n}{L_n}}{\mu_p C_{ox} \frac{W_p}{L_p}}$$

- (a). Assuming that  $\mu_n = 2.5 \mu_p$ ,  $L_n = L_p$  for simplicity, derive an expression for the percentage change in  $V_{th}$  in terms of percentage change in  $V_{TO,n}$ ,  $V_{TO,p}$  and  $W_p/W_n$ .
- (b). For nominal values of  $V_{TO,n} = 0.8$  V,  $V_{TO,p} = -0.8$  V and  $W_p = 2.5W_n$ , determine the maximum (worst-case) deviation of  $V_{th}$  for a  $\pm 0.1$  V change in both  $V_{TO,n}$  and  $V_{TO,p}$ , and a  $\pm 15\%$  change in  $W_p/W_n$ .

### SOLUTION:

- (a). Under the giving conditions, the  $V_{th}$  can be expressed by:

$$V_{th} = \frac{V_{TO,n} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{1}{k_R}}} = \frac{V_{TO,n} + \sqrt{\frac{2W_p}{5W_n}}(V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{2W_p}{5W_n}}}$$

$$\frac{\Delta V_{th}}{V_{th}} = \frac{\frac{\partial V_{th}}{\partial V_{TO,n}} \Delta V_{TO,n} + \frac{\partial V_{th}}{\partial V_{TO,p}} \Delta V_{TO,p} + \frac{\partial V_{th}}{\partial (W_p/W_n)} \Delta (W_p/W_n)}{V_{th}}$$

$$\frac{\partial V_{th}}{\partial V_{TO,n}} = \frac{1}{1 + \sqrt{\frac{2W_p}{5W_n}}}$$

$$\frac{\partial V_{th}}{\partial V_{TO,p}} = \frac{\sqrt{\frac{2W_p}{5W_n}}}{1 + \sqrt{\frac{2W_p}{5W_n}}}$$

$$\frac{\partial V_{th}}{\partial (W_p/W_n)} = \frac{\frac{1}{5} \left( \frac{2W_p}{5W_n} \right)^{-1/2} [-V_{TO,n} + V_{DD} - V_{TO,p}]}{\left( 1 + \sqrt{\frac{2W_p}{5W_n}} \right)^2}$$

$$\begin{aligned} \frac{\Delta V_{th}}{V_{th}} &= \frac{\Delta V_{TO,n} / V_{TO,n}}{1 + \sqrt{\frac{2W_p}{5W_n} \left( \frac{V_{DD} + V_{TO,p}}{V_{TO,n}} \right)}} + \frac{\sqrt{\frac{2W_p}{5W_n}} \Delta V_{TO,p} / V_{TO,p}}{\frac{V_{TO,n}}{V_{TO,p}} + \sqrt{\frac{2W_p}{5W_n} \left( \frac{V_{DD}}{V_{TO,p}} + 1 \right)}} \\ &+ \frac{\frac{1}{5} (-V_{TO,n} + V_{DD} + V_{TO,p}) \cdot \Delta (W_p/W_n) / (W_p/W_n)}{\left[ V_{TO,n} + \sqrt{\frac{2W_p}{5W_n} (V_{DD} + V_{TO,p})} \right] \left[ 1 + \sqrt{\frac{2W_p}{5W_n}} \right] \sqrt{\frac{2}{5} \left( \frac{W_p}{W_n} \right)^{-1/2}}} \end{aligned}$$

(b). For nominal values, the maximum percentage change is:

$$\begin{aligned} \frac{\Delta V_{th}}{V_{th}} &= \left| \frac{0.1/0.8}{1 + \left( \frac{5-0.8}{0.8} \right)} \right| + \left| \frac{0.1/0.8}{-1 + \left( \frac{5}{-0.8} + 1 \right)} \right| + \left| \frac{\frac{1}{5} (-0.8 + 5 - 0.8) \cdot 15\%}{[0.8 + (5-0.8)](2) \sqrt{\frac{2}{5} \left( \frac{5}{2} \right)^{-1/2}}} \right| \\ \frac{\Delta V_{th}}{V_{th}} &= 0.02 + 0.02 + 0.0255 = 0.0655 = 6.55\% \end{aligned}$$

The maximum deviation of  $V_{th}$  is:

$$\Delta V_{th,max} = 6.55\% \times V_{th} = 6.55\% \times \frac{0.8 + 5 - 0.8}{2} = 0.164 \text{ V}$$

- 15.6** A CMOS chip with three signal input terminals, one output terminal, one power supply terminal and one ground terminal is presented to you. The input signal voltages can vary between 0 and 5 V, the power supply voltage can vary between 4.5V and 5.5V, and the device operating temperature can range from 0 °C to 85 °C. We want to design an experiment so that the DC response of the chip can be described by a quadratic response surface model for three inputs, power supply voltage and the temperature.
- (a) Design a full factorial experiment.
  - (b) Design a Latin hypercube experiment.
  - (c) Design Taguchi's orthogonal array.

### SOLUTION:

(a) The number of variables are 5 in this case. For a full factorial design, the number of runs is thus 32. The column  $i_1$ ,  $i_2$ , and  $i_3$  represent the three input signals. The design is shown in the following:

Run #	$i_1(V)$	$i_2(V)$	$i_3(V)$	$V_{DD}$	T(°C)	y(DC response)
1	0	0	0	4.5	0	y1
2	0	0	0	4.5	85	y2
3	0	0	0	5.5	0	y3
4	0	0	0	5.5	85	y4
5	0	0	5	4.5	0	y5
6	0	0	5	4.5	85	y6
7	0	0	5	5.5	0	y7
8	0	0	5	5.5	85	y8
9	0	5	0	4.5	0	y9
10	0	5	0	4.5	85	y10
11	0	5	0	5.5	0	y11
12	0	5	0	5.5	85	y12
13	0	5	5	4.5	0	y13
14	0	5	5	4.5	85	y14
15	0	5	5	5.5	0	y15
16	0	5	5	5.5	85	y16
17	5	0	0	4.5	0	y17
18	5	0	0	4.5	85	y18
19	5	0	0	5.5	0	y19
20	5	0	0	5.5	85	y20
21	5	0	5	4.5	0	y21
22	5	0	5	4.5	85	y22
23	5	0	5	5.5	0	y23
24	5	0	5	5.5	85	y24
25	5	5	0	4.5	0	y25
26	5	5	0	4.5	85	y26
27	5	5	0	5.5	0	y27
28	5	5	0	5.5	85	y28
29	5	5	5	4.5	0	y29
30	5	5	5	4.5	85	y30
31	5	5	5	5.5	0	y31
32	5	5	5	5.5	85	y32

(b) The algorithm is described here.

Suppose N is the number of runs of LHS. Assume each input is independent and uniformly distributed. Divide the range of each input into N non-overlapping intervals.

For each input variable  $x_i$  {  
     select N samples randomly from each interval  
 }  
 then randomly gain the N values of  $x_1$  and  $x_2$ , and so on to obtain LHS.

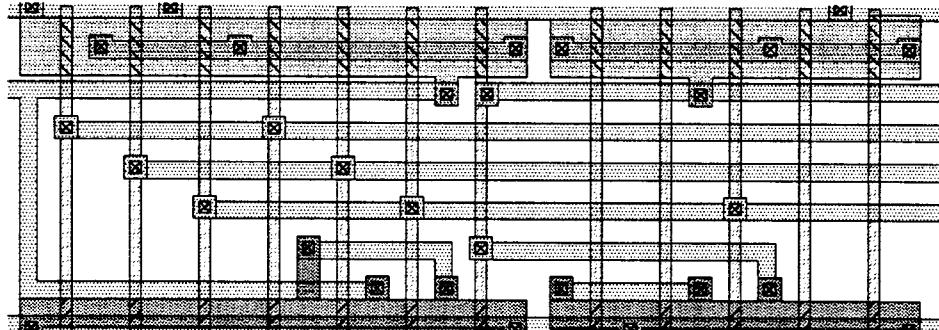
(c) Using a L16 orthogonal array for 5 parameters and 4-level, the design is shown in the following. (Ref. "Taguchi Methods Applications in World Industry" by A. Bendell, J. Disney, and W.A.Pridmore. IFS Publications). For input signals the four levels are 0V, 1.5V, 3V, and 5V. For power supply voltage, the four levels used are 4.5V, 4.8V, 5.2V, and 5.5V. For temperature, we use 0°C, 30°C, 60°C, and 85°C.

Run	$i_1$ (V)	$i_2$ (V)	$i_3$ (V)	$V_{DD}$	T(°C)	y(DC response)
1	0	0	0	4.5	0	y1
2	0	1.5	1.5	4.8	30	y2
3	0	3	3	5.2	60	y3
4	0	5	5	5.5	85	y4
5	1.5	0	1.5	5.2	85	y5
6	1.5	1.5	0	5.5	60	y6
7	1.5	3	5	4.5	30	y7
8	1.5	5	3	4.8	0	y8
9	3	0	3	5.5	30	y9
10	3	1.5	5	5.2	0	y10
11	3	3	0	4.8	85	y11
12	3	5	1.5	4.5	60	y12
13	5	0	5	4.8	60	y13
14	5	1.5	3	4.5	85	y14
15	5	3	1.5	5.5	0	y15
16	5	5	0	5.2	30	y16

- 15.7 Design a CMOS full adder circuit and its layout using  $W/L = 5/2$  for nMOS transistors and  $W/L = 10/2$  for pMOS transistors. For a capacitive load of 1 pF, determine the worst-case delay of your particular design when the range of power supply variations is 4.5 V to 5.5V and the operating temperature ranges from 25 °C to 85 °C. Also assume that the magnitude ranges of the threshold voltages are from 0.8 V to 1.2 V for both transistor types. All other parameters are assumed to be at their nominal values in this problem.

## SOLUTION:

The layout of the CMOS full adder circuit is shown below:



The worst case delay occurs when the power supply voltage is 4.5 V, the operating temperature is 85 °C, and the magnitude of threshold voltages are 1.2 V for both pMOS and nMOS. SPICE simulation input list is shown. The plot shows the delay in the case when inputs A = 0, B = 1, and C is switching. The delay found from the simulation is:

$$t_{PHL} = 4.3 \text{ ns}$$

$$t_{PLH} = 5.2 \text{ ns}$$

SPICE input list:

### CMOS full adder circuit

```

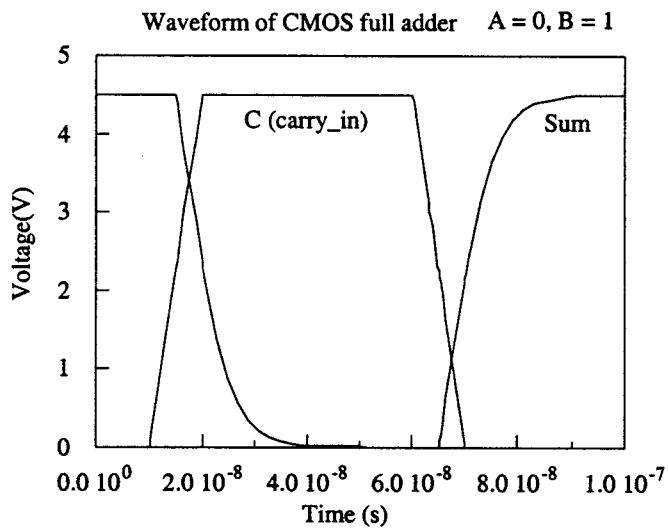
mn1 3 1 0 0 mn w=5u l=2u
mn2 3 2 0 0 mn w=5u l=2u
mn3 6 4 3 0 mn w=5u l=2u
mn4 5 2 0 0 mn w=5u l=2u
mn5 6 1 5 0 mn w=5u l=2u
mn6 9 6 0 0 mn w=5u l=2u
mn7 10 1 0 0 mn w=5u l=2u
mn8 10 2 0 0 mn w=5u l=2u
mn9 10 4 0 0 mn w=5u l=2u
mn10 11 6 10 0 mn w=5u l=2u
mn11 11 1 13 0 mn w=5u l=2u
mn12 13 2 12 0 mn w=5u l=2u
mn13 12 4 0 0 mn w=5u l=2u
mn14 17 11 0 0 mn w=5u l=2u
mp1 7 1 8 20 mp w=10u l=2u
mp2 6 2 7 20 mp w=10u l=2u
mp3 6 4 8 20 mp w=10u l=2u
mp4 8 2 20 20 mp w=10u l=2u
mp5 8 1 20 20 mp w=10u l=2u

```

```

mp6 9 6 20 20 mp w=10u l=2u
mp7 15 1 16 20 mp w=10u l=2u
mp8 14 2 15 20 mp w=10u l=2u
mp9 11 4 14 20 mp w=10u l=2u
mp10 11 6 16 20 mp w=10u l=2u
mp11 16 1 20 20 mp w=10u l=2u
mp12 16 2 20 20 mp w=10u l=2u
mp13 16 4 20 20 mp w=10u l=2u
mp14 17 11 20 20 mp w=10u l=2u
cl 17 0 1.0p
vdd 20 0 dc 4.5
va 1 0 dc 0
vb 2 0 dc 4.5
vc 4 0 dc pulse (0 4.5 10n 10n 10n 40n 100n)
.model mn nmos (vto=1.2 kp=40u gamma=0)
.model mp pmos (vto=-1.2 kp=20u gamma=0)
.options temp=85
.tran 1n 100n
.print tran v(4) v(17)
.end

```



**15.8** Determine the worst-case power dissipation for the design in Problem 15.7.

**SOLUTION:**

The worst case power dissipation for the design is when the power supply voltage is 5.5 V, the temperature is 85 °C, and the threshold voltages are 0.8 V in magnitude for both pMOS and nMOS. The power meter SPICE simulation input list is shown

below. For each pMOS transistor that is connected to  $V_{DD}$ , we assigned a power meter. The total power dissipation is the sum of power of each of these transistors. The total simulated average power for  $T = 100$  ns is 0.34 mW. The simulated power dissipation for the last stage is plotted.

SPICE input list for power meter simulation:

```

CMOS full adder power estimation

mn1 3 1 0 0 mn w=5u l=2u
mn2 3 2 0 0 mn w=5u l=2u
mn3 6 4 3 0 mn w=5u l=2u
mn4 5 2 0 0 mn w=5u l=2u
mn5 6 1 5 0 mn w=5u l=2u
mn6 9 6 0 0 mn w=5u l=2u
mn7 10 1 0 0 mn w=5u l=2u
mn8 10 2 0 0 mn w=5u l=2u
mn9 10 4 0 0 mn w=5u l=2u
mn10 11 6 10 0 mn w=5u l=2u
mn11 11 1 13 0 mn w=5u l=2u
mn12 13 2 12 0 mn w=5u l=2u
mn13 12 4 0 0 mn w=5u l=2u
mn14 17 11 0 0 mn w=5u l=2u
mp1 7 1 8 20 mp w=10u l=2u
mp2 6 2 7 20 mp w=10u l=2u
mp3 6 4 8 20 mp w=10u l=2u
mp4 8 2 24 20 mp w=10u l=2u
mp5 8 1 25 20 mp w=10u l=2u
mp6 9 6 26 20 mp w=10u l=2u
mp7 15 1 16 20 mp w=10u l=2u
mp8 14 2 15 20 mp w=10u l=2u
mp9 11 4 14 20 mp w=10u l=2u
mp10 11 6 16 20 mp w=10u l=2u
mp11 16 1 211 20 mp w=10u l=2u
mp12 16 2 212 20 mp w=10u l=2u
mp13 15 4 213 20 mp w=10u l=2u
mp14 17 11 214 20 mp w=10u l=2u

cl 17 0 1.0p

vtstp4 20 24 dc 0
fp4 0 104 vtstp4 0.0055
rp4 104 0 100k
cp4 104 0 100p

vtstp5 20 25 dc 0
fp5 0 105 vtstp5 0.0055
rp5 105 0 100k
cp5 105 0 100p

vtstp6 20 26 dc 0

```

```

fp6 0 106 vtstp6 0.0055
rp6 106 0 100k
cp6 106 0 100p

vtstp11 20 211 dc 0
fp11 0 111 vtstp11 0.0055
rp11 111 0 100k
cp11 111 0 100p

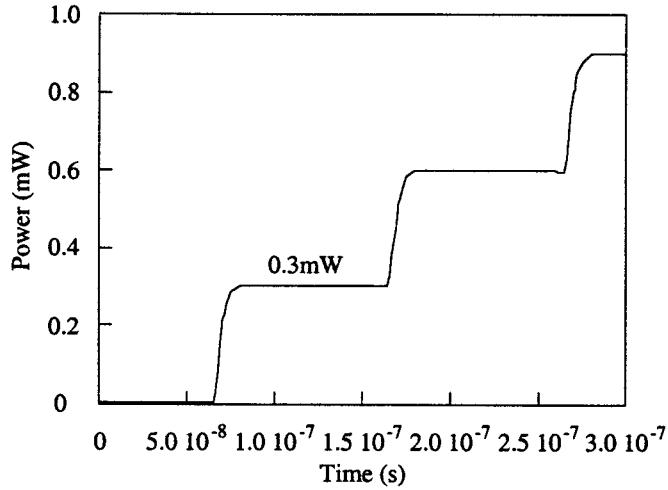
vtstp12 20 212 dc 0
fp12 0 112 vtstp12 0.0055
rp12 112 0 100k
cp12 112 0 100p

vtstp13 20 213 dc 0
fp13 0 113 vtstp13 0.0055
rp13 113 0 100k
cp13 113 0 100p

vtstp14 20 214 dc 0
fp14 0 114 vtstp14 0.0055
rp14 114 0 100k
cp14 114 0 100p

vdd 20 0 dc 5.5
va 1 0 dc 0
vb 2 0 dc 5.5
vc 4 0 dc pulse (0 5.5 10n 10n 10n 40n 100n)
.model mn nmos (vto=0.8 kp=40u gamma=0)
.model mp pmos (vto=-0.8 kp=20u gamma=0)
.options temp=85
.tran in 300n
.print tran v(104) v(105) v(106)
.print tran v(111) v(112) v(113) v(114)
.print tran v(4) v(17)
.end

```



- 15.9 Suppose that the noise parameters are jointly Gaussian. The joint probability density function of a Gaussian random vector  $\mathbf{s}$  with mean  $\mathbf{s}^o$  and variance/covariance matrix  $\mathbf{Q}$  is given by

$$f(\mathbf{s}) = \frac{1}{(\sqrt{2\pi})^{n_s} (\sigma_1 \sigma_2 \cdots \sigma_{n_s})} \exp\left[-\frac{1}{2}(\mathbf{s} - \mathbf{s}^o)^T \mathbf{Q}^{-1} (\mathbf{s} - \mathbf{s}^o)\right]$$

Consider the RC circuit model of Problem 15.1 with the performance measure being the 50% delay time  $\tau_{50\%}$ . Suppose  $R$  and  $C$  are independent Gaussian random variables.  $R$  has a mean of  $R^o = 10 \text{ K}\Omega$  and a standard deviation of  $\sigma_R = 1 \text{ K}\Omega$ .  $C$  has a mean of  $C^o = 10 \text{ pF}$  and a standard deviation of  $\sigma_C = 1 \text{ pF}$ . The worst-case direction for  $\tau_{50\%}$  is +1.

- (a). Determine the mean and standard deviation of  $\tau_{50\%}$ .
- (b).  $\tau_{50\%}$  is not a Gaussian random variable. To verify this, draw a Monte Carlo sample of  $R$  and  $C$ , use the formula given in Problem 15.1 to compute  $\tau_{50\%}$ , and plot the density of  $\tau_{50\%}$ . Compare the density to that of a Gaussian random variable having the mean and standard deviation of  $\tau_{50\%}$  that you computed in (a).
- (c). The worst-case value of  $\tau_{50\%}$  can be computed using the procedure for a non-Gaussian performance measure given in the discussion of worst-case analysis. Suppose the value is denoted by  $\tau_{50\%}^{wc}$ . To find the worst-case values of  $R$  and  $C$ , one must solve (15.31). Using the formula for the jpdf of a Gaussian random vector, reformulate the maximization of (15.31) into a minimization. The objective function for this minimization is called the "probabilistic distance". For this example, the minimization problem can be solved analytically using pencil and paper. Obtain the condition for minimization.
- (d). Use the fact that  $R^o = C^o$  and  $\sigma_R = \sigma_C$  to obtain  $R^{wc}$  and  $C^{wc}$  in terms of  $\tau_{50\%}^{wc}$ .

## SOLUTION:

(a)

The model given in 15.1 is written again here:

$$\tau = 0.38RC$$

The expected value is:

$$E[\tau] = E[0.38RC] = 0.38E[R] \cdot E[C] = 0.38R^oC^o = 38 \text{ ns}$$

$$V[\tau] = E[\tau^2] - E[\tau]^2 = 0.38^2 E[R^2] \cdot E[C^2] - E[\tau]^2$$

$$E[R^2] = \sigma_R^2 + R^o^2 = 1^2 + 10^2 = 101$$

$$E[C^2] = \sigma_C^2 + C^o^2 = 1^2 + 10^2 = 101$$

$$\sigma_\tau = \sqrt{V[\tau]} = \sqrt{0.38^2 \cdot 101^2 - 38^2} = \sqrt{29} = 5.39 \text{ ns}$$

(b) To solve this problem, one needs to write a computer program to generate the Monte Carlo sample of R and C and plot the density.

(c)

The problem is to maximize

$$\max_{R,C} f(R,C) = \frac{1}{2\pi\sigma_R\sigma_C} \exp\left[-\frac{1}{2}\left(\frac{R-R^o}{\sigma_R}\right)^2 - \frac{1}{2}\left(\frac{C-C^o}{\sigma_C}\right)^2\right]$$

subject to

$$0.38RC = \tau^{wc}$$

This is equivalent to minimize

$$\min_{R,C} \left( \frac{R-R^o}{\sigma_R} \right)^2 + \left( \frac{C-C^o}{\sigma_C} \right)^2$$

subject to

$$0.38RC = \tau^{wc}$$

$$L(R,C,\lambda) = \left( \frac{R-R^o}{\sigma_R} \right)^2 + \left( \frac{C-C^o}{\sigma_C} \right)^2 + \lambda(0.38RC - \tau^{wc})$$

$$\frac{\partial L}{\partial R} = 2\left(\frac{R-R^o}{\sigma_R}\right) \cdot \frac{1}{\sigma_R} + 0.38\lambda C = 0$$

$$\frac{\partial L}{\partial C} = 2\left(\frac{C-C^o}{\sigma_C}\right) \cdot \frac{1}{\sigma_C} + 0.38\lambda R = 0$$

$$\frac{\partial L}{\partial \lambda} = 0.38RC - \tau^{wc} = 0$$

Thus the conditions for the minimum is:

$$\frac{R - R^o}{\sigma_R} \cdot \frac{1}{\sigma_R} = \frac{C - C^o}{\sigma_C} \cdot \frac{1}{\sigma_C}$$

and

$$0.38RC = \tau^{wc}$$

(d)

From the given condition,

$$R^{wc} = C^{wc} = \sqrt{\tau^{wc} / 0.38}$$

- 15.10**
- (a) List the pros and cons of using the pessimistic worst-case analysis results in the design in view of parametric yield, design effort, and project schedule.
  - (b) Would the use of the simple-minded, pessimistic worst-case analysis technique such as the corners technique always shorten the development time?
  - (c) What can be the most serious problem that can be faced by the pessimistic analysis in a big project which involves many different organizations?

#### SOLUTION:

(a)

Pros of pessimistic worst-case analysis:

- High manufacturing yield if the design meets specifications under the pessimistic worst-case conditions.

Cons of pessimistic worst-case analysis:

- High design effort since it's difficult to meet specifications under pessimistic worst-case conditions. Sometimes it's impossible in view of conflicting requirements, e.g., area vs. delay trade-off.
- As a result, project schedule may suffer

(b)

No. Even though worst-case corners can be easily derived, much design effort may be required to meet the specifications under these conditions.

(c)

If every organization in the big project uses pessimistic analysis, the whole project may not be achieved given under certain design specifications.

- 15.11**
- Worst-case models even for the same circuit are different for different performances. For instance, the worst-case MOS model for delay time will be different from the worst-case MOS model for power dissipation. Yet, most design practices have been carried out using *slow*, *medium*, *fast* transistor models for both nMOS and pMOS transistors. Discuss how one would simulate the clock skew in a CMOS clock distribution circuit under such circumstances. What would be the correct way of

performing circuit simulation of clock skews, if the transistor models can be custom ordered by designers?

**SOLUTION:**

The clock skew can be simulated as shown in the following chart where different combinations of pMOS and nMOS models are used for each simulation and total of nine simulations are carried out under such circumstances.

<i>pMOS/nMOS</i>	<i>Slow</i>	<i>Medium</i>	<i>Fast</i>
<i>Slow</i>	<i>S/S</i>	<i>S/M</i>	<i>S/F</i>
<i>Medium</i>	<i>M/S</i>	<i>M/M</i>	<i>M/F</i>
<i>Fast</i>	<i>F/S</i>	<i>F/M</i>	<i>F/F</i>

The correct way of performing circuit simulation of clock skews would be to construct a quadratic response surface for the clock skew in terms of the transformed noise parameters.

- 15.12** Discuss the strategy for developing manufacturable specifications for chip processing in terms of required control on threshold voltages, variations in channel lengths and widths, gate oxide thickness, and substrate and tub doping profiles.

**SOLUTION:**

The strategy for developing manufacturable specifications lies in process simulation, design of experiments for process simulation, performing sensitivity studies with respect to key process steps. The process specifications are then determined such that the variations in threshold voltages, channel widths and lengths, gate oxide thickness, and substrate and tub doping profiles become manageable in view of yield and cost.

- 15.13** The so-called "throw-over-the-wall" approach overstrains the effort needed by the counterpart organization. Discuss how one can avoid such overstraining requirements with shared responsibility in order to make the whole technology development more cost effective?

**SOLUTION:**

In order to avoid overstraining requirements as evident in excessive guardbanding, multiple teams should not enforce the rigid organization boundaries. They should work closely for global optimization. For example, designers and device engineers can work jointly to develop layout rules optimal for both circuit layout, performance and chip fabrication. On the other hand, in over-the-wall type of approach, some layout rules can be made by device engineers unnecessarily costly in terms of chip area due to insufficient understanding of circuit functions.

- 15.14** The Taguchi's orthogonal array approach appeals to designers due to its simplicity; the design of experiment is readily available in a table form. Apply the L18 in MOS circuit design by using an example of your choice to demonstrate the principle of statistical design.

**SOLUTION:**

Suppose there is a four stage inverter chain circuit, the designable parameters are transistor sizes for each of the eight transistors. That's total of 8 parameters. Each transistor can have three different sizes corresponds three levels. Thus 18 runs can be done according to Taguchi's L18 orthogonal array shown on page 551 to calculate the delay.

- 15.15** From (15.31) and (15.32) derive the expression for the worst-case noise vector for two independent Gaussian random variables each with mean 0 and standard deviation of 1.

**SOLUTION:**

Suppose the worst case noise vectors are  $s_1$  and  $s_2$ , thus the problem is to minimize

$$s_1^2 + s_2^2$$

subject to:

$$r^{wc} = a + b_1 s_1 + b_2 s_2$$

Let

$$F = s_1^2 + s_2^2 + \lambda [r^{wc} - a - b_1 s_1 - b_2 s_2]$$

$$\frac{\partial F}{\partial s_1} = 2s_1 - \lambda b_1 = 0$$

$$\frac{\partial F}{\partial s_2} = 2s_2 - \lambda b_2 = 0$$

$$\frac{\partial F}{\partial \lambda} = r^{wc} - a - b_1 s_1 - b_2 s_2 = 0$$

$$s_1 = \frac{\lambda b_1}{2}$$

$$s_2 = \frac{\lambda b_2}{2}$$

$$r^{wc} - a - b_1 \frac{\lambda b_1}{2} - b_2 \frac{\lambda b_2}{2} = 0$$

$$\lambda = \frac{2(r^{wc} - a)}{b_1^2 + b_2^2}$$

## Chapter 15

# DESIGN FOR TESTABILITY

**NOTE:** All solutions numbered **16.x** ( $x = 1$  through 8) on the following pages apply to exercise problems numbered **15.x** in the 3<sup>rd</sup> edition.

There are no changes in the content and ordering.

## CHAPTER 16

### DESIGN FOR TESTABILITY

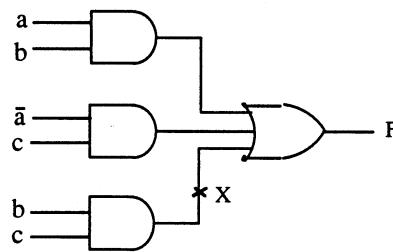
- 16.1** Give a logic circuit example in which stuck-at 1 fault and stuck-at 0 fault are indistinguishable.

**SOLUTION:**

In the circuit shown below, the output function is

$$F = ab + \bar{a}c$$

Thus the AND gate with b,c as input is redundant. So stuck-at 1 fault and stuck at 0 fault are indistinguishable at node X.



- 16.2** Show that the residue of LFSR in Figure 16.13 in the text is indeed  $R(x) = x^4+x^2$ .

**SOLUTION:**

Consider in Figure 16.13, from left to right, the D latches are named  $D_0$  to  $D_4$ . As shown in the table below, the input sequence  $\{1\ 1\ 1\ 1\ 0\ 1\ 0\ 1\}$  and the LFSR state is listed. The corresponding output sequence is  $\{0\ 0\ 0\ 0\ 0\ 1\ 0\ 1\}$ , and the register contents is  $\{1\ 0\ 1\ 0\ 0\}$

				$D_0$	$D_1$	$D_2$	$D_3$	$D_4$
1	0	1	0	1	1	1	0	0
1	0	1	0	1	1	1	0	0
1	0	1	0	1	1	1	0	0
1	0	1	0	1	1	1	0	0
1	0	1	0	1	1	1	1	0
1	0	1	0	0	1	1	1	1
1	0	0	0	0	0	1	0	
1	0	0	0	0	0	0	1	
0	0	1	0	1	0			

Thus the remainder term becomes  $R(x)=x^4+x^2$ .

- 16.3** Explain the merits or demerits of the bus structure in relation to the testability. How would it impact the chip area overhead?

**SOLUTION:**

Bus structure complicates the testing problem, but it essentially saves the chip area

- 16.4** Determine whether the leakage current test for chips should be done prior to or after the functional test. What can you say about the test frequency of chips containing dynamic circuits designed to operate at very high frequency? Can it fail the functional test at much lower frequency? If so, explain why.

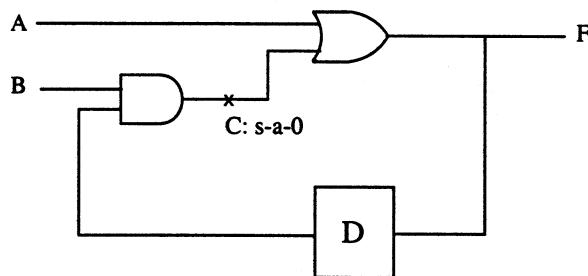
**SOLUTION:**

The leakage current test for chips should be done prior to functional test. If the chip fails the leakage current test, there is no need to do functional test anymore. The test frequency of chips containing dynamic circuits designed to operate at very high frequency should also be very high. This is because refreshing time is very short in this case. If the test frequency is too low, leakage may occur and thus causes functional fault. In real circuit operation, since the frequency is high, there will be no functional error due to leakage.

- 16.5** Show a few logic circuit examples whose logic fault coverage is dependent on the test vector sequence.

**SOLUTION:**

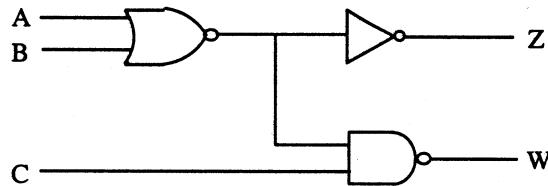
An example circuit is shown below with a D flip-flop, if the test vector sequence for A is {1,0} and B is {1,1}, then the s-a-0 fault at node C can be detected. If the test vector sequence for A is {0,1} and B is {1,1}, then the s-a-0 fault at node C can not be covered.



- 16.6** Find the set of all test vectors which detect the stuck-at-0 fault in line B in Figure 16.2. Repeat for stuck-at-1 fault in line C.

### SOLUTION:

The circuit is drawn in the following:



Test vectors for stuck-at-0 fault in line B:

$A = 0, B = 1, C = 0$  and  $A = 0, B = 1, C = 1$ . If  $Z = 0$ , then stuck-at-0 in line B.

Test vector for stuck-at-1 fault in line C:

$A = 0, B = 0, C = 0$ . If  $W = 0$ , then stuck-at-1 in line C.

- 16.7 Show that if there are undetectable stuck-at faults in a combinational circuit then the circuit can be reduced according to the following rules (the rule set for OR gates is given below; prove it and find the rules for AND, NOR, NAND, and XOR gates).

Undetectable Fault	Reduction Rule for OR Gates
Input $x_i$ s-a-0	Remove input $x_i$
Input $x_i$ s-a-1	Remove OR gate, connect output to 1
Output s-a-0	Remove OR gate, connect output to 0
Output s-a-1	Remove OR gate, connect output to 1

### SOLUTION:

Suppose for an n-input OR gate, the output F can be expressed as:

$$F = \sum_{j=1}^{j=n} X_j = \sum_{j=1}^{j=i-1} X_j + X_i + \sum_{j=i+1}^n X_j$$

Case1: Input  $X_i$  s-a-0

$$F = \sum_{j=1}^{j=n} X_j = \sum_{j=1}^{j=i-1} X_j + \sum_{j=i+1}^n X_j$$

This is the same as remove input  $X_i$ .

Case2: Input  $X_i$  s-a-1,

$$F = \sum_{j=1}^{j=n} X_j = \sum_{j=1}^{j=i-1} X_j + X_i + \sum_{j=i+1}^n X_j = 1$$

The output is always equal to 1. Thus, remove OR gate, connect output to 1.

Case3: Output s-a-0. Output is always connected to 0.

Case4: Output s-a-1. Output is always connected to 1.

Rules for AND gate:

Undetectable Fault	Reduction Rule for AND Gates
Input $x_i$ s - a - 0	Remove AND gate, connect output to 0
Input $x_i$ s - a - 1	Remove input $x_i$
Output s - a - 0	Remove AND gate, connect output to 0
Output s - a - 1	Remove AND gate, connect output to 1

Rules for NOR gate:

Undetectable Fault	Reduction Rule for NOR Gates
Input $x_i$ s - a - 0	Remove input $x_i$
Input $x_i$ s - a - 1	Remove NOR gate, connect output to 0
Output s - a - 0	Remove NOR gate, connect output to 0
Output s - a - 1	Remove NOR gate, connect output to 1

Rules for NAND gate:

Undetectable Fault	Reduction Rule for NAND Gates
Input $x_i$ s - a - 0	Remove NAND gate, connect output to 1
Input $x_i$ s - a - 1	Remove input $x_i$
Output s - a - 0	Remove NAND gate, connect output to 0
Output s - a - 1	Remove NAND gate, connect output to 1

Rules for XOR gate:

Undetectable Fault	Reduction Rule for XOR Gates
Input $x_i$ s - a - 0	Remove input $x_i$
Input $x_i$ s - a - 1	Remove input $x_i$ , add inverter to output
Output s - a - 0	Remove XOR gate, connect output to 0
Output s - a - 1	Remove XOR gate, connect output to 1

**16.8** Apply the rules in Problem 16.7 to the circuit shown in Fig.16.7.

**SOLUTION:**

Figure 16.7(a) shows an NAND gate with input s-a-1 fault. According to the rule, "Remove input  $x_i$ ", the circuit is reduced to Figure 16.7(b).