

06/01/2020

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Date _____

EC302: VLSI Design

Unit I Manufacturing Process (capacitance, resistance in circuit)
MOS transistor (large signal Model)

Unit II Scaling & small geometry effect
Wire & Electrical Wire

Unit III MOS inverter - static and transient characteristics
(DC) (AC)

Unit IV Combinational logic circuit - static
- Dynamic

Unit V Sequential logic Circuit

Unit VI Pulse Register -- VLSI Design Methodology

Delay / Bandwidth, Frequency of Circuit

MOS inverter \leq Noise Margin
Voltage Swinging
Delay

Books:

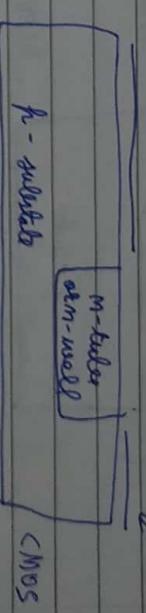
- CMOS Digital Integrated Circuits by Kang 3rd Edition
not 4th edition

- Digital Integrated Circuits by JM Rabaey

(for dynamic combinational
& Sequential)

CWS - (15) → 3 Paragraphs, 2 (Wt), Class Performance
 MTE - (20) ← (2x3) (3+4)
 PRS - (25) ← Numerical Based
 ETE - (10) ← (2)

hole performance
 8-10 steps → 1 mark each
 hole test → 2 marks
 Project → 8 marks



Masks → Photolithography (Photoresist or Electro Beam)

Photolithography

SiO_2 is first
Isolation

mask →



NMOS
making

Dry

Wet

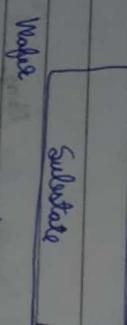
(for NMOS)
qualifying
thick layer

Photoresist put on oxide layer

oxide on
use for
NMOS
isolation

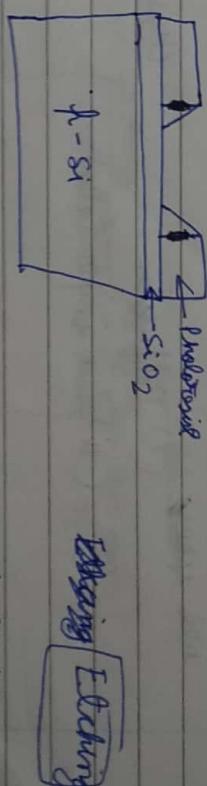
Photoresist

Single Crystalline Structure



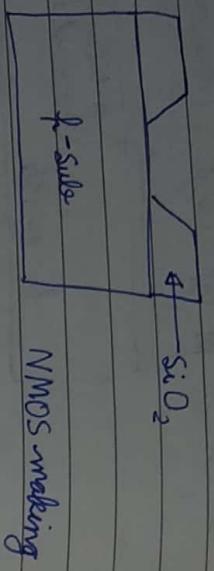
Wafer

Substrate



Etching
Etching

IC's are fabricated in
squares.



NMOS making

Device area defined on substrate
Pattern defined using SiO_2

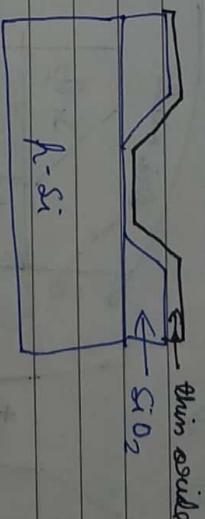
SiO_2 area is called active area.

Source, Drain, Gate to be made from NMOS device

Source → n-type

Drain → n-type
NMOS

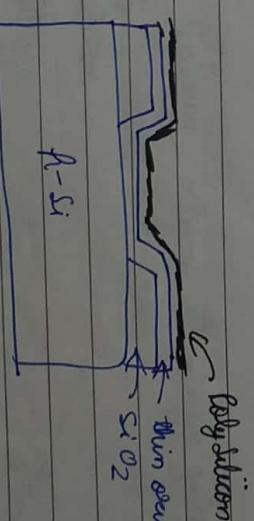
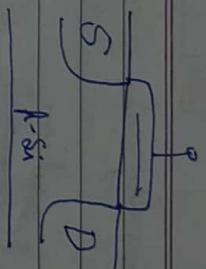
Gate →



(thin oxide)

Gate oxide to be made → Very oxidation
(thin oxide)

If substrate is small, difference
cannot be used. We then
use ion implantation.



Poly silicon used for gate. Deposited
(highly resistive)

For changing concentration (p-type to n-type)
we use

- (i) Diffusion, (High Temp)
- (ii) Ion implantation.

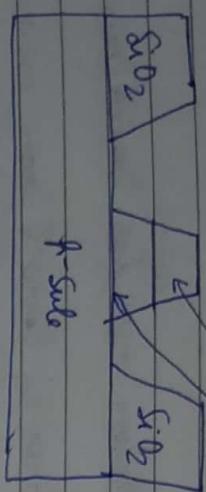
Noise starts shaking if SiO₂ is changed immediately
Annealing

Masking & Photolithography

halysin

SiO_2 layer again then photoresist, Mask applied.
Metalization done.

Mr. Redundant metal is etched



After Rattling
polyadion

卷二

Polymer is
doped with

conductivity ↑
heat loss
or melted

Masking again to make metal contact

needed to apply
nostalgia

#

Desire Isolation Techniques

Device isolation to be done here -

metals form galvanic cells
not always

NMOS making

8-4

8-4

2

۷۰

1

1

NW

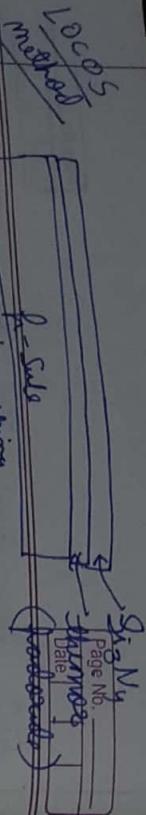
105

makur

B4

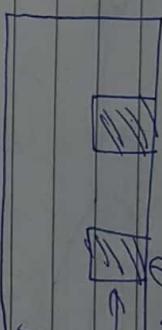
5

1



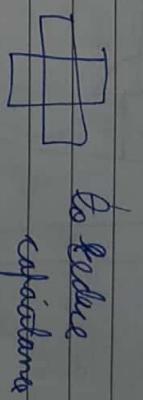
Search isolation

filled with oxide



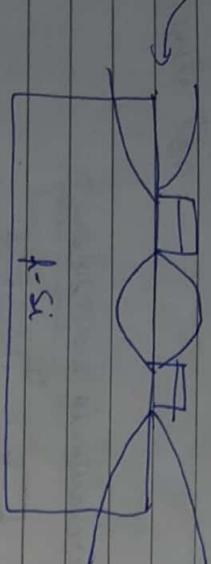
large capacitance, slow device

True Device don't like this

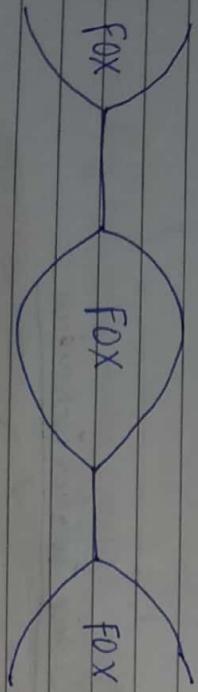


2nd method → oxide where device not to be made
1st method → oxide everywhere & etch the pattern

oxidation



F-Si
FOX - fulloxide
or
thin oxide



Q2) Implement half adder using AOI logic.

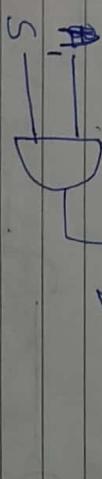
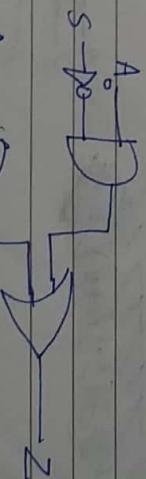
$$S = \bar{A}B + \bar{B}A$$

$$C = A \cdot B$$

10/01/2020 (Half Assistant)

Q1) Implement 2 input MUX via AOI logic

$$Z = A_0 \bar{S} + A_1 S$$

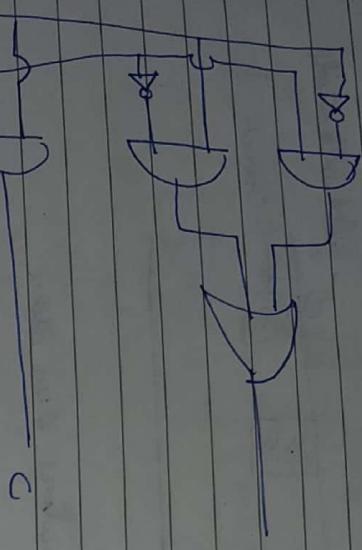


f-Si

Convert XOR gate to NOR logic



$$\overline{(\overline{A} + \overline{B})} + \overline{(\overline{A} + B)} =$$



$$A \rightarrow \overline{\text{D}} \rightarrow \overline{A} \quad \overline{A + \overline{B}} = \overline{A + \overline{B}}$$

$$B \rightarrow \overline{\text{D}} \rightarrow \overline{B} \quad \overline{A + \overline{B}} + \overline{A + B} = \overline{A + B} + \overline{A + B}$$

$$= \overline{A} \oplus B$$



Convert XOR gate to NAND logic

~~$$\overline{A}B + A\overline{B} = \overline{A}\overline{B} \cdot \overline{A}B$$~~

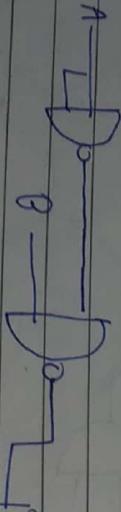
~~$$A \rightarrow \overline{\text{D}} \rightarrow \overline{A} \quad \overline{A + B} = \overline{A} + \overline{B}$$~~

$$B \rightarrow \overline{\text{D}} \rightarrow \overline{B} \quad \overline{A + B} + \overline{A + B} = \overline{A + B} + \overline{A + B}$$

~~$$\overline{A}B + A\overline{B} = \overline{A}\overline{B} \cdot \overline{A}B$$~~

$$A \rightarrow \overline{\text{D}} \rightarrow \overline{A} \quad \overline{A + B} = \overline{A} + \overline{B}$$

$$B \rightarrow \overline{\text{D}} \rightarrow \overline{B} \quad \overline{A} + \overline{B} = \overline{A} \overline{B}$$



~~$$A \rightarrow \overline{\text{D}} \rightarrow \overline{A} \quad \overline{A} + \overline{B} = \overline{A} \overline{B}$$~~

$$B \rightarrow \overline{\text{D}} \rightarrow \overline{B} \quad \overline{A} + \overline{B} = \overline{A} \overline{B}$$

Q3) Implement 3bit to 8bit Decoder in AOI logic

~~$$I_0 = \overline{A_2} \overline{A_1} \overline{A_0}$$~~

~~$$I_1 = \overline{A_2} \overline{A_1} A_0$$~~

~~$$I_2 = \overline{A_2} A_1 \overline{A_0}$$~~

~~Method of SPICE~~

$$I_0 = I_{S1} + I_{S2}$$

$$I_0 = I_{D1} + I_{D2}$$

$$I_0 = I_{P1} + I_{P2}$$

$$I_0 = I_{N1} + I_{N2}$$

$$I_0 = I_{A1} + I_{A2}$$

$$I_0 = I_{B1} + I_{B2}$$

$$I_0 = I_{C1} + I_{C2}$$

$$I_0 = I_{E1} + I_{E2}$$

$$I_0 = I_{F1} + I_{F2}$$

$$I_0 = I_{G1} + I_{G2}$$

$$I_0 = I_{H1} + I_{H2}$$

$$I_0 = I_{J1} + I_{J2}$$

$$I_0 = I_{K1} + I_{K2}$$

$$I_0 = I_{L1} + I_{L2}$$

$$I_0 = I_{M1} + I_{M2}$$

$$I_0 = I_{O1} + I_{O2}$$

$$I_0 = I_{P1} + I_{P2}$$

$$I_0 = I_{R1} + I_{R2}$$

$$I_0 = I_{T1} + I_{T2}$$

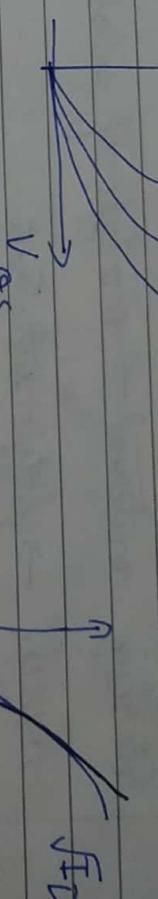
$$I_0 = I_{V1} + I_{V2}$$

$$V_T = V_{TO} + \delta \left[\sqrt{2\phi_f + V_{SB}} + \sqrt{12\phi_f} \right]$$

(calculated) ✓ (find) ✓ (Answe calculated) ✓ (Answe calculated)

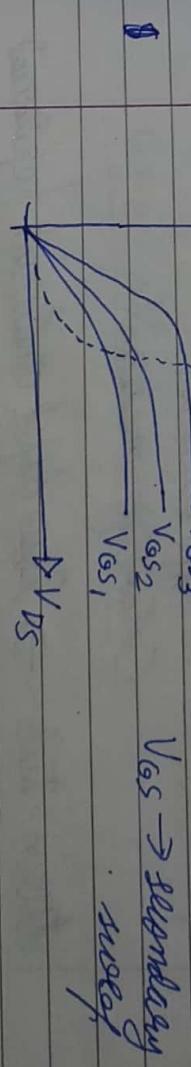
$$V_{SB} = V_{SB1} + V_{SB2} + V_{SB3}$$

$$V_T = V_{TO} + \sqrt{12\phi_f}$$



$$I_D = K_m (V_{GS} - V_{GS1})^2$$

NMOS

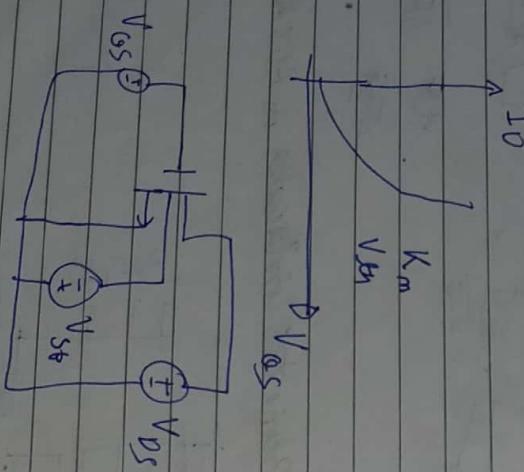


$$V_{DS} = V_{GS} - V_{SE}$$

$$\phi_f = \frac{kT}{q} \ln \left[\frac{N_A}{N_D} \right]$$

→ NCh in parameter file

Same for PMOS



13/01/2020

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Outline of the patterning of P^+ for NMOS

CMOS n-well Process

P-well

twin tube

Design Rules

CMOS Process

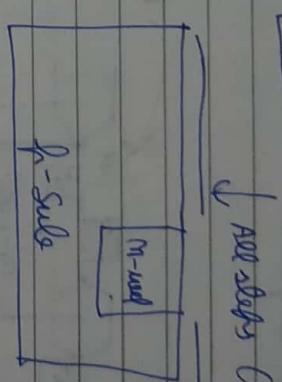
Starting material \rightarrow one type of substrate

n-well \rightarrow p-type substrate
(starting material)

p-well \rightarrow n-type substrate
(starting material)

Mask \rightarrow low doped material / pattern

Define active areas



↓ All steps (photolithography, via opening)

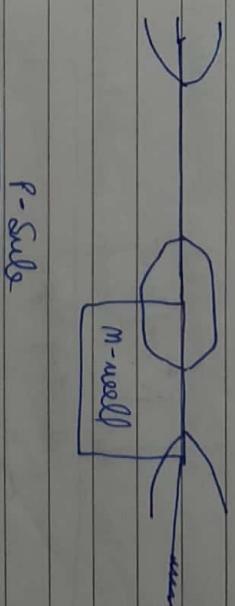
↓ Mask

NMOS n⁺ doping for S & D

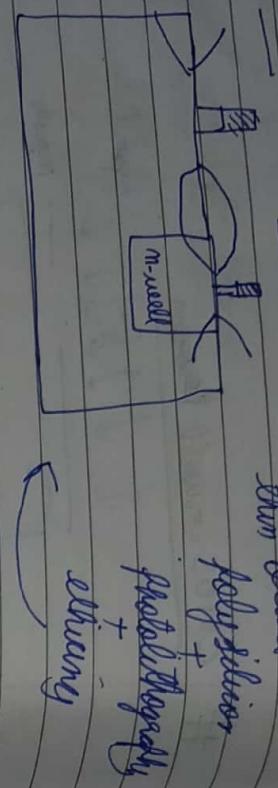
PMOS p⁺ doping for S & D

Metallization contact \rightarrow direct metal contact with interconnects.

Poly Silicon Patterning

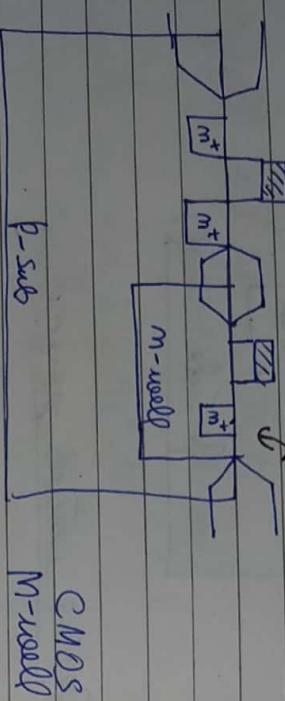


Poly Si
thin oxide
oxide



n+ implant

Bulk contact



C MOS
n-well

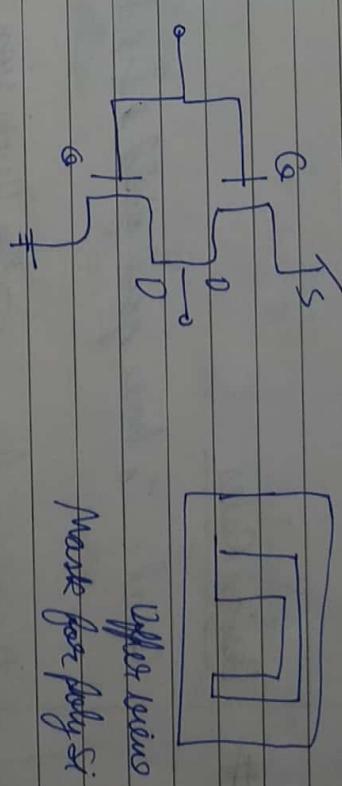
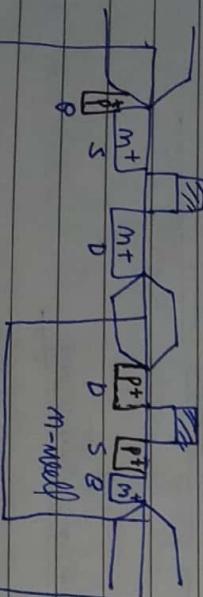
p-well → same process as n-well

n+ implant
oxidation layer

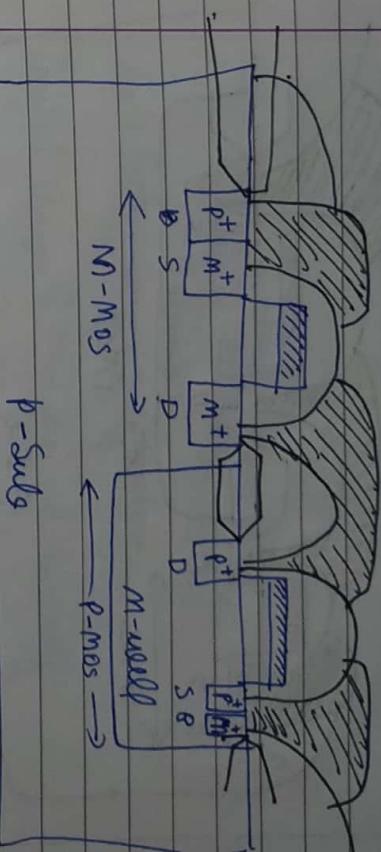
then some process

then -tub → n-well then p-well or vice versa & then some process

p - side



C MOS structure



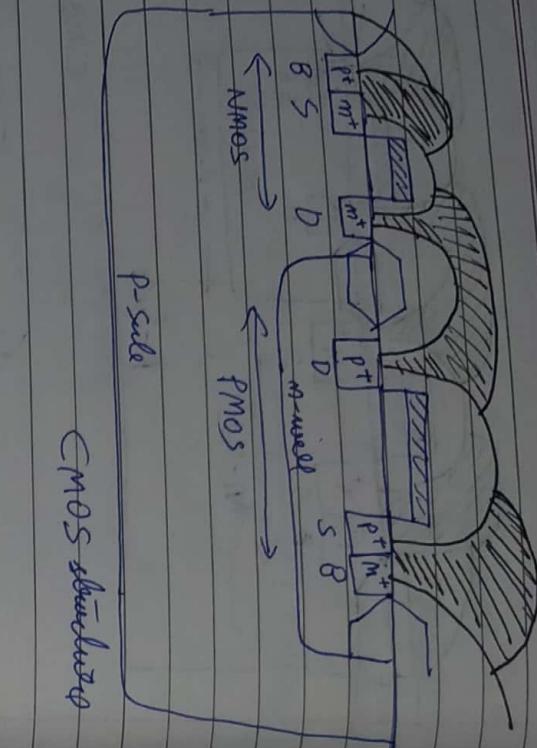
lambda \rightarrow min width = 2λ
(2)

90 nm Technology, $\lambda = 45$
45 nm Technology, $\lambda = 22.5$

Rule Book, Design Rule Check

Compact Design & Easy Design \leftarrow Tradeoff.

MOSIS Design Rules (Scalable Design Rules) Kang Book



Design Rules

Goal: To have good yield & reliable chip

	Width	Separation
Active Area	3λ	3λ
Poly	2λ	2λ

Metal 3λ 3λ

Contact Size $2\lambda \times 2\lambda$

Poly contact to active edge 3λ

Minimum distance to poly edge. 3λ

Feature Size

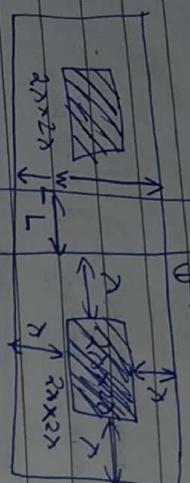
Scalable Design Rules \rightarrow lambda based design rules

Mission Based Design Rules.

Scalable Design Rules \rightarrow lambda based design rules.

2) Poly silicon

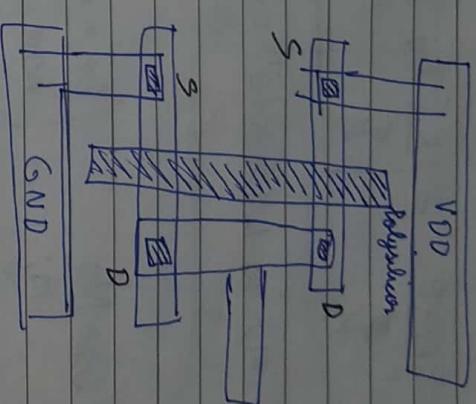
Aptar



#

VDD

Poly silicon



MOS structure

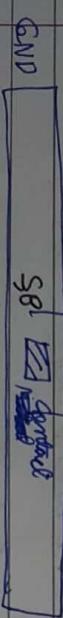
Energy Band diagram - free electrons
- MOS threshold

MOS under external bias - accum., deff., via

(accumulation) (depletion) (inversion)

Threshold Voltage

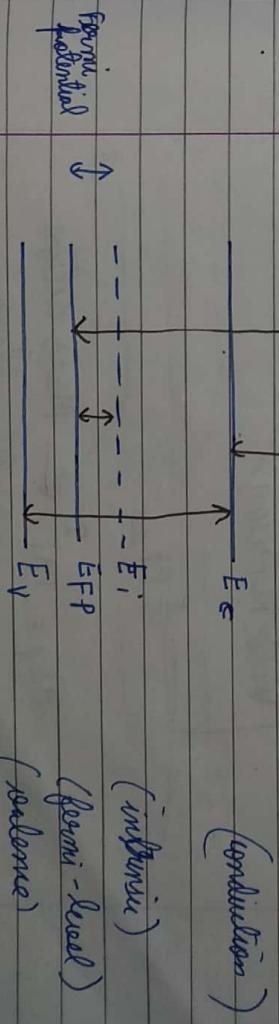
Energy Band Diagram for P-Substrate



#

Poly origin L W

C1F GDS II

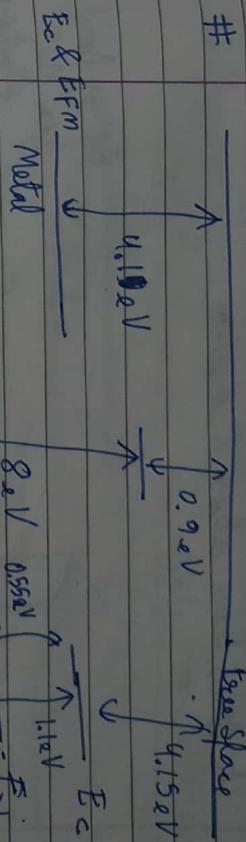
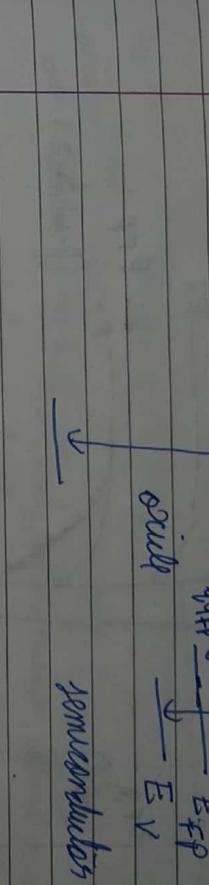


Formal Potential (ϕ_{FP})

$$= \frac{E_{FP} - E_i}{q} = \left[\frac{kT \ln \frac{n_i}{N_A}}{q} \right]$$

$$n_i \approx 1.45 \times 10^{10} \text{ cm}^{-3}$$

$$\rho_m = \frac{kT \ln \frac{N_D}{n_i}}{q} \quad \begin{cases} \text{for n-substrate} \\ \text{here, } E_{FP} \text{ is above } E_i \end{cases}$$



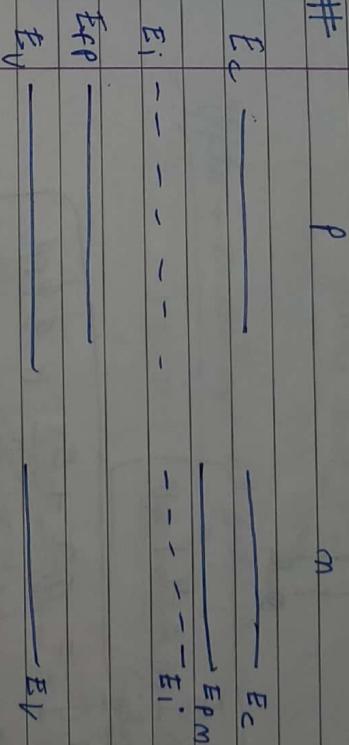
#

E_c

Band gap $g_i = 1.1 \text{ eV}$

E_V

. Free space
 $\int g_i^2 c$ (electron affinity)



#

E_c

E_V

 E_i

E_{FP}

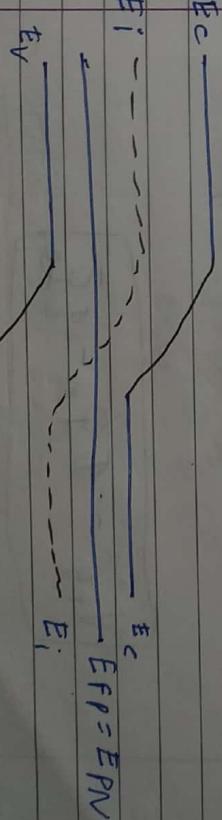
E_V

brought
together

Free space

Work function

E_{FP}

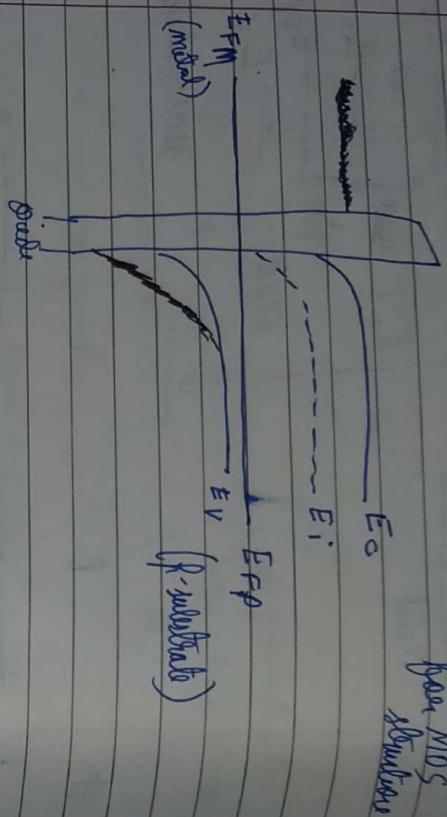


$$m_p = m_i^2 \leftarrow \text{Mass relation law}$$

The fermi level align themselves.

#

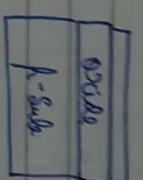
Energy band from MOS structure



$$V_{FB} = \varphi_f - \varphi_s$$

#

MOS under external bias



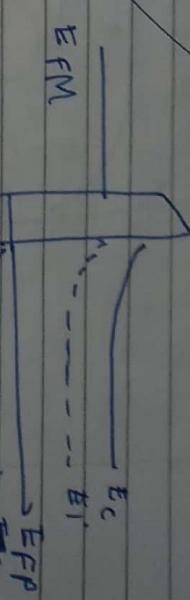
Apply +ve voltage at gate

$V_G < 0$
deaccumulated
with holes

holes attract, hole increase, band goes near
fermi level.

Apply + ve voltage at gate

$V_G > 0$ accumulated with electrons



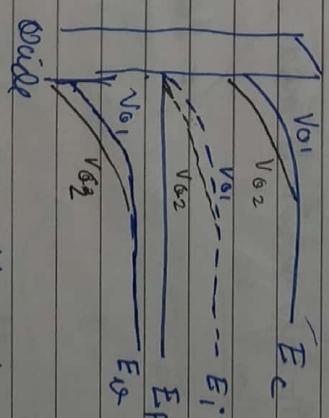
$$\varphi_f = \varphi_s + \varphi_i$$

(work function)

$$\varphi_f = \varphi_s + \frac{E_g}{2} + \varphi_i$$

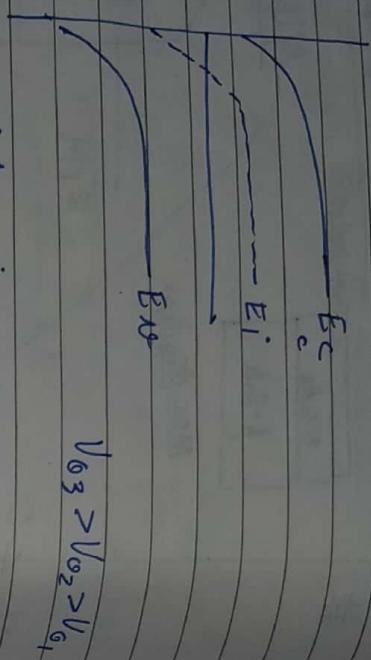
(assistic function) (electron affinity) (fermi potential)

Flat Band Voltage = voltage applied to gate for bands flat



depiction at the surface

$$V_{G2} > V_{G1}$$

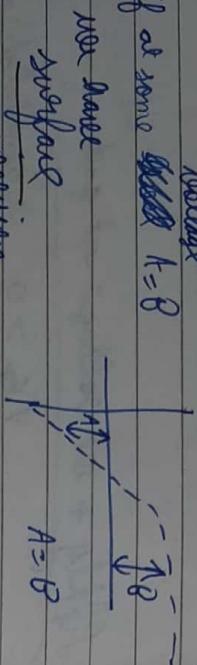


electrons increased

$$V_{G3} > V_{G2} > V_G$$

Surface potential

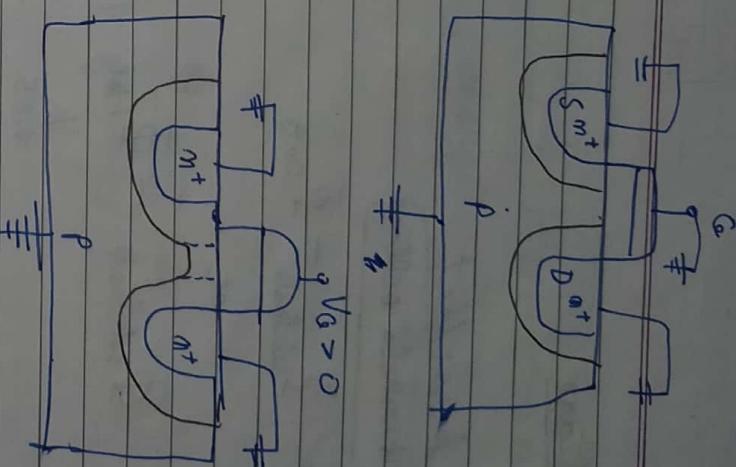
if at some time $t = \theta$



no more
surface
electron
movement

n-type substrate now. Electrons on surface
(minority)

= holes left in substrate
(majority)



$$V_G > 0$$

increase V_G more

$$V_G \geq V_{T0}$$

no current flow

Channel
created

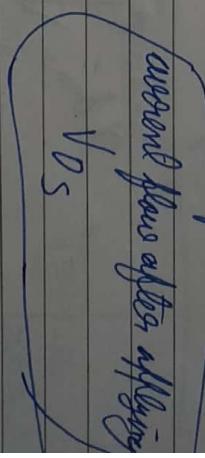
current flows after applying
 V_{DS}

#

threshold voltage = creates conducting channel

between source & drain

channel pinch-off.



Threshold voltage

$$-\sqrt{2qN_A\epsilon/2\Phi_F}$$

\rightarrow to get voltage component

(charge)

$$\text{divide } C_{ox} = \epsilon_{ox}$$

$$\frac{\Phi}{\Phi_x}$$

$$= E_0 \cdot \epsilon_x$$

$$1. \phi_{gc} = \phi_{substrate} - \phi_{oxide}$$

or

$$(for making
bands flat) \quad \phi_{substrate} = \phi_{poly} \quad (\text{polymer
instead of
metal})$$

d 0.55

17/01/2020

Threshold Voltage

2. Band bending
for surface inversion
3. $-qN_Ax_d$ (charge)

$$V_{to} = \phi_{gc} - 2\Phi_F + \frac{\sqrt{2qN_A\epsilon/2\Phi_F}}{C_{ox}} - \frac{\phi_{oxide}}{C_{ox}}$$

C_{ox} = oxide capacitance

$$x_d = \sqrt{\frac{2E}{qN_A}(-2\Phi_F)}$$

$$\Phi_F = -ve \quad \text{NMOS}$$

$$+ve \quad \text{PMOS}$$

$\checkmark V_{to} < 0$
No
substrate
bias

$$\text{Charge} = -ve \quad \text{NMOS}$$

$$+ve \quad \text{PMOS}$$

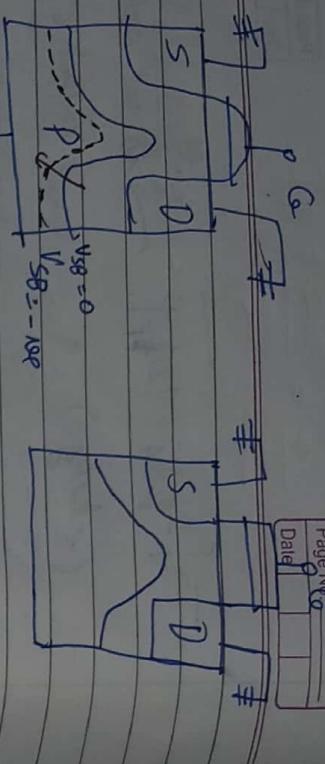
$$m \propto \frac{1}{2\Phi_F/(\text{const})}$$

$$x_d \propto \sqrt{1-2\Phi_F/}$$

Ans in Book

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Date _____

$$Q_{BD} = -\sqrt{2qN_A|\epsilon_{Si}|[1-2\phi_F]}$$



$\sqrt{m \times \text{width}}$

I_D

$V_{GS} = 0$

$V_{SD} = -V_{DS}$

(Work function gate & substrate)

(Band bending)

(Back charge)

(oxidation layer)

$$V_T = \Phi_{SC} - 2\Phi_F + \frac{\sqrt{2qN_A|\epsilon_{Si}|[1-2\phi_F]}}{C_{ox}} + \frac{qN_{ox}}{C_{ox}}$$

$$V_T = V_{T0} + \left(\frac{\sqrt{2qN_A|\epsilon_{Si}|}}{C_{ox}} (\sqrt{1-2\phi_F} + |V_{SD}|) - \sqrt{1-2\phi_F} \right)$$

under linear

Compute V_T for $N_A = 10^{16} \text{ cm}^{-3}$, poly silicon doping $N_d = 2 \times 10^{20} \text{ cm}^{-3}$, $\Phi_{BD} = 500 \text{ A}^\circ$, $N_{ox} = 4 \times 10^{10} \text{ cm}^{-2}$.

$$\epsilon_{Si} = 11.7 \quad \epsilon_0 = 8.85 \times 10^{-11} \text{ F/cm}$$

$$\epsilon_{ox} = 3.9$$

C_{ox}

$$C_{ox} = \frac{\epsilon_{ox} \epsilon_0}{d_{ox}} = \frac{3.9 \times 8.85 \times 10^{-11}}{500 \times 10^{-8}}$$

$$I_F(\text{body}) = 0.55$$

~~$$V_T = \Phi_{SC} - 2\Phi_F + \sqrt{2qN_A|\epsilon_{Si}|[1-2\phi_F]} + V_{SD}$$~~

C_{ox}

~~$$I_F(\text{body}) = 0.55$$~~

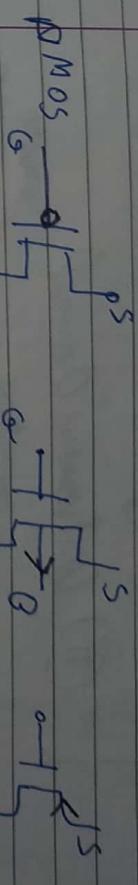
$$\phi_F = \frac{Eg}{2} = \frac{|V|}{2}$$

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Date 20/01/2023

$$\phi_{F(poly)} = -0.55$$

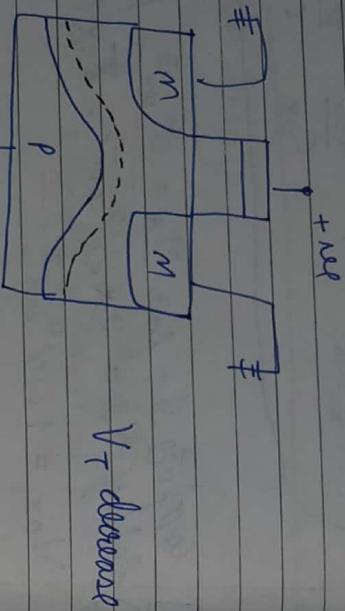
$$\phi_{substrate} = -0.35 \quad \left(\frac{K_T \text{ long}}{2} \right) \frac{V_A}{N_A}$$

MOS symbols

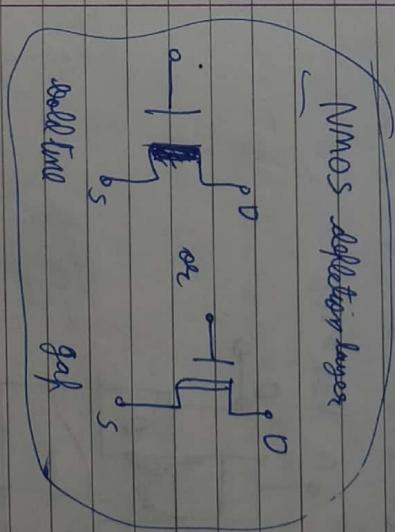
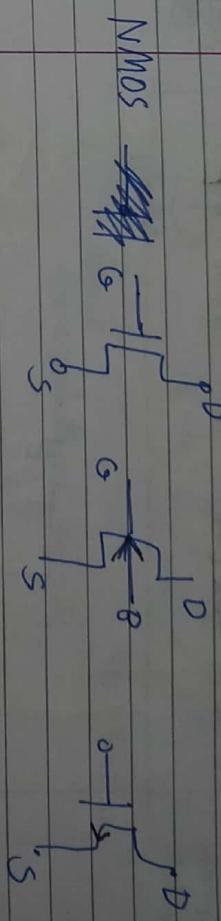


$$V_T = 0.4V$$

#



V_T decrease



Qualitative operation of MOS operation

(skipped)

Cutoff - Voltage Relationship

(connection to the simple on)

higher voltage PMOS, Source
higher voltage NMOS, Drain

for current flow, a channel must exist on at least one side

In late level = v_a or f (See parameters)
 (more parameters)

Page No.	_____
Date	_____

Page No. _____
 Date _____

Assumption

(i) Constant Channel approximation

current flow due to electric field between drain & source

(ii) Continuous channel

width

$$I = C_{ox} (V_{ds} - V_{t0} - V(y)) W \cdot \frac{4E}{L}$$

velocity

linear
Region

$$I_d = \frac{1}{2} u C_{ox} \frac{W}{L} \left[2(V_{ds} - V_{t0}) V_{ds} - V_{ds}^2 \right]$$

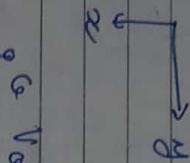
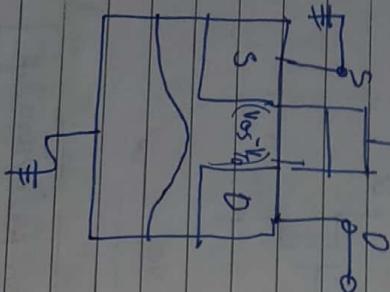
NO.S current voltage relation

Device transconductance $\leftarrow k$

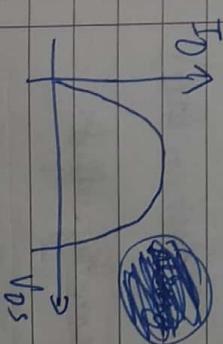
$u C_{ox} \leftarrow$ process transconductance

(k')

$\frac{W}{L} \leftarrow$ aspect ratio



$G \quad V_{ds} > V_{t0}$



$$V_{ds} = V_{gs} - V_{t0}$$

Graph Non-linear if only
saturation region formula is used.

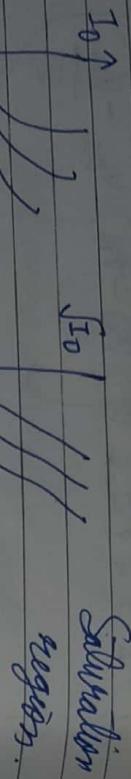
$$I_d = \int_0^L C_{ox} (V_{ds} - V_{t0} - V(y)) W u \, dy$$

saturation region

$$I_d = \frac{1}{2} u C_{ox} \frac{W}{L} (V_{ds} - V_{to})^2$$

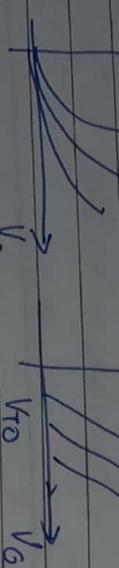
Saturation Region

$$V_{ds} \geq V_{ds} - V_{to}$$



$$I_d \uparrow$$

$V_{ds} = V_{ds} - V_{to}$ --- (some slope, practical)
(total, zero slope)



Saturation region.

$$(Linear) \quad I_d = \frac{1}{2} u C_{ox} \frac{W}{L} (2(V_{ds} - V_t) V_{ds} - V_{ds}^2)$$

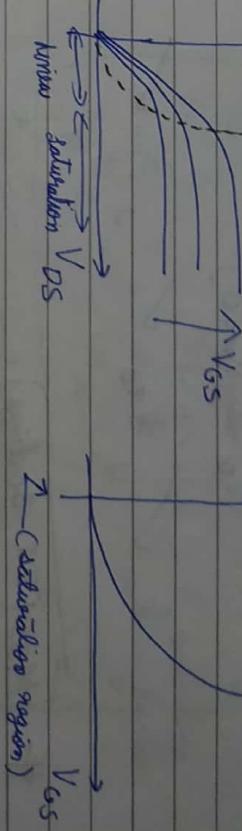
$$(Saturation) \quad I_d = \frac{1}{2} u C_{ox} \left(\frac{W}{L} \right) (V_{ds} - V_t)^2$$

if $V_{ds} = 0$, in both eqn $V_t \rightarrow V_t$

$$I_d \uparrow$$

$V_{ds} = V_{ds} - V_t$
Output characteristics

Transfer characteristics



In saturation region

$$I_d = \frac{1}{2} \frac{W}{L - \Delta L} (V_{ds} - V_t)^2 u C_{ox}$$

$$= \frac{1}{2} u C_{ox} \frac{W}{L} (V_{ds} - V_t) \left(1 + \frac{\Delta L}{L} \right)^{-1} u C_{ox}$$

$$\Delta L \ll L$$

$$= \frac{1}{2} u C_{ox} \frac{W}{L} (V_{ds} - V_t) \left(1 + \frac{\Delta L}{L} \right) \left(\Delta L \text{ is function of } V_{ds} \right)$$

MOSFET scaling & small geometry effect.

Channel length modulation
Measurement of parameter (done in lab)

20/1/2020

#

I-V characteristics

Saturation Region: $I_D = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \gamma V_{DS})$

γ = channel length modulation factor



$$(or \text{ when } V_{DS} = 0)$$

$$I_D \propto V_{DS}$$

$$I_D \propto V_T$$

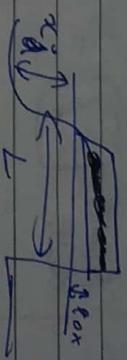
$$\begin{aligned} W' &= w/s \\ L' &= l/s \\ t_{ox}' &= t_{ox}/s \\ \alpha' &= \alpha/s \end{aligned}$$

$s > 1$

Scaled Quantities	Unscaled Quantities
w/s	w

* s is scaling factor

Geometry \rightarrow W channel width
 L channel length
 t_{ox} oxide thickness
 s simulation depth or channel length



MOSFET Scaling

Scaling down \leftarrow main focus

Full scaling
 or
 constant field scaling

Constant voltage scaling

Scaling

#

Constant Field Scaling

True only if constant field scaling or constant voltage scaling

field const

\downarrow

voltage \downarrow by s

$$V_{DS}' = V_{DS}/s$$

*

$$\sqrt{\frac{t_{ox}}{t_{ox}}} = \sqrt{\frac{t_{ox}}{s}}$$

$$V_{DS}' = V_{DS}/s$$

*

$$\Rightarrow I_D' = \frac{1}{2} \mu s C_{ox} \frac{W}{L} \left(\frac{V_{ds}}{s} - \frac{V_T}{s} \right)^2$$

$$x_d = \sqrt{\frac{2E\phi_0}{qN_A}} = \sqrt{\frac{2eV}{qN_A}}$$

$$\text{Channel depth } x_d = \sqrt{\frac{2E}{qN_A} \frac{V_s}{s}} = \frac{x_d}{s}$$

$$\Rightarrow I_D(\text{sat}) = \frac{I_D(\text{sat})}{s}$$

(Decreased by s)

$$\text{Similarly, } \frac{I_D(\text{lim})}{I_D(\text{lim})} = \frac{s}{s}$$

$$\rho' = \rho \frac{\text{Area}}{\text{Area}}$$

$$\rho' = \frac{I_D' V'}{s} = \frac{I_D V}{s^2}$$

$$\text{Density} = \frac{\rho'}{\text{Area}} = \frac{\rho}{s^2} = \frac{\rho}{\text{Area}}$$

$$I_D = \frac{1}{2} \mu s C_{ox} \left(\frac{W}{L} \right) (V_{ds} - V_T)^2 \quad (\text{ignoring channel length modulation})$$

$$I_D = \frac{1}{2} \mu s C_{ox} \left(\frac{W}{L} \right) \left[2(V_{ds} - V_T) \cdot V_{ds} - V_{ds}^2 \right]$$

$$C_{ox}' = \frac{C_{ox}}{s} = \frac{C_{ox}}{s}$$

Constant Voltage Scaling

→ voltage const

$$V_{ds}' = V_{ds}$$

$$V_{T0}' = V_{T0}$$

$$V_{ds}' = V_{ds}$$

$$I_D' = \frac{1}{2} \mu s C_{ox}' \frac{W}{L} \left[V_{ds}' - V_T' \right]^2$$

(but)

Disadvantages:

(i) Electron Migration Problem

(ii) More heat for less area

(iii) Jump to oxide, threshold voltage will change, not corner problem

$$x_d^1 = \frac{x_d}{8} = \sqrt{\frac{2eV}{q/N_A^1}}$$

$$N_A^1 = \frac{8^2 N_A}{V}$$

$$I_d = \frac{1}{2} u_{Cox} \left(\frac{W}{L} \right) (V_{DS} - V_T)^2$$

$$I_d = \frac{1}{2} u_{Cox} \left(\frac{W}{L} \right) \left[2(V_{DS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$C_{ox}^1 = 3 C_{ox} \quad (\text{same as small field})$$

$$I_d^1 = \frac{1}{2} u_{Cox} \frac{W}{L} (V_{DS} - V_T)^2$$

$$\frac{I_d^1}{I_d} = 3 \quad (\text{increasing } S)$$

$$I_D^1 = 3 I_D (\text{in})$$

$$P^1 = I^1 V^1 = 3 I \cdot V = 3 P \quad (\text{power division})$$

$$\frac{\text{Power Density}}{\text{Area}}^1 = \frac{\text{Power}}{\text{Area}} = \frac{3 P}{A_{T_3}^2} = \frac{3 \text{ Power}}{\text{Area}}$$

Small Geometry Device

Alternative route \rightarrow General Scaling

$$L \sim c \delta$$

\rightarrow short channel limitation
 \rightarrow more width \downarrow
 drift characteristics \downarrow

$$I_D = W \frac{V_D(\text{sat})}{\mu_{\text{eff}}} C_{ox} \frac{V_{DSAT}}{V_{DSAT}}$$

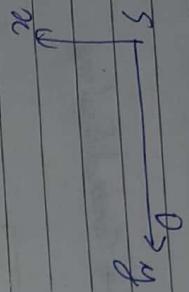
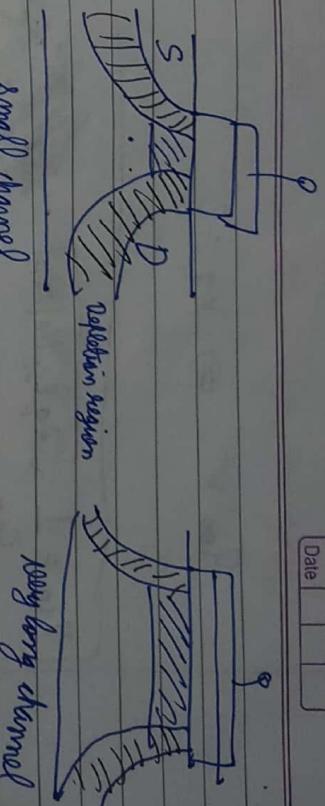
$$\frac{V_D}{\mu_{\text{eff}}} = \frac{V_{DSAT}}{V_{DSAT}}$$

$$1 + \tilde{E}_x$$

$$= \frac{\mu_{\text{eff}}}{1 + \tilde{E}_x}$$

$$\frac{I_D}{I_D^1} = \frac{V_{DS} - V_{DS}(y)}{V_{DS} - V_{DS}(0)}$$

$$= \frac{\mu_{mo}}{1 + \eta(V_{GS} - V_T)}$$



Short Channel Effect

ΔLD \curvearrowleft diffusion width due to drain bias

x_d -channel depth

ΔLS \curvearrowleft diffusion width due to source bias

source bias

In case of large dimension, $Q = -\sqrt{2q_i \epsilon_{Si} N_A / 2d_F}$

$$(x_j + x_{dP})^2 = (x_{dm})^2 + (x_j + \Delta LD)^2$$

$$\Rightarrow \Delta LD = -x_j + \sqrt{x_j^2 + 2x_j x_{dP} - (x_{dm}^2 - x_{dP}^2)}$$

$$\approx -x_j + x_j \left(1 + \frac{2x_{dP}}{x_j} \right)^{1/2}$$

$$\approx x_j \left(\sqrt{1 + \frac{2x_{dP}}{x_j}} - 1 \right)$$

$$\Delta LD = x_j \left(\sqrt{1 + \frac{2x_{dP}}{x_j}} - 1 \right)$$

$$\Delta LS = x_j \left(\sqrt{1 + \frac{2x_{dS}}{x_j}} - 1 \right)$$

$$Q_{BO} = - \left(1 - \frac{\Delta LS + \Delta LD}{2L} \right) \sqrt{2q_i \epsilon_{Si} N_A |2\phi_F|}$$

$$I_D = \frac{1}{2} n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (\eta = 0)$$

$$I_D \propto (V_{GS} - V_T)^2 \quad \begin{cases} \text{not valid in} \\ \text{small geometry} \end{cases}$$

$$x_{dS} = \sqrt{\frac{2\epsilon \phi_0}{q N_A}}$$

$$x_{dP} = \sqrt{\frac{2\epsilon (\phi_0 + V_{DS})}{q N_A}}$$

$$Q_{BD} \vee \Rightarrow V_T = ?$$

$V_{AS} < V_T$ $I \propto e^{(V_{AS} - V_T)/kT}$

DIBL

Drain Induced Barrier Lowering

$$V_{TO} = \frac{1}{C_{ox}} \sqrt{2q\epsilon_{Si} N_A |2\phi_F|}$$

~~C_{ox}~~

$$\frac{x_j}{2L} \left[\left(\sqrt{\left(1 + \frac{2x_{AS}}{x_j} \right)} - 1 \right) - \left(\sqrt{\left(1 + \frac{2x_{BD}}{x_j} \right)} - 1 \right) \right]$$

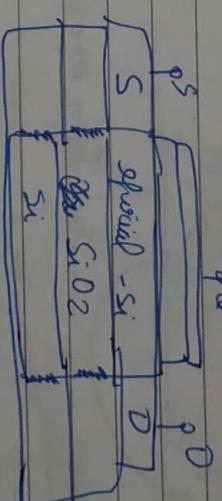
MOS Capacitors

- Oxide capacitors
- Junction capacitors

MOS capacitors

Delay & Power consumption depend on capacitors
Capacitors get charged.

Bulk Technology SOT Series

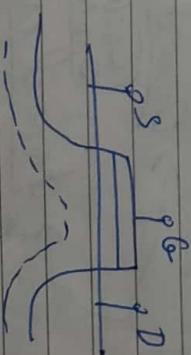


$$C_{ox} \downarrow$$

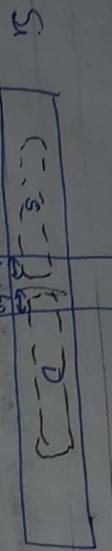
$$\frac{Q_B}{C_{ox}} \uparrow \Rightarrow |V_T| \uparrow$$

$$V_{TO} = \frac{-Q_{BD}}{C_{ox}}$$

$$V_{BS} = 0$$



poly-Si layer
Mask



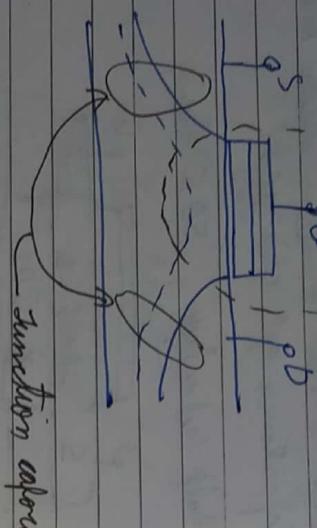
Drawn Mask Width
 L_m

Channel length
 L

$$\text{Effective Channel Length} \Rightarrow L = L_m - 2L_D$$

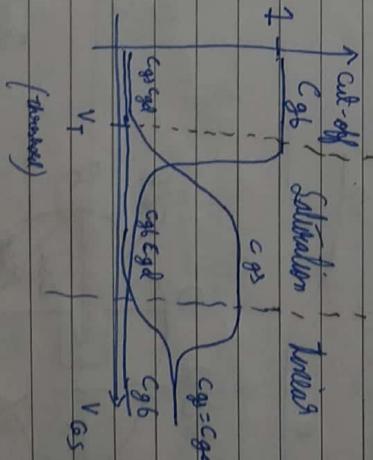
Operating Region	C_{gb}	C_{gs}	C_{gd}
Linear	0	$\frac{1}{2}C_{ox}WL$ $+ C_{oxWLD}$	$\frac{1}{2}C_{oxWL}$ $+ C_{oxWLD}$
Saturation	0	$\frac{2}{3}C_{oxWL}$ $+ C_{oxWLD}$	$0 + C_{oxWL}$

$$\text{Total capacitance} = C_{gb} + C_{gs} + C_{gd}$$



Normalized \rightarrow
Capacitance \rightarrow
unit \rightarrow
unit \rightarrow

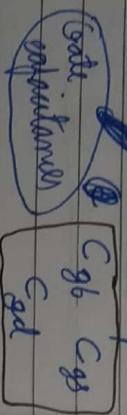
(In Book
 C_{oxWL}
 \rightarrow is neglected)



(Ignoring overlap capacitance C_{oxWL})

Oxide capacitance \rightarrow Overlap capacitance
(C_{gb} (overlap)
 C_{gs} (overlap))

channel capacitance

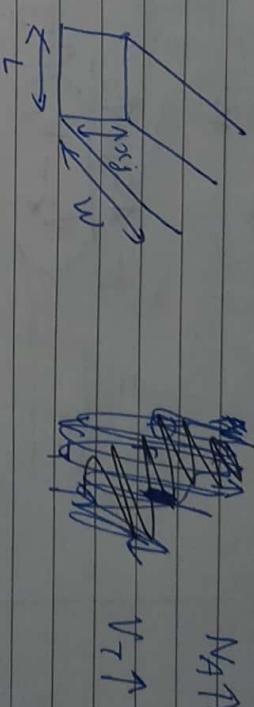


Function Capacitance



$$V_{GS} \geq V_T + V_{\tau} \text{ means}$$

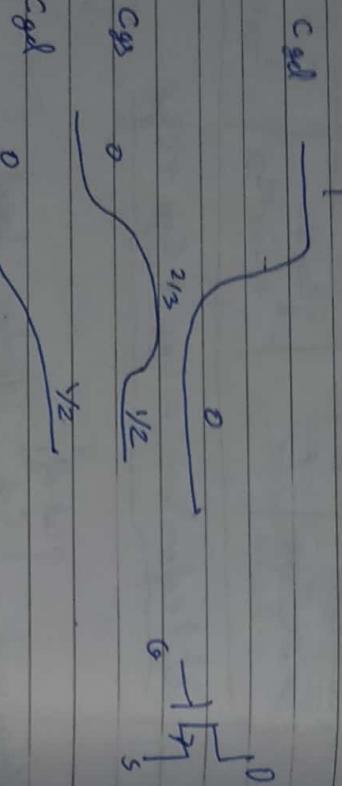
$$V_T \leq V_{GS} \leq V_{GS} + V_T \quad \text{Saturation}$$



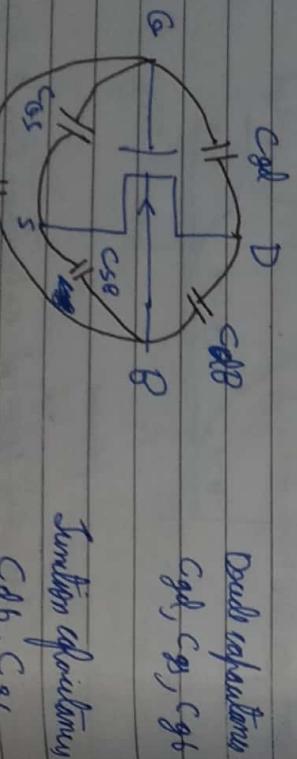
Junction Capacitance \rightarrow Schottky Jn. n^+/ρ^+
Bottom Junction: n^+/p^-

C_{sub} \downarrow
 \times Thickness \times Width of Junc \times W

$$Q_j = A_q \frac{N_D N_A}{N_D + N_A} \approx d$$



$$= A_q \frac{N_D N_A}{N_D + N_A} \int \frac{2\epsilon}{q} \frac{(\phi_0 - V)}{N_A N_D / (N_A + N_D)}$$



$$C_j = \frac{dQ_j}{dV} = A_q C_{j0} \frac{1}{(1 - V/\phi_0)}$$

$$C_{j0} = \sqrt{\frac{\epsilon_s q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{\phi_0}}$$

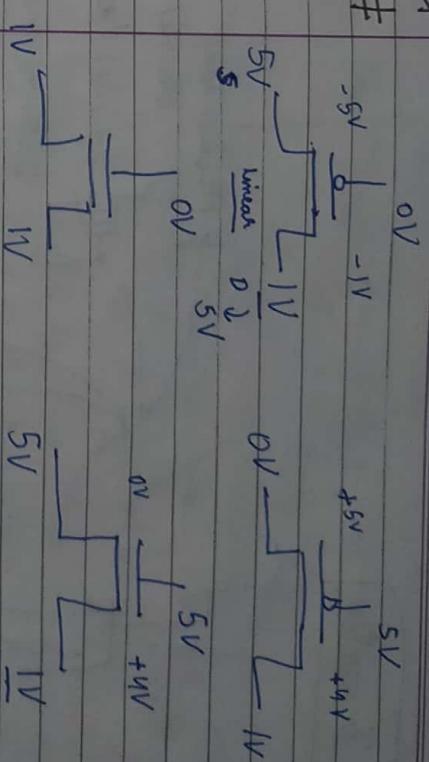
Doubt capacitance:
 C_{gd}, C_{gs}, C_{gb}

$N_A \rightarrow$ substrate doping conc.
 $N_D \rightarrow$ source/drain doping conc.

3/10/2020

$$C_{eq} = \frac{\Delta Q}{\Delta V} = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} C_J(V) dV$$

$$= - \frac{A C_{J0} \phi_0}{(V_2 - V_1)(1 - m)}$$



$$C_{eq} = A C_{J0} K_{eq}$$

$$K_{eq} = -2\sqrt{\phi_0} \left[\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1} \right]$$

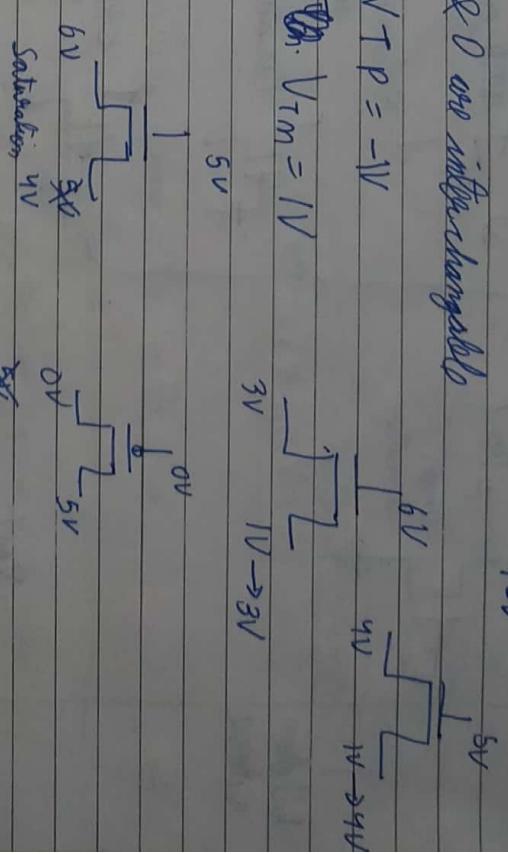
junction are RD

$$\text{So } V_2 \approx -100$$

$$C_{J0sw} = \sqrt{\frac{e \sigma g N_A (sw) N_D}{2}} \cdot \frac{1}{V_2 - V_1}$$

$$C_{jsw} = C_{j0sw} \cdot x_j$$

Side Wall
Native
Commuter
JSW

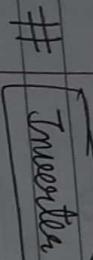


$$C_{eq(sw)} = P_{fsw} K_{eq(sw)}$$

Phase
change in
K_{eq(sw)}

$$V_{DD} \quad \boxed{\text{max} = V_{DD} - V_{TM}}$$

$$V_{DD} \quad \boxed{\text{max} = (V_{DD} - 2V_{TM})}$$



Pull up
Network

Resumes kept
meeting

$V_{out} = \sqrt{V_m} \ln(1 + e^{V_{in}/V_{th}})$
 $\frac{dV_{out}}{dV_{in}} = -1$

$V_{OH}, V_{OL} = \text{Output High/Low Voltage}$
 $V_{IH}, V_{IL} = \text{Input High/Low Voltage}$

$$NM_H = V_{OH} - V_{ZH}$$

The diagram illustrates a circuit configuration for an NMOS enhancement mode inverter. The output node, labeled V_{out} , is connected to the drain of a NMOS transistor. The source of this transistor is connected to ground through a resistor labeled R_s . The gate of the NMOS transistor is connected to the drain of a PMOS transistor, which is labeled as a "PseudoNMOS inverter". This PMOS inverter has its source connected to ground and its drain connected to the gate of the NMOS transistor. A feedback signal is provided by a resistor R_f from the output node V_{out} back to the gate of the PMOS inverter. The entire circuit is labeled "NMOS enhancement mode inverter".

$$\text{Voltage swing} = V_{OH} - V_{OL}$$

$$P_{DC} = \frac{1}{2} [P_{DC} (V_m = L_{SW}) + P_{DC} (V_m = H_{SW})]$$

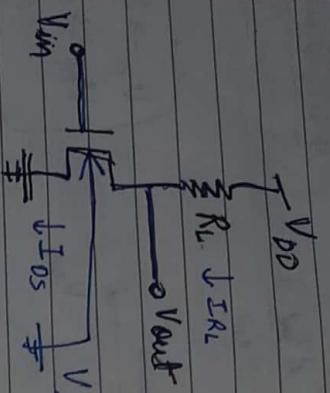
Ideal

$$V_{\text{in}} \rightarrow I_{\text{load}}$$

Channellists

#

Resistive word Insertion



$$\Rightarrow \frac{V_{DD} - V_{OL}}{R_L} = \frac{1}{2} k_m (2V_{DD}V_{OL} - 2V_{TO}V_{OL} - V_{OL}^2)$$

$$\Rightarrow \frac{1}{2} k_m V_{OL}^2 + \left(\frac{1}{2} k_m (2V_{TO}R_L - 2V_{DD}R_L) - \frac{1}{R_L} \right) V_{OL}$$

$\boxed{V_{OH}}$ NMOS off

$$I_{RL} = \frac{V_{DD} - V_{OH}}{R_L} = I_{DS} = 0$$

$$\Rightarrow \boxed{\bar{V}_{OH} = V_{DD}}$$

$$+ \frac{V_{DD}}{R_L} = 0$$

$$\Rightarrow V_{OL} = - \left(k_m V_{TO} - V_{DD} k_m - \frac{1}{R_L} \right)$$

$$\pm \sqrt{\left(k_m V_{TO} - V_{DD} k_m - \frac{1}{R_L} \right)^2 - 4 \cdot \frac{1}{2} k_m \cdot \frac{V_{DD}}{R_L}}$$

$\boxed{\bar{V}_{OL}}$ o/p = high o/p = low $V_{OS} = \text{low}$

NMOS region = ~~saturation~~ triode

$$V_{OS} < V_{OS} - V_T$$

$$k_m$$

$$I_{RL} = \frac{V_{DD} - V_{OL}}{R_L} = \frac{r_{DS}}{2} = \frac{1}{2} k_m C_{ox} \frac{W}{L} (2(V_{DD} - V_{TO})V_{OL})$$

$$I_{RL} = \frac{V_{DD} - V_{OL}}{R_L} = \frac{1}{2} k_m C_{ox} \frac{W}{L} (2(V_{TO} - V_{DD})V_{OL})$$

$$k_m$$

$$= - \int (k_m (V_{TO} - V_{DD}) \frac{1}{R_L})$$

$$\pm \int (k_m (V_{TO} - V_{DD}) - V_{RL})^2 - 2k_m \frac{V_{DD}}{R_L}$$

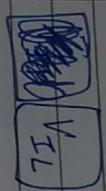
$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{R_m R_L} \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{R_m R_L}\right)^2 - \frac{2V_{DD}}{R_m R_L}}$$

$$V_{OL} = V_{DD} - V_{TO} + \frac{1}{R_m R_L} \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{R_m R_L}\right)^2 - \frac{2V_{DD}}{R_m R_L}}$$

$$\begin{aligned} &= -\frac{1}{R_L} \frac{dV_{out}}{dV_{in}} \\ &+ 2V_{out} \end{aligned}$$

$$\boxed{\frac{dV_{out}}{dV_{in}} = -1} \quad \boxed{V_{in} = V_{IH}}$$

#



#



$V_{DS} = \text{high}$ Saturation
 $V_{GS} = \text{low}$

Input - high linear
Output - low

$$\Rightarrow k_m \left[2(V_{IH} - V_{TO})(-1) - 2V_{out}(-1) \right] = \frac{-1}{R_L} (-1)$$

$$\Rightarrow k_m \left[V_{TO} - V_{IH} + 2V_{out} + V_{out} \right] = \frac{1}{R_L}$$

$$\Rightarrow k_m \left[V_{TO} - V_{IH} + 2V_{out} \right] = \frac{1}{R_L}$$

$$\Rightarrow V_{IH} = \frac{-1}{k_m R_L} + 2V_{out} + V_{TO}$$

$$\boxed{V_{IH} = -2V_{out} + V_{TO} - \frac{1}{k_m R_L}}$$

$$I_{DS,lin} = \frac{V_{DD} - V_{out}}{R_L}$$

$$= \frac{R_m}{2} \left[2(V_{in} - V_{TO})V_{out} - V_{out}^2 \right] - ①$$

Differentiate w.r.t V_{in} then substitute

$$V_{in} = V_{IH} \quad \& \quad \frac{dV_{out}}{dV_{in}} = -1$$

$$\boxed{I_{DS,lin} = \frac{V_{DD} - V_{out}}{R_L} = \frac{k_m}{2} (V_{in} - V_{TO})^2}$$

Substitute V_{TH} in eqn ①

$$\frac{k_m}{2} \int 2 \left(-\frac{1}{R_L} + 2V_{out} + V_{r0} - V_{r0}^2 \right) V_{out} - V_{out}^2 \, dV_{out}$$

$$= \frac{V_{DD} - V_{out}}{R_L}$$

$$\Rightarrow \frac{k_m}{2} \int \frac{-2V_{out} + 4V_{out}^2 - V_{out}^2}{R_m R_L} = \frac{V_{DD} - V_{out}}{R_L}$$

$$\Rightarrow -\frac{2V_{out}}{R_m R_L} + \frac{3V_{out}^2}{R_m R_L} = \frac{V_{DD}^2 - 2V_{out}}{R_L}$$

$$\Rightarrow \frac{1}{R_L} = k_m (V_{IL} - V_{r0})$$

$$\Rightarrow V_{out} = \sqrt{\frac{2}{3} \frac{V_{DD}}{k_m R_L} + V_{r0}}$$

$$V_{IH} = -\frac{1}{R_L} + \sqrt{\frac{8V_{DD}}{3k_m R_L} + V_{r0}}$$

$\boxed{V_{IL}}$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_m}{2} (V_{in} - V_{r0})$$

Differentiate

$$\frac{d}{R_L} \left(\frac{-dV_{out}}{dV_{in}} \right) = \frac{2k_m}{2} \int \frac{V_{in} - V_{r0}}{V_{IL} - V_{r0}} \, dV_{in}$$

- uncertainty

$$\rho = \frac{1}{2} V_{DD} \cdot \frac{V_{DD} - V_{out}}{R_L}$$

Impedance in

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{1}{2} k_m \left(2(V_{DD} - V_{r0})V_{out} - V_{out}^2 \right)$$

Convin



$$V_{\text{out}} = V_{\text{in}}$$

$$V_{\text{short}} = V_{\text{short}}$$

$$V_{out} = V_{drives}$$

$$\text{Vor hand} = 0$$

$\sqrt{65 \text{ dm}^2} = \sqrt{10 \text{ m}^2}$

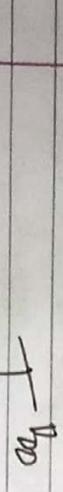
$$O = \text{sp}V = V_{\text{sp}} \text{spine} = \text{sp}V$$

卷之三

$$T_{\text{closed}} = T_{\text{closed}}(V_{\text{out}})$$

A hand-drawn diagram of a depletion-mode NMOS (DM-NMOS) circuit. On the left, there is a symbol for a depletion-mode NMOS transistor, consisting of a rectangle with a diagonal line through it, labeled 'G' (gate) at the top and 'D' (drain) at the bottom. To the right of this symbol is a vertical line labeled 'V_{DD}' at the top and 'V_S' at the bottom. A horizontal line connects the drain terminal of the NMOS symbol to the top terminal of a small circle labeled 'Source'. The bottom terminal of this circle is connected to the drain terminal of the NMOS symbol. Below the source terminal is a larger circle labeled 'Pmos'. A horizontal line extends from the Pmos circle to the right, labeled 'V_{out}' at the end. Above this output line, the word 'gate' is written above a small rectangle, which is connected to the top of the Pmos circle. Below the output line, the label 'M_f' is written above a curved arrow pointing downwards, with 'n_m' written below it. At the bottom right, the text 'Depl. NMOS' is written vertically.

Deltelco, Inc. Investors



Von Wand Danach

linear Cut-off

$$I_{D\text{load}} = \frac{K_{\text{load}}}{2} \cdot (2(V_{\text{load}} - V_T) V_{\text{Dsat}} - \frac{V^2}{0.5 \text{ load}}) = 0$$

$$V_{T\text{ final}} = V_{T0} + \gamma \left(\sqrt{V_{T0}^2 + V_{S0}^2} - \sqrt{|V_{Tf}|} \right)$$

$$\Rightarrow V_{out} = V_{DD}$$

$$V_{OH} = V_{DD}$$

#

 V_{OL} V_{OL}

Device

 $V_{DS} = 0$ $V_{DS} - \text{high}$ $V_{out} - \text{low}$ $V_{DS} - \text{low}$

$$\Rightarrow V_{DS} = V_{1,load}$$

linear region

No channel at

device end

Saturation region

purely
(load)

$$I_{load} = \frac{1}{2} n_m \sigma \mu \left(V_{DS} - V_T \right)^2 = \frac{1}{2} n_m \sigma \mu \left(-V_{DS} \right)^2$$

$\left(\frac{V_{DS}}{V_{DD}} \right)$

$$I_{load} = \frac{1}{2} n_m \sigma \mu \left(V_{DS} - V_T \right)^2 = \frac{1}{2} n_m \sigma \mu \left(-V_{DS} \right)^2$$

$\left(\frac{V_{DS}}{V_{DD}} \right)$

$$I_{DS} = \frac{1}{2} n_m \sigma \mu \left(2(V_{DS} - V_T) V_{out} - 2 \frac{dV_{DS}}{dV_{in}} (V_{DS} - V_{out}) \right)$$

dV_{in}

smaller quantity neglected

I_{D load}

$$LHS = \frac{\partial I_{DS}}{\partial V_{in}} \left[2(-V_{DS}(V_{out})) \left(\frac{-dV_{out}}{dV_{in}} \right) \right]$$

$$- 2 \frac{dV_{DS}}{dV_{in}} (V_{DS} - V_{out})^2$$

<u>V_{IL}</u>	<u>Device</u>	<u>load</u>
$V_{out} \rightarrow \text{high}$	Saturation	linear
Saturation		

$$V_{in} \rightarrow V_{DD}$$

$$V_{out} \rightarrow V_{OL}$$

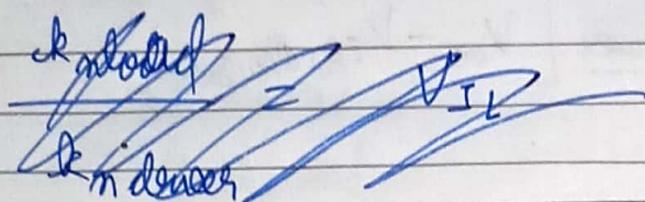
Quadratic eqn solve for V_{out}

$$\frac{dV_{out}}{dV_{in}} = \frac{dV_{DS}}{dV_{in}} \cdot \frac{dV_{out}}{dV_{DS}} = \frac{\gamma}{\beta} \cdot \frac{dV_{out}}{dV_{in}}$$

$$V_{in} \rightarrow V_{IL} \quad \frac{dV_{out}}{dV_{in}} = -1$$

$$\text{LHS} \rightarrow \frac{R_{load}}{2} \left[\alpha(-V_{T\text{diff}}) - \alpha(V_{DD} - V_{out}) \right]$$

$$= \frac{R_n}{2} \underbrace{\text{Device}}_{\alpha} \alpha (V_{IL} - V_{T\text{device}}) \quad (\text{Diff})$$



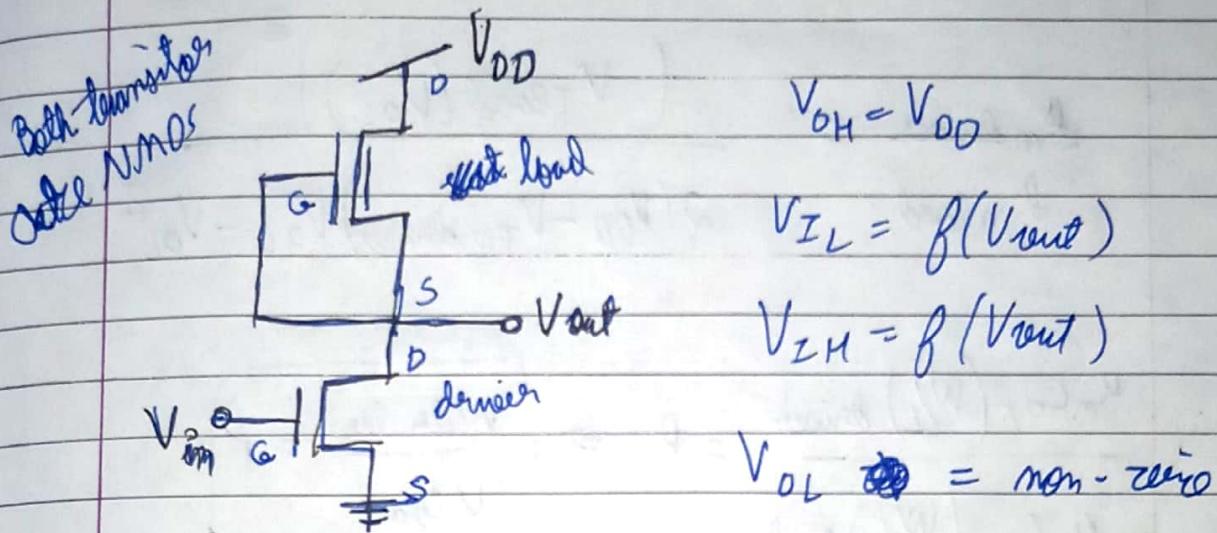
$$V_{IL} = \frac{R_{load}}{R_{device}} \left[-V_{T\text{diff}} - (V_{DD} - V_{out}) \right] + V_{T\text{device}}$$

#	<u>V_{IH}</u>	Load	Device
		Saturation	linear

$V_{T\text{diff}} (V_{out}) \leftarrow$ not neglect V_{out}

06/02/2020

Depletion load Inverter Design

Design \rightarrow (i) for given value of V_{OL}
or

(ii) for given power consumption

For given value of V_{OL}

(i) ignore if not given

driver - linear
load - sat

$$\text{for } V_{OL}, V_{in} = V_{DD}$$

$$\frac{k_m \text{ driver}}{2} \left[2(V_{DD} - V_{TO, \text{driver}}) V_{OL} - V_{OL}^2 \right]$$

$$= \frac{k_m \text{ load}}{2} |V_{T \text{ load}}(V_{OL})|^2$$

No control on: $k_m, t_{ox}, V_{TO, \text{driver}}, V_{TO, \text{load}}$

Final ($\frac{V}{L}$) ratio of both Transistor

$$\frac{R_{in,drain}}{R_{in,load}} = \frac{(V_{T0,load}(V_{OL}))^2}{2(V_{DD} - V_{T0,drain})V_{OL} - V_{OL}^2}$$

$$R_{in,drain} = \frac{1}{2} (I_{load} \times V_{DD})$$

$$\frac{V_{in,drain}(W/L)}{V_{in,load}(W/L)} = \rho \Rightarrow \frac{W_{drain}}{W_{load}} = \rho$$

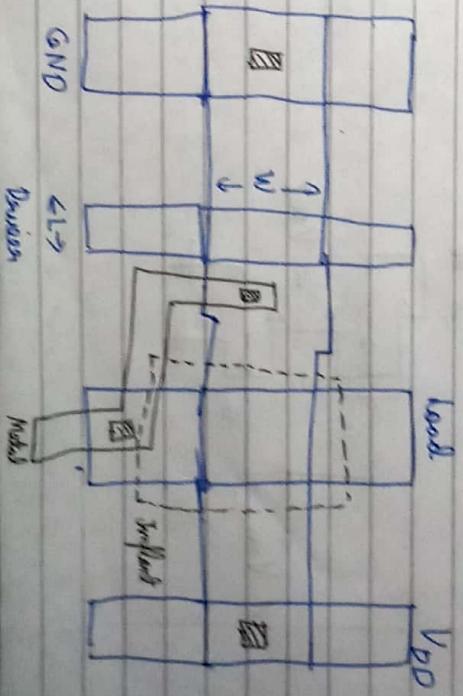
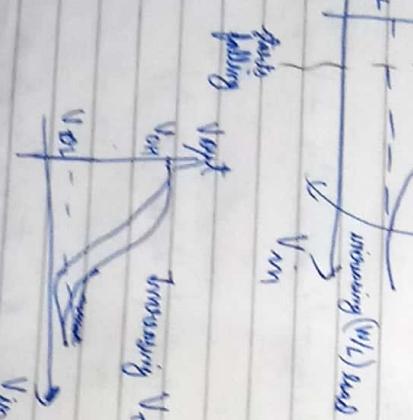
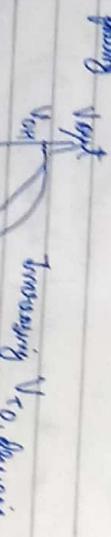
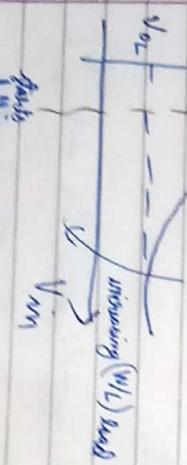
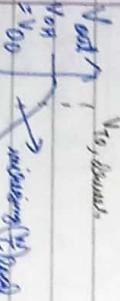
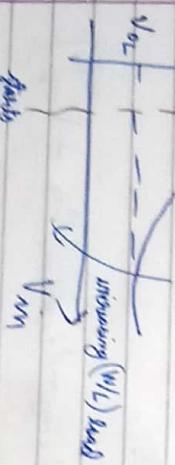
as we prefer L as min length provided by technology

for resistive load inversion

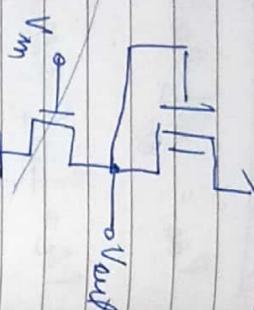
$$P_{DC} = \frac{1}{2} [I_{load} \cdot V_{DD}]$$

$$P_{DC} = V_{DD} \cdot \frac{V_{DD} - V_{OL}}{R_L} \quad \text{find } R_L$$

layout of depletion load inverter



$$\frac{(W/L)_{Device}}{(W/L)_{Load}} = 4$$



Depletion load inverter

Passes Buried Contact
or Bulking Contact

in book

$$V_{DD} \Rightarrow NMOs, P_{dc} = 0$$

$$V_{DD} \Rightarrow V_{GS,load} = V_{DD} - V_{DD} = 0 \Rightarrow V_{Topen} V_{Thresh}$$

(-ve value)

$$PMOS \text{ off}, P_{dc} = 0$$

#

CMOS inverter

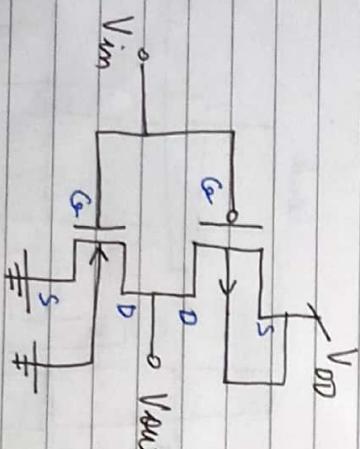
load device is replaced by PMOS

Substrate of PMOS is tied to V_{DD} NMOS is tied to GND

Advantage of CMOS inverter:
Minimal leakage power,
Static power consumption ≈ 0

Disadvantage (i) Mask fabrication complexity
(ii) Full swing

~~Disadvantage~~ (i) Mask fabrication complexity
(ii) Full swing



$$V_{OH} = V_{DD}$$

$$V_{OL} = 0$$

= Full swing