

Pass Transistor Logic

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(*) Reduce the no. of transistors.

(*) In this logic we allow the primary inputs to drive gate as well as source/drain terminals.

Suppose,

| B | A | F | M1 |
|---|---|---|-----------------|
| 1 | A | A | $w \perp$ |
| 0 | x | 0 | $M2 \quad F=AB$ |

⇒ M2 seems to be redundant but is used so that the output is not floating when M1 is off.

(*) Less no. of gates which means lower capacitance.

Logical Effort of AND Gate

① Input \bar{B} : $R = R_N$

$$C = WC_{dr}$$

$LE = \frac{1}{3}$ (which is very faster than all Passistor)

② Input \bar{A} :

$$R = 2R_N$$

$$C = 3WC_g$$

$$\therefore LE = 2$$

(which is very slower than Passistor)

③ Input B:

$$R = 2R_N$$

$$C = WC_g$$

$$\therefore LE = \frac{2}{3}$$
 (faster than Inv.)

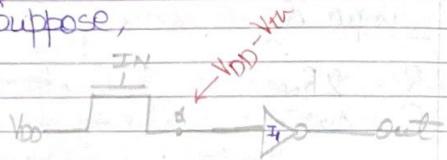
(*) Critical Signal is tied to Input B rather than Input A.

① Charge Leakage when $IN=0$

Explanation → Pg-365 (Kang)

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Suppose,



When $IN=0$, $d = z$

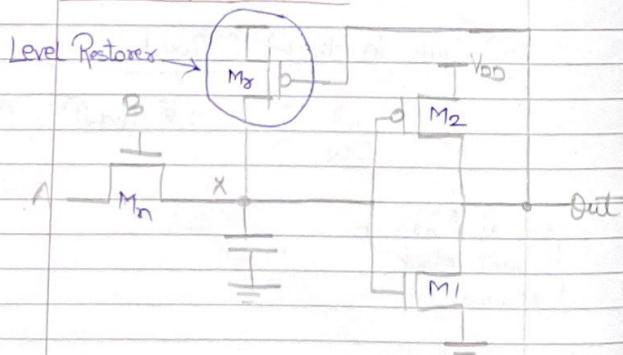
$IN = 1$, $d = VDD - Vth$

Now, the pmos of the inverter (π) is at the edge of conduction.

So there will be huge short circuit powers since NMOS will also be on at $d = VDD - Vth$.

To solve this problem we have a no. of solutions :

① Level Restorers →



Assume, $X = 0V$ when $B=VDD$ & $A=0$

Then, $Out = VDD \Rightarrow M_2$ is off

When $A = 0$

Then $X = VDD - Vth$ and M_3 is on and $V_{out} = 0$

M_3 is on, which pulls the node X upto VDD .

This eliminates the static power dissipation of inverter and, no static current path b/w level restorer and the pass transistors.

⇒ This solution seems appealing but adds complexity and make the circuit saturated.

Since M_3 tries to dec the vol of X to $VDD - Vth$ while M_2 tries to inc it to VDD .

Sizing Problem

⇒ R_s must not be made too small, such that the voltage at X doesn't drop to switching threshold of inverter.

M_3 Resistance

\Rightarrow Another disadvantage,

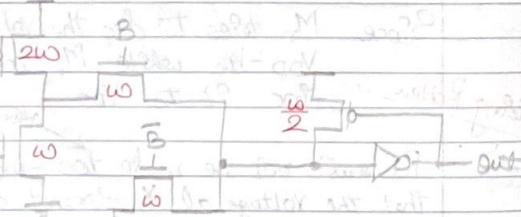
Dec. in switching speed of the device
The cap at node X is increased by
restoring device

The rise time of the gate is further
negatively affected, since M_2
fights the dec in voltage at node
X before being switched off.

Advantage \rightarrow

The fall time is reduced (+vely affected)
Since the PMOS are turned on
speeds the pull-up action.

LE with level restoration



Of B:

$$R = 4R_N \rightarrow R_P = 4R_N$$

$$C = WC_g$$

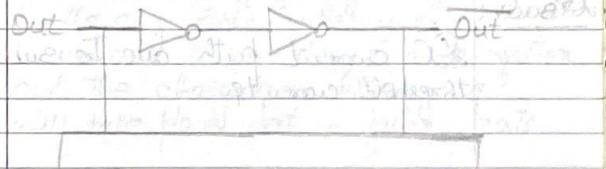
$$R_m = 2R_N$$

$$\therefore \text{Rtine} = \frac{R_m}{\left(1 - \frac{R_m}{R_P}\right)}$$

$$\therefore LF = \frac{4}{3}$$

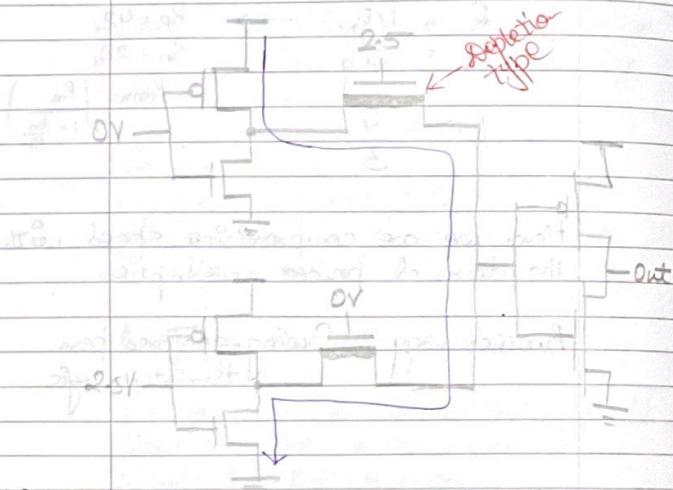
Hence we are compromising speed with
the decreased power consumption.

Another way; Swing-restored pass
transistor logic



Complementary output
NMOS pass transistor
Network

② Multiple-Threshold Transistor:



Ques:

DC current path due to sub-threshold current?

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Kang → 270 pg

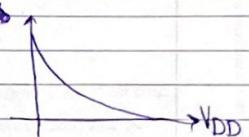
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Voltage Boosting →

It is a dynamic circuit technique for overcoming threshold voltage drops in digital circuitry.

Eg → In pass transistor logic, in enhancement load inverters

Q → Reason behind:



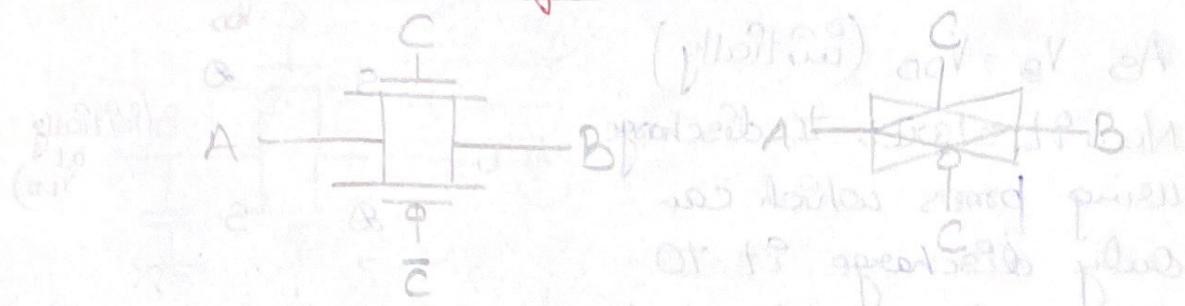
Sol → This is because, inc. the VDD will inc. the rate of flow of charge (current) in the ckt since resistance is constant. Hence the is more faster and the charging or discharging will take place at a fast rate.

Misconception:

$V_{DD} \uparrow$ the cap will have to charge to a higher value. So, more time it will take.

Because time taken to charge or dis. a cap. depends on RC , and not on V_{DD} . $(T=RC)$

③ Transmission gates.



- ★ The nmos passes strong 0 and pmos passes strong 1. So this combines the best of both device features.
- ★ TG is a bidirectional switch controlled by C.

If, $C = 1$, $A = B$
 $C = 0$; Both transistors are in cutoff
 creating an open circuit b/w A and B.

Concept of charging and discharging node B.

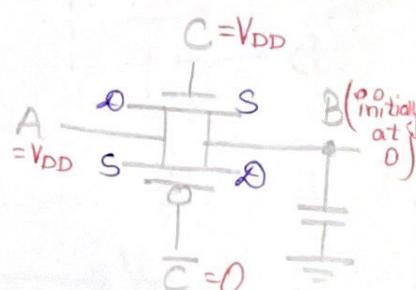
Case I: Charging node B from OV to VDD.

If only nmos was present
 then $V_B = V_{DD} - V_{th}$

After which nmos turns off

But since a pmos is also present and is ON.

So the PMOS will charge V_B upto V_{DD} .

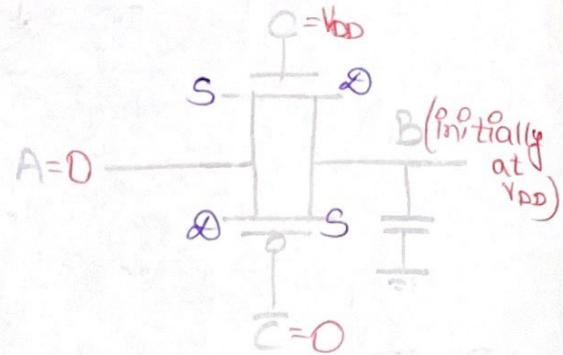


Case II: Discharging node B from V_{DD} to ground.

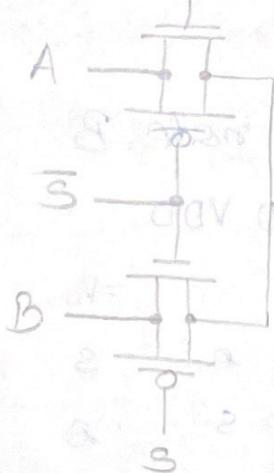
As $V_B = V_{DD}$ (initially)

Now it starts to discharge using PMOS which can only discharge it to V_{th} , since after that PMOS turns off.

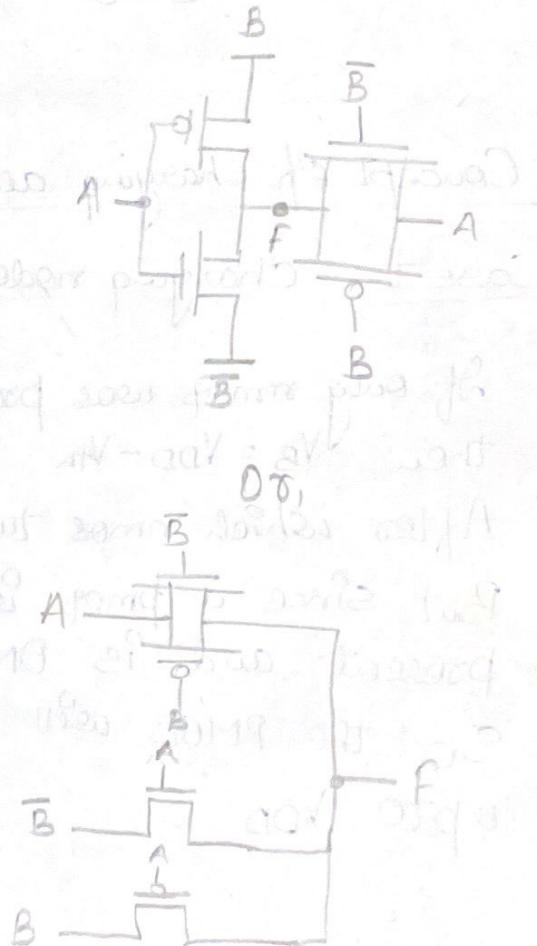
But the NMOS is still on which takes V_B to ground.



2:1 Mux using TG

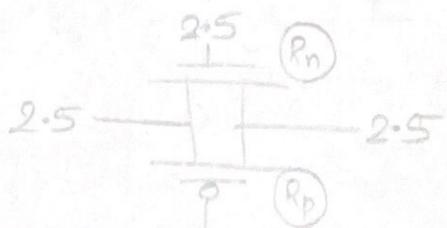


XOR using TG



(2)

Resistance of Transmission Gates



post technology Optimal design values p. 7 No. 3

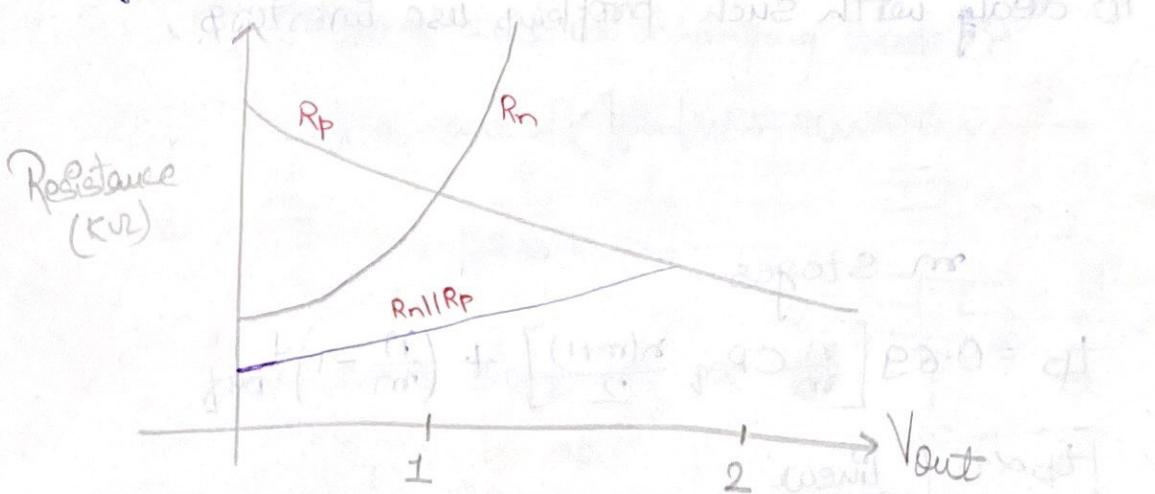
$$R_{N, PU} = 2 R_{N, PD}$$

$$R_{P, PD} = 2 R_{P, PU}$$

0 to 1: $R_{eff} = R_p \parallel 2R_n = 2R_n \parallel 2R_n = R_n$

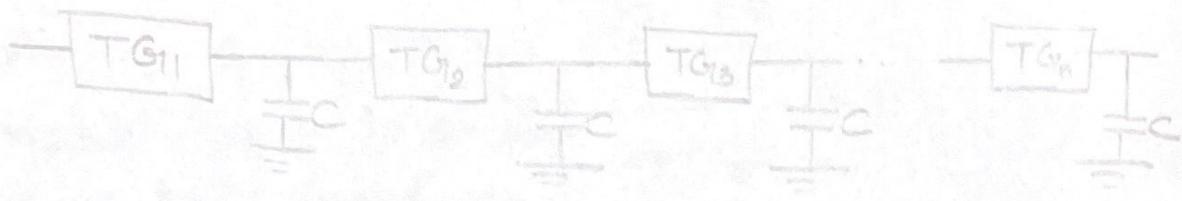
1 to 0: $R_{eff} = R_n \parallel 2R_p = R_n \parallel 4R_n = 0.8R_n$

* Both resistances are not same but for digital logic both can be approximated to be equal.

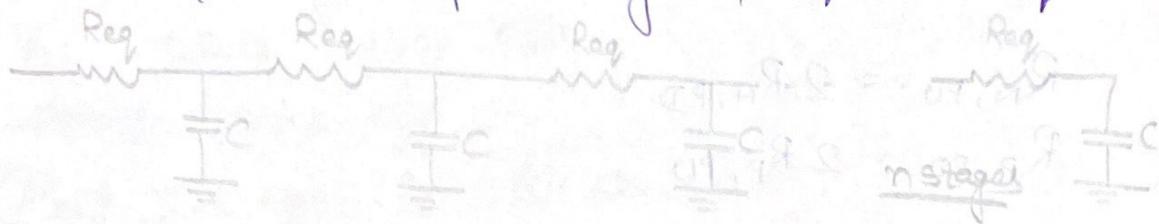


The resistance $R_n \parallel R_p$ is approximately constant

Delay associated with chain of T.G.



Each T.G. can be replaced by its equivalent Reg.

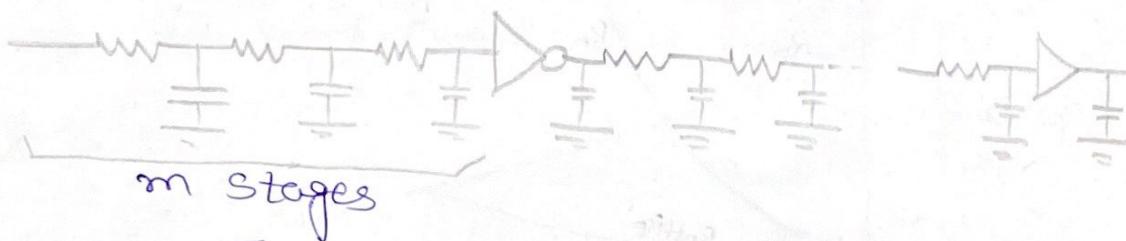


$$t_p = 0.69 \sum_{k=0}^n C_{\text{Reg}} \cdot K = 0.69 C_{\text{Reg}} \cdot \frac{n(n+1)}{2}$$

$$t_p \propto n^2$$

So, propagation delay inc. rapidly with the no. of switches.

To deal with such problems use inverters,



$$t_p = 0.69 \left[\frac{m}{m} C_{\text{Reg}} \frac{n(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{\text{buf}}$$

$$t_p \propto n \quad \text{linear}$$

Optimal value of m can be found by $\frac{\partial t_p}{\partial m} = 0$.

$$\therefore m_{\text{opt}} = 1.7 \sqrt{\frac{t_{\text{buf}}}{C_{\text{Reg}}}}$$

Dynamic CMOS Design

It's also an alternate logic design style that avoids static power consumption with $(N+2)$ transistors in addition to a clock input.



Static Circuits

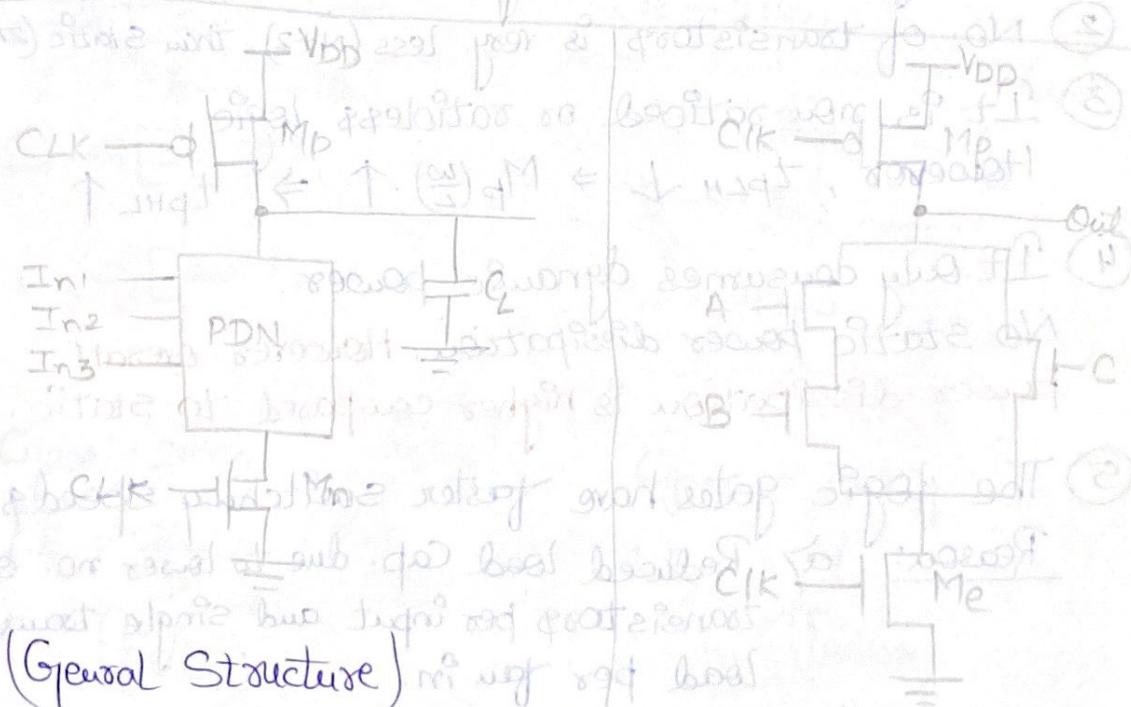
- At every point in time (except during switching) the output is connected to either VDD or GND via a low resistive path.
- If $f_{\text{fanin}} = n$

Then, $2n$ transistors
 $(N\text{-type} \rightarrow n)$
 $P\text{-type} \rightarrow n$

Dynamic Circuits

- Rely on the temporary storage of signal values on the capacitance of high impedance nodes.

- If $f_{\text{fanin}} = n$
- Then $(n+2)$ transistors
 $(N\text{-type} \rightarrow n+1)$
 $P\text{-type} \rightarrow n+1$



Example: $\text{Out} = \overline{(AB+C)}$

When,

- ① $\text{CLK} = 0$ or negative edge

$M_p \rightarrow \text{ON}$ }
 $M_e \rightarrow \text{OFF}$ } The node Out is charged to V_{dd} .
This is called precharge phase.

- ② $\text{CLK} = 1$ or positive edge.

$M_p \rightarrow \text{OFF}$ }
 $M_e \rightarrow \text{ON}$ } The node out is conditionally discharged to GND based on the input values and the pull down topology.
This is called evaluation phase.

Some properties of dynamic logic:

- ① The logic is implemented by NMOS PDN.
- ② No. of transistors is very less ($N+2$) than static ($2N$).
- ③ It is non-saturated or ratiodless logic.
However, $t_{PLH} \downarrow \Rightarrow M_p(\frac{w}{L}) \uparrow \Rightarrow t_{PHL} \uparrow$
- ④ It only consumes dynamic power.
No static power dissipation. However overall power dissipation is higher compared to static.
- ⑤ The logic gates have faster switching speeds.
Reason:
 - a) Reduced load Cap. due to lower no. of transistors per input and single transistor load per fan in.
 - b) No short circuit current, and all the current provided by the pull down devices goes towards discharging C_L .
- ⑥ Full Swinging Output.

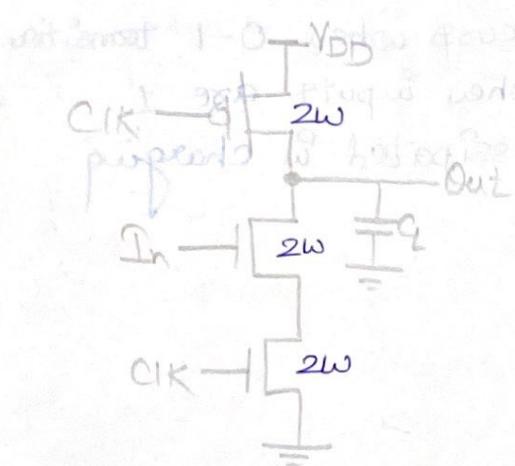
(4)

Conditions on Output

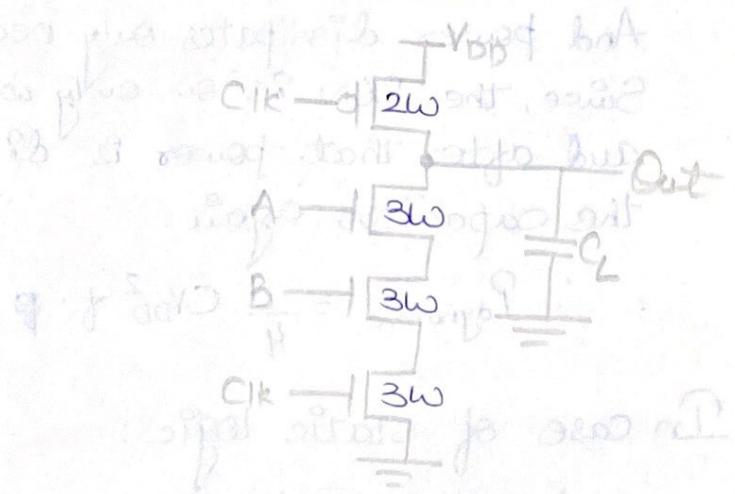
- ① Once the output of a dynamic gate is discharged, it can't be charged until the next precharge operation.
- ② Inputs to the gate can make at most one transition during evaluation.
- ③ Output can be in high impedance state during and after evaluation (PDN off), state is stored in C_L .

Logical Effort of Dynamic Gates

Inverter



NAND



$$C_{gate} = 2wC_g$$

$$LE = \frac{2}{3}$$

(Faster)

$$C_{gate} = 3wC_g$$

$$LE = 1$$

(Faster)

★ Dynamic logic gates by construction can at most have one transition per clock cycle.

So, Glitching and dynamic hazards doesn't occur in dynamic logic.

Power dissipation of dynamic logic

$$P = CV_{DD}^2 f \cdot p$$

↑ probability.

In case of dynamic logic:

$$p = \frac{1}{4} \quad (0-0, 0-1, 1-0, 1-1)$$

And power dissipates only occurs when 0-1 transition. Since, the PDN is on only when inputs are 1 and after that power is dissipated in charging the capacitor again.

$$\therefore P_{\text{dynamic}} = \frac{1}{4} CV_{DD}^2 f \cdot p$$

In case of static logic:

$$p = \frac{1}{2} \quad (0-1, 1-0)$$

$$\therefore P_{\text{static}} = \frac{1}{2} CV_{DD}^2 f$$

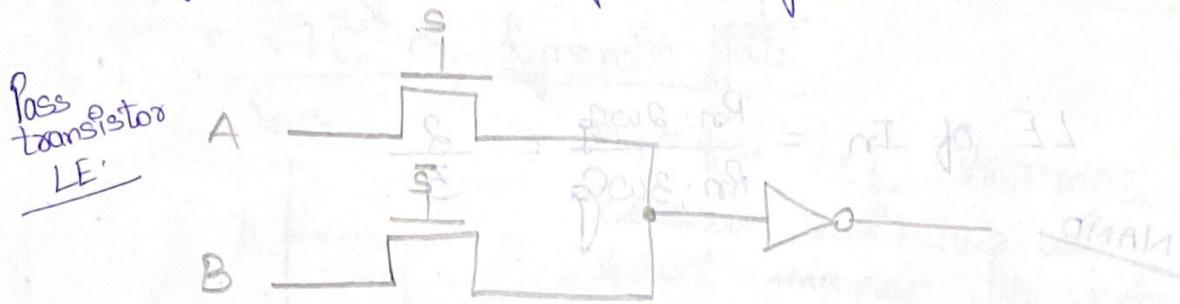
Hence static power dissipation reduces in dynamic logic.

(5)

The overall power dissipation increases because:

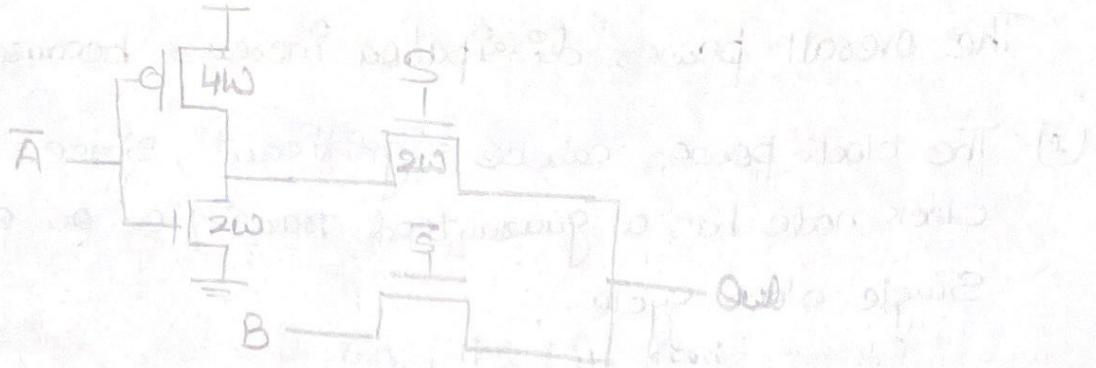
- (1) The clock power can be significant, since clock node has a guaranteed transition on every single clock cycle.
- (2) The no. of transistors is higher than the minimal set required for implementing the logic.
- (3) Short-circuit power may exist when leakage combatting devices are added.
- (4) Dynamic logic displays a higher switching activity due to the periodic precharge and discharge operations.

Logical Effort of dynamic logic

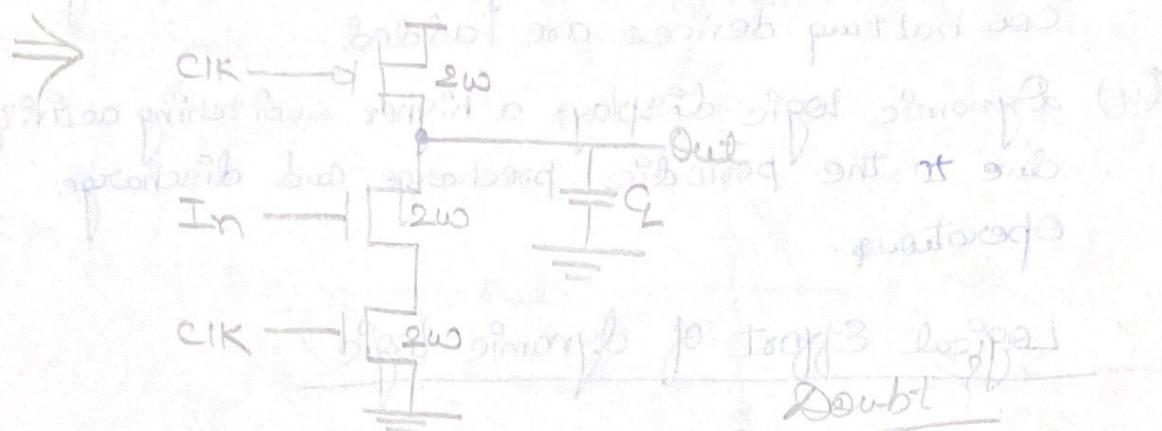


Since there is no V_{DD} or GND connection to output node, it is very difficult to analyze its LE.
It is also a bidirectional gate.

So we need to consider the previous gate to find its LE.

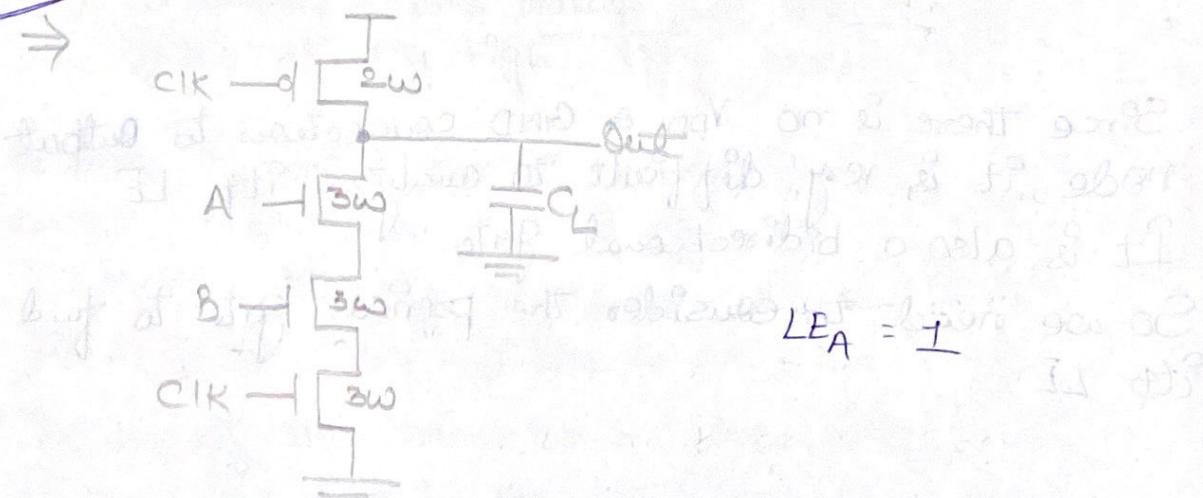


$$LE \text{ of } S = \frac{R_n \cdot 2w_g}{R_n \cdot 3w_g} = \frac{2}{3}$$

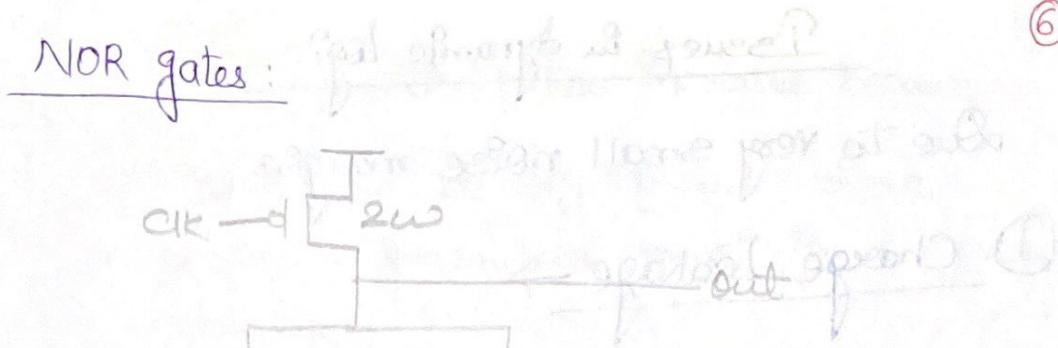


$$LE \text{ of } In = \frac{R_n \cdot 2w_g}{R_n \cdot 3w_g} = \frac{2}{3}$$

NAND



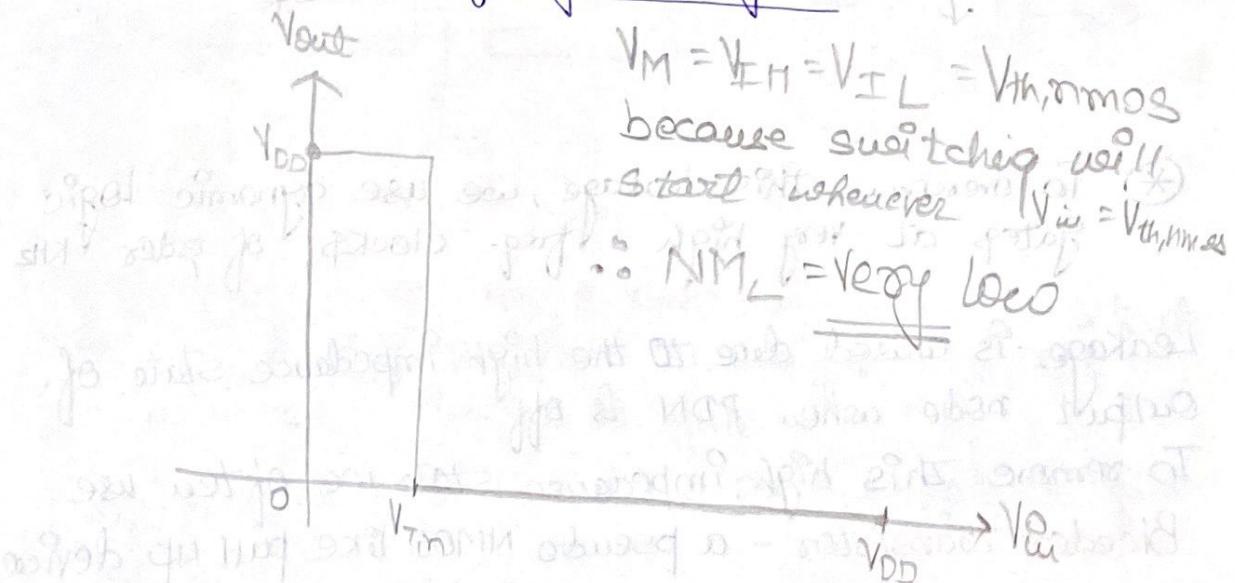
⑥

NOR gates:

$$LE = \frac{2}{3}$$

The LE of NOR < NAND in dynamic logic.
So we prefer to use nor here.)

VTC of dynamic gate



$$V_M = V_{THH} = V_{IL} = V_{th,nmos}$$

because switching will start whenever $V_{in} = V_{th,nmos}$

$$\therefore NM_L = V_{DD} \text{ bco}$$

which is high and min obtained is $V_{th,pmos}$

$$NM_L = V_{Thn} \leftarrow \text{which is very low. most diff to see off}$$

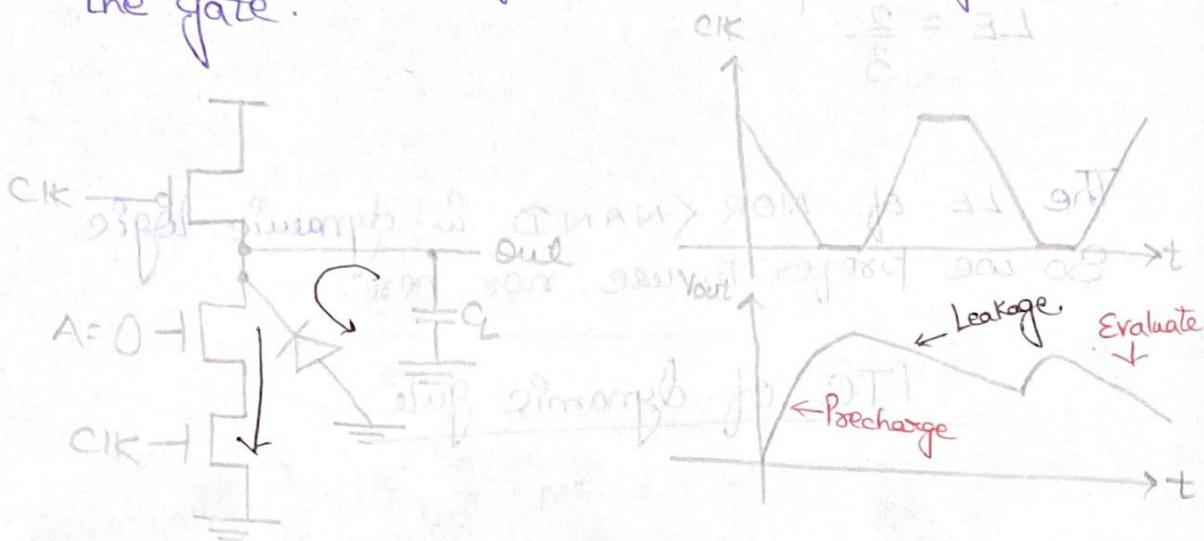
$$NM_H = 0 \leftarrow \text{switching will start least speed}$$

Tissues in dynamic logic

Due to very small noise margins.

① Charge Leakage →

When PDN is off, the output should ideally remain at V_{DD}, i.e. in precharge phase, during the evaluation phase. However, this is not practical, the charge gradually leaks away due to leakage currents, resulting in a malfunctioning of the gate.



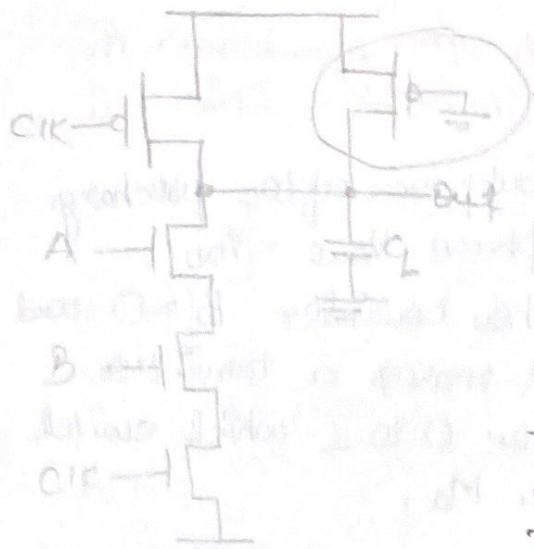
✳ To overcome this leakage, we use dynamic logic gates at very high freq. clocks of order KHz.

Leakage is caused due to the high impedance state of output node when PDN is off.

To remove this high impedance state we often use Bleeder transistor - a pseudo NMOS like pull up device.

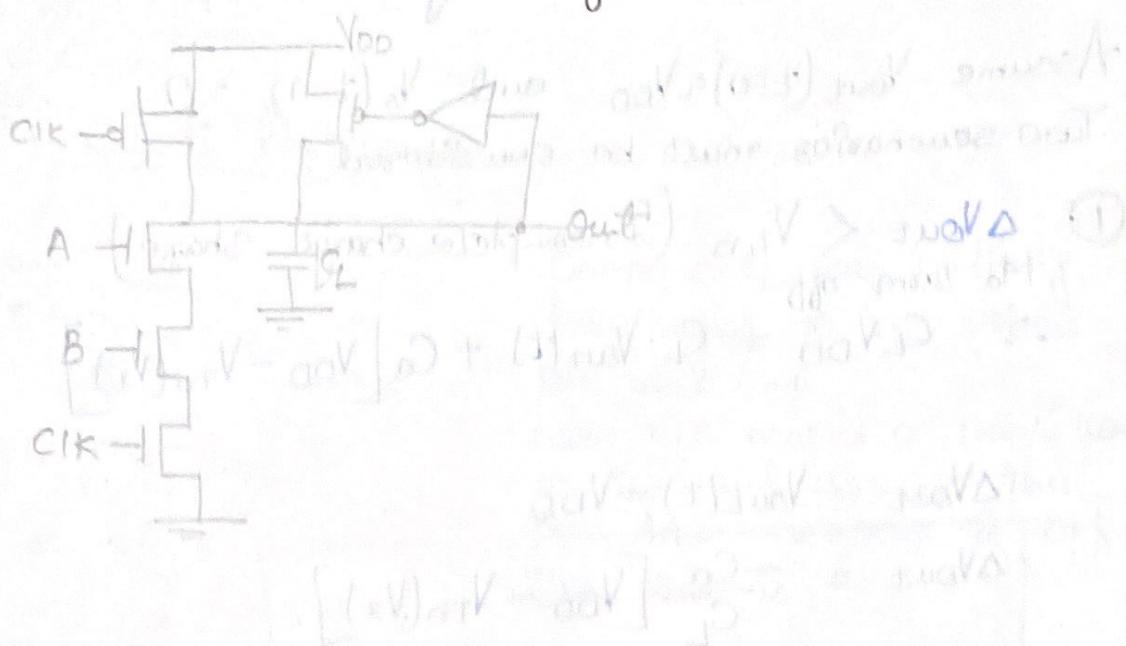
The use of this transistor is to compensate for the charge lost due to the pull down leakage path.

(7)



Bleeder ; The resistance of this is made high so that the PDN can lower the output node voltage below the switching threshold of inverter.

But the problem here is that the circuit now has static power dissipation. To eliminate this problem, we use feedback.

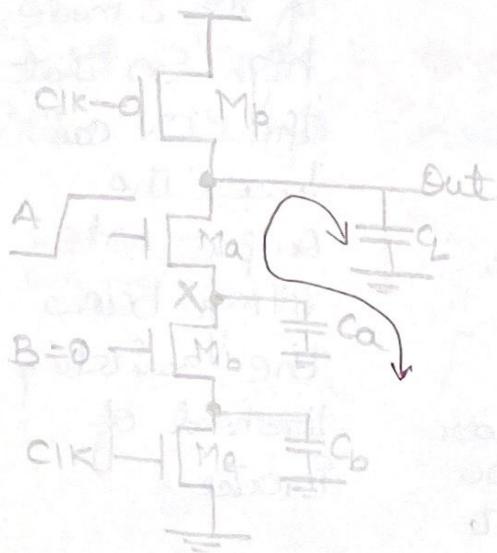


(with open drain) $v_{out} - v_{in} \leq \text{vdd}$

$$(D + P) \text{ mV} < \text{vdd}$$

$$P = 0.5 \text{ mV}$$

② Charge Sharing →



Suppose after precharge phase $V_{out} = V_{DD}$,

Then consider $B = 0$ and A makes a transition from 0 to 1 which switch on M_a .

Now the charge on C_Q is redistributed on C_a .

This causes drop in output voltage.

~~Assume $V_{out}(t=0) = V_{DD}$ and $V_x(t=0) = 0$~~

Two scenarios must be considered:

① $\Delta V_{out} < V_{Tn}$ (Incomplete charge share)

M_a turns off

$$\therefore C_L V_{DD} = C_L \cdot V_{out}(t) + C_a [V_{DD} - V_{Tn}(V_x)]$$

Body Effect

$$\Delta V_{out} = V_{out}(t) - V_{DD}$$

$$\boxed{\Delta V_{out} = -\frac{C_a}{C_L} [V_{DD} - V_{Tn}(V_x)]}$$

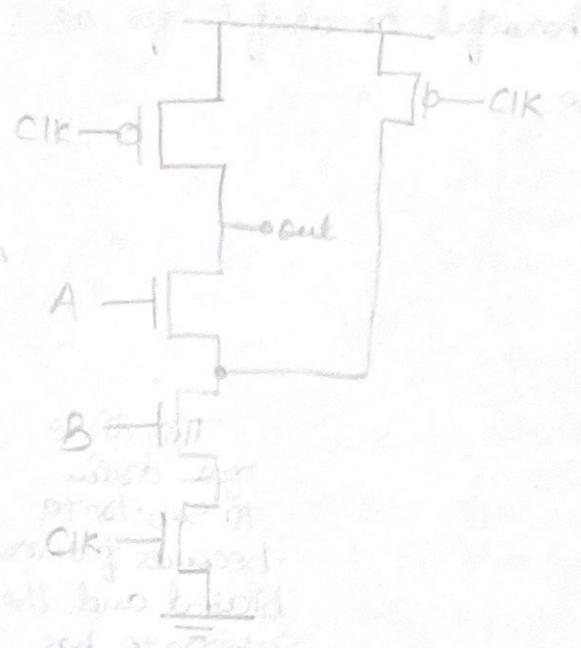
② $\Delta V_{out} > V_{Tn} - V_{out}$ (Complete charge share)

M_a turns on.

$$C_L V_{DD} = V_{out} (C_L + C_a)$$

$$\boxed{V_{out} = -V_{DD} \frac{C_a}{C_a + C_L}}$$

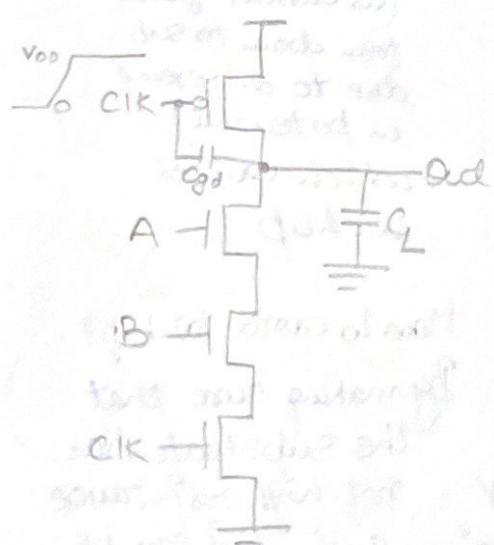
To overcome this difficulty we also precharge the critical internal nodes.



Disadvantage:

- ① Due. of capacitance
So delay inc.

③ Clock Feedthrough →



Suppose Q was initially precharged to V_{DD} when clk was low.

Now clk makes a transition to V_{DD} and assume the pull down network is off. Then V_{out} is,

$$V_{DD}(C_L + C_{gd}) = V_0 Q + (V_0 - V_{DD}) C_{gd}$$

$$V_{DD}(C_L + C_{gd}) = V_0(Q + C_{gd}) - V_{DD} C_{gd}$$

$$V_0(C_L + 2C_{gd}) = V_{DD}Q + 2V_{DD}C_{gd}$$

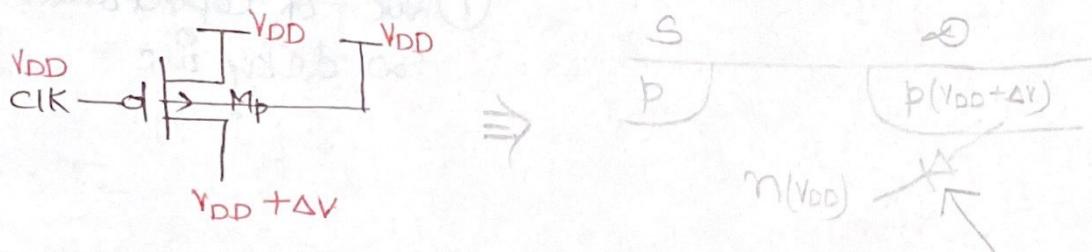
$$V_0 = V_{DD} \frac{(Q + 2C_{gd})}{(C_L + C_{gd})}$$

Here $V_o > V_{DD}$

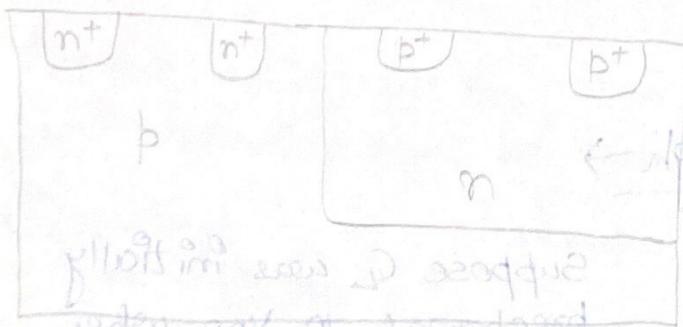
It means our output exceeds the input supply.

Q → Is this inc. in voltage harmful or useful for us?

SOL → Harmful. Because,



latchup



This npnp structure is called a thyristor.

As soon as the thyristor turns on it is very difficult to turn it off.

It is turned on as $V_{BE} = 0.6V$. A high current flows from drain to substrate which just melts the chip.

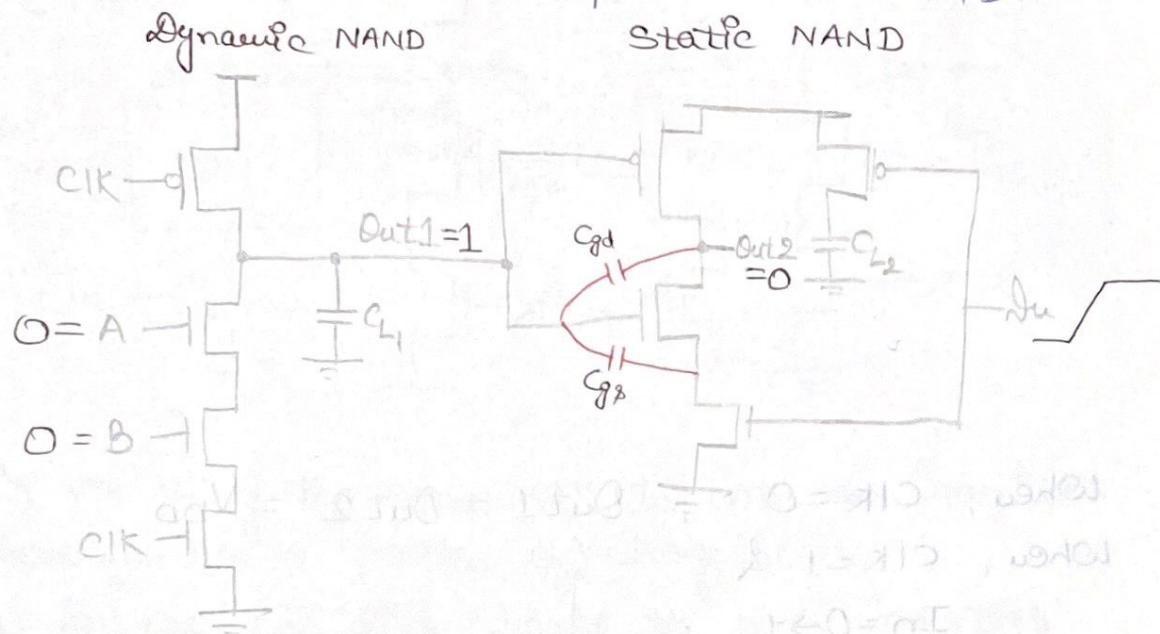
This diode from drain to substrate becomes forward biased and the substrate has resistance which creates voltage (as current flows from drain to sub. due to difference in potential) which causes latchup.

How to avoid latchup?

By making sure that the substrate has not high resistance and this can be done by reducing the length of substrate to V_{DD} or ground.

④ Backgate Coupling →

Consider a two input NAND gate (dynamic) which drives a two input static NAND.



As $Out1$ gets precharged and the other input ($O = B$) of the static NAND is switched to 1, the output of NAND ($Out2$) is 0.

Now the two capacitors C_{d1} and C_{d2} starts getting charged by $Out1$ and $Out1$ starts decreasing which can invert our logic.

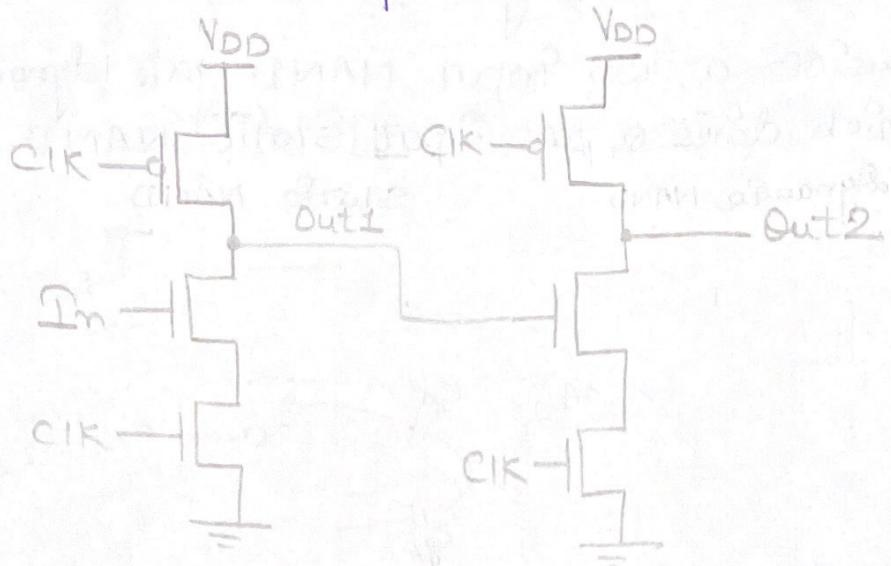
⑤ Capacitive coupling

⑥ Substrate noise

⑦ Minority charge injection

⑧ Supply noise (Ground bounce)

Cascading two Inverters



When, $C1K = 0$; $Out1 = Out2 = V_{DD}$

When, $C1K = 1$ &

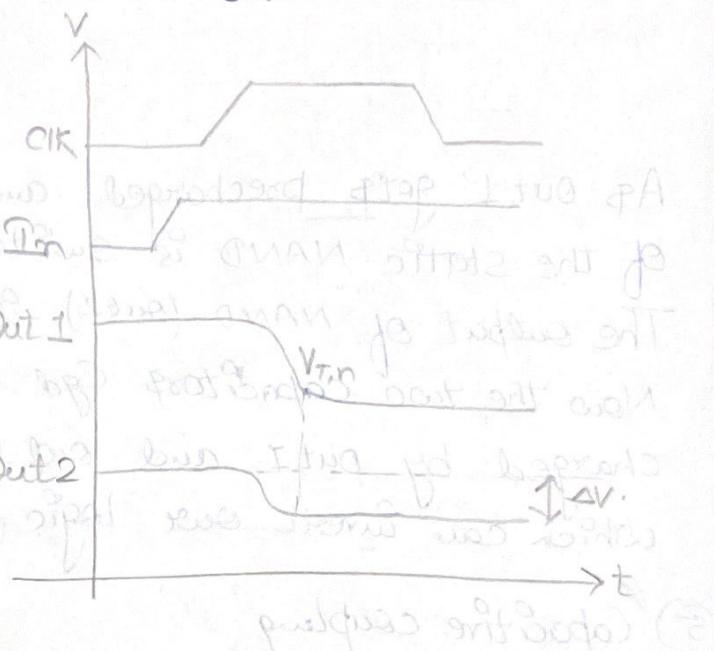
$In = 0 \rightarrow 1$;

$Out2$ is hanging
in middle at

$$V = \Delta V.$$

Hence,

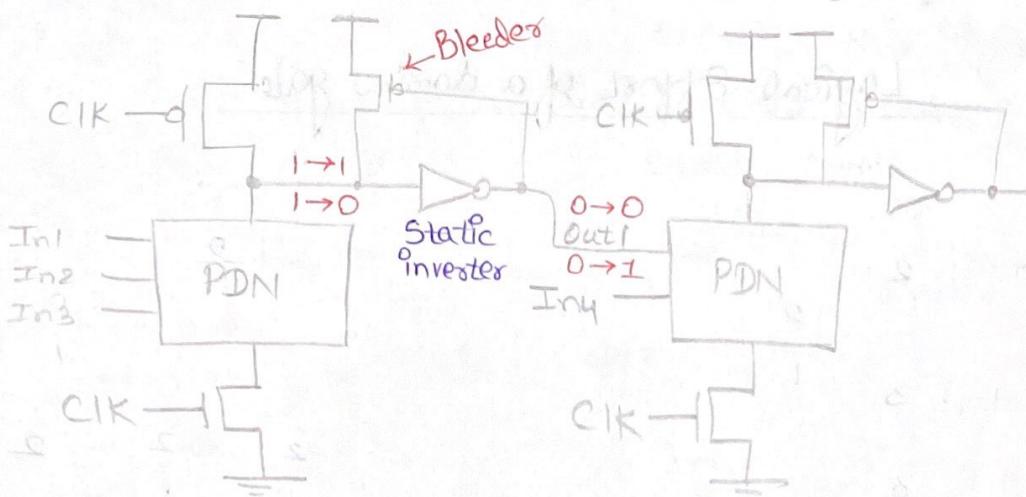
Only $0 \rightarrow 1$ transitions $Out2$
allowed at Input.



This can be solved by using an inverter in
between two inverters.

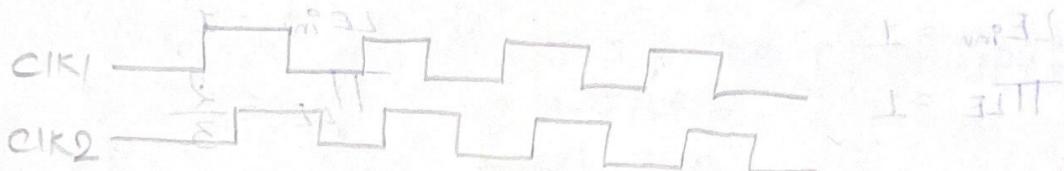
Explanation in Kang pg-382

Domino logic



If we apply the same CLK to both the inverters there can be a problem of charge loss.

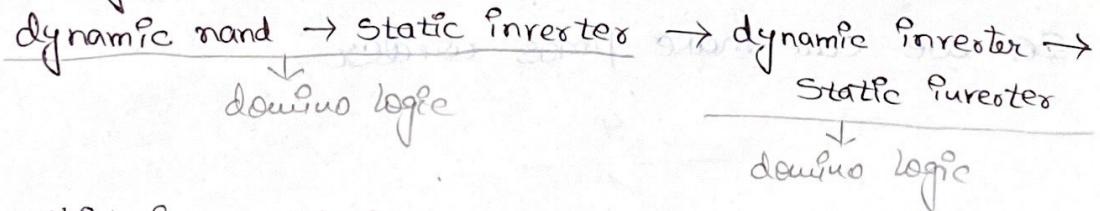
So we use two diff. clocks for both inverters.



Properties:

- ① Only non-inverting gates can be implemented using domino logic because the inverter at the output of each stage cancels the inversion.

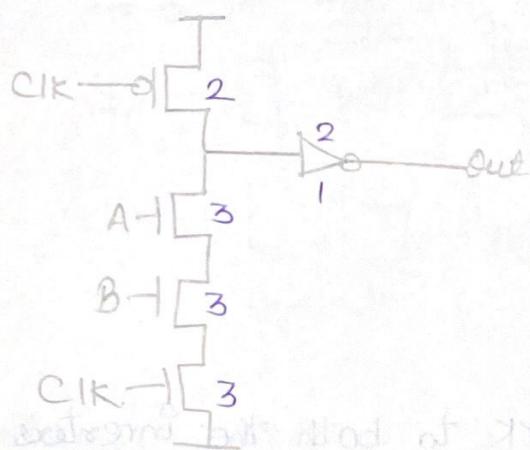
If you want to implement NAND then,



which is not NAND.

② Very high speeds can be achieved.

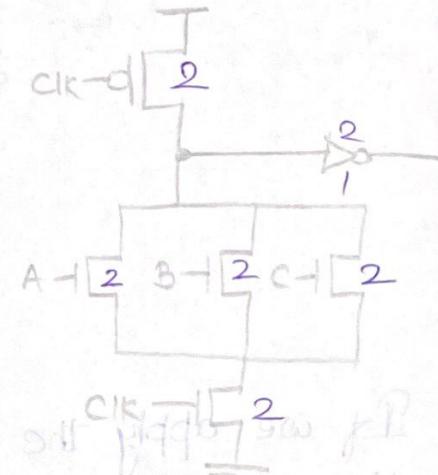
Logical Effort of a domino gate



$$LE_{dyn} = 1$$

$$LE_{inv} = 1$$

$$TTL_E = 1$$



$$LE_{dyn} = \frac{2}{3}$$

$$LE_{inv} = 1$$

$$TTL_E = \frac{2}{3}$$

∴ NOR is a better structure than NAND.

Now, we cheat a little bit:

we only care about $0 \rightarrow 1$ transition of inverter
because

so we can make pmos wider.

