# YANG model and implementation of Network Interconnect Tester

- IETF113 Hackathon
- March 19-20, 2022
- Online



# The project

## Specification:

\* draft-vassilev-bmwg-network-interconnect-tester-07

### Client side:

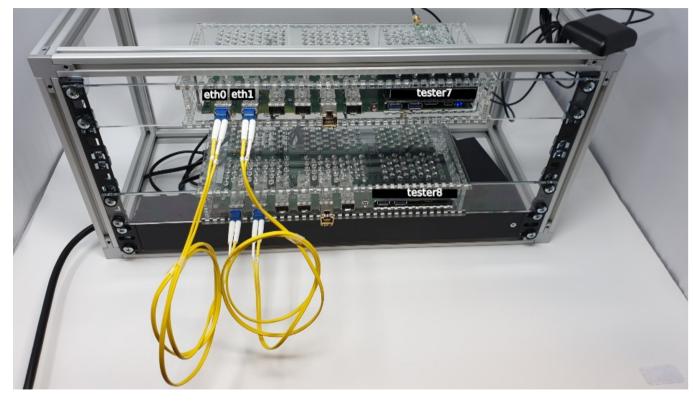
\* Example script - rfc2544.py benchmark (Python)

### Device side:

- \* Software YANG/NETCONF server instrumentation code (C)
- \* Firmware (<u>Verilog</u>)
- \* Hardware off-the-shelf FPGA module Ultra96 + 6x SFP+ network programmability kit shield (KiCAD, Walk-through)

```
eth0 |
eth1
   +-<|TG tester7 TA|<-+
   +->|TA tester8
                    TG|>-+
 eth0
eth1
   +-<|TG tester0 TA|<-+
```

# Setup



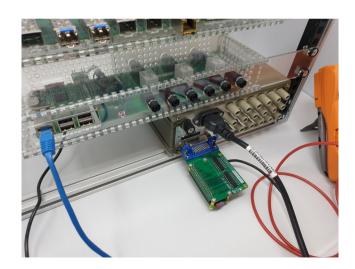
# Design and implementation

```
NETCONF Server (Model (YANG), Implementation Generator module (\underline{C}), Analyzer module (\underline{C}))
TRAFFIC-GENERATOR-SW (C)
                                         TRAFFIC-ANALYZER-SW (C)
Socket API
                                          Socket API
Kernel
        Sync ->{RTCLOCK}(Verilog)
                                             Kernel
DMA
                                           DMA
  | [AXI]
                                            [IXA]
MAC TRAFFIC-GENERATOR-HW (C, Verilog)
                                                  TRAFFIC-ANALYZER-HW (C, Verilog)
                                           MAC
   GMII MUX
      | [GMII]
                                                   [GMII]
     PHY
                                                PHY
    SFP+ TX
                                               SFP+ RX
```

\* - underlined text has links to repositories

# What got done

- \* Work on the rfc2544.py script RFC2544 sec. 26.6 Reset (Python).
- \* Work on YANG/NETCONF managed 59306A relay actuator.



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# Remaining work

\* Multi-stream implementation