

Design Rule Check

Design Rules Check

Design Rules Options | Electrical Rules | Physical Rules | ERC Matrix

Scope

- ☒ Check entire design
- ☐ Check selection

Mode

- ☐ Use occurrences
- ☒ Use instances (Preferred)

Action

- ☒ Check design rules
- ☐ Delete existing DRC markers
- ☐ Create DRC markers for warnings
- ☐ Preserve waived DRC

Ignore DRC Warnings: ...

Design Rules

- ☒ Run Electrical Rules
- ☐ Run Physical Rules

Report File: ☒ View Output

C:\WORK\W00_IGSW01_WSMW02_SCHEMATIC\IGSHARE

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Electrical Rules

- ☒ Check single node nets
- ☒ Check no driving source and Pin type conflicts
- ☒ Check duplicate net names
- ☐ Check off-page connector connections
- ☐ Check hierarchical port connections
- ☒ Check unconnected bus nets
- ☒ Check unconnected pins
- ☐ Check SDT compatibility

Custom DRC

- ☐ Run Custom DRC
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Reports

- ☐ Report all net names
- ☐ Report off-grid objects
- ☐ Report hierarchical ports and off-page connectors
- ☐ Report misleading tap connections

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Physical Rules

- ☒ Check power pin visibility
- ☒ Check missing/illegal PCB Footprint property
- ☒ Check Normal Convert view sync
- ☒ Check incorrect Pin Group assignment
- ☒ Check high speed props syntax
- ☒ Check missing pin numbers
- ☒ Check device with zero pins
- ☒ Check power ground short
- ☒ Check Name Prop consistency

Custom DRC

- ☐ Run Custom DRC
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Reports

- ☐ Report visible unconnected power pins
- ☒ Report unused part packages
- ☒ Report invalid Refdes
- ☒ Report identical part references