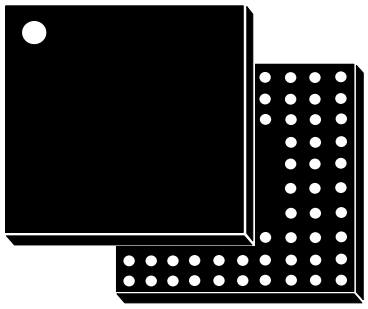
STHV64SW

64-Channels ±100 V, (from -200V÷0V to 0V÷200V), Low Harmonic Distortion, High Voltage Analog Independent Switches

TFBGA 12x12x1.2 196 BALLS



MAIN FEATURES

- 200V peak to peak input and output signal;
- Three different operative ranges:
  - From -100V to +100V
  - From 0V to 200V
  - From -200V to 0V
- Very fast input slew rate (40V/ns);
- Only +3.3V Low Voltage supply;
- Rail to Rail Input Signal
- Low on resistance (10Ω);
- Very low cross talk between channels;
- Low parasitic capacitance;
- 40kΩ bleed resistor on the outputs;
- Recirculation Current protection on both input and output
- Thermal and Under Voltage Protection;
- Latch up free;
- Control through serial interface;
- 20 MHz data shift clock frequency;
- Cascadable serial register with latches;

Applications

- Medical ultrasound imaging
- NDT ultrasound transmission
- Piezo-electric transducers driver
- Industrial

Order codes

Order Code	Package	Packaging
STHV64SW	BGA-196	Tray

Contents

1 Description

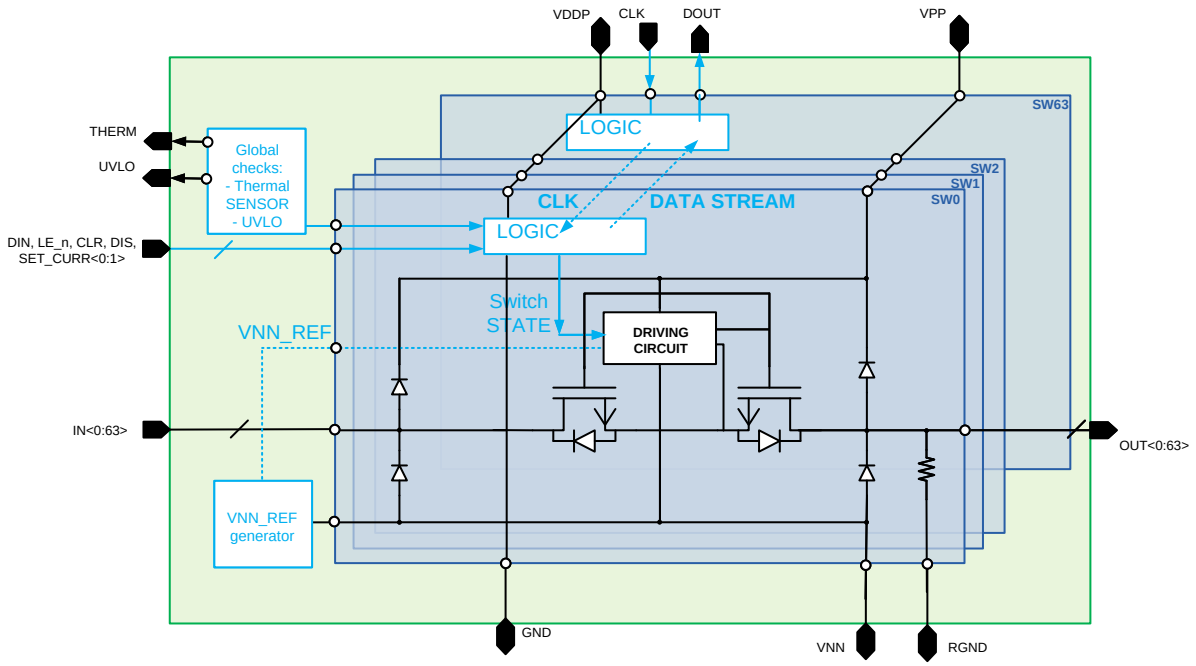


Figure 1 - STHV64SW internal block diagram

This integrated circuit features 64 independent switches.

It is designed for medical ultrasound applications, but it can also be used for driving other piezoelectric, capacitive or MEMS transducers and in industrial application, as a generic high voltage switch.

The STHV64SW comprises a shift register for serial communication, self-biased high voltage MOSFET gate drivers, high power N-channel MOSFETs for each switch, (clamping to-ground circuitry), thermal sensor, under voltage lockout. Moreover, the STHV64sw includes self-biasing and thermal shutdown blocks. The switch is able to provide up to ±3A peak output current.

The STHV64SW internal self-biasing circuitry prevents from using dedicated external high voltage rails to drive the gates of the driving circuit that turn-off the switch.

The STHV64SW requires very few external components:

- decoupling capacitors to GND tied to pins VPP (VNN) and VDDP
- resistor for the pulling up of the THERM_UVLO pin

Each switch is independently controlled by means of 1 digital bit. An external clock has to be used to communicate the data through the shift register

STHV64sw is fully power-up and power-down sequence free.

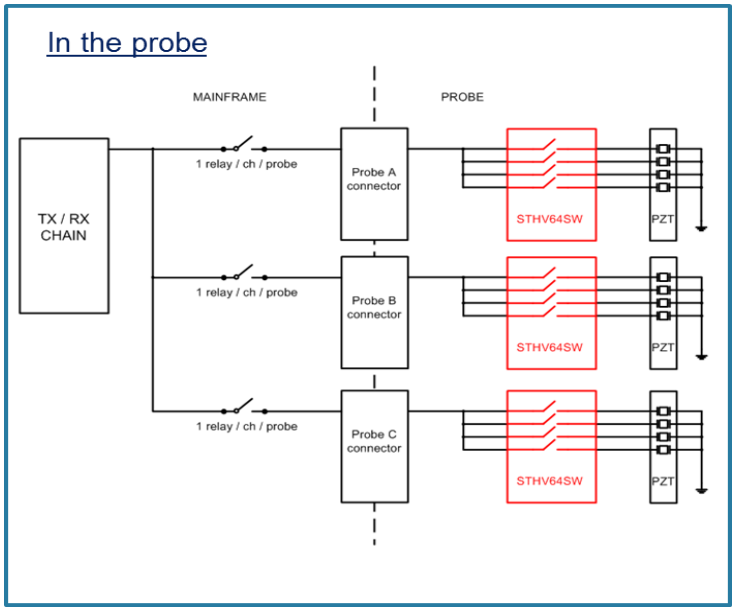


Figure 2

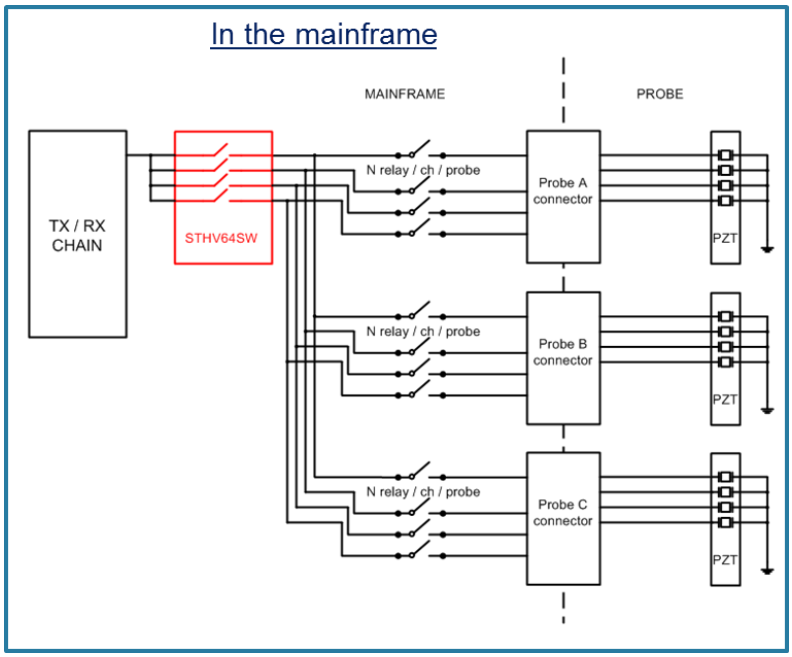
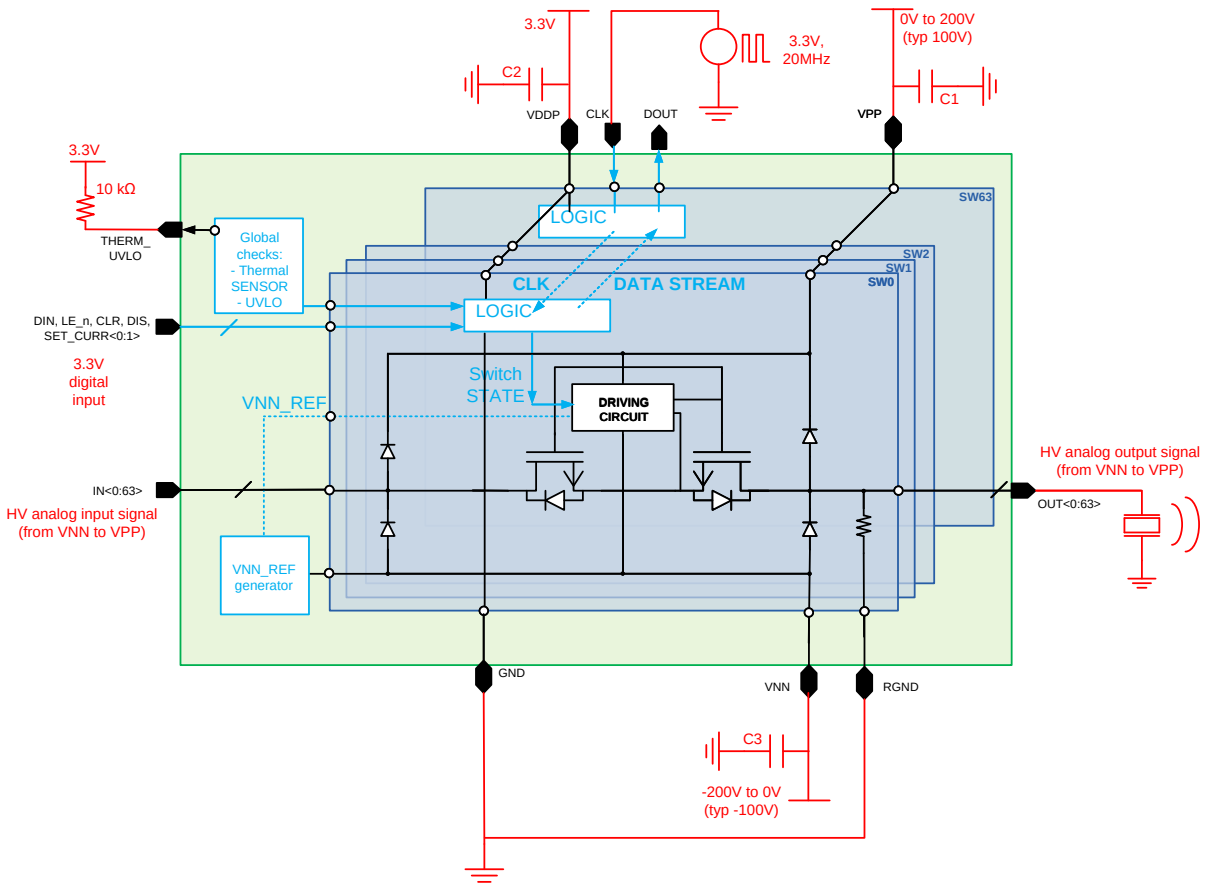


Figure 3

2 Typical Application Circuit



Filtering Cap on Power Supply: 1 µF (up to 10 µF)

3 Pinout

3.1 Ball Out (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	OUT40	IN40	OUT41	IN41	GND	GND	OUT50	IN50	OUT59	IN59	NC	NC
B	IN32	OUT32	IN39	OUT39	IN42	OUT42	IN49	OUT49	IN51	OUT51	IN58	OUT58	IN60	OUT60
C	OUT33	IN33	OUT38	IN38	OUT43	IN43	OUT48	IN48	OUT52	IN52	OUT57	IN57	OUT61	IN61
D	IN34	OUT34	IN37	OUT37	IN44	OUT44	IN47	OUT47	IN53	OUT53	IN56	OUT56	IN62	OUT62
E	OUT35	IN35	OUT36	IN36	OUT45	IN45	OUT46	IN46	OUT54	IN54	OUT55	IN55	OUT63	IN63
F	GND	GND	GND	GND	GND	VNN	VNN	VPP	VPP	VDDP	GND	GND	GND	GND
G	DIS	CLR	LE_n	DIN	GND	VNN	VNN	VPP	VPP	VDDP	VDDP	THERM_UVLO	DOUT	CLK
H	GND	GND	GND	GND	GND	VNN	VNN	VPP	VPP	VDDP	GND	GND	GND	GND
J	GND	GND	GND	GND	GND	NC	VNN	VPP	NC	VDDP	GND	GND	GND	GND
K	OUT3	IN3	OUT4	IN4	OUT13	IN13	OUT14	IN14	OUT22	IN22	OUT23	IN23	OUT31	IN31
L	IN2	OUT2	IN5	OUT5	IN12	OUT12	IN15	OUT15	IN21	OUT21	IN24	OUT24	IN30	OUT30
M	OUT1	IN1	OUT6	IN6	OUT11	IN11	OUT16	IN16	OUT20	IN20	OUT25	IN25	OUT29	IN29
N	IN0	OUT0	IN7	OUT7	IN10	OUT10	IN17	OUT17	IN19	OUT19	IN26	OUT26	IN28	OUT28
P	NC	NC	OUT8	IN8	OUT9	IN9	RGND	RGND	OUT18	IN18	OUT27	IN27	NC	NC

Figure 4 - Pin connection (top view)

3.2 Pin List

Table 1 - Pin description (P = power, A = analog, D = digital, NC = not connected)

Name	Function	IN/OUT	Type
IN0 – IN63	SW 0 to 63 HV input terminal	I	P
OUT0 – OUT63	SW 0 to 63 HV output terminal	O	P
GND	Ground	I	A
VDDP	Positive LV supply	I	A
VPP	Positive HV supply	I	P
VNN	Negative HV supply	I	P
RGND	Reference ground for the output	I	A/P
DIN	Data in	I	D
DOUT	Data out	O	D
LE_N	Enable writing state	I	D
CLR	Clear signal	I	D
CLK	Clock signal	I	D
DIS	Disable signal	I	D
THERM_UVLO	Thermal protection and Under Voltage Lock Out output	O	D
NC	No Connection	NC	NC

4 Electrical data

4.1 Absolute maximum ratings

Table 2 - Absolute maximum ratings

GND is the ground reference for all the other voltages.

Symbol	Parameter	Value	Unit
GND	Ground reference (1)	0	V
RGND	Reference ground for the output	-100 to 100	V
VDDP	Positive LV supply	-0.3 to 3.9	V
VPP	Positive HV supply	0 to 210	V
VNN	Negative HV supply	-210 to 0	V
VPP - VNN		210	V
Vpp IN - OUT	Peak to peak signal	VNN to VPP	V
DIG I/O	Digital input specified in Table 2	-0.3 to VDDP + 0.3	V
TOP	Operating temperature range	-40 to 125	°C
TSTG	Storage temperature range	-65 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3 - Thermal data

Symbol	Parameter	Value	Unit
Rth,JA	Thermal resistance junction-ambient	TBD (1)	°C/W

(1) Could be 20 °C/W or less as for previous project in similar package

4.2 Operating supply voltages and maximum average currents

Table 4 - Supply voltages

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GND	Ground reference			0		V
RGND	Reference ground for the output		-50		50	V
VDDP	Positive LV supply		2.7	3.3	3.6	V
VPP	Positive HV supply		0		200	V

VNN	Negative HV supply		-200		0	V
VSIG	Signal Peak to Peak Amplitude		0		200	V
VSIG	Signal Voltage		VNN		VPP	

4.3 Digital inputs

Table 5 - Digital inputs

Symbol	Parameter	Min.	Max.	Units
All digital signals	Input logic high-voltage	0.8xVDDP	VDDP	V
All digital signals	Input logic low-voltage	0	0.2xVDDP	V

4.4 Output signals

Table 6 - Output signals

Symbol	Parameter	Condition	Min.	Max.	Units
OUT	High-voltage output		VNN	VPP	V

5 Electrical characteristics

Table 7 - Static electrical characteristics (1)

Operating conditions, unless otherwise specified, VPP = 100 V, VNN = -100 V, VDDP = 3.3V, RGND=0V, Tamb= 25 °C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
RONS *Note (1)*	Small signal switch ON resistance	ISIG = 100mA	8.4	10	11.6	Ω
RONL *Note (1)*	Large signal switch ON resistance	ISIG = 1.7A, 100ns pulse	5.06	6.09	7.12	Ω
RBLEED	Bleed resistor		30	42	50	kΩ
VOS *Note (1)*	Switch-off DC offset	Load 100kΩ	39	46	56	mV
IL *Note (1)*	Switch-OFF leakage *Note (4)*	VSIG=200V	0.002	0.02	0.5	uA
IMAX *Note (2)*	Switch Output peak current - RC load (100Ohm // 300pF)	100ns pulse width		3.33		A
IVPPQON	Quiescent VPP supply current	All switches on	60	240	796	uA
IVNNQON	Quiescent VNN supply current	All switches on	31	102	314	uA
IVDDPQON	Quiescent VDDP supply current	All switches on		830		uA
IVPPQOFF	Quiescent VPP supply current	All switches off			1	nA
IVNNQOFF	Quiescent VNN supply current	All switches off	1.6	2.3	3.5	uA
IVDDPQOFF	Quiescent VDDP supply current	All switches off		780		uA
CON *Note (2)*	ON capacitance SW to GND	VSIG = 0V , f = 1MHz		15.91		pF
COFF *Note (2)*	OFF capacitance SW to GND	VSIG = 0V , f = 1MHz		5		pF

Note (1): Test Circuit Available in Section 6 Test Circuits
Note (2): Guaranteed by characterization; not production tested

Table 8 - AC electrical characteristics (1)

Operating conditions, unless otherwise specified, VPP = 100 V, VNN = -100 V, VDDP = 3.3V, RGND=0V, Tamb= 25 °C.

	Parameter	Test condition	Min.	Typ.	Max.	Units
IVPP	Average VPP supply current	All switches are turning on and off at 50kHz with no load	8	8.3	9.1	mA
IVNN	Average VNN supply current	All switches are turning on and off at 50kHz with no load	5.57	5.63	6.15	mA
IVDDP	Average VDDP supply current	All switches are turning on and off at 50kHz with no load	5.2	5.6	6.2	mA
dv/dt *Note (2)*	Maximum VSIG slew rate	Load 100Ω//300pF		20		V/ns
fBW	Small Signal Bandwidth	Load C=200pF	65	76	90	MHz
KO *Note (1)* *Note (2)*	Off isolation *Note (4)*	f = 5MHz load 1kΩ//15pF		-30		dB
		f = 5MHz load 50Ω		-52		dB
KCR *Note (1)* *Note (2)*	Switch crosstalk	f = 5MHz load 50Ω		-65		dB
VSPK *Note (1)*	Voltage Spike			200		mV
QCI	Charge injection (per switch)	VPP = 100V, VNN = -100V, VIN = VOUT = 0V	447	464	484	pC

Note (1): Test Circuit Available in Section 6 Test Circuits
Note (2): Guaranteed by characterization; not production tested
Note (3): SUPPLY POSITIVE condition (as long as SUPPLY NEGATIVE) not production tested
Note (4): This spec is guaranteed only for VOUT > VNN+5V

Table 9 - Digital characteristics

Operating conditions, unless otherwise specified, VDDP = 3.3 V, fCK = 20MHz, Tamb = 25 °C.

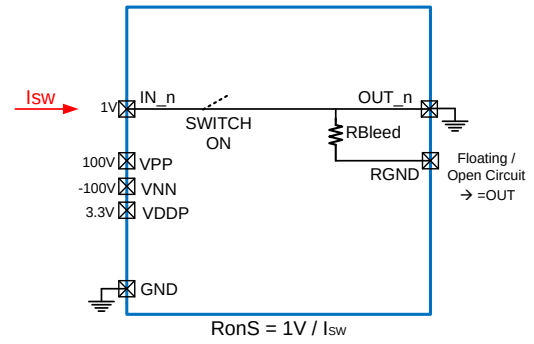
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
IDOUT	Data out current capability	Source current		10		mA
		Sink current		22		mA
ITHERM_UVLO		Sink current		22		mA
CIN	Logic input capacitance			10		pF
fCK	Clock frequency			20	50	MHz
tCLE	Set up time before LE_N fall (*)		6			ns
tWLE	Time width of LE_N		2			ns
tDO	Clock delay time to data out (**)			2.7		ns
tWCLR	Time width of CLR		2			ns
tSU	Set up time data to clock		100			ps
tH	Hold time data from clock		5			ns
tR tF	Clock rise and fall time				10	ns
UVLO_th *Note (1)*	Falling	VDDP from 3.3V to 0V	1.7	2.12		V
	Rising	VDDP from 0 to 3.3V		2.46	2.78	V
	Hysteresis	Calculated		0.34		V
POR_th *Note (1)*	Falling	VDDP from 3.3V to 0V	0.86	1.4		V
	Rising	VDDP from 0 to 3.3V		1.9	2.19	V
	Hysteresis	Calculated		0.5		V

(*) From the last clock rising edge
(**)From the last clock falling edge

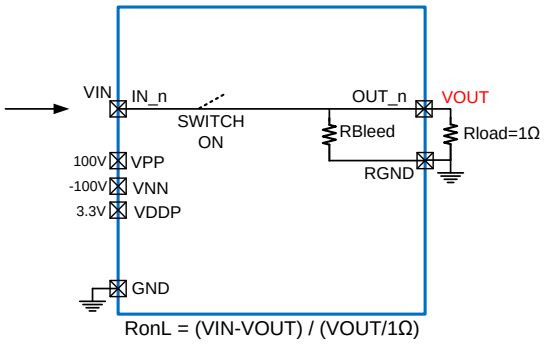
DIGITAL PARAMETERS

- tSU → set up data to clock.
- tH → hold time data to clock
- tDO → clock delay time to data out
- tCLE → clock to LE_n time
- tWLE → time width of LE_n
- tCLR → time width of CLR

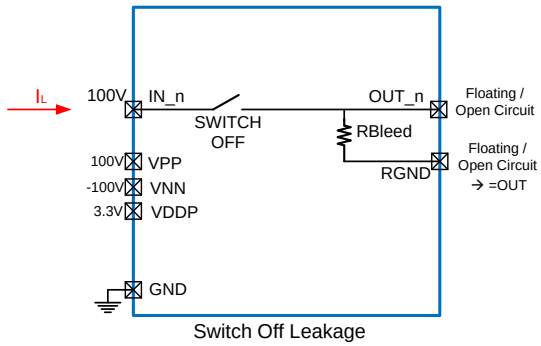
6 Test Circuits



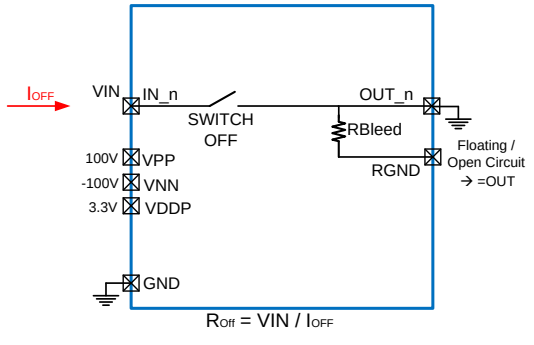
RonS = 1V / I_{SW}



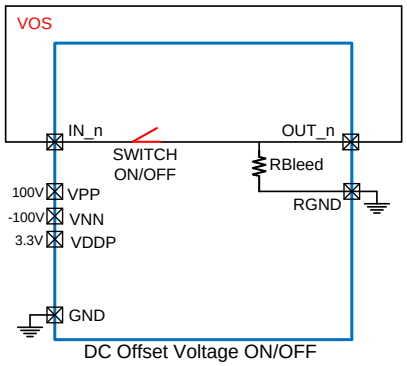
RonL = (VIN-VOUT) / (VOUT/1Ω)



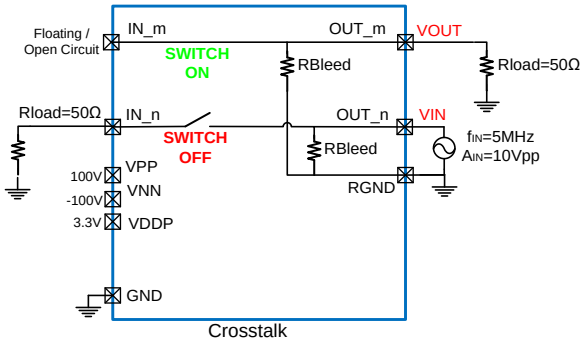
Switch Off Leakage



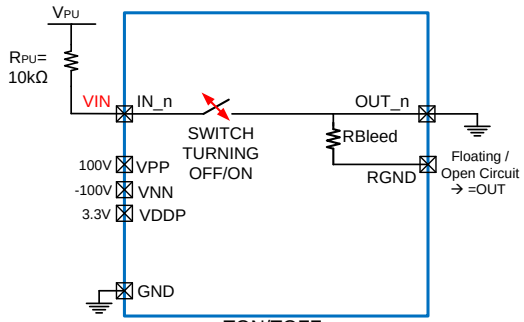
R_{Off} = VIN / I_{OFF}



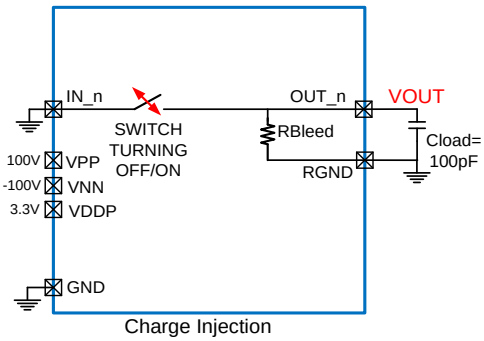
DC Offset Voltage ON/OFF



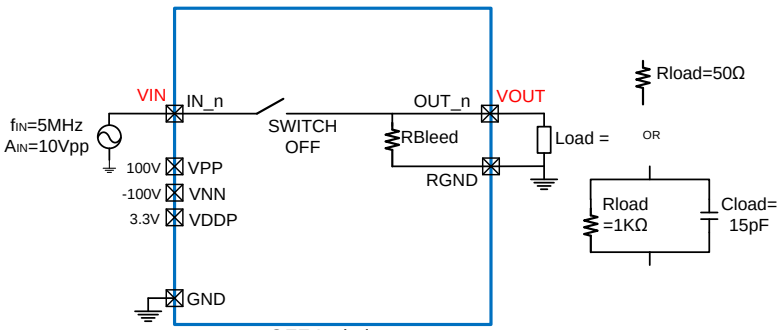
Crosstalk
K_{CR}=20log(VOUT/VIN)



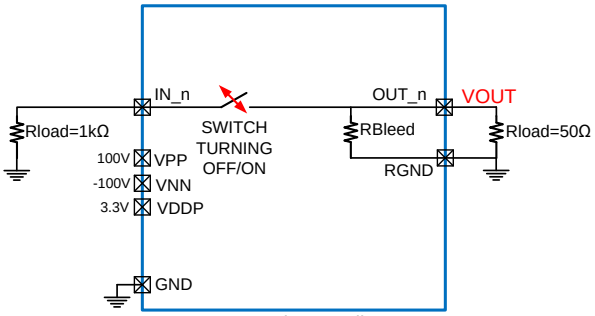
TON/TOFF



Charge Injection
QCI=100pF*VOUT



OFF Isolation
KO=20log(VOUT/VIN)



Output Voltage Spike

7 General Information

7.1 Power-up / Power-down voltage sequence

The device is fully power-up/power-down sequence free, meaning that there is no recommended sequence to follow in order to power up/down the STHV64SW.

7.2 Single channel

7.2.1 Block description

The single switch is implemented with two power transistors (**Figure 5**). The single switch block includes also a bleeding resistor connected between output OUT and RGND (RGND being a dedicated ground for resistors).

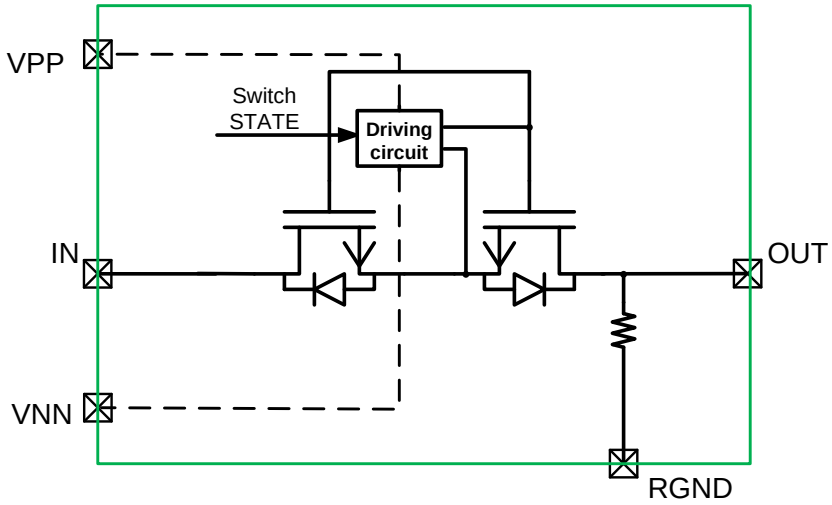


Figure 5

The Driving Circuit contains a Low Voltage Logic and the High Voltage Drivers.
The LV Logic consists of FFs connected in daisy chain for serial communication, latches for switch state bit memorization, and the actual logic for the generation of signals for Drivers actuation (**Figure 6**).

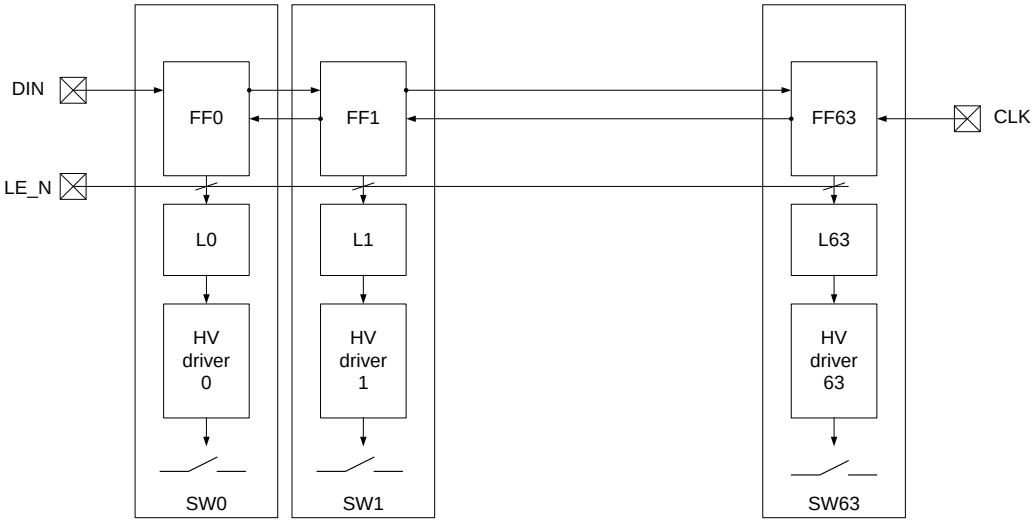


Figure 6

This kind of serial communication requires a minimum set of 3 signals: DIN (data in) and CLK (clock signal) to write 64 bits (one for each switch. Bit 1 for ON-status, 0 for OFF-status) in the shift register. The third signal, LE_N (latch enable) writes the bit in the latches and makes the switch status effective.
The availability of DOUT (data out) pin allows also to connect more than one chip in daisy chain configuration. (**Figure 7**)

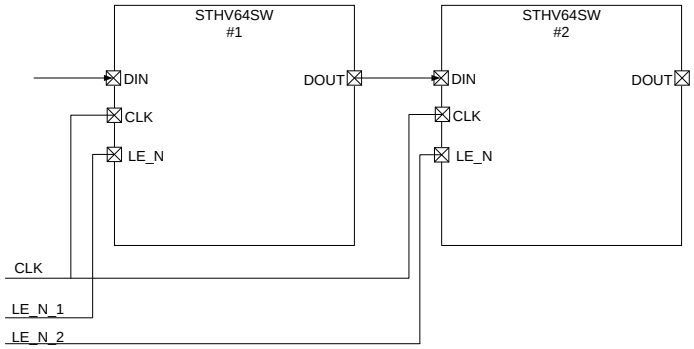


Figure 7

The HV Drivers Turn ON/OFF the power transistors.

7.2.2 Switch – State Configuration

Truth Table

The shift register is load by a streaming data after 64 clock pulses, where the first loaded bit will set the last FF of the chain.

D0	D1	…	D63	D64	LE_n	CLR	DIS	SW0	SW1	..	SW63	SW64
L	-		-	-	L	L	L	OFF	-		-	-
H	-		-	-	L	L	L	ON	-		-	-
-	L		-	-	L	L	L	-	OFF		-	-
-	H		-	-	L	L	L	-	ON		-	-
-	-		-	-	L	L	L	-	-		-	-
…		…	…							…	…	
-	-		-	-	L	L	L	-	-		-	-
-	-		L	-	L	L	L	-	-		OFF	-
-	-		H	-	L	L	L	-	-		ON	-
-	-		-	L	L	L	L	-	-		-	OFF
-	-		-	H	L	L	L	-	-		-	ON
X	X	X	X	X	H	L	L	HOLD PREVIOUS STATE				
X	X	X	X	X	X	H	L	ALL SWITCHES OFF				
X	X	X	X	X	X	X	H	ALL SWITCHES OFF / no Chip current consumption				

7.3 Logic Timing Waveforms

Standard Pattern

The shift register is load by a streaming data after 64 clock pulses, where the first loaded bit will set the last FF of the chain.

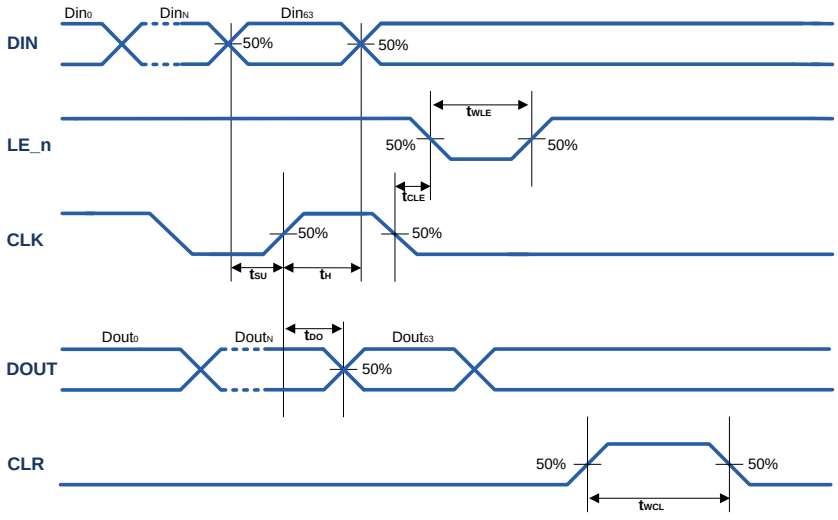


Figure 8 – Timing

7.4 Global Signals and Interrupts

- DIS – Disable

  Global Disable. When in Disable, the chip current consumption drops to zero even if the chip is supplied. All flip flops are reset (both those in the shift register, and those recording the switch state information)

- CLR – Clear

  Clear Signal resets the Switch-State Flip Flop, so that all the switch are Open.
  Voltage Reference Generation Block, Polarization Currents Generation Block and UVLO/THERM Check Blocks are still consuming current.

Internal THERMAL Event Check	Internal UNDER VOLTAGE Event Check	THERM_UVLO ball with pull-up
L	L	H
H	L	L
L	H	L

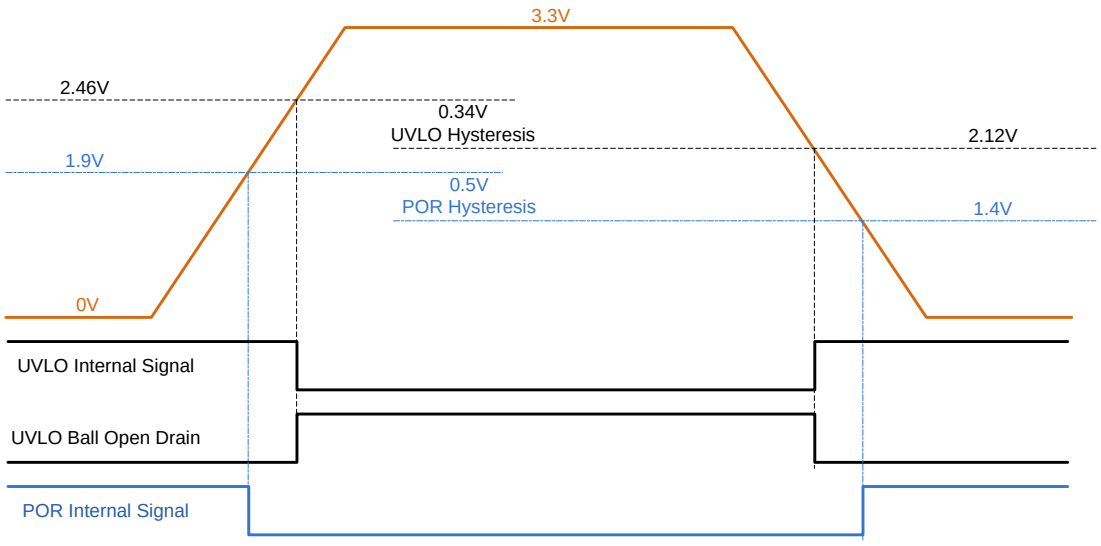


Figure 9 – UVLO and POR

8 Package - TFBGA 12x12x1.2 196 F14x14 pitch 0.8 ball 0.4

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.20			1.20	(1)
A1	0.21	0.29		0.21	0.29		
A2		0.20		0.16	0.20	0.24	
A4	0.48	0.53	0.58	0.48	0.53	0.58	
b	0.35	0.40	0.45	0.35	0.40	0.45	(2)
D	11.85	12.00	12.15	11.90	12.00	12.10	
D1		10.40			10.40		
E	11.85	12.00	12.15	11.90	12.00	12.10	
E1		10.40			10.40		
e		0.80			0.80		
Z		0.80			0.80		
ddd			0.10			0.10	
eee			0.15			0.15	(3)
fff			0.08			0.08	(4)

NOTES:

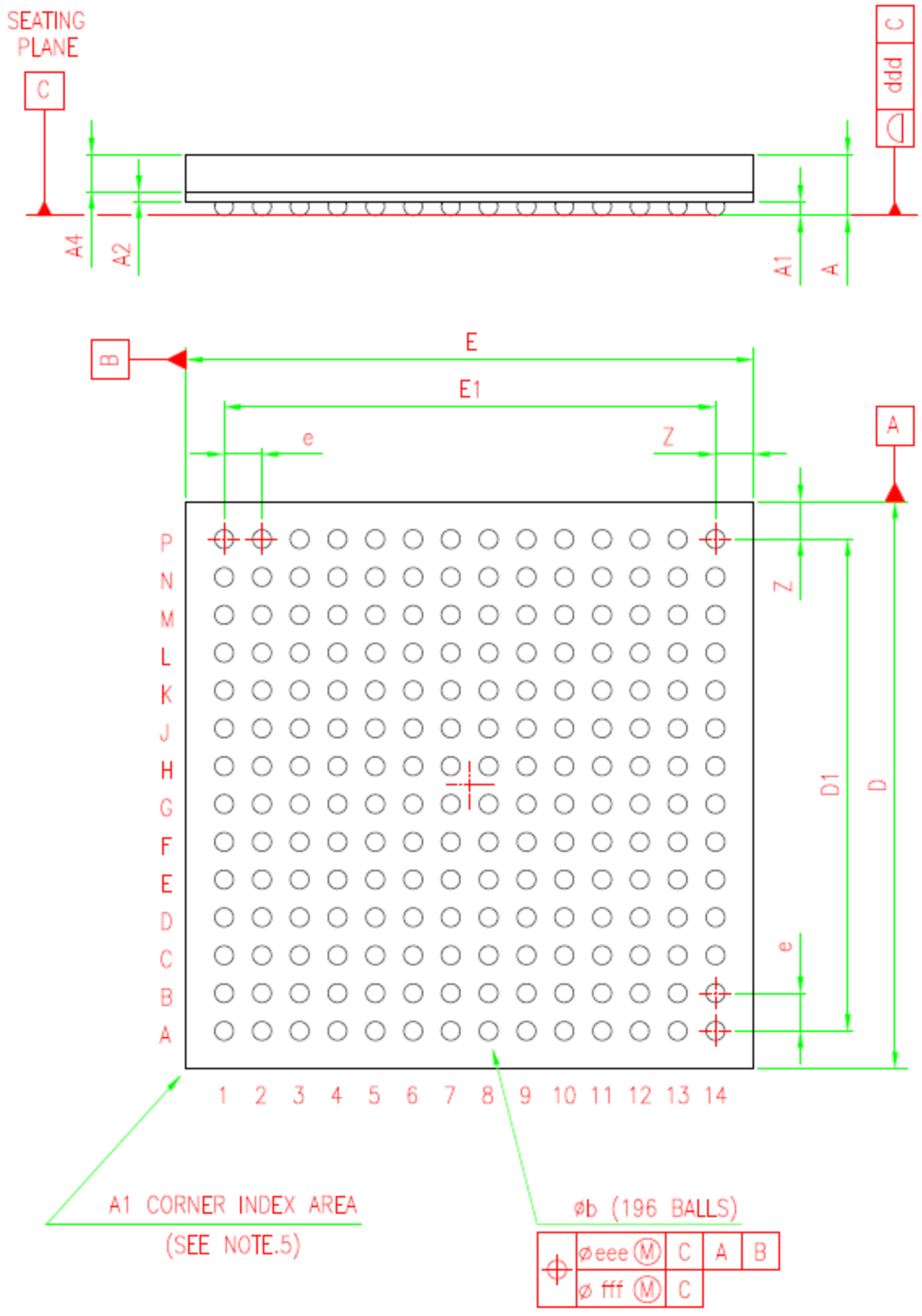
(1) – LFBGA stands for **L**ow Profile **F**ine Pitch **B**all **G**rid **A**rray.
– Low Profile: 1.20mm < A ≤ 1.70mm / Fine pitch: e < 1.00mm.
– The total profile height (Dim A) is measured from the seating plane "C" to the top of the component.
– The maximum total package height is calculated by the RSS method (Root Sum Square):
A Max = A Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2 + A2^2 + A4^2}$ tolerance values)

(2) – The typical balls diameters before mounting is 0.40mm.

(3) – The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

(4) – The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

(5) – The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
– A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.


SEATING
PLANE
C
ddd
C
A4
A2
A1
A
B
E
E1
e
Z
A
P
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M
L
K
J
H
G
F
E
D
C
B
A
Z
D1
D
e
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A1 CORNER INDEX AREA
(SEE NOTE.5)
øb (196 BALLS)
øeee M C A B
ø fff M C

9 Revision history

Table 12. Document revision history

Date	Revision	Changes
05 / 10 / 2015	1	Initial release
14 / 10 / 2015	2	Draft
13 / 11 / 2015	3	With Descriptive Paragraphs
20 / 01 / 2016	4	With Package
21/06/2017	5	Final Version