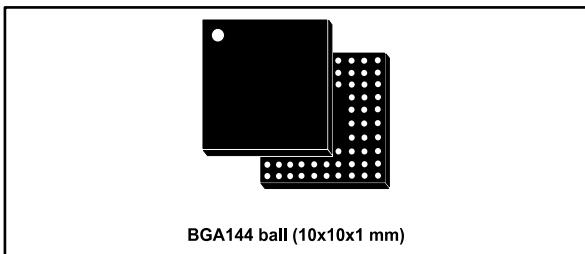




16 channel ± 100 V, $\pm 2/\pm 4$ A, 5/3-level RTZ, TR switch, high-speed ultrasound pulser with integrated transmit beamformer

Datasheet - production data



Features

- 0 to 200 V peak-to-peak output signal
 - Up to 30 MHz operating frequency
 - Power-up/down sequence free
 - Gate driver self-biased architecture; no filtering capacitors required
 - Pulsed wave (PW) mode operation:
 - 5/3 level output
 - ± 2 A / ± 4 A source and sink current
 - Continuous wave (CW) mode operation:
 - 150 mW power consumption/channel
 - 270 fs RMS jitter (100 Hz-20 kHz)
 - -147 dBc/Hz @ 1 kHz phase noise
 - Elastography mode operation
 - Programmable fine-tuning delays to minimize second harmonic distortion
 - Fully integrated real clamping-to-ground function
 - 11 Ω synchronous active clamp
 - ± 2 A source and sink current
 - Fully integrated T/R switch
 - 9 Ω ON resistance
 - 28 pF parasitic capacitance
 - Compliant with receiver multiplexing function
 - Auxiliary integrated circuits
 - Noise blocking diode function
 - Recirculation current protection
 - Anti-memory feature
 - Thermal protection
 - Undervoltage protection and bias supply checks
- Programmable power management to optimize the performance into a probe
 - TX Beamforming in transmission mode
 - Programmable single-channel delay for beam steering and beam focusing
 - Clock frequency up to 200 MHz
 - From 5 ns to 327 μ s delay resolution
 - 425 ns minimum delay table writing time
 - Embedded memory to store transmission patterns
 - 65 kbits
 - Waveform compression algorithm
 - Up to 256 non repetitive states
 - Up to 4 states sequence repetition up to 2^{18} times
 - Easy driving control
 - Control through serial interface
 - Few input signals to drive several devices
 - Single interrupt as alert signal
 - Fully automatic and programmable single trigger to manage TX/RX phases
 - Anti-glitch on trigger signal during TX phase
 - Checksum and parity check
 - Very low package thermal resistance
 - Latch-up free due to HV SOI technology
 - Only a few passive components required
 - LVDS/CMOS digital inputs

Applications

- Medical ultrasound imaging
- Pulse waveform generators
- NDT ultrasound transmission
- Piezoelectric transducer drivers

Table 1: Device summary

Order Code	Package	Packaging
STHV1600	BGA-144	Tray

Contents

1	Description.....	6
2	Block schematic and ball configuration	7
2.1	Ball description.....	9
2.2	Input/output digital signal description	10
3	Operating mode.....	11
3.1	PW mode	11
3.2	CW mode	13
3.3	Elastography mode	15
4	Analog description	17
4.1	Power up/down sequence, HV supply constraints	17
4.2	Output nodes.....	17
4.3	I/O block description.....	18
4.4	Delay calibration to improve HD2 performance.....	19
4.5	Global functions	19
5	Digital system description.....	21
5.1	Digital system main parameters	23
6	Memory structure	25
6.1	Setting beamformer delay values for each channel	26
6.2	Setting channel enable/disable in RX/TX	27
6.3	Waveform selection for each channel	28
6.4	Setting waveform description	29
7	Configure repetition algorithm	32
8	Configure receiving mode	34
9	Transmission and receiving phases management	36
9.1	Default mode.....	36
9.2	Trigger, TX_ON signals.....	37
9.3	CW mode	38
10	SPI description	42
10.1	Writing.....	42
10.2	Reading.....	44

STHV1600	Contents
11 Advanced features	47
11.1 State inversion	47
11.2 SRAM 0 value initialization procedure.....	47
11.3 Power saving features.....	47
11.3.1 SRAM power down.....	47
11.3.2 Current reference enable options.....	48
11.3.3 I/O LVDS interface enable options.....	48
11.3.4 Overall low power mode	48
11.3.5 CMOS input configuration	48
12 Interrupt and communication checks	49
12.1 Communication checks	49
12.1.1 Parity.....	49
12.1.2 Checksum.....	50
12.2 Interrupt.....	52
13 Output phase noise measurement in CW mode.....	57
14 Multiple device management.....	58
15 Maximum ratings	62
16 Operating supply voltages and maximum average currents	64
17 Outputs	65
18 Electrical characteristics	66
19 Register map.....	68
20 Package information	89
20.1 LFBGA 10x10x1.4 package information.....	89
20.2 LFBGA 10x10x1.4 packaging information.....	90
21 Revision history	93

List of tables

Table 1: Device summary	1
Table 2: Ball description.....	9
Table 3: Current consumption from each supply channel	14
Table 4: Settings to reduce power consumption	15
Table 5: Device overstress avoidance guidelines	16
Table 6: LVDS signal parameters.....	18
Table 7: Trade-off between waveform complexity and memory capability.....	22
Table 8: Memory capability gain from repetition algorithm in cases of repetitive waveforms	22
Table 9: Digital pin naming	23
Table 10: Performance specifications.....	23
Table 11: Digital pin timing characteristics	23
Table 12: Delay table registers, storing 16-bit delay values for each channel	26
Table 13: enable_tx and enable_rx registers	27
Table 14: Channel behavior.....	28
Table 15: Wave form table registers, storing the address from which waveform generation starts	28
Table 16: Channel states and related code to be set	29
Table 17: Example of memory configuration	30
Table 18: Receiving mode summary	35
Table 19: CW pulse mode with two states	38
Table 20: CW pulse mode with three states	39
Table 21: CW pulse mode with four states	40
Table 22: State inversion table	47
Table 23: Interrupt functions table	54
Table 24: Status register description	55
Table 25: Absolute maximum ratings	62
Table 26: Thermal data.....	62
Table 27: Supply voltages	64
Table 28: Output signals	65
Table 29: Static electrical characteristics..	66
Table 30: AC electrical characteristics.....	67
Table 31: Register map.....	68
Table 32: LFBGA 10x10x1.4 mechanical data	89
Table 33: Document revision history	93

List of figures

Figure 1: Block schematic.....	7
Figure 2: Ball configuration (top view)	7
Figure 3: Ball definition	8
Figure 4: PW mode	11
Figure 5: PW mode main phases	12
Figure 6: CW mode.....	13
Figure 7: Total power consumption (mW) vs. number of channels	14
Figure 8: Elastography mode.....	15
Figure 9: THD vs. signal amplitude.....	17
Figure 10: LVDS signals	18
Figure 11: Input interface.....	19
Figure 12: System overview	21
Figure 13: Memory structure.....	25
Figure 14: Memory address set	26
Figure 15: SRAM row data content (waveform state description)	29
Figure 16: Resulting waveform from example memory configuration	30
Figure 17: Two SRAM rows set to implement two state sequence repetition	32
Figure 18: Waveform resulting from previous example	32
Figure 19: Three SRAM rows set to implement three state sequence repetition	33
Figure 20: Waveform resulting from previous example	33
Figure 21: Receiving mode description	34
Figure 22: TX/RX operation example	36
Figure 23: External control trigger signal	37
Figure 24: TX_ON used to close the loop trigger signal	38
Figure 25: TX_ON used to generate the trigger signal	38
Figure 26: CW pulse mode with two states	39
Figure 27: CW pulse mode with three states	39
Figure 28: CW pulse mode with four states	40
Figure 29: CW pulsing example.....	41
Figure 30: Single write operation	42
Figure 31: Single write operation, 4-bit vectors sampled.....	43
Figure 32: Continuous mode write operation, 4-bit vectors sampled	44
Figure 33: Read operation data out stream	45
Figure 34: Read operation data out stream	45
Figure 35: Continuous mode read operation with different sampling modes	46
Figure 36: Parity check example	50
Figure 37: Checksum example	52
Figure 38: Interrupt event vs. supply variation.....	56
Figure 39: Measurement setup – CK1=640 MHz; CK2=5 MHz	57
Figure 40: FSUP8 spectrum and phase noise output plot.....	57
Figure 41: Individual control example of a 128 channel system.....	59
Figure 42: Shared control example of a 128 channel system	60
Figure 43: TBD.....	61
Figure 44: 3D die thermal map	62
Figure 45: LFBGA 10x10x1.4 package outline	89
Figure 46: LFBGA 10x10x1.4 packaging dimensions (1 of 3).....	90
Figure 47: LFBGA 10x10x1.4 packaging dimensions (2 of 3).....	91
Figure 48: LFBGA 10x10x1.4 packaging dimensions (3 of 3).....	92

Description	STHV1600
-------------	----------

1 Description

This monolithic, high-voltage, high-speed pulse generator features 16 independent channels and integrates a 16-channel beamformer for pulse generation in multi-channel medical ultrasound applications targeted at low power portable systems.

A pure analog section provides each channel with voltage level translators, noise blocking diode function, two identical high voltage P-channel and two identical high voltage N-channel MOSFETs as the output stage (the two half bridges are called TX0 and TX1), clamping to-ground circuitry, anti-leakage, anti-memory block, thermal sensor, recirculation current protection and a T/R switch structure which guarantees effective isolation during the transmission phase.

Each channel can support up to five output levels with two independent half bridges. Both PW output stages (TX0 and TX1) are able to provide up to ± 2 A peak output current, independent from the HV power supply pins. The two half bridges can be driven in parallel with a current capability up to ± 4 A. The clamp circuit, used to carry the output pin XDCR to GND with a resistance of $11\ \Omega$, has a current capability of up to 2 A during the transition. Each channel is provided with strong recirculation protection on the high voltage output node (XDCR) to preserve the device using inductive load without any external diode protection. The 16 independent T/R switches comprise an active circuit that can be used in both a dedicated RX chain per channel or in a multiplexing configuration.

The STHV1600 also includes some global blocks, thermal protection both for the logic and for each channel, undervoltage on VDDP3V3, VDDM3V3 and DVDD, POR on DVDD, global self-biased high-voltage MOSFET gate drivers with internal check of the correct value, and a check of the HV supply values.

Twelve low voltage capacitors are included in the package. Ceramic capacitors are mandatory on the HV supplies and VDDP3V3 and VDDM3V3 on the PCB. The ball-out is designed to simplify application board routing and to prevent unexpected coupling between HV and LV.

All functions of the STHV1600 are managed by a digital core logic working at a maximum clock frequency of 200 MHz. This block is responsible for managing channel delay transmission used in beamformer, waveform generation and compression algorithm, store setting and data, managing all device operations in the correct sequence.

Starting from an IDLE state in which device can be configured by SPI interface and channels are in CLAMP state, transmission TX starts after the rising edge of the external trigger signal is provided. When transmission ends, a RX_WAIT state is performed, forcing channels in CLAMP state to clean signals from previous pulsing. The automatic receiving state, RX, starts and persists until a falling edge of the external trigger signal is provided, putting the device in the initial IDLE state.

It also sets all configurations to perform transmission in continuous mode (CW) when a pulse sequence must be repeated indefinitely (until the falling edge of the trigger is provided) or pulse waves (PW) when a finite pulse sequence must be performed.

2 Block schematic and ball configuration

Figure 1: Block schematic

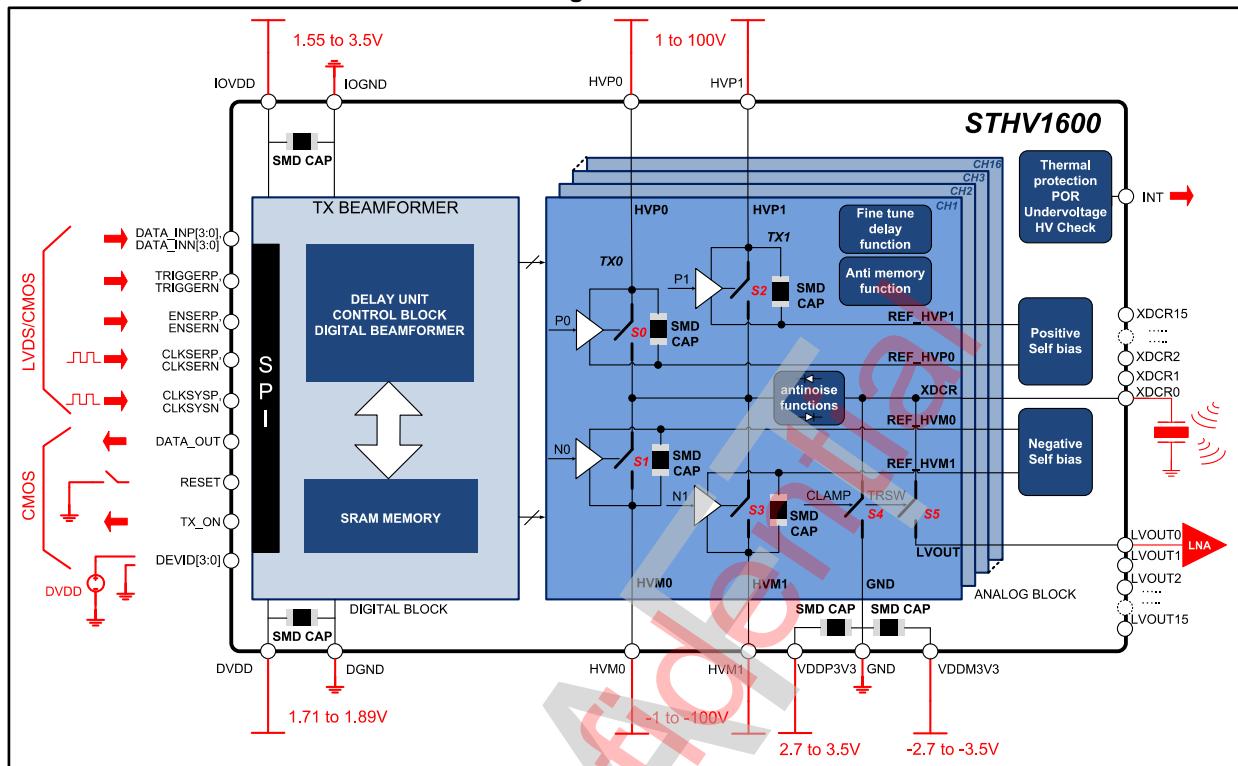
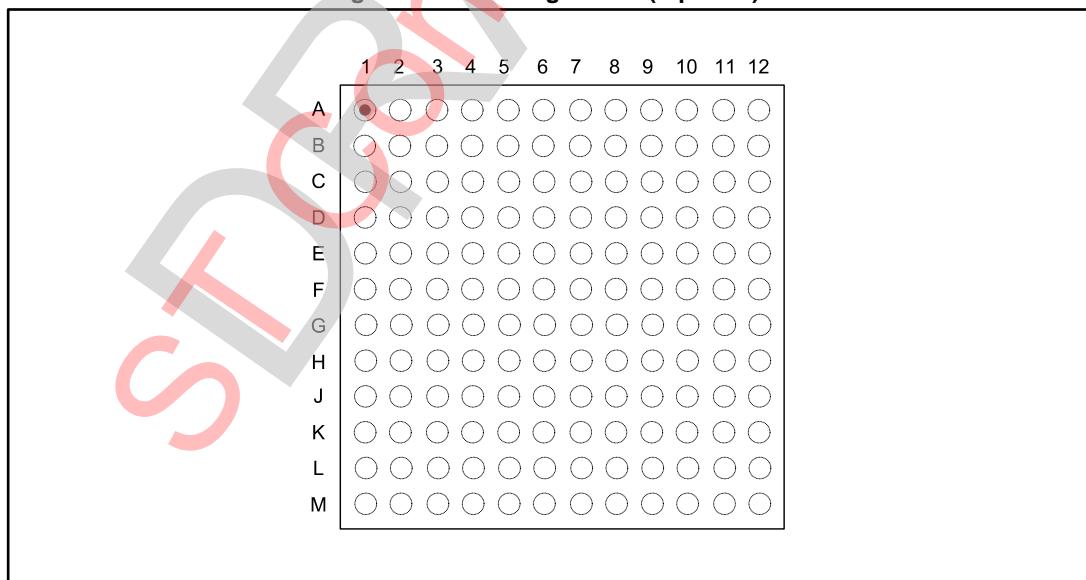


Figure 2: Ball configuration (top view)



Block schematic and ball configuration**STHV1600****Figure 3: Ball definition**

●	1	2	3	4	5	6	7	8	9	10	11	12
A	XDCR15	GND	LVOUT6	LVOUT5	LVOUT13	LVOUT15	GND	HVP0	HVP1	DVDD	TX_ON	DATA_OUT
B	XDCR14	GND	LVOUT7	LVOUT4	LVOUT12	LVOUT14	GND	HVP0	HVP1	DVDD	ENSRN	ENSERP
C	XDCR7	GND	GND	GND	GND	GND	GND	HVP0	HVP1	DVDD	TRIGGERN	TRIGGERP
D	XDCR6	VDDP3V3	VDDP3V3	HVP0	HVP0	HVP0	HVP0	HVP0	HVP1	DVDD	DEVID[1]	DEVID[0]
E	XDCR13	XDCR5	VDDP3V3	HVP0	HVP1	HVP1	HVP1	HVP1	HVP1	DGND	CLKSYSN	CLKSYSP
F	XDCR12	XDCR4	VDDP3V3	VDDP3V3	VDDP3V3	VDDP3V3	VDDP3V3	VDDP3V3	DGND	DGND	DEVID[3]	DEVID[2]
G	XDCR11	XDCR3	VDDM3V3	VDDM3V3	VDDM3V3	VDDM3V3	VDDM3V3	VDDM3V3	IOGND	IOGND	CLKSERN	CLKSERP
H	XDCR10	XDCR2	VDDM3V3	HVM0	HVM1	HVM1	HVM1	HVM1	HVM1	IOGND	INT	RESET
J	XDCR1	VDDM3V3	VDDM3V3	HVM0	HVM0	HVM0	HVM0	HVM0	HVM1	IOVDD	DATA_INP[1]	DATA_INP[3]
K	XDCR0	GND	GND	GND	GND	GND	GND	HVM0	HVM1	IOVDD	DATA_INN[1]	DATA_INN[3]
L	XDCR9	GND	LVOUT1	LVOUT3	LVOUT11	LVOUT9	GND	HVM0	HVM1	IOVDD	DATA_INP[0]	DATA_INP[2]
M	XDCR8	GND	LVOUT0	LVOUT2	LVOUT10	LVOUT8	GND	HVM0	HVM1	IOVDD	DATA_INN[0]	DATA_INN[2]

2.1 Ball description

Table 2: Ball description

Name	Function	IN/OUT	Type ⁽¹⁾
XDCR15 to XDCR0	Channel 0 to 15, high voltage output	I/O	P
LVOUT15 to LVOUT0	Channel 1 to 15, low voltage output	O	A
HVM0	TX0 negative high voltage supply	I	P
HVM1	TX1 negative high voltage supply	I	P
HVP0	TX0 positive high voltage supply	I	P
HVP1	TX1 positive high voltage supply	I	P
VDDP3V3	Positive low voltage supply (3.3 V)	I	A
VDDM3V3	Negative low voltage supply (-3.3 V)	I	A
GND	Device ground	I	A
DGND	Logic ground	I	D
DVDD	Positive logic supply (+1.8 V)	I	D
INT	Interrupt pin (open drain or CMOS)	O	D
DATA_INP[3:0]	SPI four data input lines (positive pin for LVDS interface or single pin for CMOS interface)	I	D
DATA_INN[3:0]	SPI four data input lines (negative pin for LVDS interface)	I	D
DATA_OUT	SPI single data output line (CMOS interface)	O	D
ENSERP	SPI enable (positive pin for LVDS interface or single pin for CMOS interface)	I	D
ENSERN	SPI enable (negative pin for LVDS interface)	I	D
CLKSERP	SPI clock (positive pin for LVDS interface or single pin for CMOS interface)	I	D
CLKSERN	SPI clock (negative pin for LVDS interface)	I	D
CLKSYSP	System clock (positive pin for LVDS interface or single pin for CMOS interface)	I	D
CLKSYSN	System clock (negative pin for LVDS interface)	I	D
TRIGGERP	Input trigger pin (positive pin for LVDS interface or single pin for CMOS interface)	I	D
TRIGGERN	Input trigger pin (negative pin for LVDS interface)	I	D
RESET	System reset (CMOS interface)	I	D
DEVID[3:0]	Device ID (CMOS interface)	I	D
TX_ON	Device in transmission state (CMOS interface)	O	D
IOVDD	CMOS IO supply	I	D
IOGND	CMOS IO ground	I	D

Notes:

⁽¹⁾Type defines the domain of all nets in the PCB layout. A: Analog D: Digital P: Power and High Voltage noisy nets

2.2 Input/output digital signal description

Interface signals (see [Section 10: "SPI description"](#))

- DATA_INP[3:0], DATA_INN[3:0]: Four parallel data input lines used by SPI to write internal memory (pattern description, delay table and configuration registers)
- DATA_OUT: Single data output used by SPI to read all registers in the memory
- ENSERP, ENSERN: SPI communication enable signal (active low)
- CLKSERP, CLKSERN: SPI serial clock

Other signals

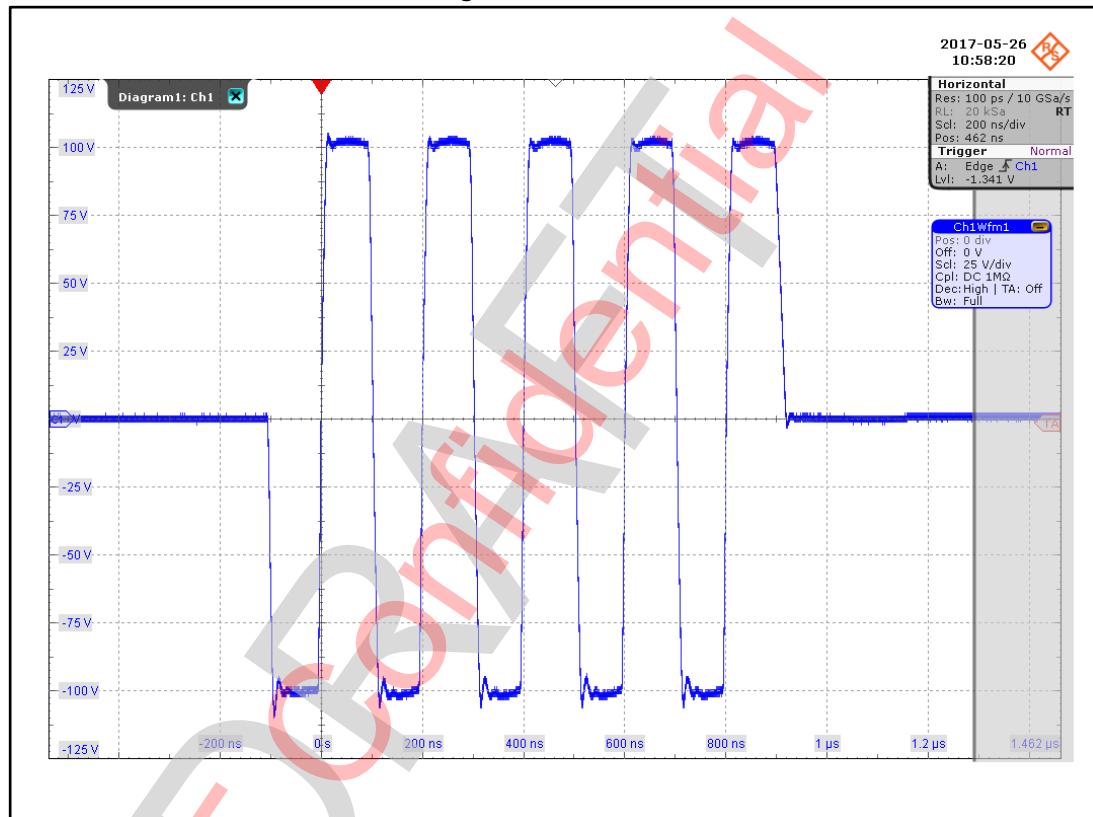
- CLKSYSP, CLKSYSN: System clock
- INT: Global interrupt pin to alert to unsafe conditions (active low; see [Section 12.2: "Interrupt"](#))
- RESET: Asynchronous system reset (active low)
- TRIGGERP, TRIGGERN: Transmission phase starts on rising edge, and idle phase on falling edge (see [Section 9: "Transmission and receiving phases management"](#))
- TX_ON: Transmission phase on-going (active high)
- DEVID[3:0]: Device identifier to drive several STHV1600 devices in parallel (up to 16 device codifications, meaning systems with 256 channels; see [Section 14: "Multiple device management"](#))

3 Operating mode

3.1 PW mode

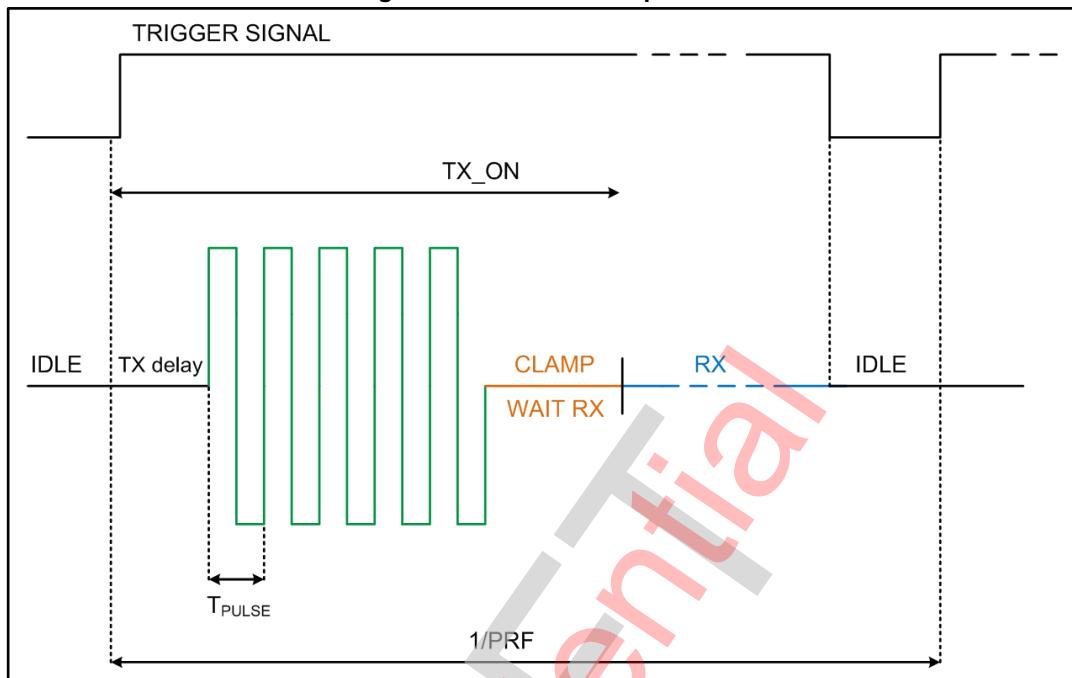
Pulse Wave (PW) mode is a condition with a low duty cycle (transmission time/ repetition time). In the transmission phase the patterns can be set fully flexible and the high voltage supplies can be the maximum values. In the device this is the default operating mode. In this condition TX0, TX1, TX0&TX1 or a mixed signal can be used.

Figure 4: PW mode



Operating mode**STHV1600**

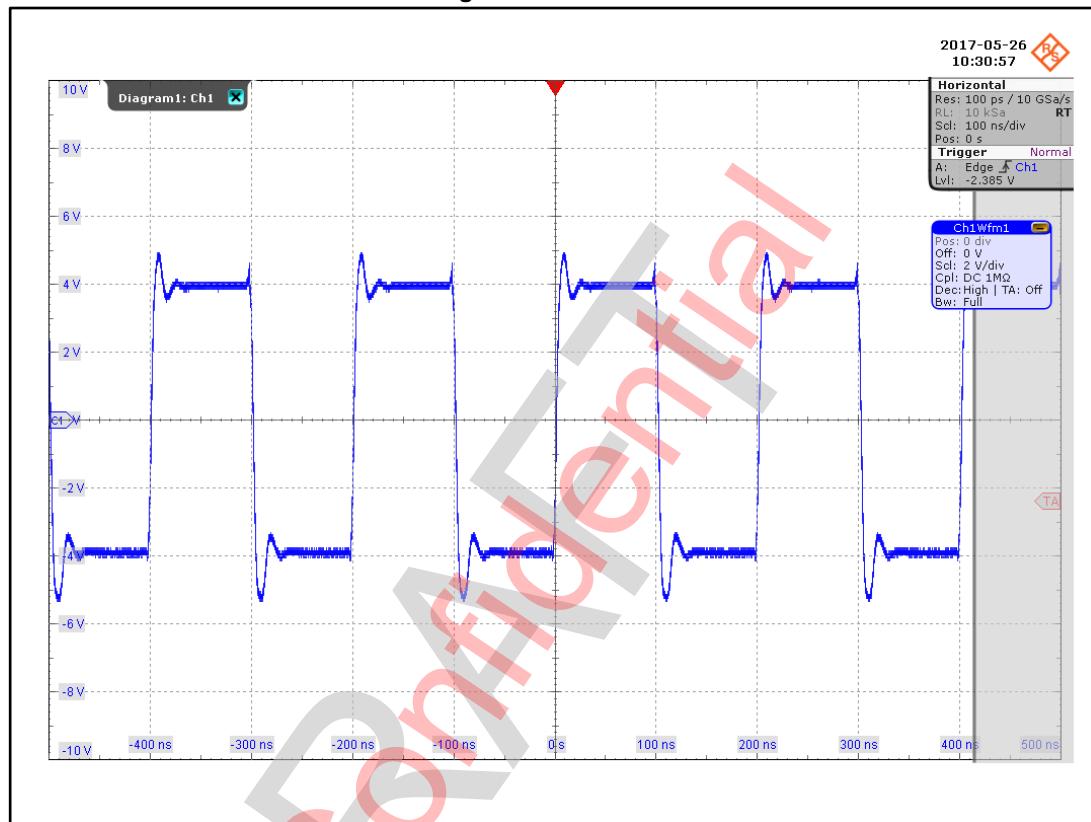
In the figure below, the main phases are shown in relation to the trigger signal.

Figure 5: PW mode main phases

3.2 CW mode

Continuous Wave (CW) mode is a condition in which the high voltage output can switch continuously. Only TX1 is used in this operative mode and the high voltage supplies must be decreased according to the maximum power consumption allowed. Each channel can be set neither in TX or RX state. Among all channels a delay can be set in accordance with the delay table.

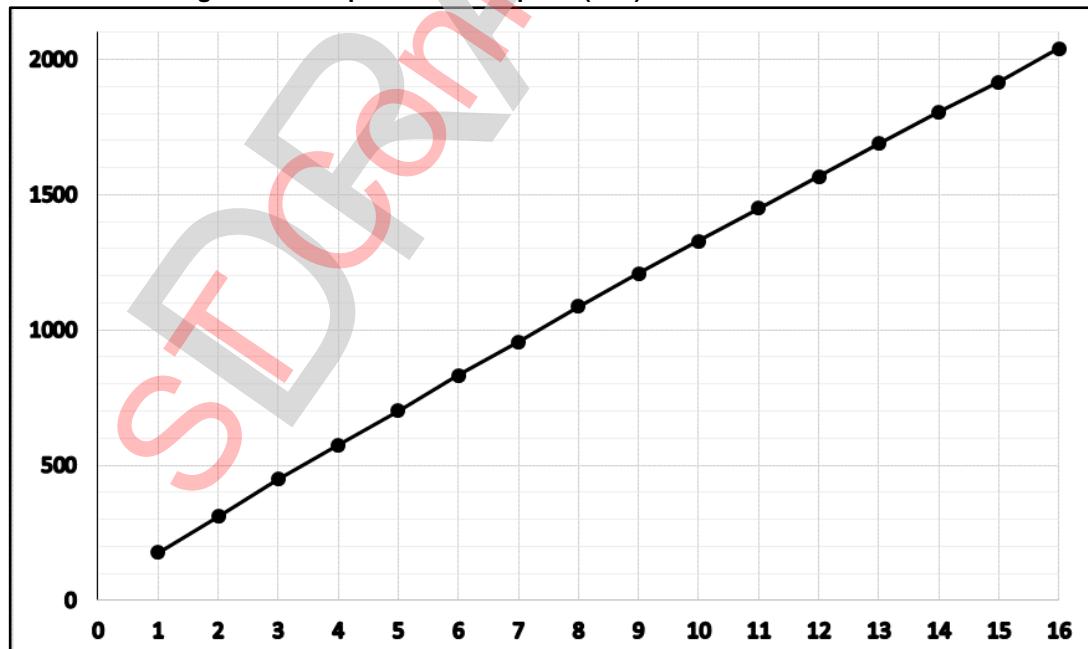
Figure 6: CW mode



The current consumption from each supply are listed in the table below. The output frequency is 5 Mhz, the HV supplies are ± 5 V and the device works without load, so they are the intrinsic values to drive the output capacitance of the device. These values can be used to estimate the power consumption and the temperature of the device during this mode.

Operating mode**STHV1600****Table 3: Current consumption from each supply channel**

# channels	Current consumption (mA)					Total power consumption (mW)
	HVP1	HVM1	VDDP3V3	VDDM3V3	DVDD	
1	12.8	8.5	7.5	7	13	178
2	25	17	10	13	14	311
3	38	25	13	20	14	449
4	50	33	15	26	14	576
5	61	41	17	33	14.5	701
6	73	49	20	39	15	832
7	83	58	23	45	15.5	957
8	96	65	26	51	16	1088
9	108	73	28	55	16.5	1209
10	118	80	30	63	17	1328
11	129	88	33	68	17.5	1450
12	140	95	35	74	18	1567
13	151	103	37	80	18.5	1689
14	162	110	40	85	19	1807
15	171	118	42	90	19.5	1916
16	183	125	45	96	20	2041

Figure 7: Total power consumption (mW) vs. number of channels

In order to minimize power consumption, the current capability of the half bridge can be reduced by setting the register **XXX**. In this condition the values become:

Table 4: Settings to reduce power consumption

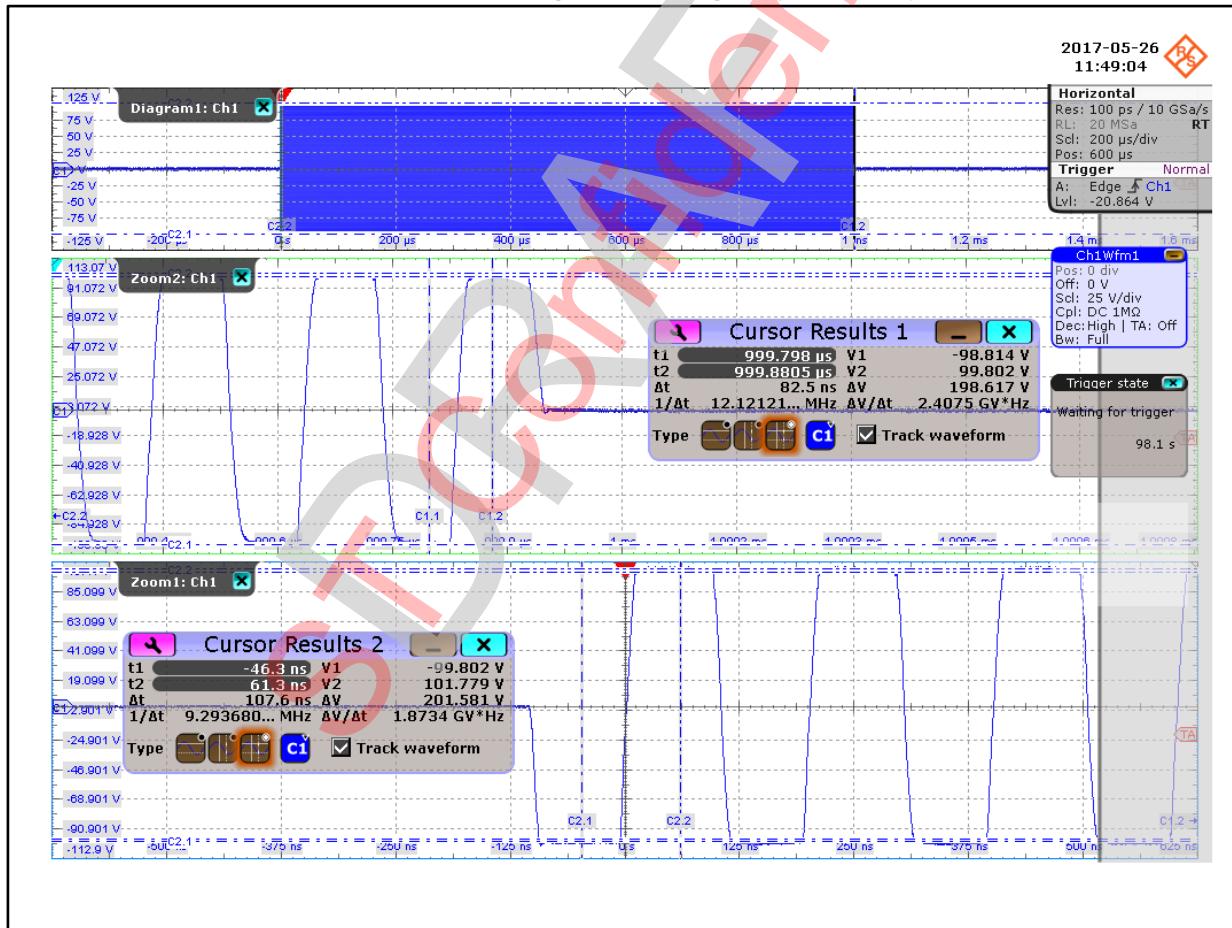
# channels	Current consumption (mA)					Total power consumption (mW)
	HVP1	HVM1	VDDP3V3	VDDM3V3	DVDD	
1	10.5	8	6.7	4.5	13	153 (-14%)
...
16	154	114	35	68	20	1716 (-16%)

3.3 Elastography mode

Elastography condition is a new application field in which very long high voltage patterns must be generated to energize the transducers. This device is designed to fully support this mode.

In the figure below, a train of 1 ms of pulses @ 5 MHz is shown. High voltage supplies are ± 100 V and the load is 300 pF//100 Ω .

Figure 8: Elastography mode



In this condition, the device is able to use all 16 channels in parallel. In this mode the board and the external power supplies must be carefully dimensioned to support the high power and current consumption.

Operating mode**STHV1600**

To avoid overstress conditions for the device, follow the guidelines in the table below.

Table 5: Device overstress avoidance guidelines

Output frequency	High voltage supply	Pulse train duration
Up to 5 MHz	Up to ± 100 V	Up to 1 ms
5 MHz – 7.5 MHz	Up to ± 90 V	Up to 1 ms
	± 100 V	Up to 750 μ s
7.5 MHz – 10 MHz	Up to ± 80 V	Up to 1 ms
	± 100 V	Up to 500 μ s

4 Analog description

4.1 Power up/down sequence, HV supply constraints

The device is fully power-up/power-down sequence free, meaning that there is no recommended sequence to power up or power down the STHV1600.

During the transmission phase, due to the recirculation protection circuit (see next section), the following two conditions must be respected:

$$\text{HVM0} \leq \text{HVM1}$$

$$\text{HVP0} \geq \text{HVP1}$$

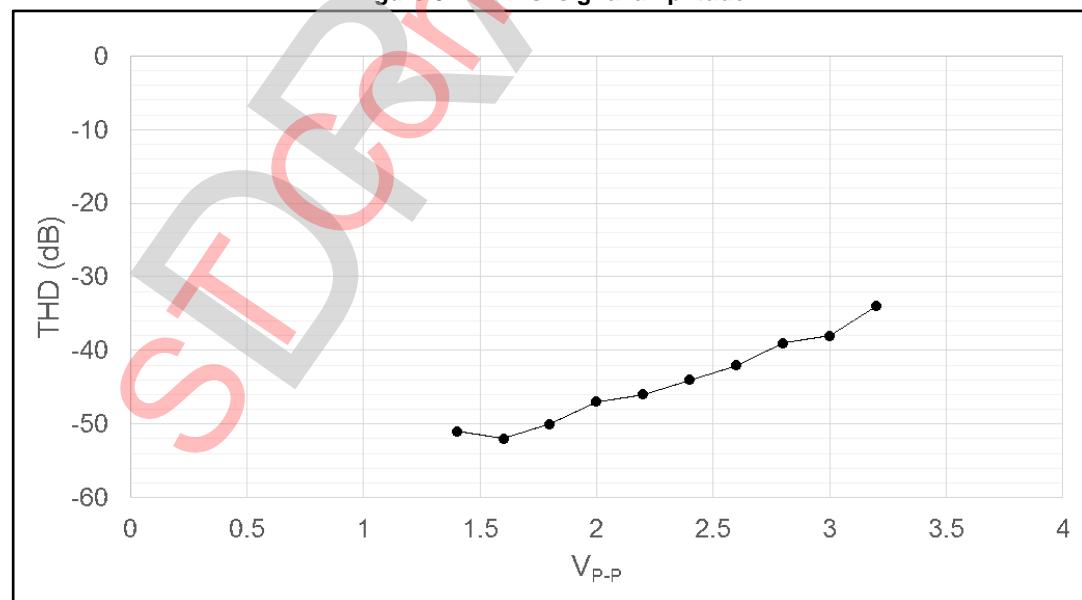
Both these constrains are checked before the transmission phase when a trigger rising edge occurs. If not respected, all channels can be stopped and an interrupt can be generated.

4.2 Output nodes

High voltage outputs signals (XDCR) are directly protected from HVP0 and HVM0 supplies by a dedicated structure. This structure is designed to correctly manage the recirculation currents due to the inductance of the load and to prevent any overvoltage stress on the device. STHV1600 is designed to be able driving high inductive load and it doesn't require any additional external diodes.

Low voltage output signals (LVOUT) are protected toward ground. The maximum amplitude signal on this nets is 2.6 V peak to peak. In this range the THD is lower than -40 dB as shown in the graph below. Using amplitude values lower than 1.5 V the THD is lower than -50 dB. For these measures is used a signal frequency of 1 MHz.

Figure 9: THD vs. signal amplitude



4.3 I/O block description

TX_ON, DATA_OUT and INT are standard CMOS signals. They switch rail-to-rail between IOGND (logic state 0) and IOVDD (logic state 1).

Each output has a typical current capability of 20 mA.

The INT pin can be in a standard CMOS configuration (setting pad_b_opdrain=0 on ana_lvds_set_r register) or in "open drain" configuration (set as default mode). In this case, a pull-up resistor towards IOVDD, with a minimum value of 10 k Ω , must be included on the PCB. This allows sharing of the interrupt signal among different devices.

RESET and DEVID[3:0] are standard CMOS inputs, so they can switch between IOVDD (logic state 1) and IOGND (logic state 0). The reset state is active low, can be shared among different devices and must have a minimum width of 10 T_{CLKSYS}. The input impedance of each pin has a typical value of C=0.5 pF and R>100 M Ω .

DATA_INP[3:0], DATA_INN[3:0], ENSERP, ENSERN, CLKSERP, CLKSERN, CLKSYS, CLKSYSN, TRIGGERP and TRIGGERN are, in default mode, LVDS signals due to their high frequency behavior.

LVDS is a standard differential interface where the logic signal is the difference between two terminals, the P and N pins; if P is higher than N, the logic value is 1, while if P is lower than N, the logic value is 0.

Figure 10: LVDS signals

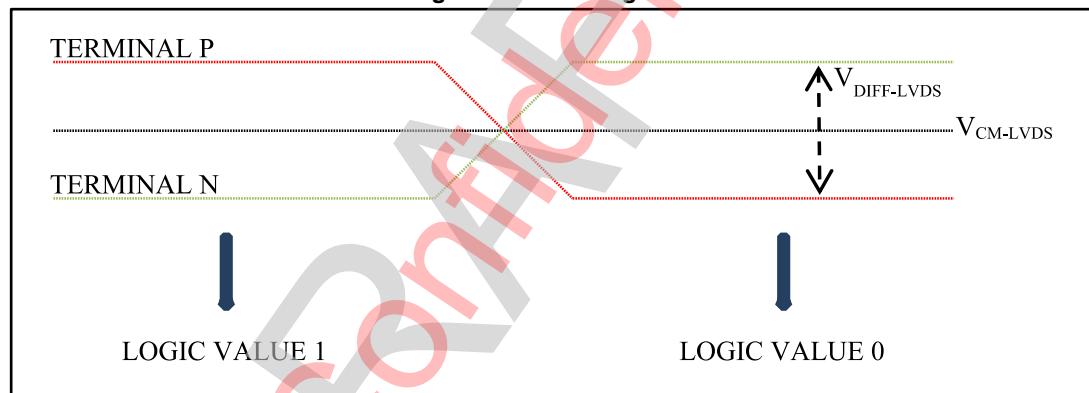


Table 6: LVDS signal parameters

	Min	Typ	Max
V _{DIFF-LVDS}	± 100 mV	± 300 mV	\pm IOVDD/2
V _{CM-LVDS}	0.2 V	1.2 V	1.8 V

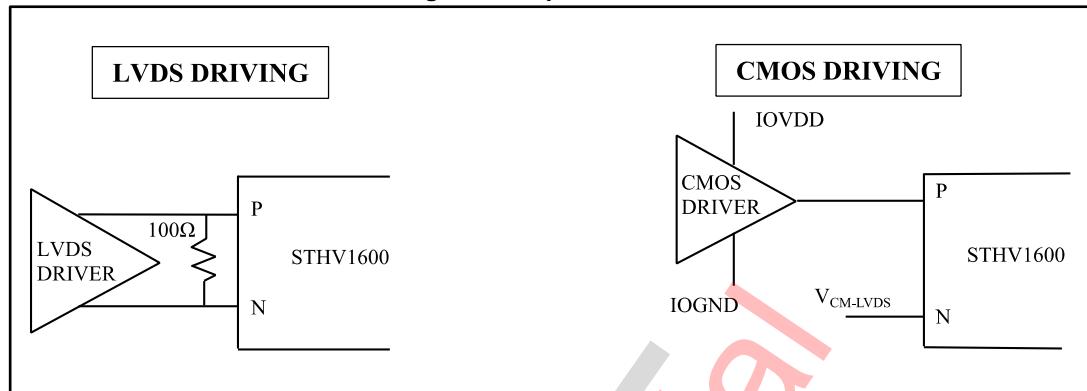
The LVDS interface needs a 100 Ω terminator resistor between terminals P and N on the PCB. This allows sharing of the input lines among different devices. The input impedance of each pin has a typical value of C=1.5 pF and R>100 M Ω .

All the previous high frequency inputs are also compatible with the CMOS interface. In this case terminal N must be forced to a DC supply voltage (typically 1 V) and terminal P must be driven by a standard CMOS signal switching between IOVDD and IOGND (100 Ω input resistance is not required). V_{CM-LVDS} can be generated by a resistive partition because the N terminals are high impedance pins.

If the SPI signals used are CMOS, it is possible to reduce consumption by properly setting SPI register lvds_set_r (lvds_data_lowhi=1, lvds_data_highi=0).

If CLKSYS and TRIGGER are CMOS, it is possible to reduce consumption by properly setting SPI register lvds_set_r (lvds_clk_lowhi=1 and lvds_clk_highhi=0). The two conditions can be used together.

Figure 11: Input interface



4.4

Delay calibration to improve HD2 performance

Some registers are dedicated to a fine calibration of the delays to improve the HD2 performance.

With this tuning, the optimum configuration can be reached with different probes or different HV supplies. Six registers of four bits can be set to delay all the XDCR transitions (the rising and falling edges of TX0 and TX1, and the clamp transitions). The resolution is 100 ps (typ).

4.5

Global functions

Some global checks are implemented to ensure correct functionality of the device.

Thermal protection: the device includes two thermal sensors for each channel plus four sensors dedicated to the logic block in order to guarantee the correct temperature range while the device is functioning.

The thermal sensor of the logic has a threshold of around 120 °C. In case of an overtemperature warning, it forces all channels into HZ state and provides an interrupt event.

The thermal sensor on the channels has a threshold of around 150 °C. In case of an overtemperature warning, it force the only channel in the warning to HZ and, if at least one thermal failing event occurs and register 'enable_shutdown_th'=1, a digital control block provides an interrupt event and puts all channels in HZ (see [Table 23: "Interrupt functions table"](#)).

DVDD supply is checked: for values lower than 1.2 V a POR circuit resets the digital block to the default configuration (all data stored in memory is deleted). For values between 1.2 V and 1.6 V, if 'enable_underv'=1, the XDCR outputs are forced to HZ state, further TXs are disabled (the rising edge of the trigger has no effect) and an interrupt event occurs (the memory maintains the stored data). See [Table 23: "Interrupt functions table"](#).

VDDP3V3 supply is checked only on the trigger rising edge: if 'enable_voltage_check'=1, for values lower than 1.5 V an interrupt event occurs, current TX is stopped and further TXs are disabled (the rising edge of the trigger has no effect). To wake up the device and enable the TX bit, enable_sys_from_int of register conf_1_r must be written to '1' (see [Table 23: "Interrupt functions table"](#)).

Analog description**STHV1600**

VDDM3V3 supply is checked only on the trigger rising edge: if ‘enable_voltage_check’=1, for values higher than -1.5 V an interrupt event occurs, current TX is stopped and further TXs are disabled (the rising edge of the trigger has no effect). To wake up the device and enable the TX bit, enable_sys_from_int of register conf_1_r must be written to ‘1’ (see [Table 23: "Interrupt functions table"](#)).

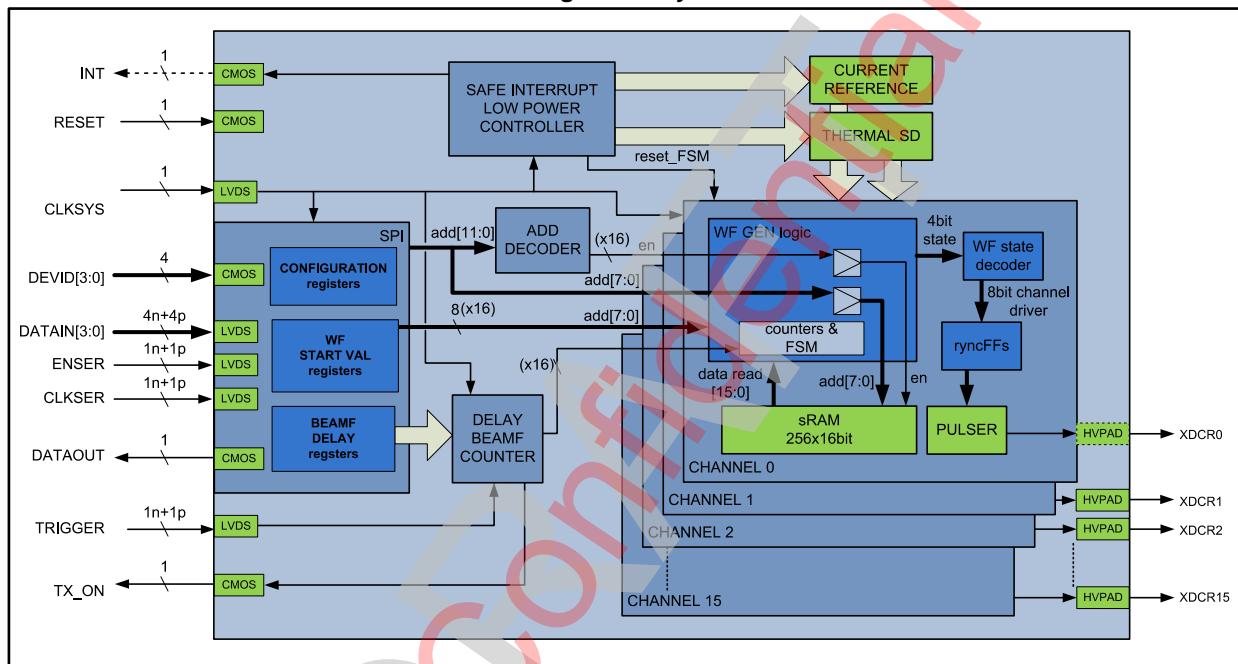
REF_HV are checked only on the trigger rising edge: internal reference voltages are generated for each HV supply to drive the pull-up and pull-down output stages. If at least one voltage is out of its functionality range and ‘enable_voltage_check’=1, an interrupt event occurs, current TX is stopped and further TXs are disabled (the rising edge of the trigger has no effect). To wake up the device and enable the TX bit, enable_sys_from_int of register conf_1_r must be written to ‘1’ (see [Table 23: "Interrupt functions table"](#)).

ST Confidential

5 Digital system description

The STHV1600 contains a digital core logic working at a maximum system clock frequency of 200 MHz: this specification impacts the minimum time resolution of the output waveform and the minimum time resolution of the transmission delay. To set the configuration registers, waveform data descriptions and beamformer delay values for the STHV1600, an SPI protocol is used. The maximum serial clock frequency is 200 MHz and data is transmitted through 4 dedicated input lines. One output line allows the reading of all configuration registers and SRAM blocks. The ultrasound transmission and receiving phases are managed by one trigger signal: on its rising edge the transmission of the stored waveform with the stored delay starts, followed by the preset receiving phase, and on its falling edge the receiving phase stops and the device goes into an idle state.

Figure 12: System overview



The digital core of the STHV1600 implements the following functions:

- Beamformer: for each channel it is possible to store a transmission delay value from a minimum of 1 to a maximum of 2^{16} clock pulses, in order to manage constructive or destructive interference among different elements (for a detailed description, refer to [Section 6.1: "Setting beamformer delay values for each channel"](#) and [Section 9: "Transmission and receiving phases management"](#)).
- Waveform generation: There are 16 independent waveform generators, one for each channel, capable of driving pulsers in 9 possible states: high impedance, clamp to ground, receive, and negative or positive pulse with TX0 or TX1 or both half bridges. The duration of the pulse, clamp and high impedance states can be configured from a minimum of 2 to a maximum of $2^7 + 1$ clock pulses (for a detailed description refer to [Section 6.4: "Setting waveform description"](#) and [Section 9: "Transmission and receiving phases management"](#)).
- An 8 Kbyte memory is implemented to store waveform data with maximum versatility (256 x 16 bit SRAM rows for each channel). Each row can contain one of the 9 states used to produce the waveform and to drive the pulser. This means that for each channel the user can store a number of waveforms depending on the related

complexity that is defined by the state number (for a detailed description refer to [Section 6: "Memory structure"](#)).

Table 7: Trade-off between waveform complexity and memory capability

State number	Storable waveform number
255	1
127	2
63	4
...	...
4	51
2	85

- Compression (repetition) algorithm: to optimize the trade-off between waveform versatility and memory capability, it is possible to repeat the pulsing sequence containing from 1 to 4 states. This allows an increase in memory capability in cases of repetitive waveforms (for a detailed description refer to [Section 7: "Configure repetition algorithm"](#)).

Table 8: Memory capability gain from repetition algorithm in cases of repetitive waveforms

Repeated state	Max number repeated	Waveform complexity (max number of states)	Max number of waveforms (memory capability)
2	$1+2^8$ times	$2 \times (1+2^8)$	127
3	$1+2^{13}$ times	$3 \times (1+2^{13})$	64
4	$1+2^{18}$ times	$4 \times (1+2^{18})$	51

- Diagnostic functions: power supply, thermal and communication checks with debug status registers and single interrupt output signal INT (for a detailed description refer to [Section 12.2: "Interrupt"](#)).
- The entire TX-RX cycle is managed by a simple square wave signal provided by an external control system to the input TRIGGER. The TX_ON output signal can be used to close the control loop (for a detailed description refer to [Section 9.2: "Trigger, TX_ON signals"](#)).
- Fast inversion state: it is possible to invert polarity of all waveforms stored by writing only one bit in the configuration registers states (for a detailed description refer to [Section 11.1: "State inversion"](#)).
- Power save functions (for a detailed description refer to [Section 11.3: "Power saving features"](#)).

To further simplify the system description, digital control signals will be named without the n/p differential annotation, in accordance with the following table:

Table 9: Digital pin naming

Name	Reference	
	LVDS	CMOS
DATA_IN[3:0]	Differential DATA_INN[3:0] and DATA_INP[3:0] signals	DATA_INP[3:0]
ENSER	Differential ENSERN and ENSERP signals	ENSERP
CLKSER	Differential CLKSERN and CLKSERP signals	CLKSERP
CLKSYS	Differential CLKSYSN and CLKSYSP signals	CLKSYSP
TRIGGER	Differential TRIGGERN and TRIGGERP signals	TRIGGERP

5.1 Digital system main parameters

Table 10: Performance specifications

	Parameter	Min	Max	Unit
SPI interface	Frequency	10	200	MHz
	Data rate	40	800	Mbit/s
Delay between two channels	Within same device or in different devices using shared trigger signal	5	327680	ns
Pulse state	Duration without repetition set	10	650	ns
	Resolution	5		ns
Number of states for each channel	Without repetition set		256	
Number of waveforms for each channel	2 state waveforms		85	
	3 state waveforms		64	
	4 state waveforms		51	
Number of waveform repetitions	2 state waveforms		257	
	3 state waveforms		8193	
	4 state waveforms		262145	

Table 11: Digital pin timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Fclk_sys	System clock frequency	10		200	MHz
THclk_sys	CLKSYS pulse width high	3			ns
TLclk_sys	CLKSYS pulse width low	3			ns
Fclk_ser	Serial clock frequency	10		200	MHz
THclk_ser	CLKSER pulse width high	3			ns
TLclk_ser	CLKSER pulse width low	3			ns
TSUen_ser	Setup time ENSER to CLKSER rising edge		0.8		ns
THen_ser	Hold time ENSER to CLKSER rising edge		0.8		ns

Digital system description**STHV1600**

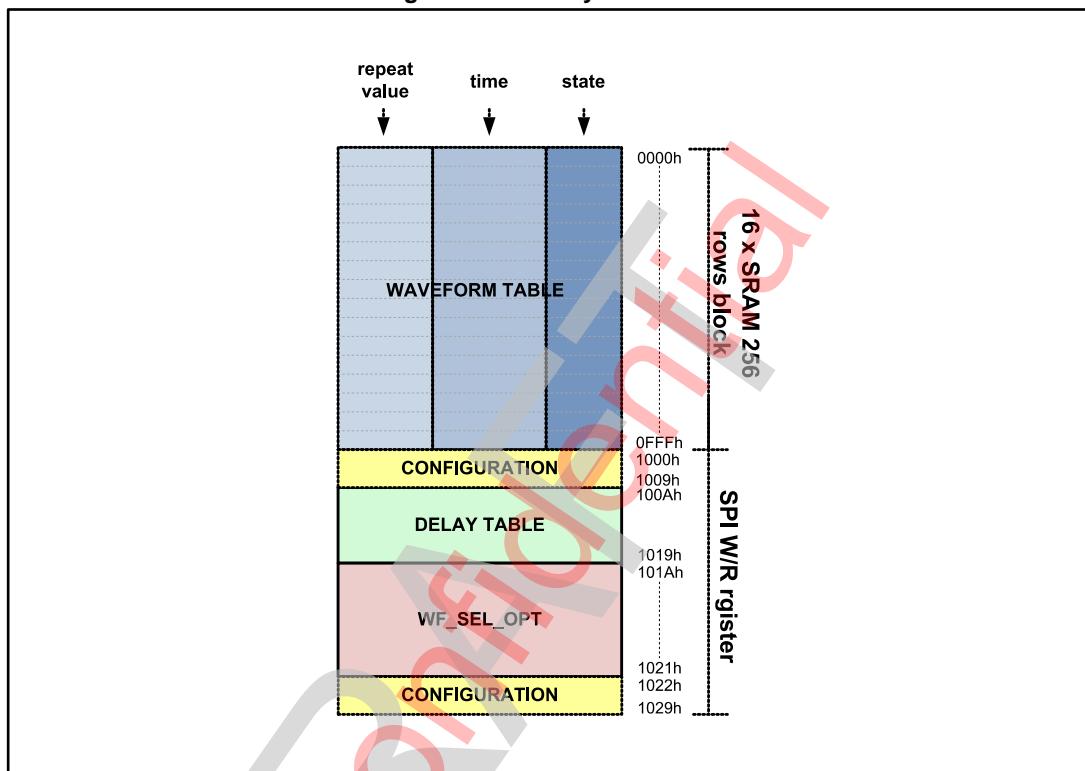
Symbol	Parameter	Min	Typ	Max	Unit
TSU-din	Setup time DATA_IN to CLKSER rising edge		0.8		ns
TH-din	Hold-up time DATA_IN to CLKSER rising edge		0.8		ns
TDV	Enable to DATA_OUT valid time		5.0		ns
TDH	DATA_OUT hold time		0.8		ns
TSU-trigger	Setup time trigger to CLKSYS rising edge		0.8		ns
TH-trigger	Hold-up time trigger to CLKSYS rising edge		0.8		ns

ST Confidential

6 Memory structure

The STHV1600 implements 16 static RAM blocks used to store waveform data, one for each channel and 37 FFs registers to store configuration settings. Both FFs and SRAM memory spaces can be written or read in the same way using the SPI interface and can be addressed as shown in *Figure 13: "Memory structure"* by a 13 bit address:

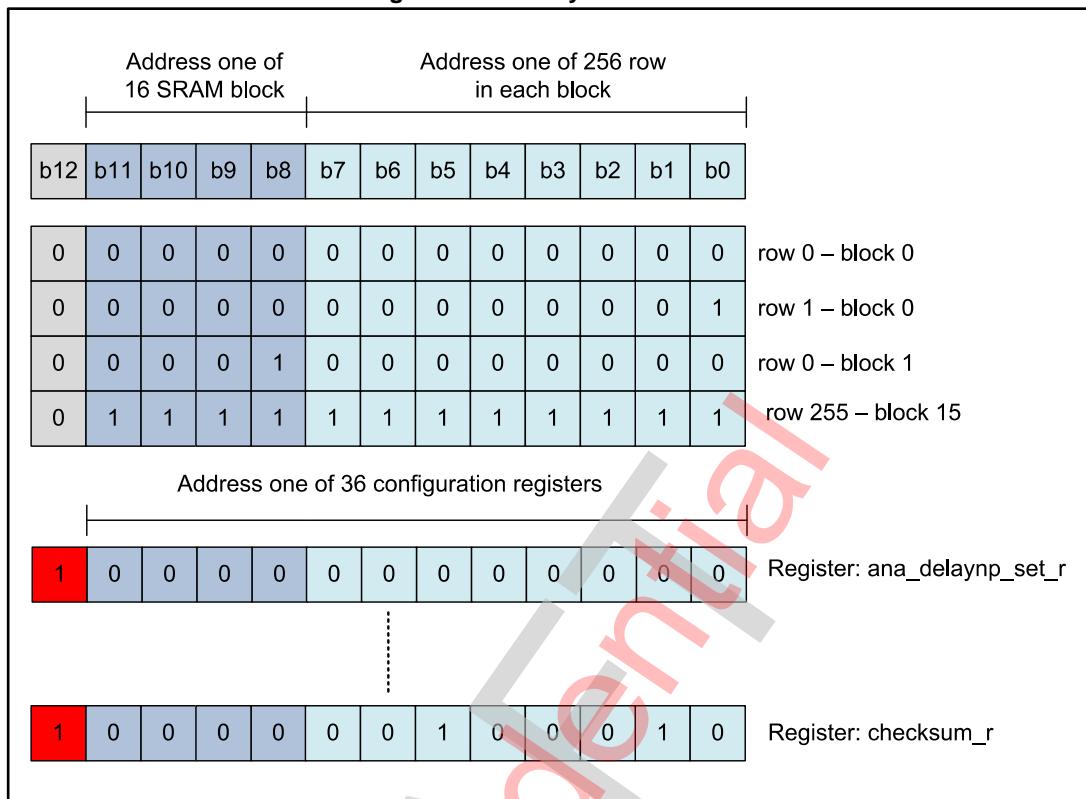
Figure 13: Memory structure



From address 0x0000 to 0x0FFF the memory consists of 16 x SRAM blocks. The first 256 address values are related to the first SRAM block associated with channel 0 whose 256 rows are incrementally addressed from first row with address 0x0000 to last row with address 0x00FF. The next 256 address values are related to the second SRAM block associated with channel 1, whose rows are incrementally addressed from first row with address 0x1000 to the last one with address h01FF. The behavior is the same for all remaining 14 SRAM blocks.

Address 0x1000 and all addresses with the MSB=1 are related to configuration registers, which set particular features and behavior on TX and RX operations, the beamformer delay values and the waveform index to be transmitted.

Figure 14: Memory address set



6.1

Setting beamformer delay values for each channel

From `0x100A` to `0x1019` the memory contains the sixteen 16-bit registers `delay_tab_[15:0]_r`, one for each channel, used to store the delay values. This means that for two channels within the same device or two channels belonging to different devices managed by external shared trigger, the maximum delay allowed is $2^{16} \times \text{Tclk}$.

Table 12: Delay table registers, storing 16-bit delay values for each channel

Delay table		
Register name	Address	TX delay channel
<code>delay_tab_0_r</code>	<code>0x100A</code>	Channel 0
<code>delay_tab_1_r</code>	<code>0x100B</code>	Channel 1
<code>delay_tab_2_r</code>	<code>0x100C</code>	Channel 2
<code>delay_tab_3_r</code>	<code>0x100D</code>	Channel 3
<code>delay_tab_4_r</code>	<code>0x100E</code>	Channel 4
<code>delay_tab_5_r</code>	<code>0x100F</code>	Channel 5
<code>delay_tab_6_r</code>	<code>0x1010</code>	Channel 6
<code>delay_tab_7_r</code>	<code>0x1011</code>	Channel 7
<code>delay_tab_8_r</code>	<code>0x1012</code>	Channel 8
<code>delay_tab_9_r</code>	<code>0x1013</code>	Channel 9
<code>delay_tab_10_r</code>	<code>0x1014</code>	Channel 10
<code>delay_tab_11_r</code>	<code>0x1015</code>	Channel 11

Delay table		
Register name	Address	TX delay channel
delay_tab_12_r	0x1016	Channel 12
delay_tab_13_r	0x1017	Channel 13
delay_tab_14_r	0x1018	Channel 14
delay_tab_15_r	0x1019	Channel 15

6.2 Setting channel enable/disable in RX/TX

All channels have one bit used to enable/disable the transmission and one bit used to enable/disable the receiving phase, independent of the associated RAM memory content. These two bits are respectively set in two 16-bit registers: enable_tx_r and enable_rx_r. (see table below).

Table 13: enable_tx and enable_rx registers

enable_rx_x		enable_tx_x	
bit	Channel enabled	bit	Channel enabled
0	CH0	0	CH0
1	CH1	1	CH1
2	CH2	2	CH2
3	CH3	3	CH3
4	CH4	4	CH4
5	CH5	5	CH5
6	CH6	6	CH6
7	CH7	7	CH7
8	CH8	8	CH8
9	CH9	9	CH9
10	CH10	10	CH10
11	CH11	11	CH11
12	CH12	12	CH12
13	CH13	13	CH13
14	CH14	14	CH14
15	CH15	15	CH15

Table 14: Channel behavior

enable_rx_x	enable_tx_x	Channel behavior with default setting
0	0	Channel always remains in clamp
1	0	Only RX starts with modality set by wait_rx_r[15] rx_start_mode bit
0	1	Only TX starts. It starts at (delay table value + 10) x Tclk after rising edge of trigger signal provided. After TX phase, channel goes in clamp instead of RX state
1	1	Both TX and RX are performed. TX starts at (delay table value + 10) x Tclk after rising edge of trigger signal provided. After TX phase, channel goes in RX mode.

6.3

Waveform selection for each channel

The waveform selection table is an 8 rows x 16 bit memory registers array wf_sel_opt_[7:0]_r addressed from 0x101A to 0x1021, containing the starting TX address. This is the SRAM row address from which the waveform generator starts to read the first waveform state information. To select one of the 256 address rows, 8 bits are needed for each SRAM block that stores waveform descriptions.

Table 15: Wave form table registers, storing the address from which waveform generation starts

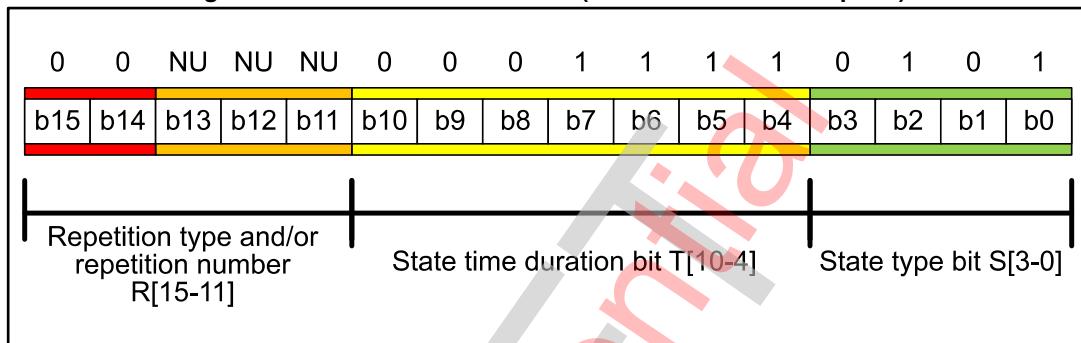
Wave form start TX TABLE			
Register name	Address	Row bit position	TX start address
Wave form start TX TABLE			
wf_sel_opt_0_r	0x101A	8 MSB	Channel 1
		8 LSB	Channel 0
wf_sel_opt_1_r	0x101B	8 MSB	Channel 3
		8 LSB	Channel 2
wf_sel_opt_2_r	0x101C	8 MSB	Channel 5
		8 LSB	Channel 4
wf_sel_opt_3_r	0x101D	8 MSB	Channel 7
		8 LSB	Channel 6
wf_sel_opt_4_r	0x101E	8 MSB	Channel 9
		8 LSB	Channel 8
wf_sel_opt_5_r	0x101F	8 MSB	Channel 11
		8 LSB	Channel 10
wf_sel_opt_6_r	0x1020	8 MSB	Channel 13
		8 LSB	Channel 12
wf_sel_opt_7_r	0x1021	8 MSB	Channel 15
		8 LSB	Channel 14

6.4 Setting waveform description

Each channel has a dedicated static RAM block containing 256 16-bit rows. Each row stores state type in the 4 least significant bits, time duration of the state in bit [10:4] and repetition data related to the repeat algorithm in the 5 most significant bits.

This means that the user can store for each channel m pulse state values into m SRAM rows related to n waveforms that must always be completed by an “end transmission” state. Waveform selection is carried out by setting the start memory address containing the first state to be generated. The waveform generator will start to produce states from the address selected until the “end transmission” is found.

Figure 15: SRAM row data content (waveform state description)



State type takes 4 bits, from b3 to b0, which are used to code one of the 10 states in which the pulser can be driven. The states and related code values are listed in the following table:

Table 16: Channel states and related code to be set

State name	Code	Description
“nop”	0000	No operations (clamp state)
“hz”	0010	Pulser HV output in high impedance
“clamp”	1111	Pulser HV output clamped to ground
“cl_wt_rx”	1110	End TX sequence, RX starts if enabled
“hvm0”	1010	Enable pull down of TX0
“hvp0”	0101	Enable pull up of TX0
“hvm1”	1001	Enable pull down of TX1
“hvp1”	0110	Enable pull up of TX1
“hvmm”	1011	Enable pull down of both TX0 and TX1
“hvpp”	0100	Enable pull up of both TX0 and TX1

The time duration takes 7 bits and allows an increase in the minimum duration of a state in the range:

$$2 \times \text{Tclk} < T < 129 \times \text{Tclk}$$

Generally the time duration is set using the following formula:

$$T = (2 + n) \times \text{Tclk}$$

Where n = bit [10:4] of the SRAM row.

Memory structure**STHV1600**

The waveform generated and transmitted by the pulser is a sequence of stored states, read from consecutive memory rows, starting from the memory address set in `wf_sel_opt_[7:0]_r` registers and stopping at the SRAM memory row that has been set with the `cl_wt_rx` state value. This state stops transmission.

For example, considering the following configuration:

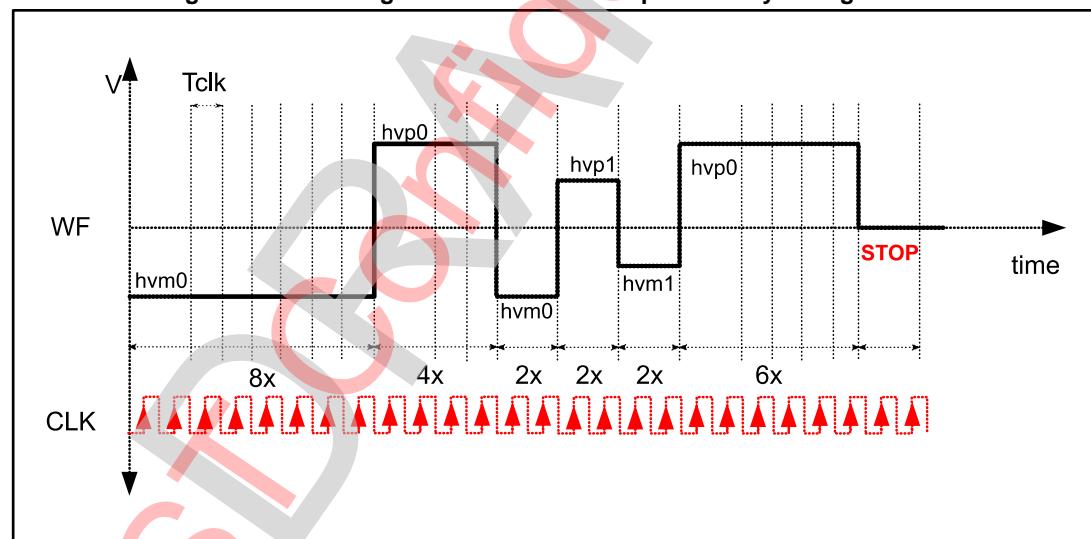
`wf_sel_opt_0_r = 0x0003` the starting address for channel 0 is set to 0x0003.

The SRAM memory data is set as in following table:

Table 17: Example of memory configuration

Address row	MSB 5 bit	7 bit	LSB 4 bit	State name	Waveform results
0x0003	00000	0000110	1010	"hvm0"	(2+6) Tclk of hvm0 state
0x0004	00000	0000010	0101	"hvp0"	(2+2) Tclk of hvp0 state
0x0005	00000	0000000	1010	"hvm0"	(2+0) Tclk of hvm0 state
0x0006	00000	0000000	0110	"hvp1"	(2+0) Tclk of hvp1 state
0x0007	00000	0000000	1001	"hvm1"	(2+0) Tclk of hvm1 state
0x0008	00000	0000100	0101	"hvp0"	(2+4) Tclk of hvp0 state
0x0009	00000	0000000	1110	"cl_wt_rx"	stop TX

The resulting waveform is shown in the following diagram:

Figure 16: Resulting waveform from example memory configuration

The “`cl_wt_rx`” state means that the channel stops transmitting and automatically goes into a clamp state, waiting for the receiving start.

Note that it is mandatory to fill the right number of memory rows according to the waveform that will be produced. In the last example the waveform takes 6 states and stops the transmitting state, meaning 7 memory rows to be written, starting at the address (0x0003) that will be put into the `wf_sel_opt_[7:0]_r` register. It is recommended to perform the memory initialization procedure ([Section 11.2: "SRAM 0 value initialization procedure"](#)) before starting the setting, configuration and transmission operations. If this is the case and the starting address written into `wf_sel_opt_[7:0]_r` points to an empty memory row, this means that a clamp state will be produced on the channels output.

As described in [Section 6: "Memory structure"](#), 16 SRAM blocks addressed by address bit [11:8], are set with the waveform description related to each channel. Address bit [7:0] are used to configure each memory row with the waveform state, related to the memory block addressed. If the system needs the same waveform set for all channels, it is not required to write the same content for each of the 16 memory blocks. In this case, to save setting time it is possible to write the bit conf_0_r[1] write_same_wf_to_all to 1 and configure the waveform description into rows belonging to only one memory block. The same data will also be written in all memory blocks at the same time. Memory block address bit [11:8] will not have any impact and can be set to "0000" addressing the channel 0 memory block. Address bit [7:0] related to rows must be set accordingly to the waveform to be configured.

ST Confidential

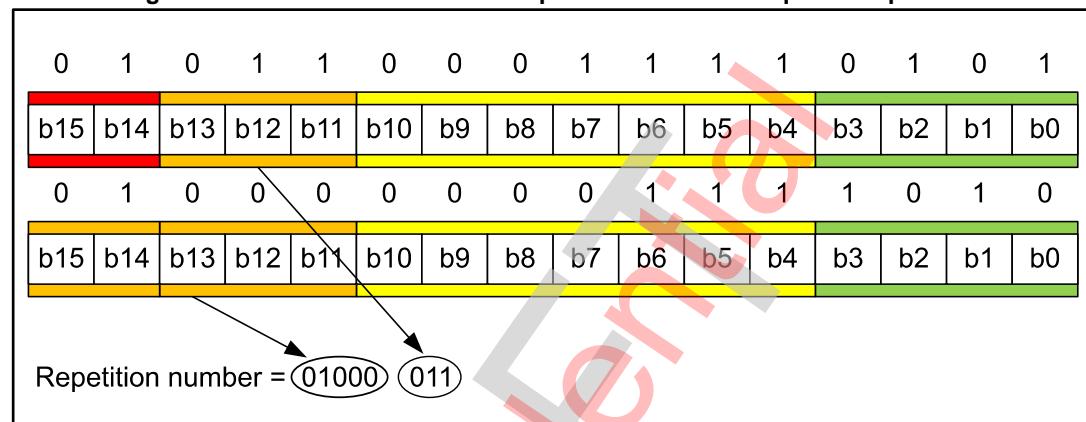
7

Configure repetition algorithm

A repetition sequence of repetitive multiple states stored in consecutive row memory is available and can be set using the 5 most significant bits from b15 to b11. Three scenarios can be configured:

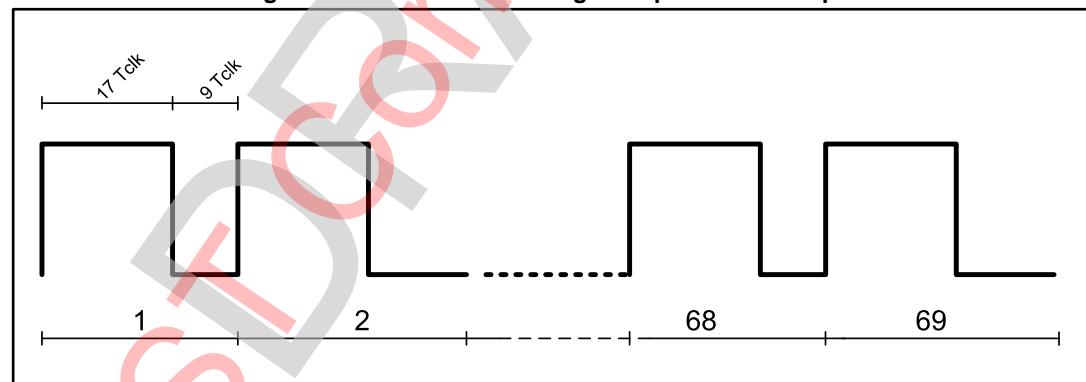
- If the first two most significant bits of the row are set to b15='0' b14='1' a repetition of two state sequence, stored in two consecutive SRAM rows, is performed. The first is described by the current row, the second by the next row.

Figure 17: Two SRAM rows set to implement two state sequence repetition



In the example, the first row will produce a state hv₀ (0101) taking $2 + 15(0001111) = 17$ Tclk. The second row produces a state hv_{m0} (1010) taking $2 + 7(0000111) = 9$ Tclk. Since the 2 most significant bits are set to "01" a repetition of the sequence formed by two states described will be performed, as shown below:

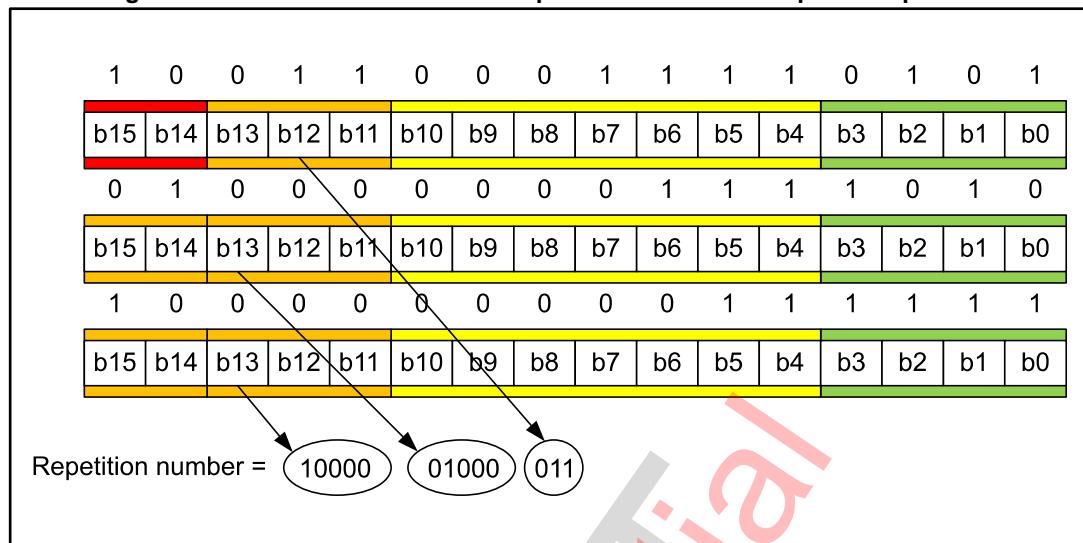
Figure 18: Waveform resulting from previous example



The least significant bit of the repetition number is given by the bit b13 b12 b11 of the first row involved, the 5 most significant bits are given by the most significant bit of the next row involved. In the example, the sequence will be repeated $2 + "01000" "011" = 69$ times.

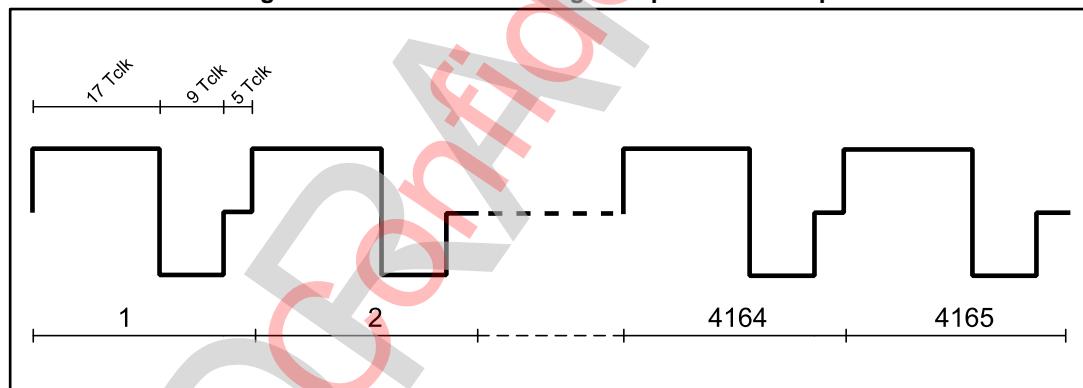
- If first two most significant bits of the row are set to b15=1 b14=0 a repetition of three state sequence, stored in three consecutive SRAM rows, is performed. The first is described by the current row, the second by the next row the third described by the subsequent row.

Figure 19: Three SRAM rows set to implement three state sequence repetition



In the example, the first row will produce a state hv₀ (0101) taking $2 + 15(0001111) = 17$ Tclk. The second row produces a state hv_{m0} (1010) taking $2 + 7(0000111) = 9$ Tclk. The third row produces a state clamp (1111) taking $2 + 3 (0000011) = 5$ Tclk. Since the 2 most significant bits are set to "10" a repetition of the sequence formed by three states described will be performed, as shown below.

Figure 20: Waveform resulting from previous example



The least significant bit of the repetition number is given by the bit b₁₃ b₁₂ b₁₁ of the first row involved, the next 5 bits are given by the most significant bit of the next row involved and the 5 most significant bits are given by the most significant bit of the third consecutive row. In the example, the sequence will be repeated $2 + "10000" "01000" "011" = 4165$ times.

- If the first two most significant bits of the row are set to b₁₅=1 b₁₄=1 a repetition of four state sequence, stored into four consecutive SRAM rows, is performed. The behavior is the same as the previous scenario, but with four states instead of three.

This means that if b₁₅=0 and b₁₄=1 the sequence repetition is the first type (two states) and the maximum number of repetitions allowed is $1+2^8$. If b₁₅=1 and b₁₄=0 the sequence repetition is of the second type (three states) and the maximum number of repetitions will be $1+2^{13}$. If b₁₅ = 1 and b₁₄ = 1 the sequence repetition is of the third type (four states) and the maximum number of repetition is $1+2^{18}$.

8 Configure receiving mode

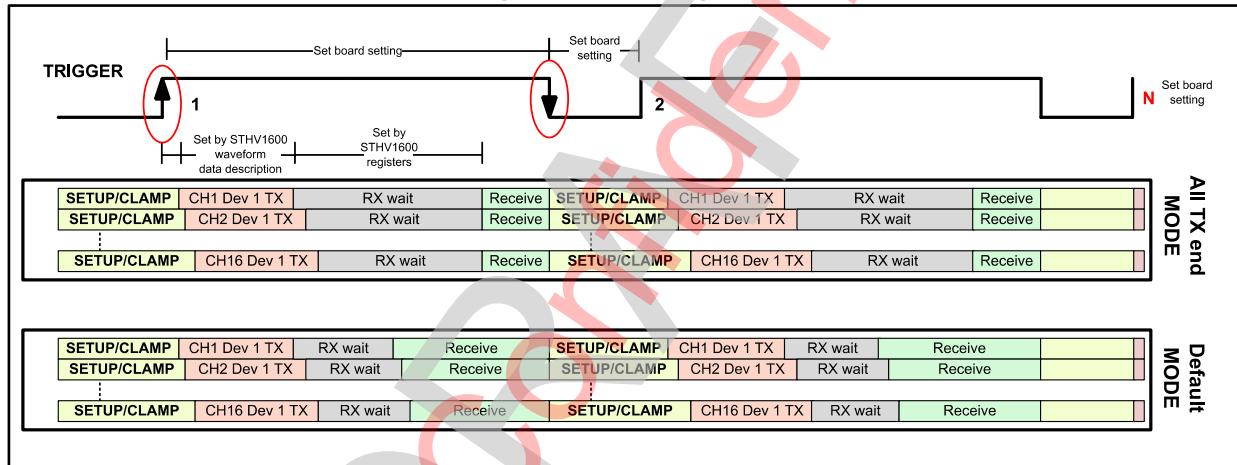
The “cl_wt_rx” state means that the channel stops transmitting and automatically goes into a clamp state, waiting for the receiving phase to start.

This waiting time takes a number of Tclk configured in the 15 LSB of the wait_rx_r register ([Table 31: "Register map"](#)). The default value is set to 0x000A, which means 11 clock pulses. The minimum value allowed is 1 x Tclk, while the maximum is 2^{15} x Tclk. After this duration has passed, if the related enable_rx_r bit is set to ‘1’ the channel is automatically put into a receiving state.

In cases of both receive and transmission enabled channels, two receiving modalities are available:

- “Default mode” when wait_rx_r[15] = 0: After the end of its own STOP clamp, the channel starts to receive only as an effect of the STOP state “cl_wt_rx” stored in its memory block, independent of other channel behavior.
- All “TX end mode” when wait_rx_r[15] = 1: The receiving operation of all channel starts at the same time, when the STOP clamp phase of the last transmitting channel ends.

Figure 21: Receiving mode description



If the related `enable_tx_r` bit is set to ‘0’ and `enable_rx_r` bit is set to ‘1’ the channel is disabled in transmission mode but enabled in receiving mode. In this case, three scenarios are possible:

- If `rx_start_mode` bit is ‘1’ the RX channel starts receiving at the rising edge of the trigger signal, independent of the `wait_rx_mode` value, which can be used to configure RX+TX channels.
- If `rx_start_mode` bit is ‘0’ and `wait_rx_mode = 0`, the RX channel starts receiving after the delay time set in the related delay register.
- If `rx_start_mode` bit is ‘0’ and `wait_rx_mode = 1`, the RX channel starts receiving after the last transmitting channel ends its wait receiving phase.

The following table summarizes all of the scenarios available and related register settings required.

Table 18: Receiving mode summary

16-bit register	16-bit register	Bit 13 of conf_0_r	MSB of wait_rx_r	
enable_rx	enable_tx	rx_start_mode	wait_rx_mode	Channel behavior
1	0	1	/	RX starts just at the trigger rising edge
1	0	1	/	
1	0	0	1	RX when last ends (all together)
1	0	0	0	RX with the delay set
0	1	/	/	Channel is in clamp after TX ends
1	1	/	1	RX when last ends (all together)
1	1	/	0	RX with the delay set
0	0	/	/	Channel always in clamp

In CW mode the behavior of the RX modes and related setting modalities are basically the same. There are two cases in which the configuration $wait_rx_mode = 1$ and $rx_start_mode = 0$ is meaningless, since in this configuration RX enabled channels start receiving after the last transmitting channel ends its wait receiving phase.

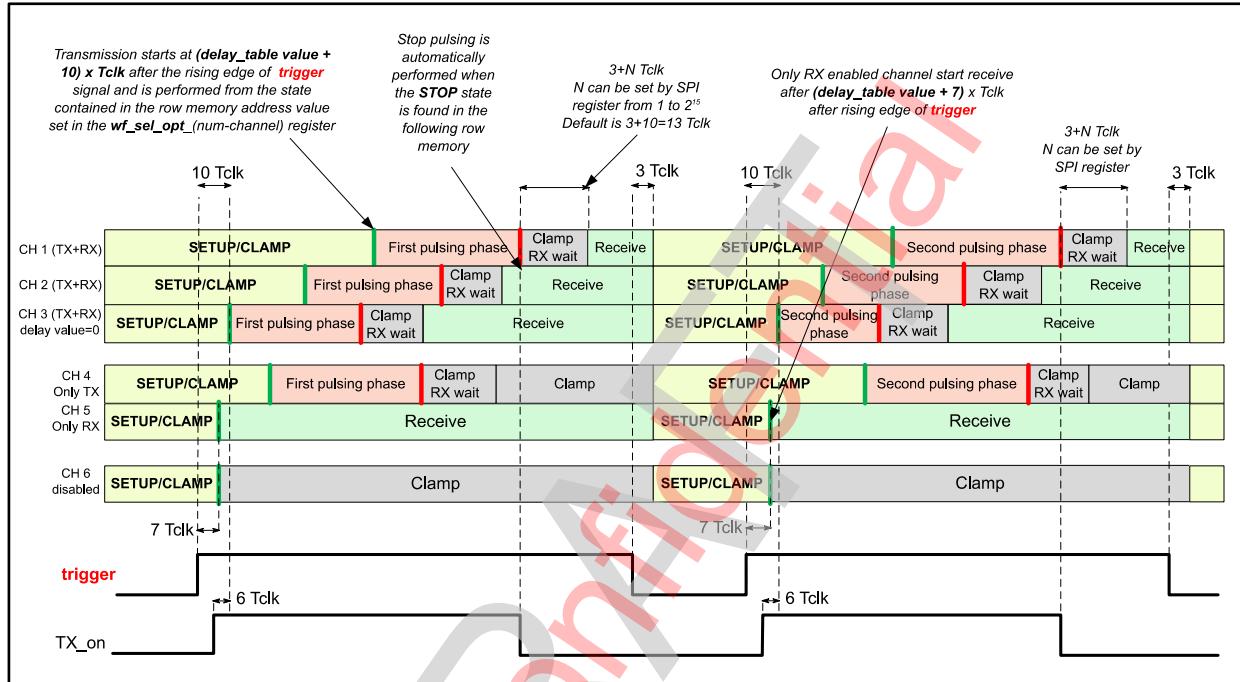
- In CW, TX enabled channels are continuously transmitting and never go into the wait receiving phase, meaning that the event causing RX enabled channel receiving never occurs, leaving them in clamp.
- If all 16 channels are RX enabled, the condition is the same as previous case. No channels are transmitting so the event causing RX enabled channel receiving never occurs, leaving them in clamp.

9 Transmission and receiving phases management

9.1 Default mode

An example of transmission with channel set in a different configuration is shown in [Figure 22: "TX/RX operation example"](#).

Figure 22: TX/RX operation example



Channel 1 and 2 are TX and RX enabled. Considering channel 1, just at the rising edge of the external trigger signal, it starts transmission after the following time:

$$\text{TX wait time} = (\text{delay_tab_0_r value} + 10) \times \text{Tclk}$$

After this time the waveform generator starts to read the SRAM row content addressed by the value set in 8 LSB of register `wf_sel_opt_0_r`. The following rows are read and the related state translated into waveforms until a "cl_wt_rx" state is found, which stops transmission. This event puts the channel in a clamp state waiting the RX phase. This time is configurable as follows:

$$\text{RX wait time} = (\text{wait_rx_r}[14:0] \text{ value} + 3) \times \text{Tclk}$$

After this time ends the channel goes into RX condition until a falling edge of the external trigger signal is provided and the channel is put into clamp state, ready for the next operation.

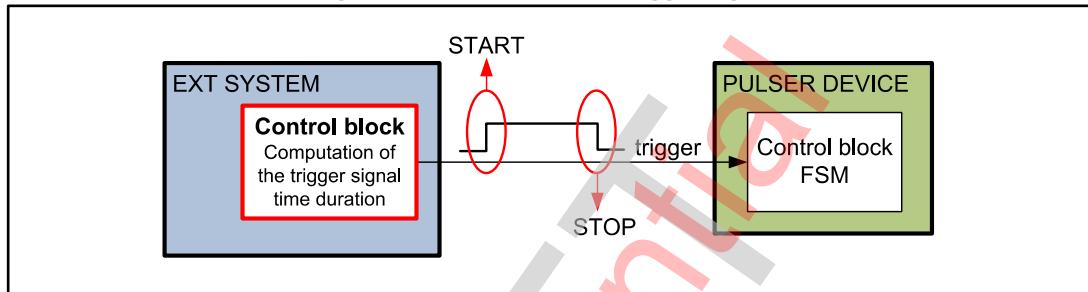
- Channel 3 has the same configuration as channel 1 and 2, but for the beamformer delay value of register `delay_tab_2_r` that is 0x0000. In this case, the channel starts TX after the default time 10 x Tclk
- Channel 4 is only TX enabled. A clamp state is performed instead of the RX condition

- Channel 5 is only RX enabled. The RX starts after the following time:
 $\text{RX wait time} = (\text{delay_tab_0_r value} + 7) \times \text{Tclk}$
 and stops after a falling edge of external trigger signal that put channel in clamp state.

9.2 Trigger, TX_ON signals

Once all device configurations are set, only the external signal trigger is used to manage all operations. In case of channel fully enabled, the rising edge of the trigger starts channel transmission after $(\text{delay_tab_0_r value} + 10) \times \text{Tclk}$. When $\text{enable_tx_r} = '0'$, the channel is enabled only in receiving operations, which starts after $7 \times \text{Tclk}$ from the rising edge of the trigger.

Figure 23: External control trigger signal



When all channels end transmission, automatically they go into a waiting receive state and then, if enabled, into a receive state that is externally stopped for all channels at the same time by the falling edge of the trigger signal.

This signal is basically used to start all the operation sequences produced by the internal FSM and stop the last running operations (receiving or clamp) in order to put the device in a new idle state. During idle condition, further SPI communications are possible to change delay values or waveform selections and the device is ready for a new rising edge of the trigger which starts a new transmission. The pulsing frequency of the trigger sets the PRF, and the duty cycle sets the RX versus SETUP/CLAMP time duration.

The signal TX_on goes high 6 Tclk before the first channel starts pulsing and 4 Tclk after the rising edge of the trigger is provided. It goes low just when the last channel transmitting ends its waveform and stops pulsing if bit conf_1r[3] (tx_run_type) = 0, otherwise it goes low after the wait RX phase ends.

The signal trigger must respect some constraints for correct device operation:

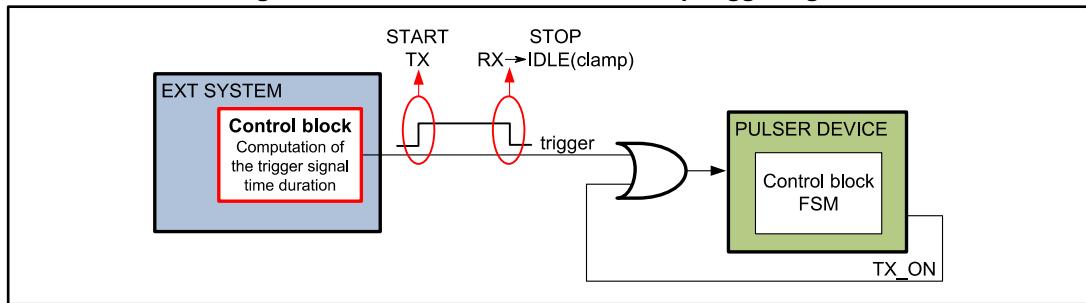
- It must be glitch free
- The falling edge must be provided only when the device ends transmission and RX wait operation of all channels
- The falling edge must be provided only during receiving

The TX_on signal can be used to generate the external signal trigger, with the required constraints:

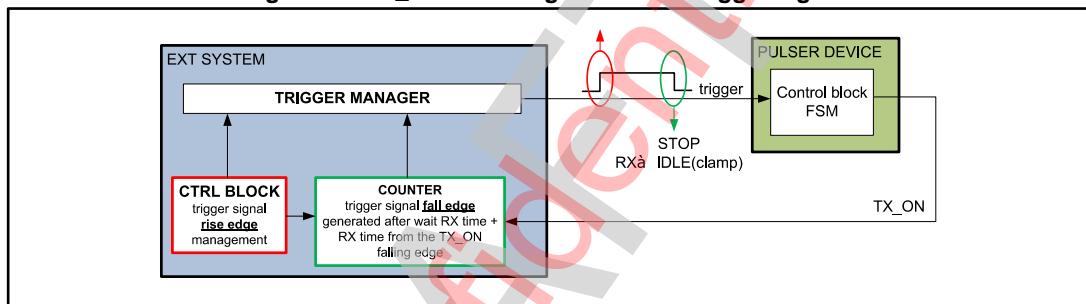
- To ensure that the trigger signal will not go low and have no glitches during transmission operations, it can be generated by an OR condition between the trigger generated by an external system and the TX_on signal generated by the device (Figure 24: "TX_ON used to close the loop trigger signal").

Transmission and receiving phases management

STHV1600

Figure 24: TX_ON used to close the loop trigger signal

- Signal TX_on is useful to generate the trigger signal in external system without considering a complex computation of all waveform configurations and all the beamformer delay. The system can set the high state time duration of the trigger signal as the sum of the high state time duration of the TX_on signal, the RX wait time and the receiving time desired ([Figure 25: "TX_ON used to generate the trigger signal"](#)).

Figure 25: TX_ON used to generate the trigger signal**9.3 CW mode**

When bit 3 of conf_0_r register is set to '1' the CW mode is enabled. In this case channels with related TX enable bit enable_tx_r = '1' continuously transmit a repetition sequence of multiple states stored in maximum 4 consecutive rows of memory.

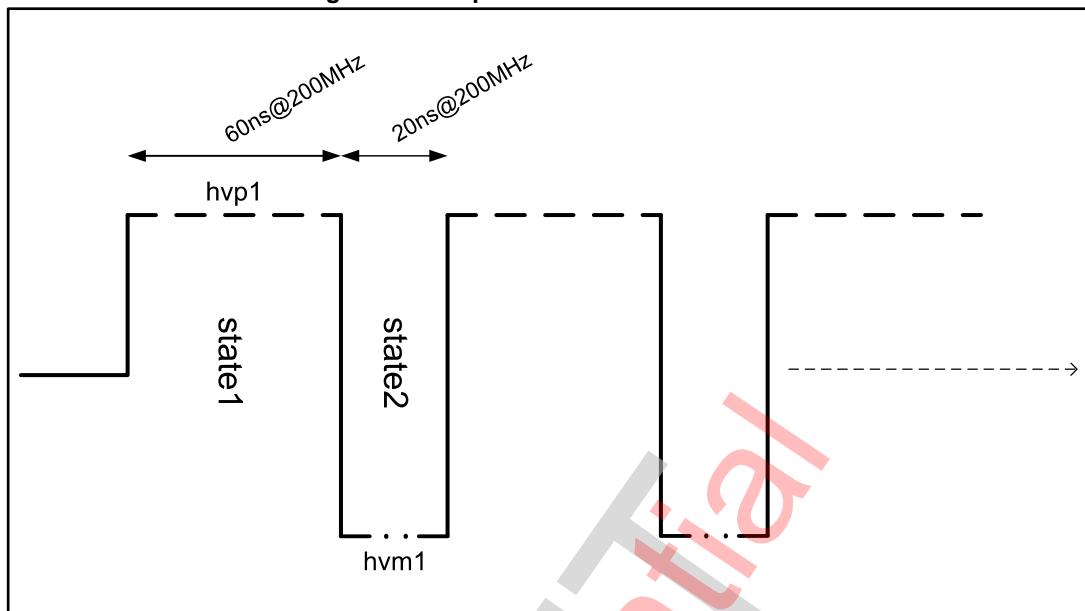
In this configuration, the output waveform can be described following the rules in the repetition algorithm ([Section 7: "Configure repetition algorithm"](#)):

- To output a continuous sequence of two states, two SRAM rows are needed and must be configured as:

Table 19: CW pulse mode with two states

RAM row	Repetition states bit [15:14]	In CW must be 0	State duration @ 200 MHz bit [10:4]	State type bit [3:0]
1	01 2 state	000	0000101 60 ns	0110 HVP1
2	00	000	0000010 20 ns	1001 HVM1

Figure 26: CW pulse mode with two states

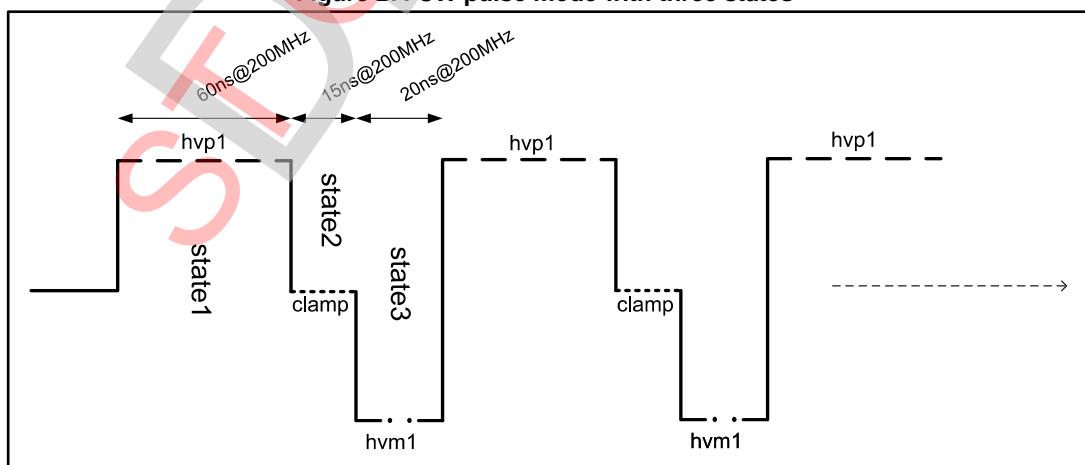


- To output a continuous sequence of three states, three SRAM rows are needed and must be configured as:

Table 20: CW pulse mode with three states

RAM row	Repetition states bit [15:14]	In CW must be 0	State duration @ 200 MHz bit [10:4]	State type bit [3:0]
1	10 3 state	000	0000101 60 ns	0110 HVP1
2	00	000	0000001 15 ns	1111 CLAMP
3	00	000	0000010 20 ns	1001 HVM1

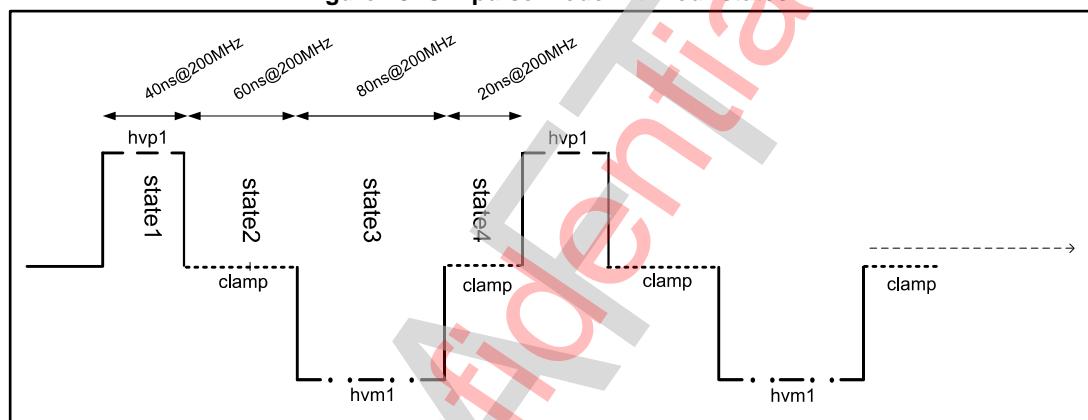
Figure 27: CW pulse mode with three states



- To output a continuous sequence of four states, four SRAM rows are needed and must be configured as:

Transmission and receiving phases management**STHV1600****Table 21: CW pulse mode with four states**

RAM row	Repetition states bit [15:14]	In CW must be 0	State duration @ 200 MHz bit [10:4]	State type bit [3:0]
1	11 4 state	000	0000110 40 ns	0110 HVP1
2	00	000	0001010 60 ns	1111 CLAMP
3	00	000	0001110 80 ns	1001 HVM1
4	00	000	0000010 20 ns	1111 CLAMP

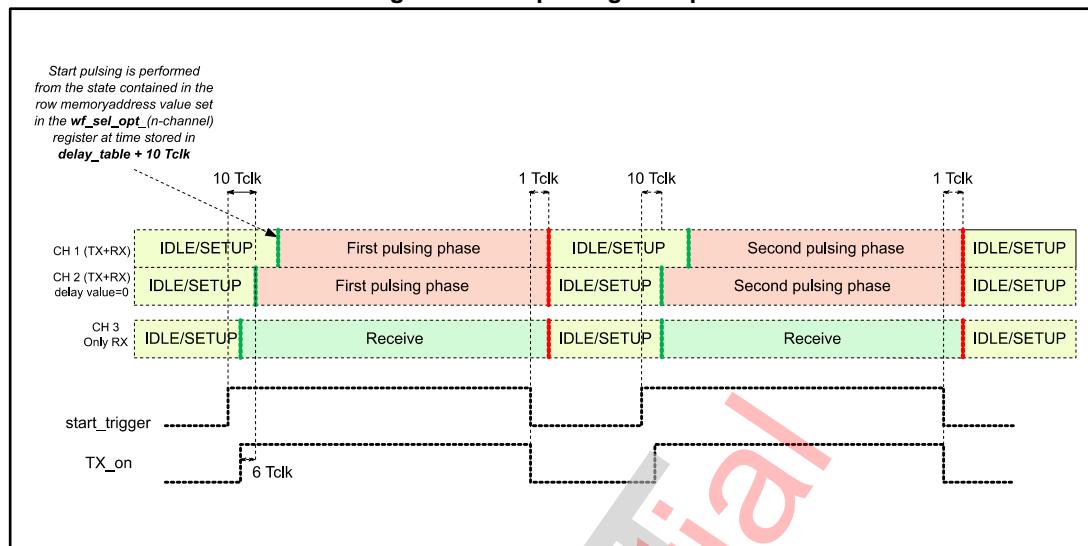
Figure 28: CW pulse mode with four states

Starting point memory, containing the first row of the previous configuration, can be selected using the `wf_sel_opt_[7:0]_r` register. In this way, one of the several waveforms that can be stored in related channel memory can be used and selected for each channel by only setting 8 16-bit registers.

Note that it is mandatory to fill in the correct number of memory rows in accordance with the CW repetition chosen. In the last example, the repetition is related to four state, meaning four memory rows to be written, starting at the address that will be put into the `wf_sel_opt_[7:0]_r` register. It is mandatory to perform the memory initialization procedure before starting the setting, configuration and transmission operations. If this is the case and the starting address written into `wf_sel_opt_[7:0]_r` points to an empty memory row, a clamp will be produced to the channel outputs.

In CW mode, the state “cl_wt_rx” is not needed since transmitting or receiving is continuously performed and stopped externally by a trigger signal.

Figure 29: CW pulsing example



10 SPI description

The SPI protocol allows configuration of all rows of the memory. Writing and reading operations related to SRAM blocks or registers are managed in the same way by the protocol. To increase bit rate and reduce the configuration time as much as possible, 4 input data lines DATA_IN must be used in the SPI protocol communication.

10.1 Writing

Each write operation needs 10 clock pulses during which the 4 DATA_IN[3:0] input pins must be properly driven as described in [Figure 30: "Single write operation"](#). The first 5 clock pulses sample the communication header containing a 13 bit address, 1 bit to select the operation (to write it must be 0), 4 bit device address and two meaningless bits supposed to be '0' as described in the [Figure 31: "Single write operation, 4-bit vectors sampled"](#).

The next 4 clock pulses sample the 16 data to be stored. The last clock pulse samples an optional parity code. All data bits are sampled by the SPI device on the rising edge of the serial clock. The parity check can be enabled/disabled, when enabled, if the check fails, the related writing operation will not be performed and one clock period pulse is output on the interrupt pad. Otherwise when check is disabled, 4 parity bits and related clock pulse must be provided anyway, with a value of '0'.

The four bit parity is calculated as follows:

P3 = 1 if the number of 1 in bit stream of DATA_IN[3] (header+data) is odd, otherwise it is 0

P2 = 1 if the number of 1 in bit stream of DATA_IN[2] (header+data) is odd, otherwise it is 0

P1 = 1 if the number of 1 in bit stream of DATA_IN[1] (header+data) is odd, otherwise it is 0

P0 = 1 if the number of 1 in bit stream of DATA_IN[0] (header+data) is odd, otherwise it is 0

Figure 30: Single write operation

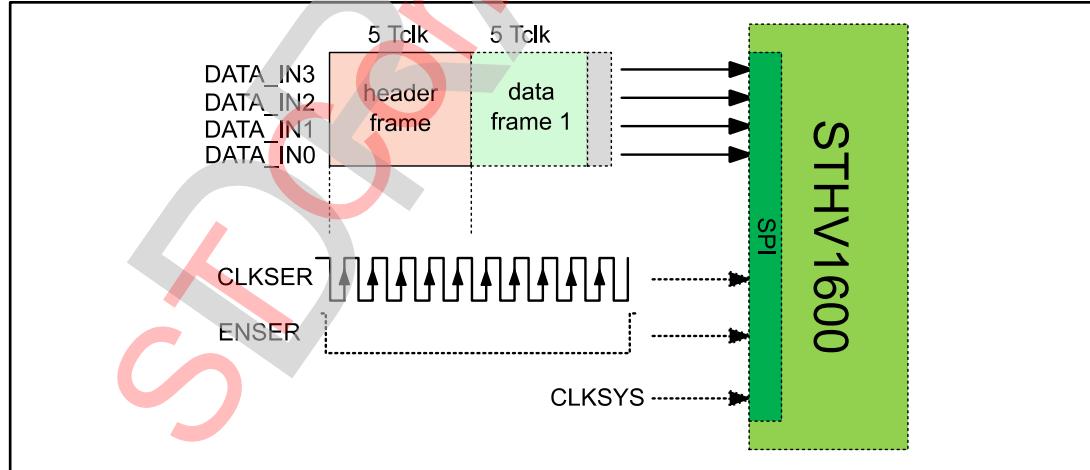
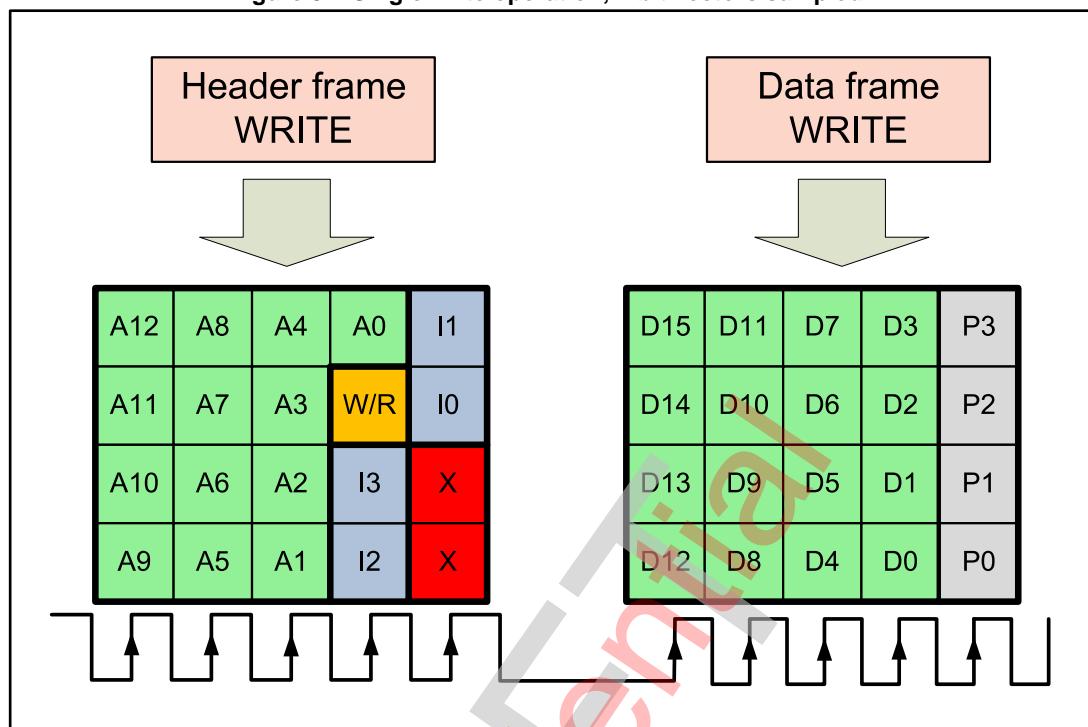
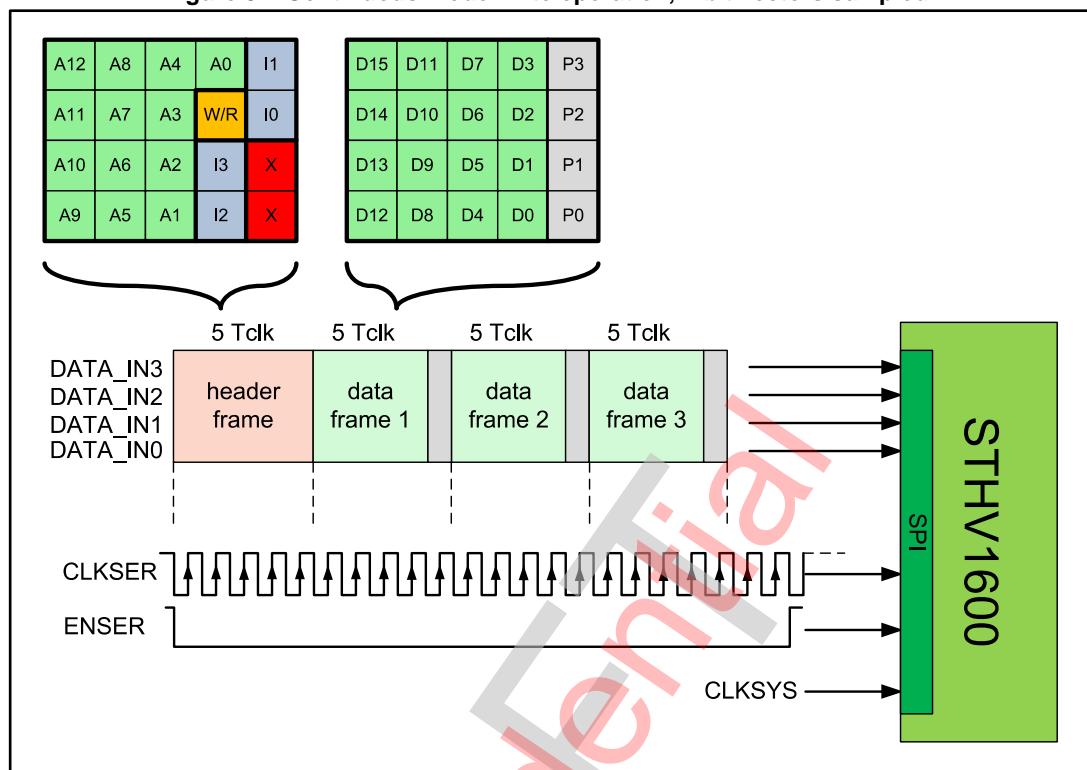


Figure 31: Single write operation, 4-bit vectors sampled



The SPI protocol also implements a “burst” continuous mode, in which providing only one header allows the writing of several registers with consecutive addresses. The header contains the start address of the first register to be written with data frame sampled by the next 5 serial clock pulses. The following data frames are written into registers with start address incremented by one (see [Figure 32: "Continuous mode write operation, 4-bit vectors sampled"](#)).

Figure 32: Continuous mode write operation, 4-bit vectors sampled



In this case only first parity value is calculated considering the bit streaming of header + data frame 1 (see previous description). The next parity values are calculated only on the following data frame 2 - 3.

P3 = 1 if the number of 1 in bit stream of DATA_IN[3] (only data) is odd, otherwise it is 0

P2 = 1 if the number of 1 in bit stream of DATA_IN[2] (only data) is odd, otherwise it is 0

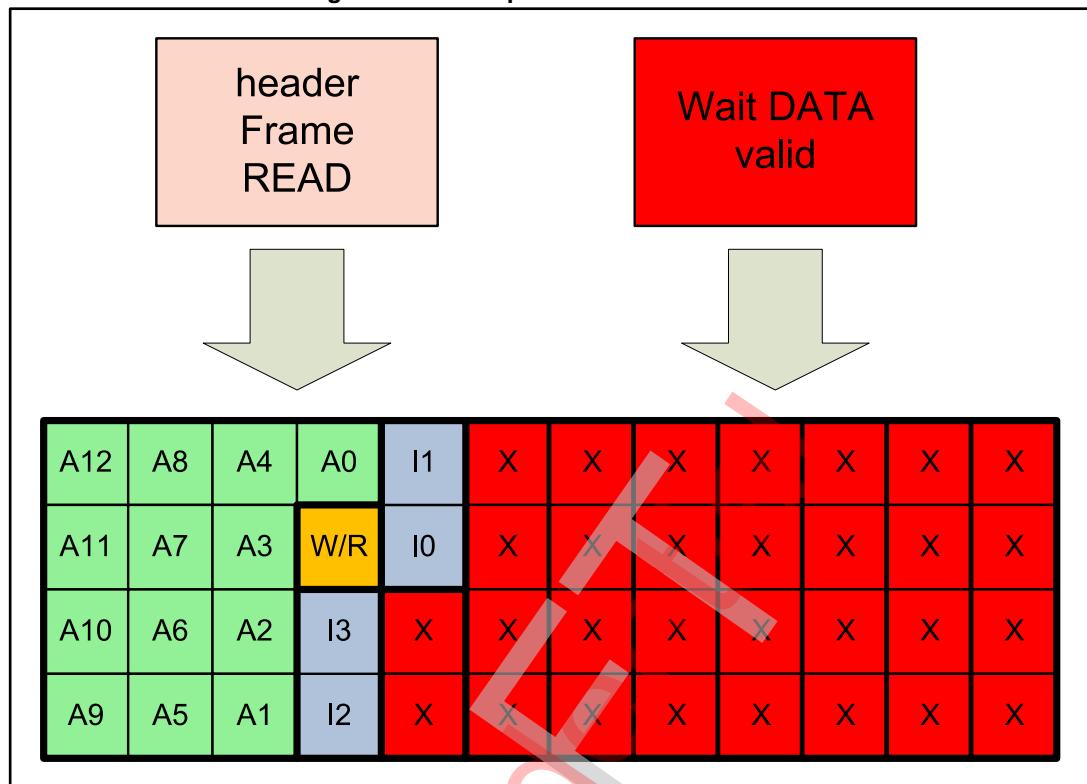
P1 = 1 if the number of 1 in bit stream of DATA_IN[1] (only data) is odd, otherwise it is 0

P0 = 1 if the number of 1 in bit stream of DATA_IN[0] (only data) is odd, otherwise it is 0

10.2 Reading

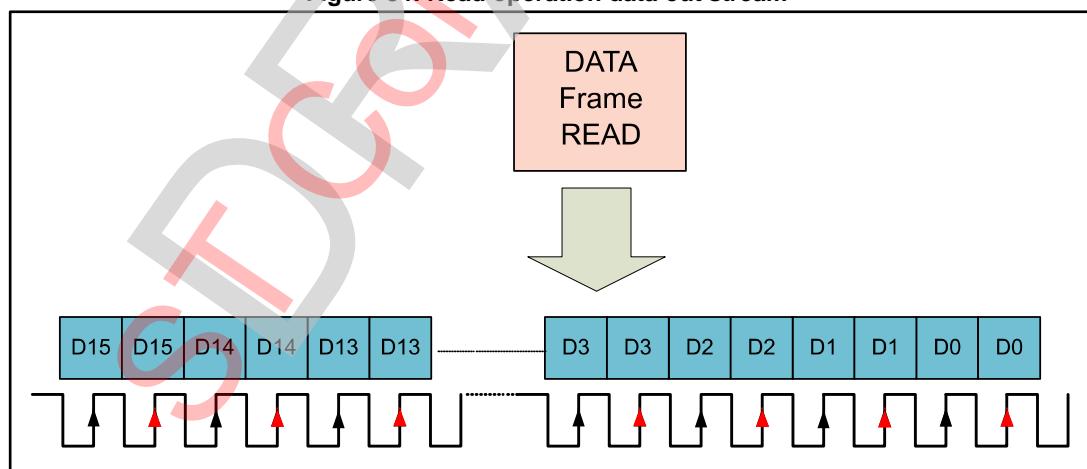
Each read operation needs 44 clock pulses during which the 4 DATA_IN[3:0] input pins must be properly driven. The first 5 clock pulses sample the communication header, containing 13 bit address, 1 bit to select the operation (to read it must be 1), 4 bit device address. Once the header is provided, after seven serial clock pulses ([Figure 33: "Read operation data out stream"](#)), the data is available to the DATA_OUT pin and can be sampled by 32 (64) clock pulses.

Figure 33: Read operation data out stream



To sample data out, 32 clock pulses are needed (twice the data bit number) since each bit of the data frame takes 2 serial clock pulses, and the valid bit must be sampled on the second rising edge, shown with a red arrow in [Figure 34: "Read operation data out stream"](#).

Figure 34: Read operation data out stream



Conf_1_r[4] bit is used to select the read mode at the DATA_OUT pin. If it is 0 the data bit takes 2 serial clock pulses, meaning that the valid bit must be sampled on the 2nd one. If it is 1 the data bit takes 4 serial clock pulses and the valid bit must be sampled on the 4th (see [Figure 35: "Continuous mode read operation with different sampling modes"](#)).

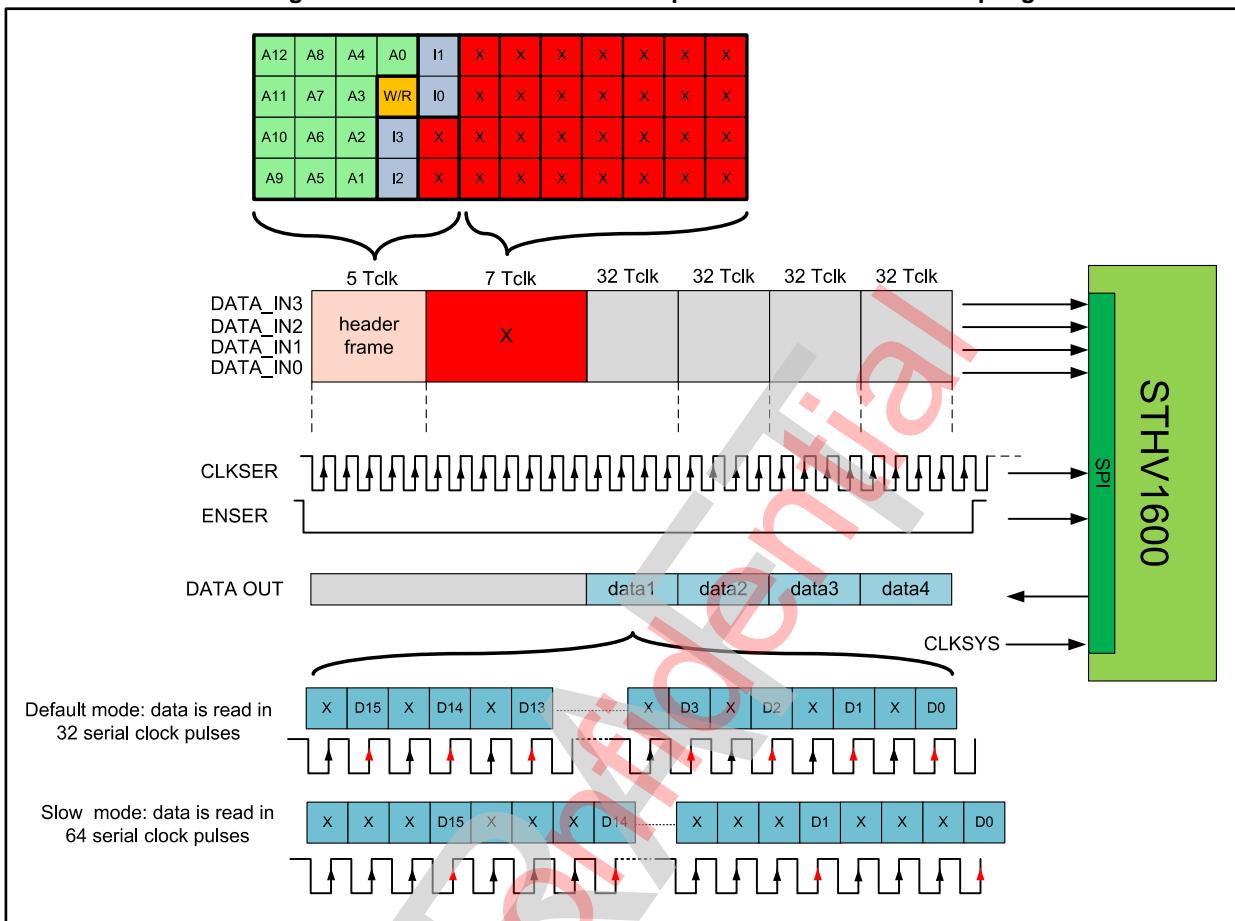
Read operations also support burst continuous mode. It is only needed to provide the proper number of clock pulses and the device will output several data frames to the

SPI description

STHV1600

DATA_OUT pin, starting from those addressed by the start address of the header (data1) and following the data addressed by the start address incremented by one (data2, data3, etc.).

Figure 35: Continuous mode read operation with different sampling modes



11 Advanced features

11.1 State inversion

When the bit 5 of register conf0_r called state_inversion is set to '1', the waveform generated presents positive and negative voltage level states, inverted compared to those stored in memory. This is useful to output a complementary waveform quickly, without writing one by one the new inverted value into the SRAM, only setting to '1' one bit of configuration register.

Table 22: State inversion table

State name	Code stored	Description	Invertible	Output when state_inversion ='1'
nop	0000	No operation (clamp)	no	0000
hz	0010	Pulser output in HZ	no	0010
clamp	1111	Pulser output in clamp	no	1111
cl_wt_rx	1110	End TX, RX starts if enabled.	no	1110
hvm0	1010	Enable negative voltage 0	yes	0101
hvp0	0101	Enable positive voltage 0	yes	1010
hvm1	1001	Enable negative voltage 1	yes	0110
hvp1	0110	Enable positive voltage 1	yes	1001
hvmm	1011	Enable both negative voltage 0&1	yes	0100
hvpp	0100	Enable both positive voltage 0&1	yes	1011

11.2 SRAM 0 value initialization procedure

When bit 12 of register conf0_r, called start_ram_wrtozero, is set to '1', an internal procedure starts and writes all bits of all SRAM cells to a '0' value. This initialization procedure takes the following time:

$$\text{Twr_all_to_zero} = 256 \times \text{TCLKSYS}$$

It is recommended to start this procedure after power-on of the device to ensure that all states stored are NOP.

11.3 Power saving features

11.3.1 SRAM power down

SRAM blocks can be put in low leakage mode when neither read nor write operations are needed, meaning that this mode cannot be used during transmission and IDLE states in which the device can be configured by SPI, but only when channels are receiving. There are two ways to enable this feature:

1. Manually writing the bit 7 of register conf0_r to a '1' value. This enables the low leakage mode of all SRAM blocks.
2. Writing bit 6 of register conf0_r to a '1' value, an auto-management mode of the SRAM low leakage mode is enabled. In this case, the device automatically forces SRAM blocks into low leakage mode ONLY during receiving operations.

11.3.2 Current reference enable options

Current reference blocks can be switched off to limit power consumption when not needed. Obviously, during the transmission phase, the current reference blocks must be enabled but also during the IDLE state, at least 2 us before the transmission phase. There are two ways to enable this feature:

1. Writing bit 9 of register conf0_r to a '1' value, the manual management of reference power-down is enabled. To selectively switch on/off the reference blocks, refer to register ref_por_set_r (bit 7:4).
2. Writing bit 8 of register conf0_r to a '1' value, current references are automatically disabled during receiving and enabled when in TX and IDLE.

11.3.3 I/O LVDS interface enable options

IO LVDS, related to SPI (DATA_IN[3:0], ENSER, CLKSER), can be disabled in order to reduce power consumption when device configuration by SPI is not required. When channels are transmitting or receiving, SPI is not used and any changes in device configuration can be unwanted or dangerous.

Writing bit 14 of register conf0_r to a '1' value, LVDS IO cells are automatically disabled during TX+RX cycles and enabled during IDLE conditions. This means that during TX and RX, SPI communications are disabled.

11.3.4 Overall low power mode

Writing bit 10 of register conf0_r to a '1' value, all analog blocks are disable and the overall device is put into low power mode. In this mode, LVDS input buffer (DATA_IN[3:0], ENSER, CLKSER), current reference blocks and SRAM blocks are disabled.

The only two way to wake up the device are:

1. Provide a system reset (all register values previously written will be deleted)
2. Provide a trigger pulse. In this mode no transmission starts, and the device is ready and put in functional mode.

11.3.5 CMOS input configuration

To use CMOS interface, it is sufficient to supply N balls at 1 V (typ) and to drive P balls.

In this case, to save power consumption lvds_set_r bit 7 & 5 can be put into a logic state '1' and bit 6 & 4 to '0'. This condition allows reduction of DVDD consumption from 8 mA to 1 mA.

12 Interrupt and communication checks

12.1 Communication checks

12.1.1 Parity

A 4-bit vector must be provided at the end of a write communication after the data frame, driving the 4 input lines DATA _IN[3:0]. The parity [3:0] vector is calculated as:

P3 = 1 if the number of 1 in the bit stream of DATA _IN[3] (header+data) is odd, otherwise 0.

P2 = 1 if the number of 1 in the bit stream of DATA _IN[2] (header+data) is odd, otherwise 0.

P1 = 1 if the number of 1 in the bit stream of DATA _IN[1] (header+data) is odd, otherwise 0.

P0 = 1 if the number of 1 in the bit stream of DATA _IN[0] (header+data) is odd, otherwise 0.

When a burst continuous communication starts, the parity vector is calculated only from the data frame.

P3 = 1 if the number of 1 in the bit stream of DATA _IN[3] (only data) is odd, otherwise 0.

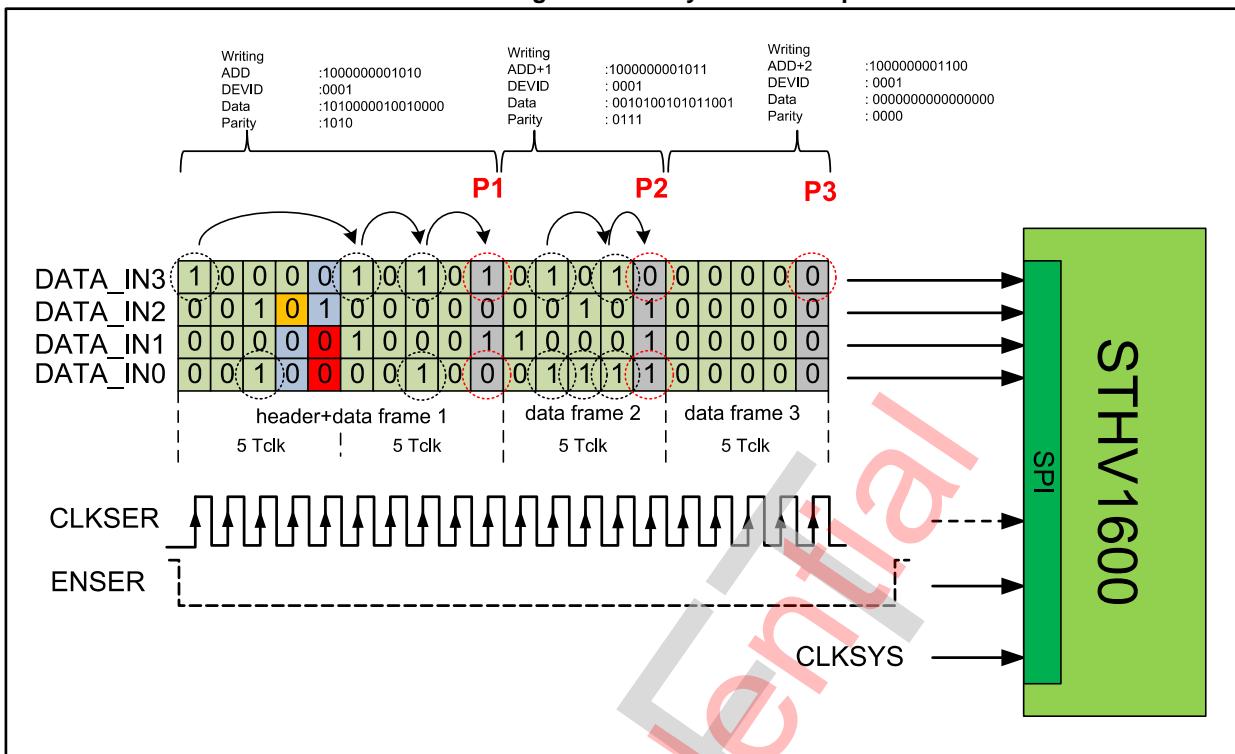
P2 = 1 if the number of 1 in the bit stream of DATA _IN[2] (only data) is odd, otherwise 0.

P1 = 1 if the number of 1 in the bit stream of DATA _IN[1] (only data) is odd, otherwise 0.

P0 = 1 if the number of 1 in the bit stream of DATA _IN[0] (only data) is odd, otherwise 0.

Parity check is always enabled and fail information is always available to bit 14 of the status register. It is also possible to enable the INT pin to provide parity fail information by writing bit 11 of conf_0r to a '1' value. In this case, the INT pin goes low when a parity fail occurs and can be reset by reading the status register. Optional behavior is available through writing bit 2 of register conf_1r: the INT pin will go low for one clock pulse each time parity fails. With this configuration the system can identify each SPI communication fail during the data stream. If the parity check function is not used, the parity code can be always put to a "0000" value, parity INT must be disabled (conf_0r[11]='0') and the system will not care about bit 14 of the status register.

Figure 36: Parity check example



12.1.2 Checksum

The checksum feature can be enabled by setting bit 4 of conf0_r register to 1. In this case the device calculates internally a 16-bit sum CS of all provided 4-bit vectors driving the 4 input lines DATA_IN[3:0], considering the header frame and data frame of all the writing operations performed, for a maximum number of 430 write communications. Just before starting pulser transmission, the CS value, calculated by the external system, must be written to the 16-bit register checksum_r. If the written value matches the internally calculated value, the system works normally, otherwise an internal signal goes high, disabling all transmission and the external trigger signal will have no effect, until a new communication sequence with the correct CS is provided. When bit 4 of the conf0_r register is set to 0 (default), the checksum feature is disabled. In this case, the checksum_r register content has no influence on the system and can be ignored.

When checksum is not verified, all transmissions triggered after the checksum register write operation are disabled, bit 13 of the status read register and interrupt output signal go to a '1' value.

The suggested procedure is:

1. Enable checksum check writing bit 4 of conf0_r to 1
2. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x0000 to 0x1021, storing all waveform data descriptions in 16 SRAM blocks and all the configuration data into registers.
3. Write checksum calculated as the sum of all 4-bit vectors provided to the DATA_IN pins during point 2, into register 0x1022. The check is performed just at the end of this operation.

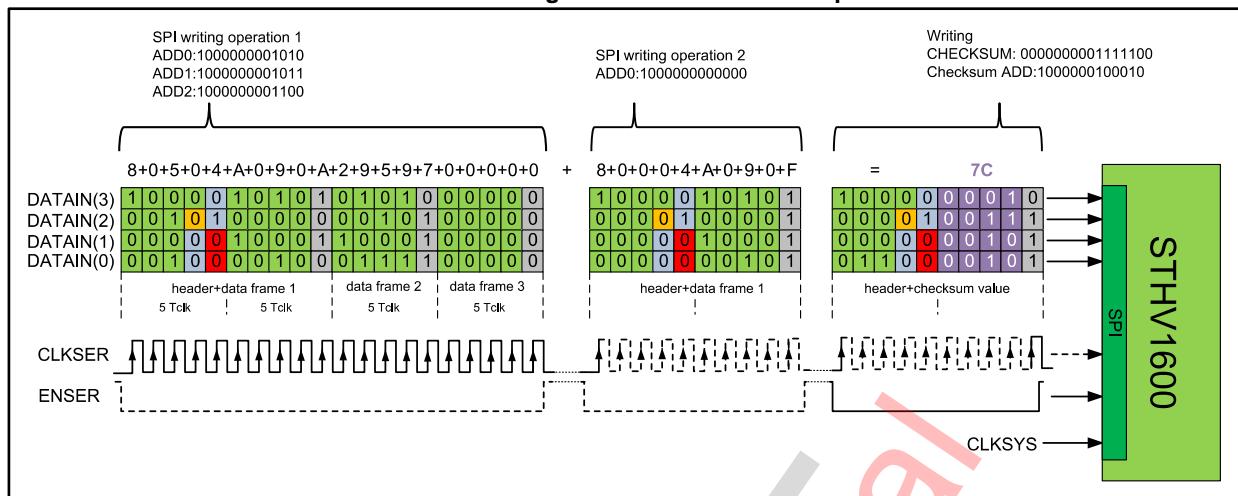
In case not all the 256 rows containing waveform description data are needed, the recommended procedure is to provide several checksum values:

1. Enable checksum check writing bit 4 of conf0_r to 1
2. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x0000, storing all the waveform data descriptions needed into SRAM block 1.
3. Write checksum value calculated as the sum of all 4-bit vectors provided to DATA_IN pins during point 2 into register 0x1022. The check is performed just at the end of this operation.
4. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x0100, storing all the waveform data descriptions needed into SRAM block 2.
5. Write checksum value calculated as the sum of all 4-bit vectors provided to DATA_IN pins during point 4 into register 0x1022. The check is performed just at the end of this operation.
6. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x0200, storing all the waveform data descriptions needed into SRAM block 3.
7. Write checksum value calculated as the sum of all 4-bit vectors provided to DATA_IN pins during point 6 into register 0x1022. The check is performed just at the end of this operation.
8. Repeat points 6-7 to write and check remaining SRAM blocks.
9. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x1000 to 0x1021, storing all the configuration data into registers.
10. Write checksum value calculated as the sum of all 4-bit vectors provided to the DATA_IN pins during point 9 into register 0x1022. The check is performed just at the end of this operation.

In case the “write same waveform to all channels” option is enabled, the recommended procedure is to provide several checksum values:

1. Enable checksum check writing bit 4 of conf0_r to 1
2. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x0000, storing all the waveform data description needed into SRAM blocks.
3. Start a multi-writing operation using the SPI in burst mode, starting from the register address 0x1000 to 0x1021, storing all the configurations data into registers.
4. Write checksum value calculated as the sum of all 4-bit vectors provided to the DATA_IN pins during point 9 into register 0x1022. The check is performed just at the end of this operation.

Figure 37: Checksum example



12.2 Interrupt

Interrupt signals are internally generated to put the device and the overall system into a safe condition in case of undesired events. All of these checks can be disabled by default and can be enabled with the SPI register bit.

Several checks are internally performed to put the device and the overall system into a safe condition in case of undesired events. Digital checks are:

- TX time out: enabled by setting bit *time_out_f[15]* = '1'. If the TX operation takes more than the number of clock pulses set in *time_out_f[14:0]* the INT signal goes high and a dedicated bit in the status register is set to 1 until a read of status register is performed. TX stop at the end of time-out time and FSM is reset.
- SPI parity: always enabled and checks if the parity value provided at the end of each data frame matches with the internally computed parity value. This is the sum of all 10 4-bit DATA_IN vectors contained in header+data frame streaming bit vectors. In case of SPI burst mode it is the sum of 4 4-bit DATA_IN vectors contained in further data frames. When a fail occurs, a dedicated clear on read bit assume '1' value into status register. INT signal can be enabled to provide parity fail information, writing *conf_0_r[11]* = '1'. When enabled, in case of parity fail, it goes low until a status register is read. If *conf_0_r[2]* bit (parity_type) is 0 or 1 it goes low for a system clock pulse if *conf_0_r[2]* bit is 1. In this case it is possible at every fail event, allowing to get several parity errors during SPI communication.
- Checksum: it is enabled setting bit 4 of register *conf_0_r* to '1'. In this case it is possible to write the checksum value related several SPI communications into the proper register *checksum_r* at address 0x1022. If it does not match the internal computed value bit 12 of status register goes high and INT signal goes low until status register is read at address 0x1028.
- Wrong state: each waveform state read by memory and driving transmitter is checked, in order to avoid transmission of non-existent states set by user in sRAM blocks. In this case a clamp is generated instead of storing the non-existent state. It also checks that during CW transmission states coding hvp0 or hvm0 are not used. When one of these two events occurs, bit 13 of the status register goes high and the INT signal goes low until the status register is read. This check is always enabled.
- NOP check: if waveform state code stored in memory is "0000", meaning that sRAM memory blocks is not properly configured and a start transmission is performed (trigger signal rising edge) the waveform generator is reset and transmission stops. This check is always enabled.

All analog checks are enabled by analog enable bit (conf_1_r[9], conf_1_r[10], conf_1_r[11], conf_1_r[12]) and the related information is available from the INT pin and status register, 1024 system clock pulses after the power supply has been provided. Analog voltage checks are performed only at the rising edge of the trigger signal.

Analog check can also impact functionality if the related digital enable bits are enabled (conf_1_r[1], conf_1_r[6], conf_1_r[7], conf_1_r[8]). If any problems occurs, current transmission is stopped, FSMs are reset, channel outputs are forced into HZ and further trigger rising edges will not be considered until a wakeup bit conf_1_r[0] = '1' is provided. All these actions differ from one check to another: the correspondence is described in the following table.

ST Confidential

Interrupt and communication checks

STHV1600

Table 23: Interrupt functions table

Name	Analog enable	Digital enable	Effect	Wakeup	Status reg INT output enable	Status reg INT output reset
TX time out	/	<i>time_out_en</i> <i>time_out_r[15] = '1'</i>	FSM reset and TX stop if timeout set ends before the trigger falling edge	/	<i>time_out_en</i>	read status
SPI parity	/	<i>enable_parity</i> <i>conf_0_r[11] = '1'</i>	/	/	<i>enable_parity</i>	read status
SPI checksum	/	<i>enable_checksum</i> <i>conf_0_r[4] = '1'</i>	/	/	<i>enable_checksum</i>	read status
Wrong state	/	always enabled	If a not allowed state code is used a clamp is the resulting output channel. Also check the right states used in CW.	/	always enabled	read status
Channel T fail	<i>en Ana_th</i> <i>conf_1_r[10] = '1'</i>	<i>enable_shutdown_th</i> <i>conf_1_r[1] = '1'</i>	FSM reset, channel outputs are forced to HZ and further TX are blocked.	<i>enable_sys_from_int</i> <i>conf_1_r[0] = '1'</i> enable TX, FSM and channels	always enabled (5us after reset)	read status
Digital T fail	<i>en Ana_th</i> <i>conf_1_r[10] = '1'</i>	<i>enable_sd_logic_t her</i> <i>conf_1_r[7] = '1'</i>	FSM reset, channel outputs are forced to HZ.	<i>enable_sys_from_int</i> <i>conf_1_r[0] = '1'</i> enable FSM and channels	always enabled (5 us after reset)	read status
Digital V fail	<i>en Ana_uv_1v8</i> <i>conf_1_r[9] = '1'</i>	<i>enable_underv</i> <i>conf_1_r[6] = '1'</i>	FSM reset, channel outputs are forced to HZ and further TX are blocked.	<i>enable_sys_from_int</i> <i>conf_1_r[0] = '1'</i> enable TX, FSM and channels	always enabled (5 us after reset)	read status
Analog V fail	<i>en Ana_uv_all_v</i> <i>conf_1_r[11] = '1'</i> <i>en Ana_wrg_hv</i> <i>conf_1_r[12] = '1'</i>	<i>enable_voltage_c heck</i> <i>conf_1_r[8] = '1'</i>	Only checked on trigger rising edge, if analog voltage are not the expected one, stop current TX and blocks further TX.	<i>enable_sys_from_int</i> <i>conf_1_r[0] = '1'</i> enable TX	always enabled (on rising trigger)	read status

If an interrupt state is generated, the external system can be advised in two ways: the INT signal and the data stored in the status register.

- When the following checks fail, the interrupt pad (INT) goes low:
 - **parity**: parity data frame fails.
 - **wrong_state**: check for non existing states stored in memory or wrong CW states
 - **checksum**: checksum SPI communication fails
 - **porlv_rhvm0**: undervoltage of reference bias for half bridge 0 low-side
 - **porlv_rhvm1**: undervoltage of reference bias for half bridge 1 low-side
 - **porlv_rhvp0**: undervoltage of reference bias for half bridge 0 high-side
 - **porlv_rhvp1**: undervoltage of reference bias for half bridge 1 high-side
 - **wrong_hvm0**: wrong high negative voltage on half bridge 0 (warning if HVM0>HVM1)
 - **wrong_hvp0**: wrong high positive voltage on half bridge 0 (warning if HVP0<HVP1)
 - **por_vddp3v3**: undervoltage of VDDP3V3 (+3.3 V)
 - **por_vddm3v3**: undervoltage of VDDM3V3 (-3.3 V)
 - **ther_logic_fail**: thermal fail of the logic circuitry
 - **interrupt_underv**: undervoltage of the digital power supply DVDD (1.8 V)
 - **time_out_interrupt**: time out fail in transmission
 - **analog_thermal_interrupt**: thermal fail on channels

In case of multi-device board, we there can be two scenarios:

- By default, a dedicated path is connected to this pad and driven in CMOS mode.
- Several devices have this pad connected to the same path and share the interrupt advice. In this case, setting bit 9 of the lvds_set_r register int_opdrain to 1, the pad goes into open drain mode.

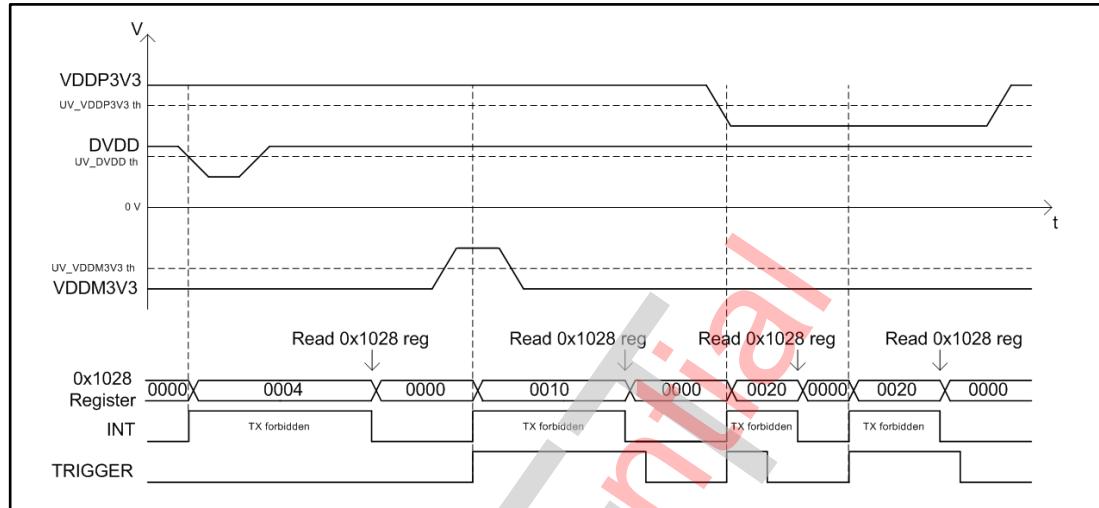
The status read register status_1r provides the following information:

Table 24: Status register description

Name	Bit	Advice interrupt	Reset
parity	14	parity fails	Read reg
wrong_state	13	wrong state programmed	Read reg
checksum	12	checksum fails	Read reg
porlv_rhvm0	11	hvm0 under voltage	Read reg
porlv_rhvm1	10	hvm0 under voltage	Read reg
porlv_rhvp0	9	hvm0 under voltage	Read reg
porlv_rhvp1	8	hvm0 under voltage	Read reg
wrong_hvm0	7	hvm0 V wrong value	Read reg
wrong_hvp0	6	hvp0 V wrong value	Read reg
por_vddp3v3	5	under voltage 3.3V	Read reg
por_vddm3v3	4	under voltage -3.3V	Read reg
ther_logic_fail	3	thermal logic check fails	Read reg
interrupt_underv	2	undervoltage 1.8 logic	Read reg
time_out_interrupt	1	TX timeout fails	Read reg
analog_thermal_interrupt	0	thermal analog check fails	Read reg

To better understand how the STHV1600 responds, in terms of interrupt events and code written in the STATUS register, the following waveform graph provides an example with different supply variation cases (VDDP3V3, VDDM3V3 and DVDD).

Figure 38: Interrupt event vs. supply variation



13**Output phase noise measurement in CW mode****Typical performance characteristics**

Unless otherwise stated, the following conditions apply:

$VDDP = +3.3 \text{ V}$, $VDDM = -3.3 \text{ V}$, $DVDD = +1.8 \text{ V}$, $HVP = +5 \text{ V}$, $HVM = -5 \text{ V}$, NO Load, $F_{in} = 5 \text{ MHz}$, $T_A = 25^\circ \text{C}$.

Figure 39: Measurement setup – CK1=640 MHz; CK2=5 MHz

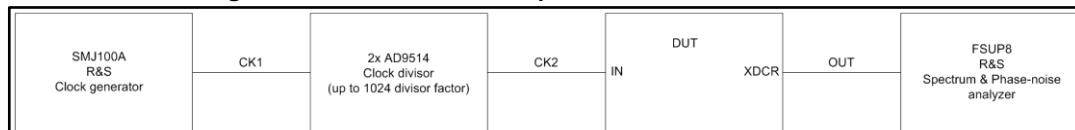
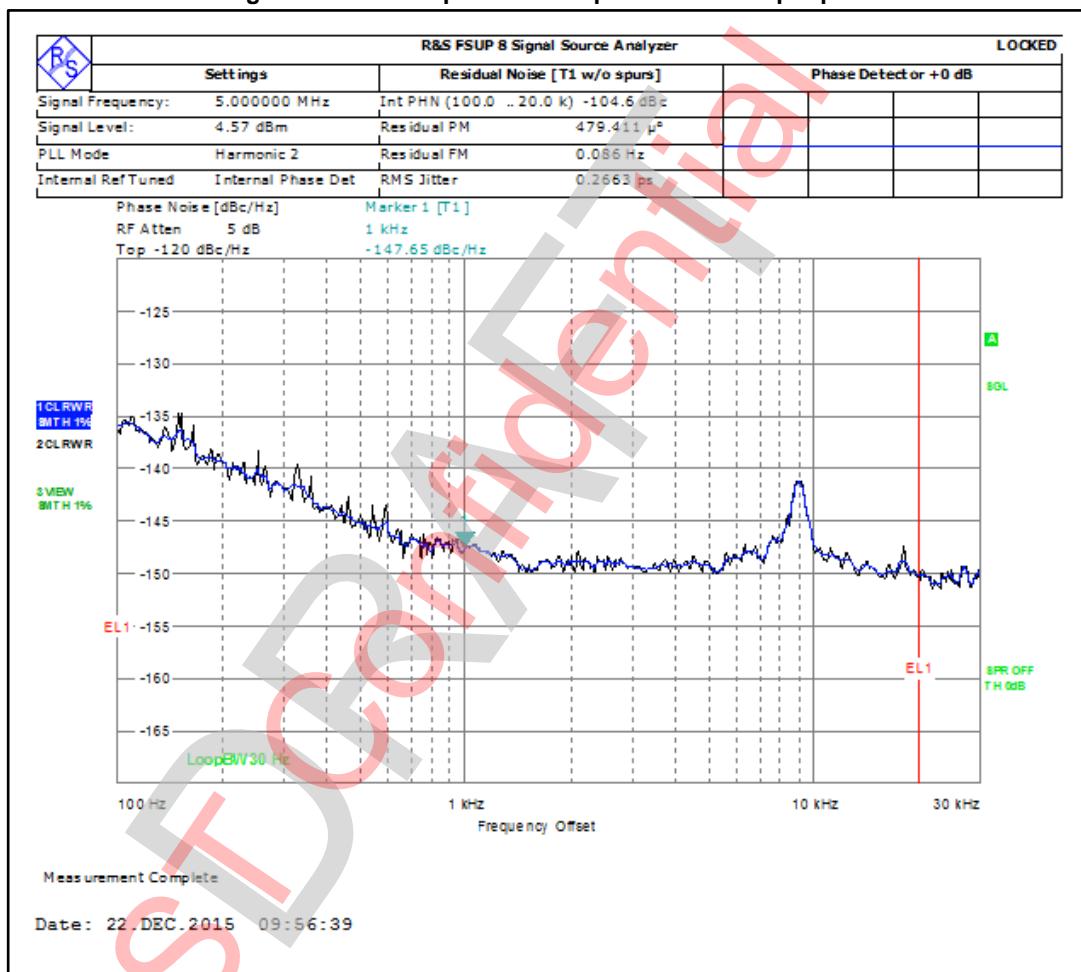


Figure 40: FSUP8 spectrum and phase noise output plot



Significant results from the output have been extracted (*):

- Phase noise: -147 dBc/Hz @ 1 kHz
- RMS jitter [BW 100 Hz – 20 kHz]: 270 fs
- Phase noise (with 2 channels running simultaneously): -147 dBc/Hz @ 1 kHz
- RMS jitter (with 2 channels running simultaneously) [BW 100 Hz – 20 kHz]: 270 fs
- Phase noise (with 4 channels running simultaneously): -145 dBc/Hz @ 1 kHz
- RMS jitter (with 4 channels running simultaneously) [BW 100 Hz – 20 kHz]: 330 fs

(*) Values measured leave room for improvement; as such, they are affected by a non-optimized setup.

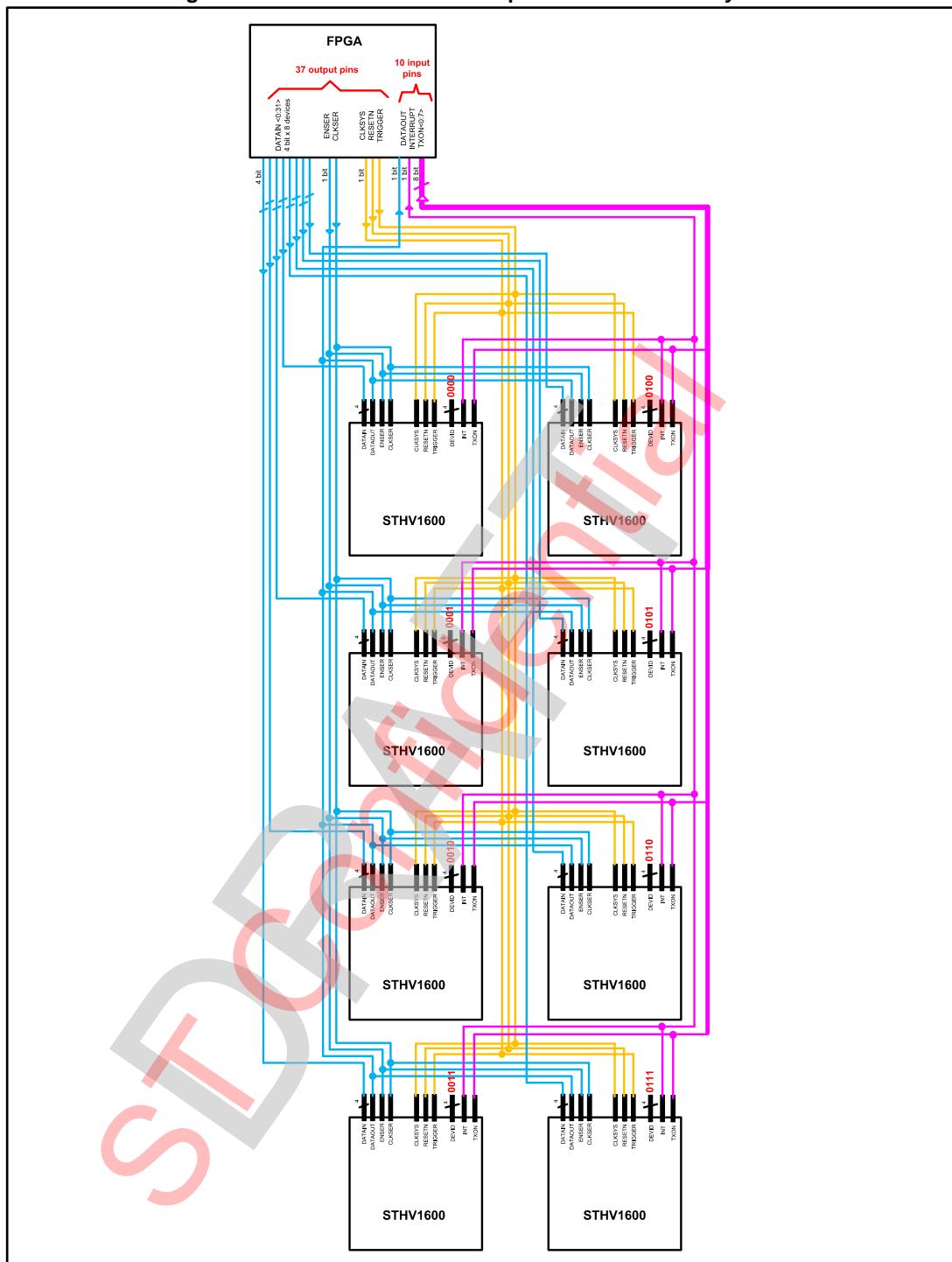
14 **Multiple device management**

Up to 16 devices can be uniquely addressed using DEVID<3:1> input balls to save lines on the system and IO ports of the FPGA controller. In this way the writing time increases, but very few lines are required to drive the whole system.

An individual control example of a 128 channel system is shown in the figure below. This configuration allows maximization of the sample rate. Each device has 4 dedicated data in lines and all other signals can be shared. Only one trigger signal is enough to synchronize all 128 channels according to the stored delay matrix. Both system and serial clock can be shared demanding to the application board an appropriate and robust clock tree. Interrupt and data out can be shared. Data out is managed by the internal logic as a buffer tri-state, which means that it is high impedance in default state and can be shared among different devices without additional external components. The system must address each device by its DEVID and the single STHV1600 can communicate to the system activating its data out pin.

TX_ON is a feedback signal of each device in order to control its working activity. In this scenario, the FPGA needs 37 outputs and 10 inputs to drive 128 channels.

Figure 41: Individual control example of a 128 channel system

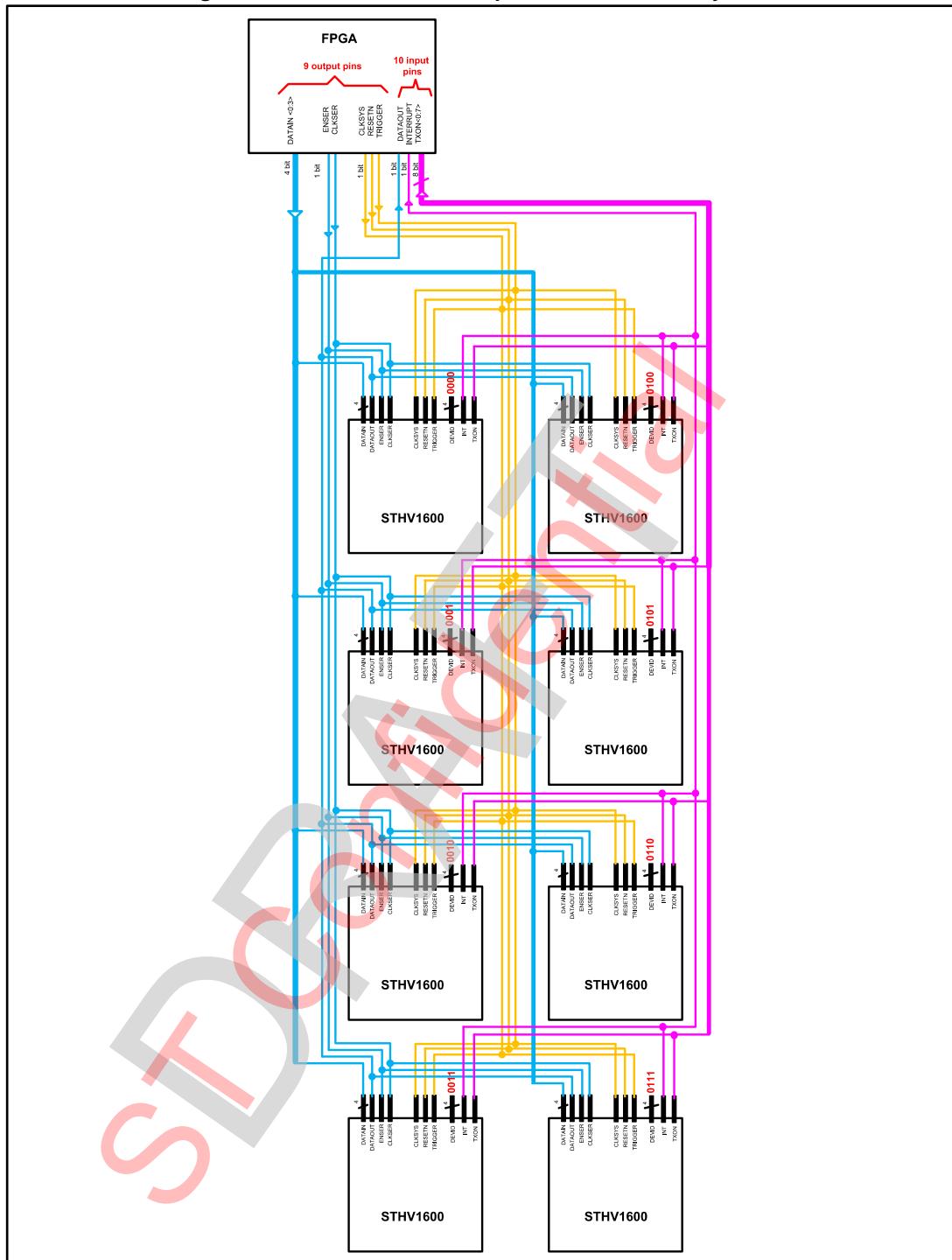


The figure below shows a shared control example of a 128 channels system. This configuration allows minimization of the routing, but the configuration time increases. The main difference is that the data in lines are shared among all devices. In this scenario, the FPGA needs only 9 outputs and 10 inputs to drive all 128 channels.

Multiple device management

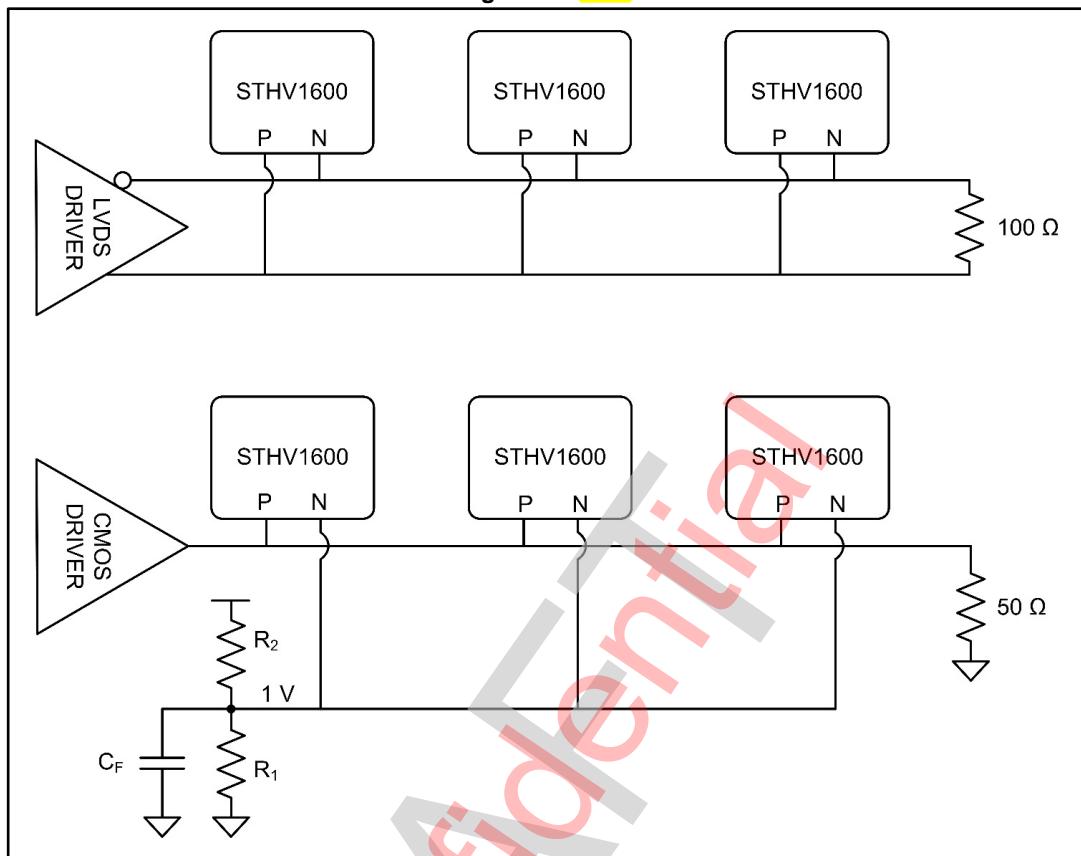
STHV1600

Figure 42: Shared control example of a 128 channel system



Sharing a line among different devices is mandatory to ensure good signal integrity at the input pin of all devices. The intrinsic parasitic of each pin as well as external contributions due to the PCB routing must be taken into consideration. Both CMOS and LVDS protocols can be shared, as shown in the diagram below. LVDS configuration ensures a more robust signal integrity at high frequency, especially if the signal paths are very long. A CMOS interface can be used for low frequency signals (up to 100 MHz) or in small PCB routing (ultraportable systems).

Figure 43: TBD



15 Maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

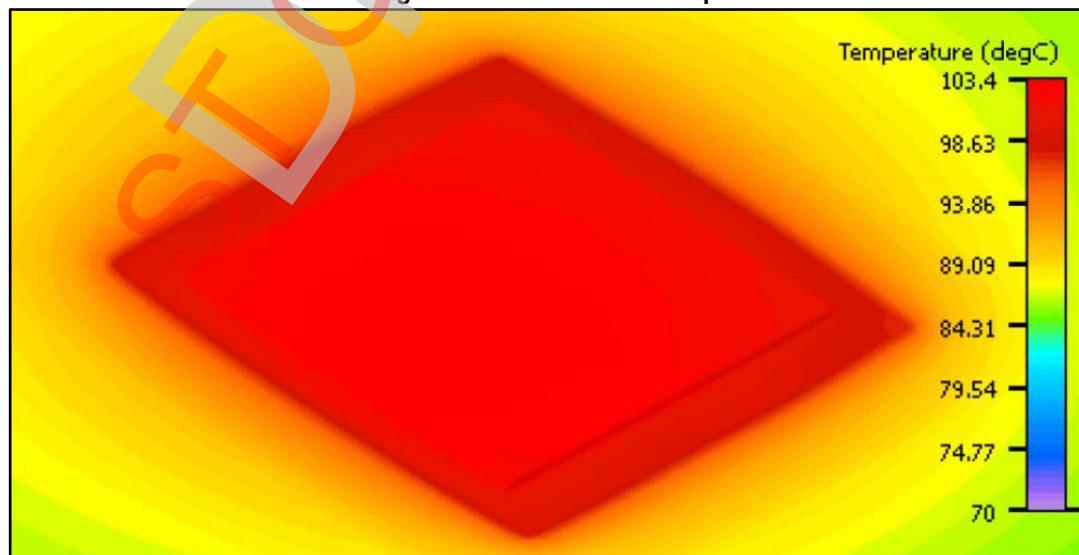
Table 25: Absolute maximum ratings

Symbol	Parameter	Value	Unit
GND	Analog ground reference	-300 to 300	mV
DGND	Digital ground	0	mV
IOGND	IO ground	-300 to 300	mV
VDDP3V3	Positive supply voltage	-0.3 to 3.9	V
VDDM3V3	Negative supply voltage	0.3 to -3.9	V
DVDD	Positive logic voltage	-0.3 to 2	V
HVP0	TX0 high-voltage positive supply	110	V
HVP1	TX1 high-voltage positive supply	110	V
HVM0	TX0 high-voltage negative supply	110	V
HVM1	TX1 high-voltage negative supply	110	V
XDCR	High-voltage output	HVM0 to HVP0	V
LVOUT	Low-voltage output	-1.6 to 1.6	V
T _{OPJ}	Operating junction temperature range	-40 to 125	°C
T _{STG}	Storage temperature range	-65 to 150	°C

Table 26: Thermal data

Symbol	Parameter	Value	Unit
R _{THJA}	Junction-to-ambient thermal resistance	16.7	°C/W

Figure 44: 3D die thermal map



STHV1600

Maximum ratings

Thermal simulation boundary condition: 6-layer board (35 μm metal thickness and 70% Cu coverage). 61 staggered through vias on the bottom of the package (300 μm diameter). The value obtained can be decreased using more vias or in-line with balls. Natural convection, $T_{\text{amb}} = 70^\circ\text{C}$ and $P_{\text{diss}} = 2\text{ W}$ in static condition evenly distributed on the chip (i.e. CW application).

ST Confidential

16 Operating supply voltages and maximum average currents

Operating conditions, unless otherwise specified: XDCR load 300 pF/100 Ω , HVP0 = 100 V, HVP1 = 100 V, HVM0 = -100 V, HVM1 = -100 V, VDDP3V3 = 3.3 V, VDDM3V3 = -3.3 V, DVDD=IOVDD= 1.8 V, T = 25 °C, all channel active, f_CLKSYS = 100 MHz, CMOS interface.

Table 27: Supply voltages

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDDP3V3	Positive supply voltage		2.7	3.3	3.5	V
I _{VDDP3V3}	Positive supply current	CW mode ⁽¹⁾			45	mA
		PW mode ⁽²⁾		7.5		
VDDM3V3	Negative supply voltage		-2.7	-3.3	-3.5	V
I _{VDDM3V3}	Negative supply current	CW mode ⁽¹⁾			95	mA
		PW mode ⁽²⁾		8		
DVDD	Positive logic voltage		1.71	1.8	1.89	V
I _{DVDD}	Logic supply current	CW & PW mode			30	mA
IOVDD	IO positive supply		1.55		3.3	V
I _{IOVDD}	IO supply current				5	mA
HVP0	High-voltage positive supply		1		100	V
I _{HVP0}	HV positive supply current	PW mode ⁽²⁾			24	mA
HVP1	High-voltage positive supply		1		100	V
I _{HVP1}	HV positive supply current	CW mode			390	mA
HVM0	High-voltage negative supply		-100		-1	V
I _{HVM0}	HV negative supply current	PW mode			21	mA
HVM1	High-voltage negative supply		-100		-1	V
I _{HVM1}	HV negative supply current	CW mode			330	mA
T _A	Operating ambient temperature range	0 to 80				

Notes:

⁽¹⁾In CW (continuous wave mode) the average current is measured on one period. The values include the power consumption on the load and are useful to size the system power supply. HVM1 is set to ±5 V, which means about 8 Vpp on XDCR, and an output signal frequency of 5 MHz.

⁽²⁾In PW (pulse wave mode) the average current is measured over a 5 pulse waveform, single-state duration of 100 ns and repetition time of 300 us. These values include the power dissipation on the XDCR loads.

17 Outputs

Table 28: Output signals

Symbol	Parameter	Min.	Max.	Units
XDCR	High-voltage output	-100	100	V
LVOUT	Low-voltage output (-40 dB HD2)	-1.3	1.3	V
DATA_OUT	Digital output		IOVDD	V
TX_ON	Digital output		IOVDD	V

ST Confidential

18 Electrical characteristics

Operating conditions, unless otherwise specified: HVP0 = 60 V, HVP1 = 60 V, HVM0 = -60 V, HVM1 = -60 V, VDDP3V3= 3.3 V, VDDM3V3 = -3.3 V, T = 25 °C, DVDD=IOVDD= 1.8 V, f_CLKSYS = 100 MHz, CMOS interface.

Table 29: Static electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{P0}	Saturation current pull up TX0		1.7	2		A
I _{N0}	Saturation current pull down TX0		1.7	2		A
I _{P1}	Saturation current pull up TX1		1.7	2		A
I _{N1}	Saturation current pull down TX1		1.7	2		A
R _{highside}	Pull up TX0 or TX1 resistance	I = 50 mA		7.5		Ω
R _{lowside}	Pull down TX0 or TX1 resistance	I = 50 mA		6		Ω
R _{highside01}	Pull up TX0 and TX1 resistance	I = 50 mA		3.7		Ω
R _{lowside01}	Pull down TX0 and TX1 resistance	I = 50 mA		3		Ω
I _{CL}	Clamp saturation current			2		A
I _L	Output leakage current	HVP = 100 V, HVM = -100 V			1	μA
P _{RX}	Total power dissipation	All channel in RX state, HV=±10 V			40	mW
T _{OTP}	Overtemperature threshold	HVP =10 V, HVM = -10 V	130	153	160	°C
T _{HYS}	OTP hysteresis	HVP =10 V, HVM = -10 V		40		°C
R _{ON}	T/R SW on resistance (S4)	XDCR=0, LVOUT=0.1 V		9	12	Ω
R _{OFF}	T/R SW off resistance (S4)				100	MΩ
C _{T/R SW}	T/R SW capacitance			28		pF
C _{LVOUT}	Parasitic capacitance on LVOUT when the switch is open			5		pF

Table 30: AC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
f_{XDCR}	XDCR output frequency	PW mode, 5 pulses, no load, TX0, TX1 or both		50		MHz
		PW mode, 5 pulses load 300 pF//100 Ω 15 16 TX0 or TX1	15	16		
		PW mode, 5 pulses load 300 pF//100 Ω 32 TX0 and TX1		32		
f_{CK}	System clock frequency		10		200	MHz
T_{j-CW}	CW output jitter	HVP1=5V, HVM1=-5V, continuous wave mode		270		fs rms
SR	Slew rate fall and rise edge	Load 300 pF//100 Ω		6		V/ns
		No load		35		
t_d	Propagation delay from rise trigger edge and waveform on XDCR start			10 * Tclk + 6		ns
$t_{T/R\ SW}$	T/R SW turn-on / turn-off time			100		ns
$T_{Cl_before\ rx}$	Min clamp time before RX starts			300		ns
HD2	2nd harmonic distortion	1 period; $f = 5\text{MHz}$		-45		dBc
		5 periods; $f = 5\text{MHz}$		-55		dBc
HD2PC	Pulse cancellation	$f = 5\text{MHz}$ original and inverted pulse		-45		dBc
PD_CW	Power dissipation, x channel	CW mode, $f = 5\text{MHz}$, no load		150		mW
T/R SWSPIKE	T/R SW spike on LVOUT			100		mVpp
XTALK1	Cross talk between XDCR and XDCR	$V(f_c)_{CH1} / V(f_c)_{CH2}$		-70		dB
XTALK2	Cross talk between XDCR and LVOUT	$V(f_c)_{CH1} / V(f_c)_{CH2}$		TBD		dB
XTALK3	Cross talk between LVOUT and LVOUT	$V(f_c)_{CH1} / V(f_c)_{CH2}$		TBD		dB

19 Register map

Configuration registers are addressed by a 13-bit value. As the convention used for this document, the registers and bus definition is from MSB to LSB with the annotation [MSB:LSB].

In the following table, NOT_USED means a bit that physically does not exist and if it is read, a 0 is returned. RESERVED means that the bit physically exists and if written the device behavior can differ from the expected behavior. So RESERVED bits must be set with the default value.

Table 31: Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
delaynp_set_r ADD: 0x1000 TYPE: RW	15	0	ana_delayp1[3:0]	Increase the delay of rising transitions of TX1. Defines with resolution of 0.1ns the rising transition delay of TX1, according to the following formula: $n \times 0.1\text{ns}$ where $0 \leq n \leq 15$
	14	0		
	13	0		
	12	0		
	11	0	ana_delayn1[3:0]	Increase the delay of falling transitions of TX1. Defines with resolution of 0.1ns the falling transition delay of TX1, according to the following formula: $n \times 0.1\text{ns}$ where $0 \leq n \leq 15$
	10	0		
	9	0		
	8	0		
	7	0	ana_delayp0[3:0]	Increase the delay of rising transitions of TX0. Defines with resolution of 0.1ns the rising transition delay of TX0, according to the following formula: $n \times 0.1\text{ns}$ where $0 \leq n \leq 15$
	6	0		
	5	0		
	4	0		
	3	0	ana_delayn0[3:0]	Increase the delay of falling transitions of TX0. Defines with resolution of 0.1ns the falling transition delay of TX0, according to the following formula: $n \times 0.1\text{ns}$ where $0 \leq n \leq 15$
	2	0		
	1	0		
	0	0		
delayclp_set_r ADD: 0x1001 TYPE: RW	15	0	internal_sample_edge	'0': Data will be internally sampled by rising edge of CLKSYS '1': Data will be internally sampled by falling edge of CLKSYS
	14	0	RESERVED	/
	13	0	trigger_masked_by_TXON	'0': TRIGGER from pad will be used '1': TRIGGER from pad will not be used, it will be masked by TX_ON before use. Use it to filter spikes on TRIGGER in case of noisy environment
	12	0	RESERVED	/
	11	0	RESERVED	/

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
lvds_set_r ADD: 0x1002 TYPE: RW	10	0	RESERVED	/
	9	0	RESERVED	/
	8	0	RESERVED	/
	7	0	ana_delayclpp[3:0]	Increase the delay time of the rising clamp transitions. Each delay is defined with 4 bits and the resolution is 0.1ns
	6	0		
	5	0		
	4	0		
	3	0	ana_delayclpn[3:0]	Increase the delay time of the falling clamp transitions. Each delay is defined with 4 bits and the resolution is 0.1ns
	2	0		
	1	0		
	0	0		
	15	0	NOT_USED	/
	14	0	NOT_USED	/
	13	0	NOT_USED	/
	12	0	NOT_USED	/
	11	0	NOT_USED	/
	10	0	NOT_USED	/
	9	1	int_opdrain	'0': CMOS output mode for INT pin '1': Open drain output mode for INT pin
	8	1	RESERVED	/
	7	0	lvds_data_lowhi	configure the LVDS input buffer for DATA_IN[3:0], ENSER, CLKSER inputs (lvds_data_lowhi and lvds_data_highi) and for CLKSYS and TRIGGER inputs (lvds_clk_lowhi and lvds_clk_highi): <lowhi, highi> = '00' -> lvds+ cmos high current '10' -> only cmos allowed (very low consumption) '01' -> lvds+ cmos medium current '11' -> lvds+ cmos low current
	6	0	lvds_data_highi	
	5	0	lvds_clk_lowhi	
	4	0	lvds_clk_highi	
	3	1	RESERVED	/
	2	1	lvds_hys	'0': Disable hysteresis on LVDS input buffers '1': Enable hysteresis on LVDS input buffers
	1	0	cmos_drv[1:0]	Set CMOS IO driver current: '00' -> minimum current '11' -> maximum current
	0	0		
ref_por_set_r	15	0	NOT USED	/

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
ADD: 0x1003 TYPE: RW	14	0	NOT USED	/
	13	0	NOT USED	/
	12	0	NOT USED	/
	11	0	sel_refhv_lp_val[1:0]	Define the value of HV1 reference voltages (only if ref_por_set_r[3] = '1', p_conf_0_r[9] = '1', ref_por_set_r[5] = '0' ref_por_set_r[7] = '0') '00' -> HV – REFHV = 3.3V '10' -> HV – REFHV = 3V '01' -> HV – REFHV = 2.5V '11' -> HV – REFHV = 2V
	10	0		
	9	0	sel_refhv_val[1:0]	Define the value of all HV reference voltages (both TX0 and TX1) '00' -> HV – REFHV = 3.3V '10' -> HV – REFHV = 3V '01' -> HV – REFHV = 2.5V '11' -> HV – REFHV = 2V
	8	0		
	7	1	en_refhvp1	It works only if p_conf_0_r[9] = '1' : '0': Disable HVP1 reference voltages '1': Enable HVP1 reference voltages
	6	1	en_refhvp0	It works only if p_conf_0_r[9] = '1' : '0': Disable HVP0 reference voltages '1': Enable HVP0 reference voltages
	5	1	en_refhvm1	It works only if p_conf_0_r[9] = '1' : '0': Disable HVM1 reference voltages '1': Enable HVM1 reference voltages
	4	1	en_refhvm0	It works only if p_conf_0_r[9] = '1' : '0': Disable HVM0 reference voltages '1': Enable HVM0 reference voltages
	3	0	en_ref_lowp	Manage only HV1 reference voltages consumption, it works only if p_conf_0_r[9] = '1', ref_por_set_r[5] = '0' ref_por_set_r[7] = '0': '0': Standard consumption '1': Low current consumption (to be used only in CW mode or with low number of channel switching)
	2	1	RESERVED	/
	1	1	RESERVED	/
	0	1	RESERVED	/
p_time_out_r ADD: 0x1004 TYPE: RW	15	0	time_out_en	'0' : disables time out feature '1' : enables time out feature
	14	0	time_out_val[14:0]	Set the time out for transmission operation.

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_wait_rx_r ADD: 0x1005 TYPE: RW	15	0	wait_rx_mode	'1' : channels receive when last channel ends TX '0' : each channel receive after its own delay profile, when RX wait time (<i>p_wait_rx_r</i> [14:0]) ends
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	1		
	2	0		
	1	1		
	0	0		
p_enable_tx_r ADD: 0x1006 TYPE: RW	15	0		
	14	0		
	13	0		
			enable_tx_ch[15:0]	'0': Disable TX for each channel '1': Enable TX for each channel

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_enable_rx_r ADD: 0x1007 TYPE: RW	15	0	enable_rx_ch[15:0]	'0': Disable RX for each channel '1': Enable RX for each channel
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_conf_0_r ADD: 0x1008 TYPE: RW	15	0	NOT_USED	/
	14	0	auto_spi_lvds_en	'0' : Normal mode '1' : Enables automatic management of SPI LVDS input buffer (DATA_IN[3:0], ENSER, CLKSER) power down. If enabled the SPI buffers are switched off during TX and RX operation

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	13	0	rx_start_mode	when CW is disabled, it chooses if the channel in RX mode only start to receive just after trigger pulsing or after the sequence stored is ended
	12	0	start_ram_wrzero	It starts a write sequence of all RAM value data to '0'. It reset all RAM bits to 0
	11	0	enable_parity	'0' : Disable parity check on write operations '1' : Enables parity check on write operations
	10	0	low_power	'0' : Normal mode '1' : put all devices in low_power mode (references OFF, ram OFF, SPI buffers OFF unless TRIGGER and SYSCLK). All can be enabled by a pulse of trigger signal
	9	0	manual_ref_pd_en	'0' : Disable manual control of HV reference voltages '1' : Enable manual control of HV reference voltages. The power-down is managed through ref_por_set_r [7:4] bits
	8	0	auto_ref_pd_en	if p_conf_0_r [9] = '0' '0' : Disable auto management of HV reference power down '1' : Enable auto management of HV reference power down
	7	0	power_down_ram	if p_conf_0_r [6] = 0 : '0' : Disable of RAM power down '1' : Enable of RAM power down
	6	0	auto_ram_pd_en	'0' : Disable auto management of RAM power down '1' : Enable auto management of RAM power down
	5	0	state_inversion	'0' : use stored states without inversion '1' : invert high/low level of memory state content
	4	0	enable_checksum	'0' : Disables checksum in SPI writing operation '1' : Enables checksum in SPI writing operation
	3	0	cw_mode	'0' : Normal mode '1' : Enables CW mode
	2	0	NOT_USED	/
	1	0	write_same_wf_to_all	'0' : Normal mode '1' : all 16 SRAM blocks are written at the same time (with the same content)

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_conf_1_r ADD: 0x1009 TYPE: RW	0	0	ser_trigger_tx	Equivalent trigger generated from SPI
	15	0	NOT_USED	/
	14	0	NOT_USED	/
	13	0	RESERVED	/
	12	1	en_ana_wrg_hv	'0' : Disable check of wrong HV supply – no interrupt event '1' : Enable analog check on analog high voltage relative values – in case of error, interrupt event
	11	1	en_ana_uv_all_v	'0' : Disable check of analog supply values – no interrupt event '1' : Enable analog check on analog supply values (VDDP3V3, VDDM3V3 and all HV ref voltages) – in case of error, interrupt event
	10	1	en_ana_th	'0' : Disable thermal check – no interrupt event '1' : Enable analog check on logic and channels thermal – in case of error, interrupt event
	9	1	en_ana_uv_1v8	'0' : Disable digital voltage check – no interrupt '1' : Enable analog check on DVDD supply value
	8	0	enable_voltage_check	It works only if p_conf_1_r[12]=1 or p_conf_1_r[11]=1 '0' : Disable digital check of analog supply – in case of error only interrupt event '1' : Enable digital check of analog supply voltage (VDDP3V3 and VDDM3V3 and all HV ref voltages) – in case of error, it stop current TX, it blocks further TX and interrupt event
	7	0	enable_sd_logic_ther	It works only if p_conf_1_r[10]=1 '0' : Disable digital check of logic thermal condition – in case of error only interrupt event '1' : Enable digital check of logic thermal condition – in case of error, channels output forced to HZ and interrupt event
	6	0	enable_underv	It works only if p_conf_1_r[9]=1 '0' : Disable digital check of DVDD supply – in case of error, only interrupt event '1' : Enable digital check on DVDD supply – in case of error, it stop current TX, it blocks further TX and interrupt event
	5	0	NOT_USED	/

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	4	0	spi_read_mode	'0': data read from DATA_OUT pin takes 2 CLKSER pulses, where valid data must be sampled on the second clock pulse. '1': DATA_OUT takes 4 CLKSER pulses, where valid data must be sampled on the fourth clock pulse.
	3	0	tx_running_type	'0': TX_ON goes high only during TX operation. '1': TX_ON goes high during TX and WAIT RX operation, it goes low just before the receiving.
	2	0	parity_type	It works if conf_0_r[11]=1 '0': parity interrupt on INT pin goes high until the status register is read (no indication on further parity fails is provided). '1': parity interrupt goes high for one system clock pulse at each parity fail occurrence.
	1	0	enable_shutdown_th	It works only if p_conf_1_r[10]=1 '0' : Disable digital check of channels thermal condition – in case of error only interrupt event '1' : Enable digital check of channels thermal condition – in case of error, channels output forced to HZ and interrupt event
	0	0	enable_sys_from_int	Restore system after an overall system interrupt
p_delay_tab_0_r ADD: 0x100A TYPE: RW	15	0	delay_tab_0b[15:0]	Beamformer transmission delay for channel 0
14	0			
13	0			
12	0			
11	0			
10	0			
9	0			
8	0			
7	0			
6	0			
5	0			
4	0			
3	0			
2	0			
1	0			

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	0	0		
p_delay_tab_1_r ADD: 0x100B TYPE: RW	15	0	delay_tab_1b[15:0]	Beamformer transmission delay for channel 1
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_2_r ADD: 0x100C TYPE: RW	15	0	delay_tab_2b[15:0]	Beamformer transmission delay for channel 2
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_3_r ADD: 0x100D	15	0	delay_tab_3b[15:0]	Beamformer transmission delay for channel 3
	14	0		

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
TYPE: RW	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_4_r ADD: 0x100E TYPE: RW	15	0	delay_tab_4b[15:0]	Beamformer transmission delay for channel 4
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_5_r ADD: 0x100F TYPE: RW	15	0	delay_tab_5b[15:0]	Beamformer transmission delay for channel 5
	14	0		
	13	0		
	12	0		
	11	0		

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_6_r ADD: 0x1010 TYPE: RW	15	0	delay_tab_6b[15:0]	Beamformer transmission delay for channel 6
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_7_r ADD: 0x1011 TYPE: RW	15	0	delay_tab_7b[15:0]	Beamformer transmission delay for channel 7
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_delay_tab_8_r ADD: 0x1012 TYPE: RW	7	0	delay_tab_8b[15:0]	Beamformer transmission delay for channel 8
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
p_delay_tab_9_r ADD: 0x1013 TYPE: RW	7	0	delay_tab_9b[15:0]	Beamformer transmission delay for channel 9
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_delay_tab_10_r ADD: 0x1014 TYPE: RW	4	0	delay_tab_10b[15:0]	Beamformer transmission delay for channel 10
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
p_delay_tab_11_r ADD: 0x1015 TYPE: RW	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
	15	0	delay_tab_11b[15:0]	Beamformer transmission delay for channel 11
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	1	0		
	0	0		
p_delay_tab_12_r ADD: 0x1016 TYPE: RW	15	0	delay_tab_12b[15:0]	Beamformer transmission delay for channel 12
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_13_r ADD: 0x1017 TYPE: RW	15	0	delay_tab_13b[15:0]	Beamformer transmission delay for channel 13
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_14_r	15	0	delay_tab_14b[15:0]	Beamformer transmission delay for

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
ADD: 0x1018 TYPE: RW	14	0		channel 14
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_delay_tab_15_r ADD: 0x1019 TYPE: RW	15	0	delay_tab_15b[15:0]	Beamformer transmission delay for channel 15
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_wf_sel_opt_0_r ADD: 0x101A TYPE: RW	15	0	wf_sel_opt_ch1b[7:0]	8 bit transmission start address memory select the waveform on channel 1
	14	0		
	13	0		
	12	0		

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_wf_sel_opt_1_r ADD: 0x101B TYPE: RW	11	0	wf_sel_opt_ch0b[7:0]	8 bit transmission start address memory select the waveform on channel 0
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
p_wf_sel_opt_2_r ADD: 0x101C TYPE: RW	1	0	wf_sel_opt_ch2b[7:0]	8 bit transmission start address memory select the waveform on channel 2
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
p_wf_sel_opt_5_r ADD: 0x101D TYPE: RW	7	0	wf_sel_opt_ch5b[7:0]	8 bit transmission start address memory select the waveform on channel 5
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_wf_sel_opt_3_r ADD: 0x101D TYPE: RW	8	0	wf_sel_opt_ch4b[7:0]	8 bit transmission start address memory select the waveform on channel 4
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
p_wf_sel_opt_6_r ADD: 0x101D TYPE: RW	14	0	wf_sel_opt_ch7b[7:0]	8 bit transmission start address memory select the waveform on channel 7
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
p_wf_sel_opt_4_r ADD: 0x101E TYPE: RW	4	0	wf_sel_opt_ch6b[7:0]	8 bit transmission start address memory select the waveform on channel 6
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
p_wf_sel_opt_8_r ADD: 0x101E TYPE: RW	10	0	wf_sel_opt_ch9b[7:0]	8 bit transmission start address memory select the waveform on channel 9
	9	0		
	8	0		
	7	0		
	6	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
p_wf_sel_opt_9_r ADD: 0x101E TYPE: RW	10	0	wf_sel_opt_ch8b[7:0]	8 bit transmission start address memory select the waveform on channel 8
	9	0		
	8	0		
	7	0		
	6	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_wf_sel_opt_5_r ADD: 0x101F TYPE: RW	5	0	wf_sel_opt_ch11b[7:0]	8 bit transmission start address memory select the waveform on channel 11
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_wf_sel_opt_6_r ADD: 0x1020 TYPE: RW	15	0	wf_sel_opt_ch13b[7:0]	8 bit transmission start address memory select the waveform on channel 13
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
p_wf_sel_opt_7_r ADD: 0x1021 TYPE: RW	15	0	wf_sel_opt_ch12b[7:0]	8 bit transmission start address memory select the waveform on channel 12
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_wf_sel_opt_7_r ADD: 0x1021 TYPE: RW	2	0	wf_sel_opt_ch15b[7:0]	8 bit transmission start address memory select the waveform on channel 15
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
p_checksum_r ADD: 0x1022 TYPE: RW	3	0	wf_sel_opt_ch14b[7:0]	8 bit transmission start address memory select the waveform on channel 14
	2	0		
	1	0		
	0	0		
	15	0		
	14	0		
	13	0		
	12	0		
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		
Checksum[15:0]				Register must be written with the checksum value, in case check of data written until this point are correct

STHV1600

Register map

Register description ADD=[12:0]	Bit	Default	Bit name	Description
p_status_1_r ADD: 0x1028 TYPE: R	15	0	NOT_USED	/
	14	0	parity_status	'0' : No issue '1': SPI communication parity error
	13	0	wrong_state_status	'0': No issue '1': not existing state is programmed into the state field of memory or CW mode is performed using the wrong bridge (TX0)
	12	0	checksum_status	'0' : No issue '1' : SPI communication checksum error
	11	0	porlv_rhvm0_status	'0' : No issue '1' : HVM0 reference voltage issue
	10	0	porlv_rhvm1_status	'0' : No issue '1' : HVM1 reference voltage issue
	9	0	porlv_rhvp0_status	'0' : No issue '1' : HVP0 reference voltage issue
	8	0	porlv_rhvp1_status	'0' : No issue '1' : HVP1 reference voltage issue
	7	0	wrong_hvm0_status	'0' : No issue '1' : high voltage analog supply issue (HVM1 > HVM0)
	6	0	wrong_hvp0_status	'0' : No issue '1' : high voltage analog supply issue (HVP1>HVP0)
	5	0	por_vddp3v3_status	'0' : No issue '1' : low voltage VDDP3V3 supply issue
	4	0	por_vddm3v3_status	'0' : No issue '1' : low voltage VDDM3V3 supply issue
	3	0	ther_logic_fail_status	'0' : No issue '1' : thermal issue on logic
	2	0	interrupt_underv_status	'0' : No issue '1' : digital DVDD supply issue
	1	0	time_out_interrupt_status	'0' : No issue '1' : time-out issue. Transmission time duration is greater than the time set
	0	0	analog_thermal_interrupt_status	'0' : No issue '1' : thermal issue on channels
th_ch_fail_num_r ADD: 0x1029 TYPE: R	15	0	th_ch_fail_num_r[15:0]	These bits define which channel has been put in HZ for thermal issue.
	14	0		
	13	0		
	12	0		

Register map

STHV1600

Register description ADD=[12:0]	Bit	Default	Bit name	Description
	11	0		
	10	0		
	9	0		
	8	0		
	7	0		
	6	0		
	5	0		
	4	0		
	3	0		
	2	0		
	1	0		
	0	0		

ST Confidential

20 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

20.1 LFBGA 10x10x1.4 package information

Figure 45: LFBGA 10x10x1.4 package outline

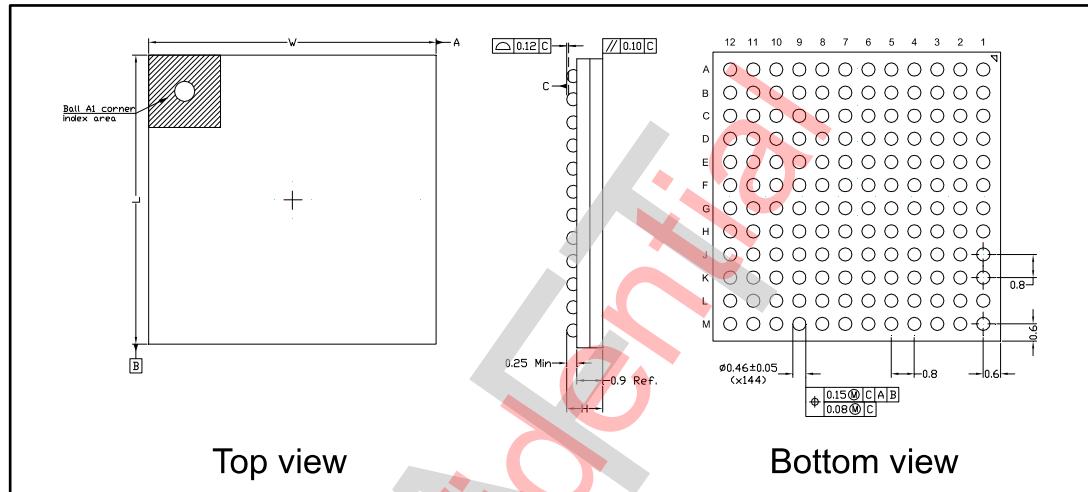


Table 32: LFBGA 10x10x1.4 mechanical data

Symbol	Dimensions ⁽¹⁾	Tolerance ⁽²⁾
L	10.00	± 0.1
W	10.00	± 0.1
H	1.0	Max

Notes:

⁽¹⁾Dimensions are in millimeters unless otherwise specified.

⁽²⁾General tolerance is ±0.1 mm unless otherwise specified.

20.2 LFBGA 10x10x1.4 packaging information

Note: All dimensions are in millimeters unless otherwise specified.

Figure 46: LFBGA 10x10x1.4 packaging dimensions (1 of 3)

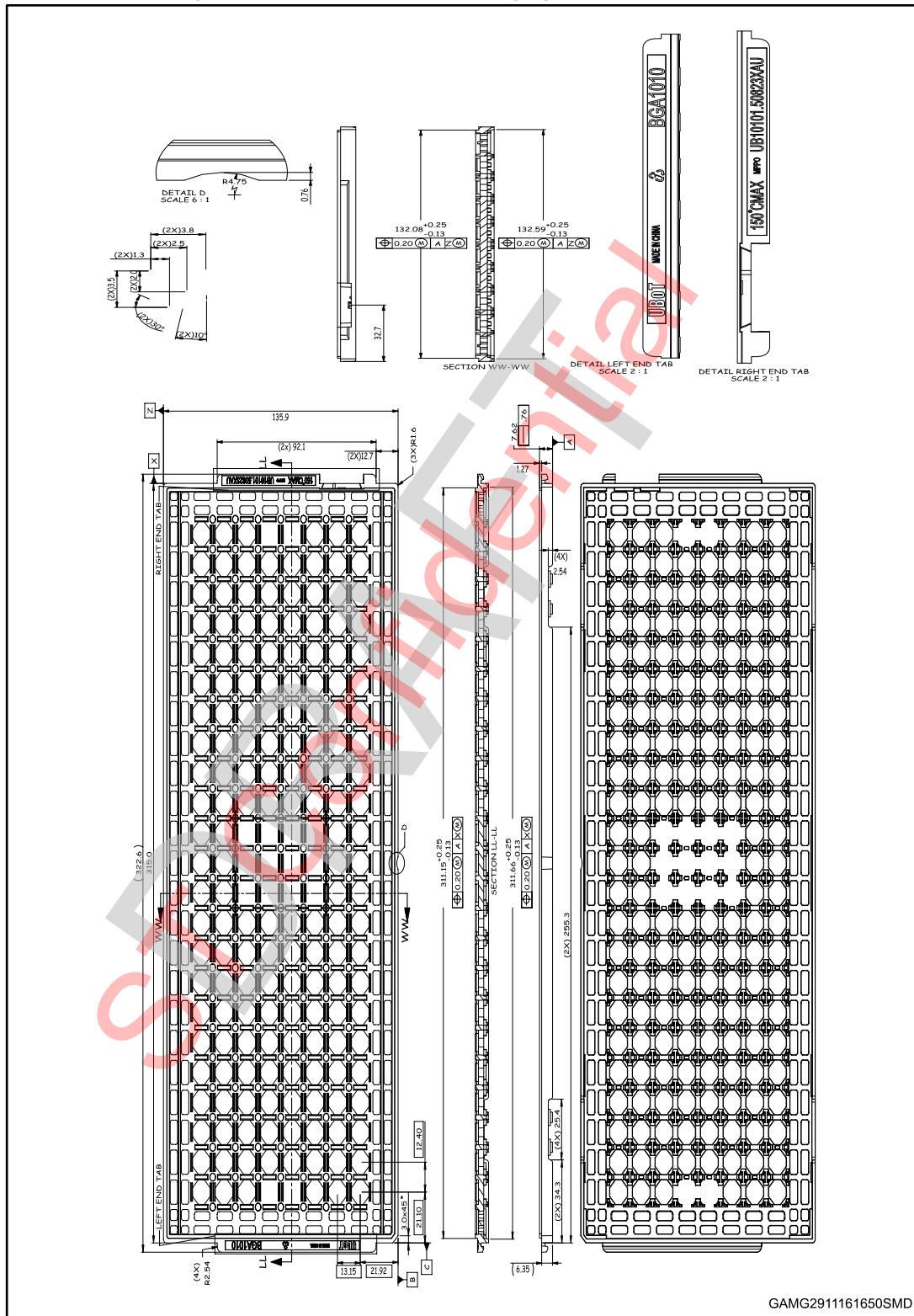
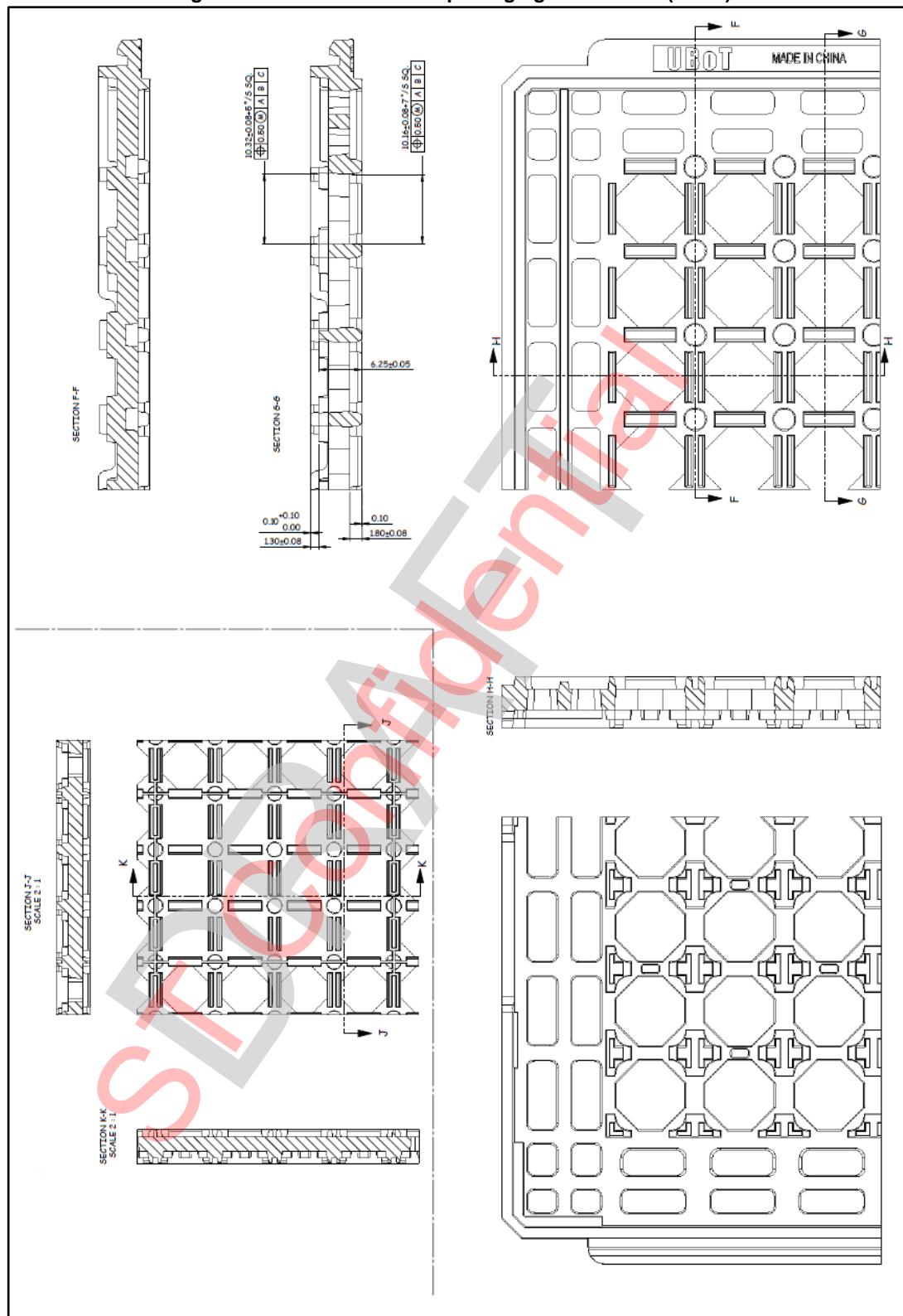


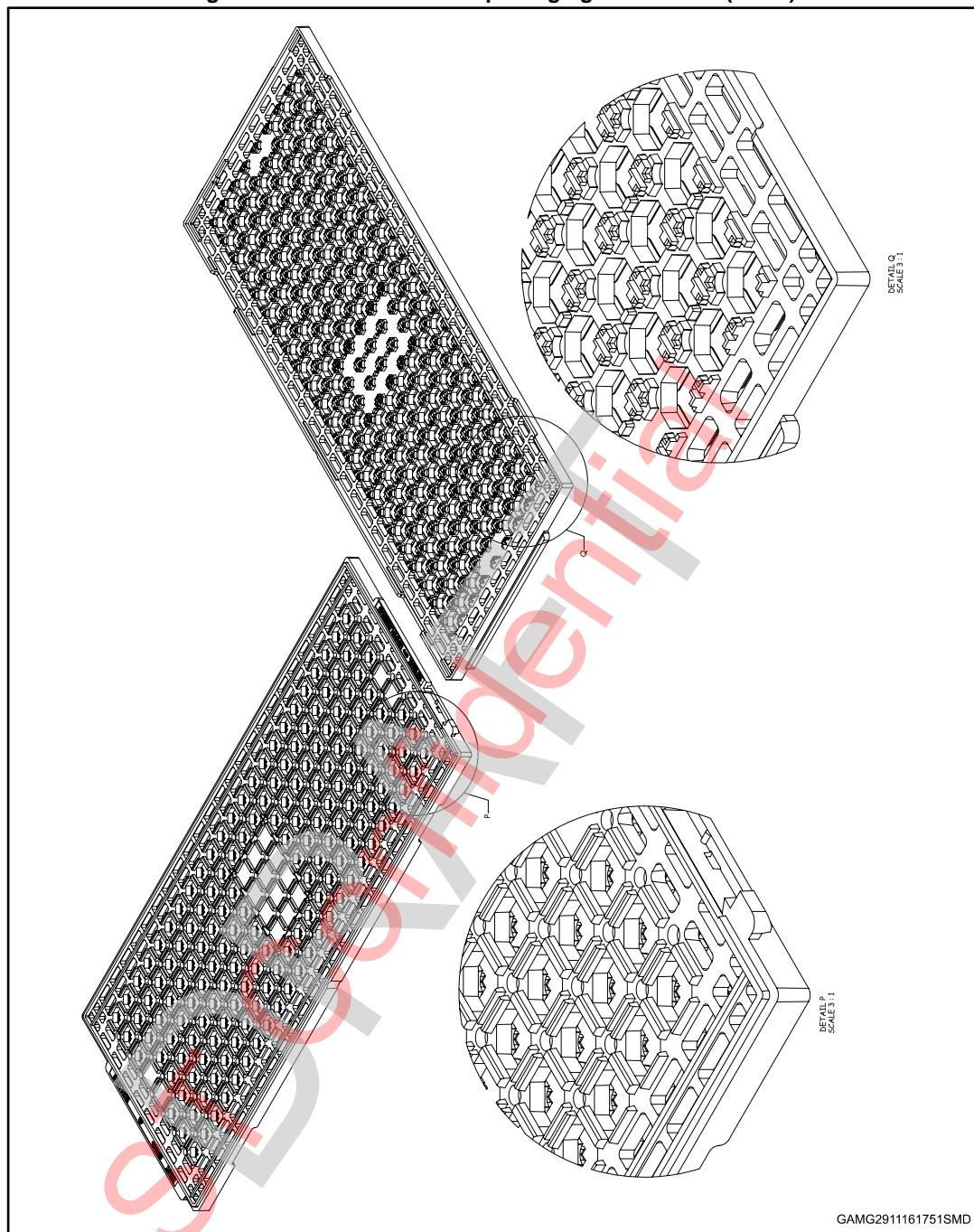
Figure 47: LFBGA 10x10x1.4 packaging dimensions (2 of 3)



Package information

STHV1600

Figure 48: LFBGA 10x10x1.4 packaging dimensions (3 of 3)



21 Revision history

Table 33: Document revision history

Date	Version	Changes
07-Jul-2017	1	Initial release.

ST Confidential

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved