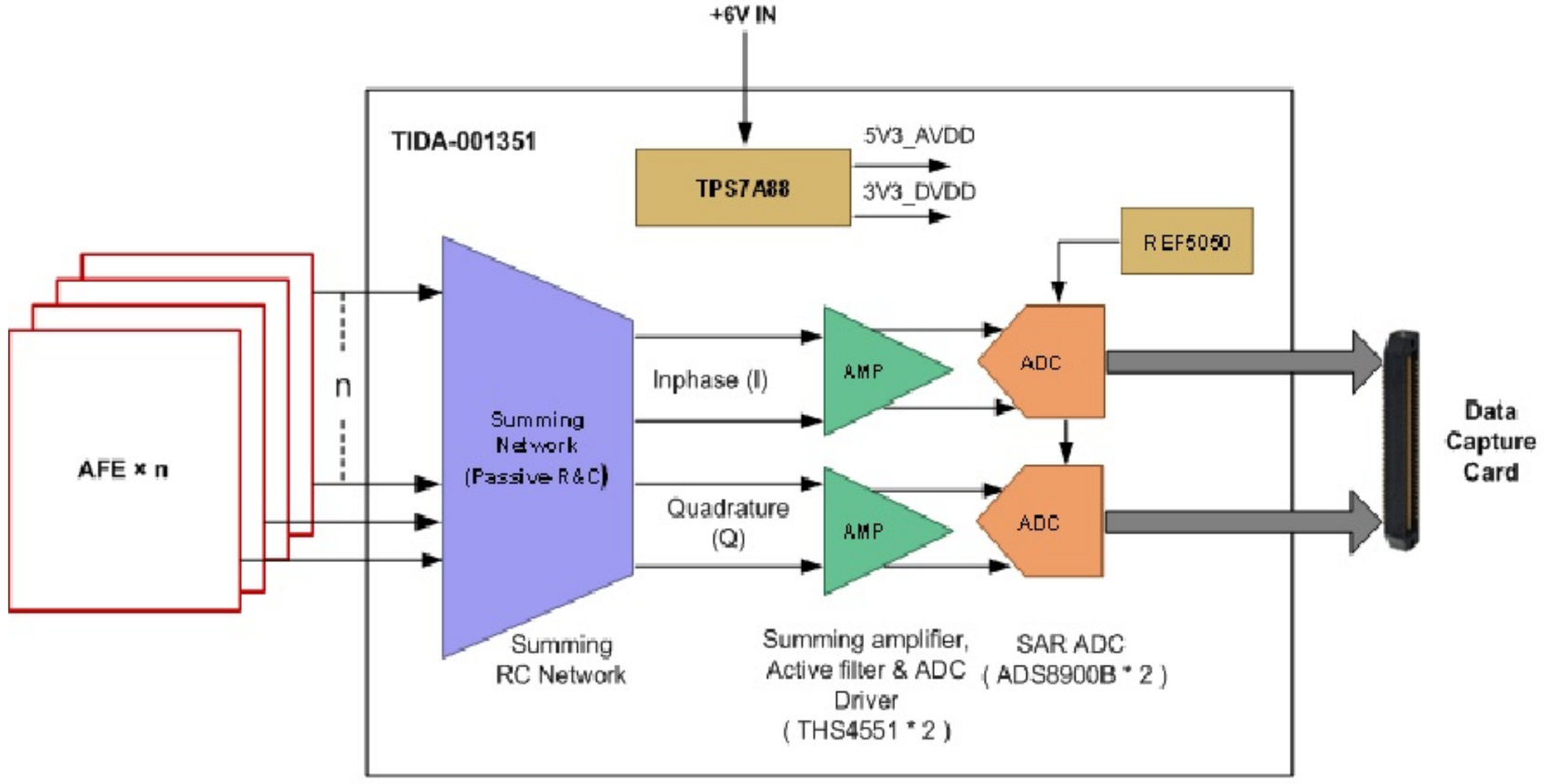
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



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Orderable: N/A		Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351		Project Title: CW Signal Conditioning	
Number: TIDA-01351	Rev: E1	Sheet Title: Block Diagram	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 7
Drawn By: Sanjay Pithadia		File: TIDA-01351_Block_Diagram.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	

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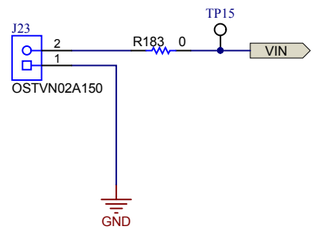
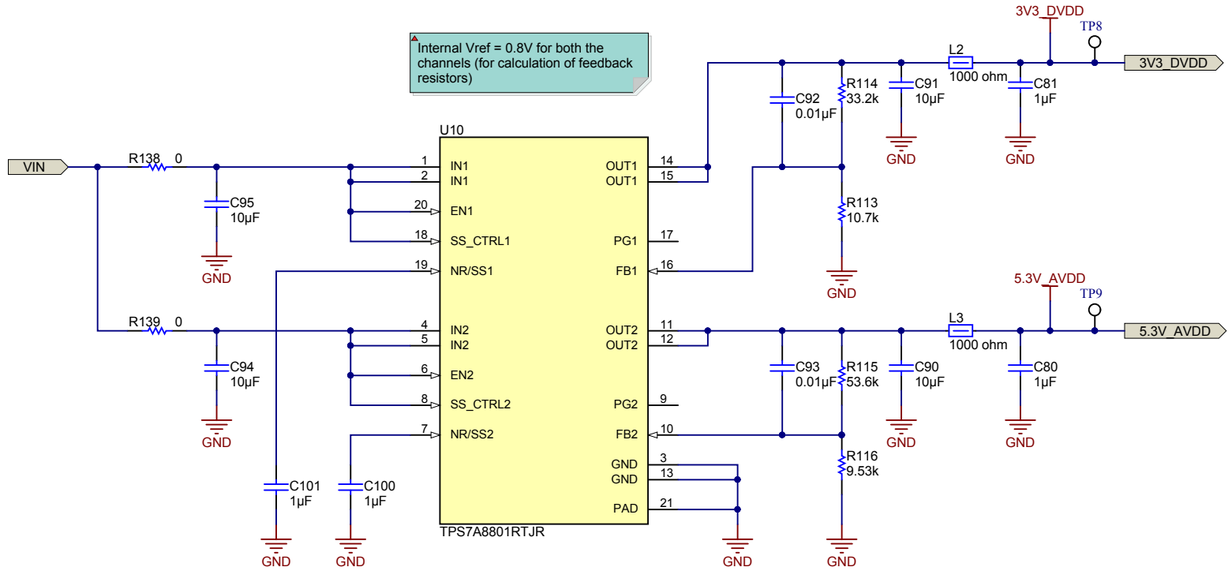
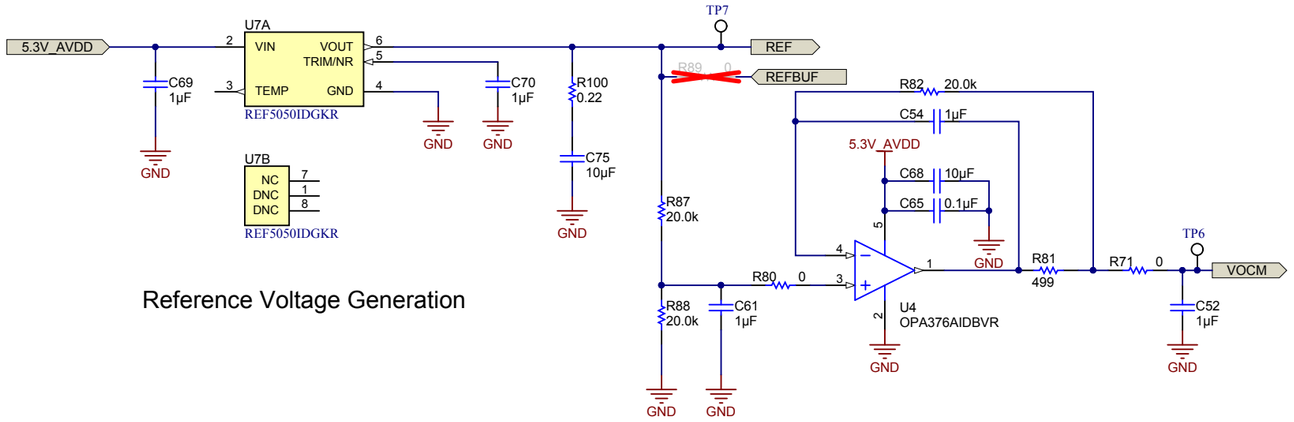


Input Connector

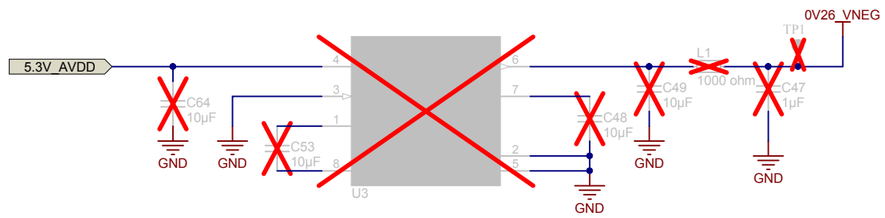


3.3V DVDD and 5.3V AVDD Generation



Reference Voltage Generation

CM Voltage Generation



Negative Bias Generation

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Orderable: N/A	Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: Power-Ref-Generation	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351-Power-Ref-Generation.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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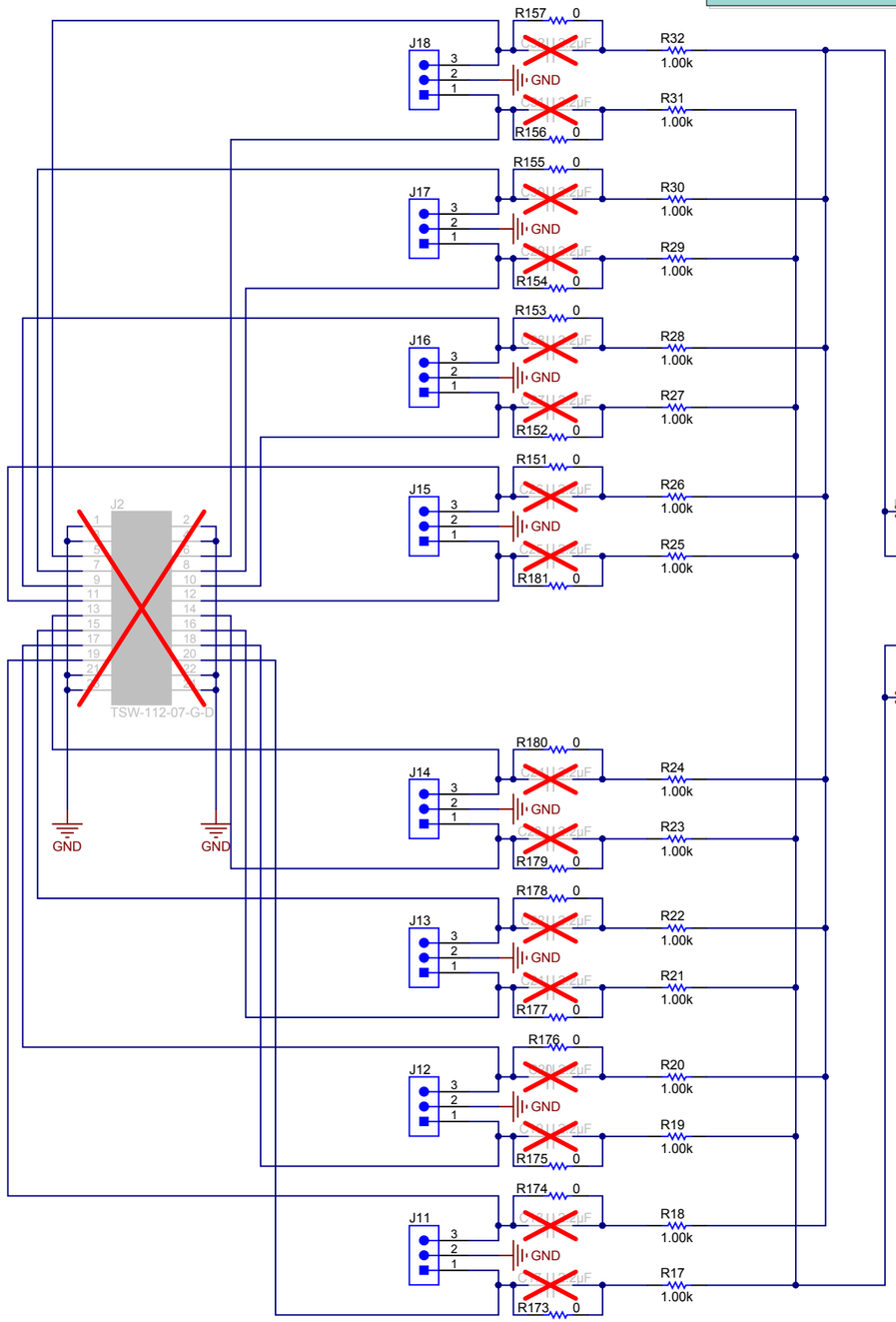
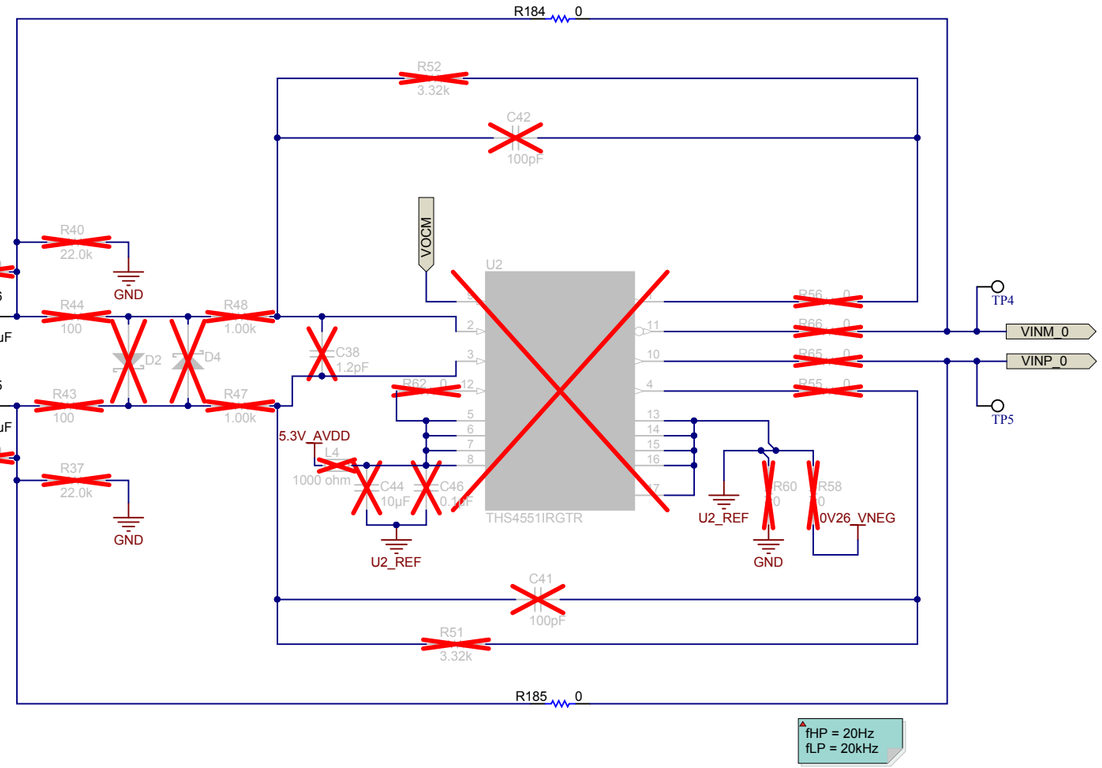
Series capacitors are for DC Blocking.
If the AFE has inbuilt DC Blocking caps, open the external DC blocking cap and place the zero ohms resistors in parallel.





fHP = 20Hz
fLP = 20kHz

Bandpass Filter for I-Channel

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Orderable: N/A	Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: Filter and Summing (I-ch)	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351_Filter_Summing-I.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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Series capacitors are for DC Blocking.
If the AFE has inbuilt DC Blocking caps, open the external DC blocking cap and place the zero ohms resistors in parallel.

J1 TSW-112-07-G-D

R172 0 — R16 1.00k — J10 — R171 0 — R15 1.00k
R170 0 — R14 1.00k — J9 — R169 0 — R13 1.00k
R168 0 — R12 1.00k — J8 — R167 0 — R11 1.00k
R166 0 — R10 1.00k — J7 — R165 0 — R9 1.00k
R164 0 — R8 1.00k — J6 — R163 0 — R7 1.00k
R162 0 — R6 1.00k — J5 — R182 0 — R5 1.00k
R161 0 — R4 1.00k — J4 — R160 0 — R3 1.00k
R159 0 — R2 1.00k — J3 — R158 0 — R1 1.00k

GND

R186 0

R50 3.32k

C40 100pF

R35 0 — R36 22.0k — GND

C34 3.3µF — R42 100 — R46 1.00k — D1 — D3

C33 3.3µF — R41 100 — R45 1.00k — R34 0

R33 22.0k — GND

VOCM

U1 THS4551IRGTR

C37 1.2pF

R61 0

5.3V_AVDD — L5 1000 ohm — C43 10µF — C45 0.1µF — U1_REF

R54 0 — R64 0 — R63 0 — R53 0 — TP2 VINM_1 — VINP_1 — TP3

R59 0 — R57 0 — U1_REF — GND — 0V26_VNEG

C39 100pF

R49 3.32k

R187 0

fHP = 20Hz
fLP = 20kHz

Bandpass Filter for Q-Channel

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Orderable: N/A	Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: Filter and Summing (I-ch)	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351_Filter_Summing-Q.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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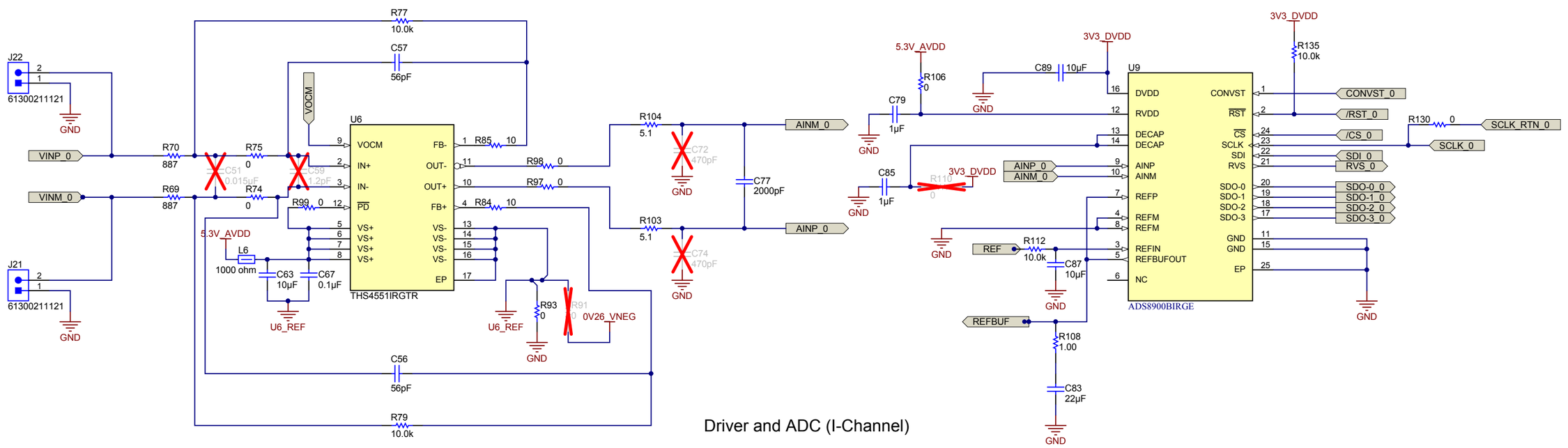

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Preliminary Version. Not Tested. Subject to change without notice.

Orderable: N/A	Designed for: Public Release	Mod. Date: 12/16/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: ADC	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 5 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351_ADC.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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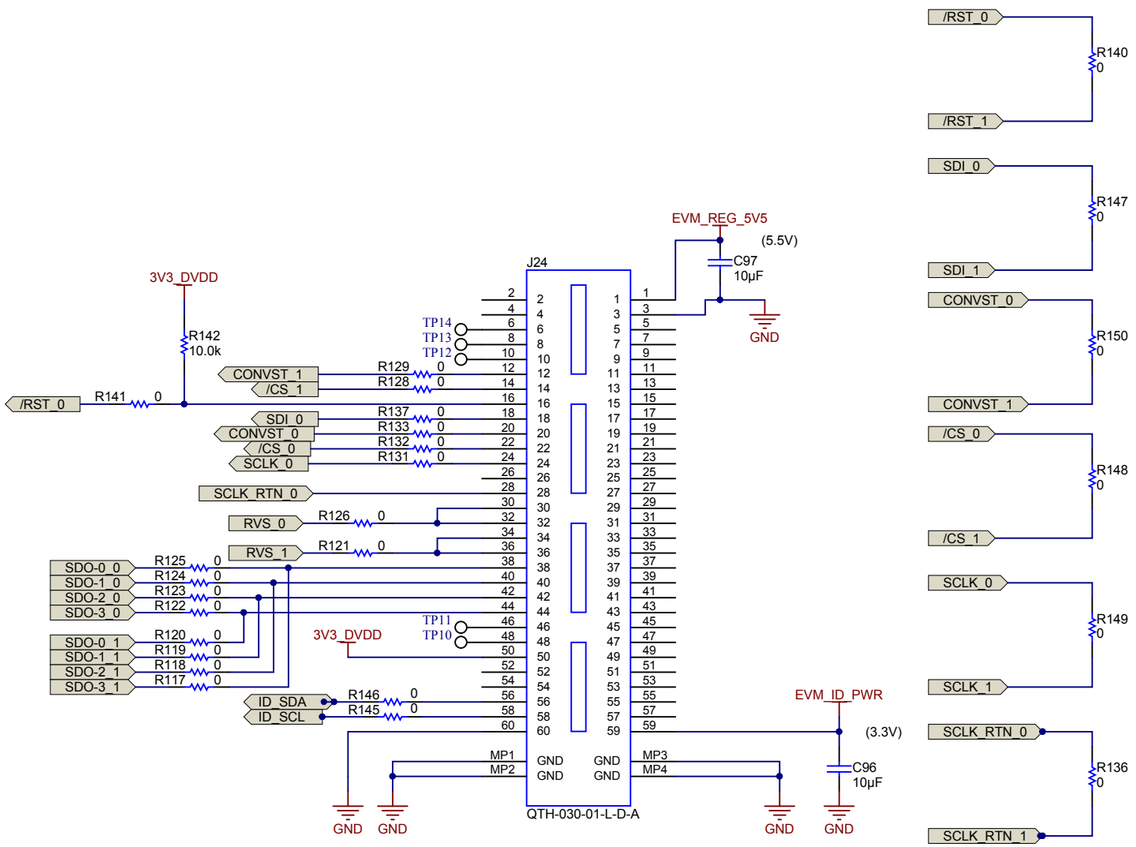
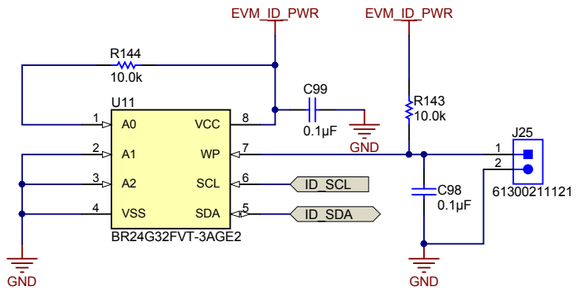
Cannot open file C:\Users\a0393901\Desktop\Pin-out-Capture-TIDA-01351.jpg



Connection to PHI Board for data capture



EEPROM for ADC Identification

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Preliminary Version. Not Tested. Subject to change without notice.

Orderable: N/A	Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: Capture	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 6 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351_Capture.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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H2
1
NY PMS 440 0025 PH

H6
1
NY PMS 440 0025 PH

H1
1
NY PMS 440 0025 PH

H5
1
NY PMS 440 0025 PH

H14
1902C

H8
1902C

H13
1902C

H7
1902C

FID1 FID3 FID2

FID6 FID4 FID5

H4
9774050360R

H3
9774050360R

PCB Number: TIDA-01351
PCB Rev: E1

PCB LOGO
Pb-Free Symbol

PCB LOGO
FCC disclaimer

PCB LOGO

Variant/Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ4
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ3
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ1
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: N/A	Designed for: Public Release	Mod. Date: 12/8/2016
TID #: TIDA-01351	Project Title: CW Signal Conditioning	
Number: TIDA-01351 Rev: E1	Sheet Title: Hardware	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 7 of 7
Drawn By: Sanjay Pithadia	File: TIDA-01351_Hardware.SchDoc	Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support	

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