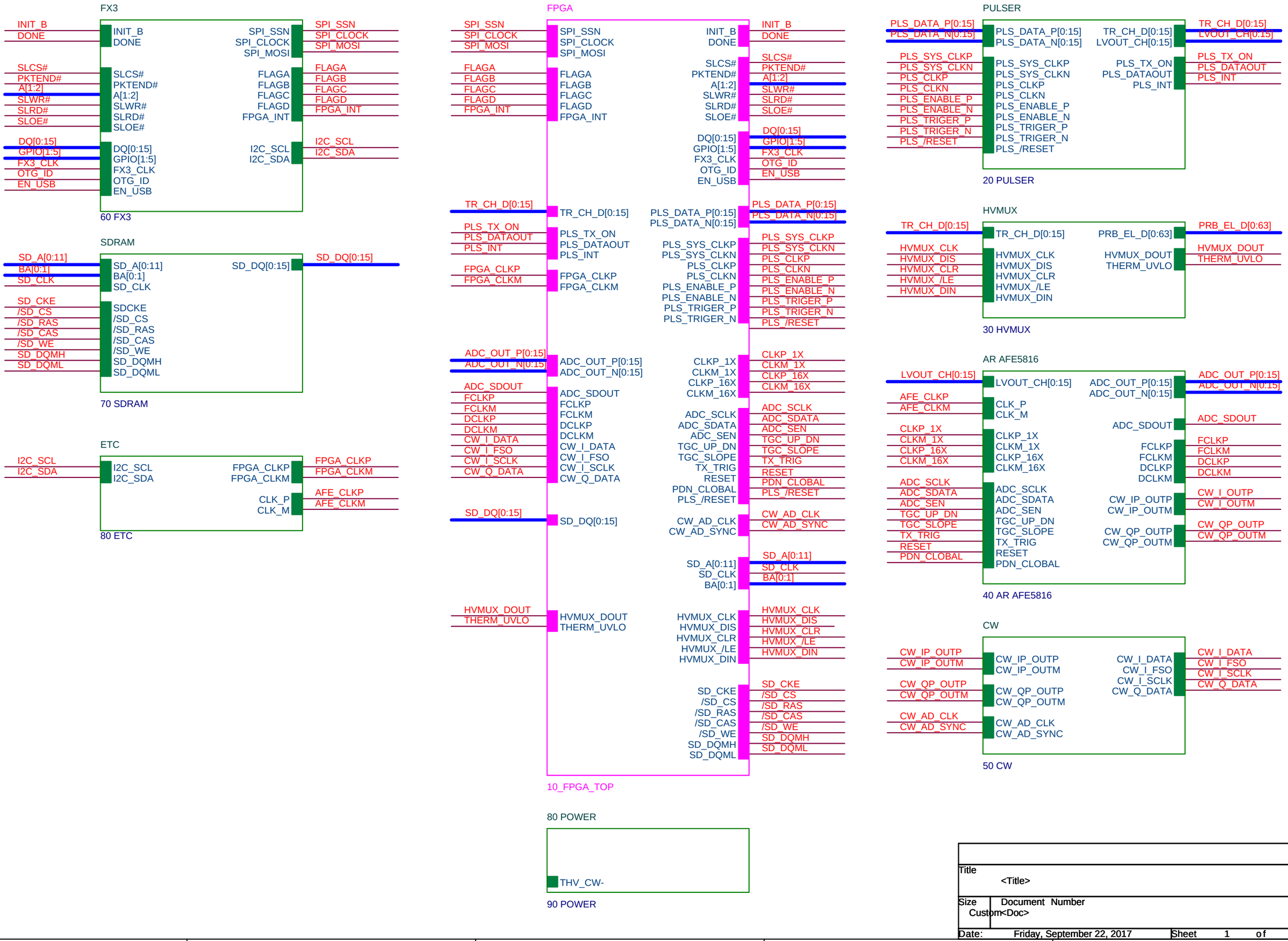

FX3
INIT_B
DONE
SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#
DQ[0:15]
GPIO[1:5]
FX3_CLK
OTG_ID
EN_USB
SPI_SSN
SPI_CLOCK
SPI_MOSI
FLAGA
FLAGB
FLAGC
FLAGD
FPGA_INT
I2C_SCL
I2C_SDA
60 FX3
SDRAM
SD_A[0:11]
BA[0:1]
SD_CLK
SD_CKE
/SD_CS
/SD_RAS
/SD_CAS
/SD_WE
SD_DQMH
SD_DQML
SD_DQ[0:15]
70 SDRAM
ETC
FPGA_CLKP
FPGA_CLKM
CLK_P
CLK_M
AFE_CLKP
AFE_CLKM
80 ETC
FPGA
TR_CH_D[0:15]
PLS_TX_ON
PLS_DATAOUT
PLS_INT
FPGA_CLKP
FPGA_CLKM
ADC_OUT_P[0:15]
ADC_OUT_N[0:15]
ADC_SDOUT
FCLKP
FCLKM
DCLKP
DCLKM
CW_I_DATA
CW_I_FSO
CW_I_SCLK
CW_Q_DATA
PLS_DATA_P[0:15]
PLS_DATA_N[0:15]
PLS_SYS_CLKP
PLS_SYS_CLKN
PLS_CLKP
PLS_CLKN
PLS_ENABLE_P
PLS_ENABLE_N
PLS_TRIGER_P
PLS_TRIGER_N
PLS_/RESET
CLKP_1X
CLKM_1X
CLKP_16X
CLKM_16X
ADC_SCLK
ADC_SDATA
ADC_SEN
TGC_UP_DN
TGC_SLOPE
TX_TRIG
RESET
PDN_CLOBAL
CW_AD_CLK
CW_AD_SYNC
HVMUX_CLK
HVMUX_DIS
HVMUX_CLR
HVMUX_/LE
HVMUX_DIN
HVMUX_DOUT
THERM_UVLO
10_FPGA_TOP
80 POWER
THV_CW-
90 POWER
PULSER
20 PULSER
HVMUX
PRB_EL_D[0:63]
30 HVMUX
AR AFE5816
LVOUT_CH[0:15]
TR_CH_D[0:15]
40 AR AFE5816
CW
50 CW
Title
<Title>
Size
Custom
Document Number
<Doc>
Rev
<RevCode>
Date:
Friday, September 22, 2017
Sheet
1
of
1

INIT_B
DONE

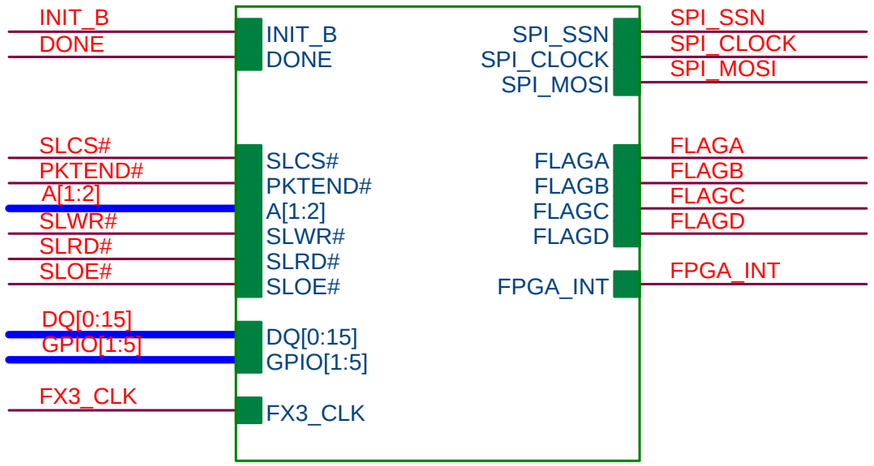
SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#

DQ[0:15]
GPIO[1:5]

FX3_CLK

OTG_ID
EN_USB

Data BUS_Control Signal



61 FX3_Data BUS_Control Signal

SPI_SSN
SPI_CLOCK
SPI_MOSI

FLAGA
FLAGB
FLAGC
FLAGD

FPGA_INT

I2C_SCL
I2C_SDA

Power_Port

62 FX3_Power_Port

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I2C_SCL
I2C_SDA

FPGA_CLKP
FPGA_CLKM

CLK_P
CLK_M

EEPROM&TEMPERATURE

I2C_SCL
I2C_SDA

I2C_SCL
I2C_SDA

82 EEPROM

VOTLAGE_MONITORING

I2C_SCL
I2C_SDA

I2C_SCL
I2C_SDA

83 VOTLAGE_MONITORING

CLOCK

FPGA_CLKP
FPGA_CLKM

AFE_CLKP
AFE_CLKM

FPGA_CLKP
FPGA_CLKM

AFE_CLKP
AFE_CLKM

81 CLOCK

Title <Title>		
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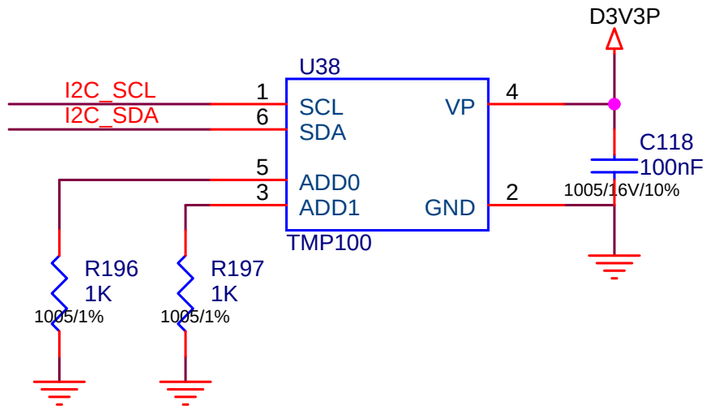
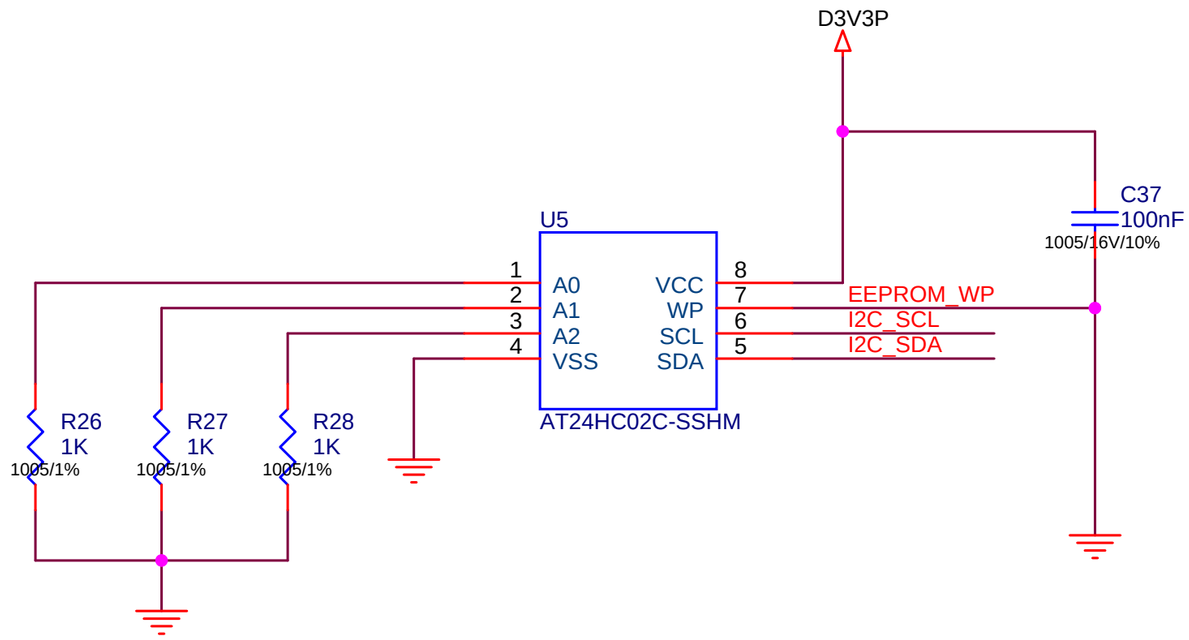
I2C_SCL
I2C_SDA

Board	Temperature I2C Address
FE	1001000



Board	Board ID EEPROM I2C Address
FE	1010000



Title <Title>		
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I2C_SCL
I2C_SDA

HV_AHVP_ HV_AHVN_ A5VP A5VP_AR A3.3VP_VCNTL A5VN_PLS A3.3VN_VCNTL A3.3VP_AR A3VP_PLS A1.8VP_AR A5VP_PLS D1.8VP_AR D3.3V_FPGA D2.5V_FPGA

R? 200K 1005/1%
R? 200K 1005/1%
R188 4.3K 1005/1%
R189 4.3K 1005/1%
R190 4.3K 1005/1%
R191 1K 1005/1%
R197 1K 1005/1%
R198 4.3K 1005/1%
R199 4.3K 1005/1%
R200 4.3K 1005/1%
R201 4.3K 1005/1%
R202 4.3K 1005/1%
R203 4.3K 1005/1%
R204 4.3K 1005/1%

R? 6K 1005/1%
R? 6K 1005/1%
R192 4.3K 1005/1%
R193 4.3K 1005/1%
R194 1K 1005/1%
R195 4.3K 1005/1%
R196 4.3K 1005/1%
R208 1K 1005/1%
R? 1K 1005/1%
R764 4.3K 1005/1%
R? 1K 1005/1%

A5VP_ADC

A5VP_ADC
C? 100nF 1005/16V/10%

U19
CD4067BPW

24	VDD	INHIBIT	15 VMON_EN
9	S0	A0	10 VMON_A0
8	S1	A1	11 VMON_A1
7	S2	A2	14 VMON_A2
6	S3	A3	13 VMON_A3
5	S4		
4	S5		
3	S6		
2	S7		
23	S8		
22	S9	D	1 PRE_VMON_OUT → TP30
21	S10		
20	S11		
19	S12		
18	S13		
17	S14		
16	S15	VSS	12

C1526 100pF 1005/25V/10%

R740 15K 1005/1%
R743 15K 1005/1%
R751 15K 1005/1%
R752 15K 1005/1%
R749 1.5K 1005/1%
VMON_OUT
C1523 100nF 1005/16V/10%
C1525 100nF 1005/16V/10%
U65B OP462HRUZ
U66C OP462HRUZ
A5VP_ADC

R754 15K 1005/1%
R760 15K 1005/1%
R762 15K 1005/1%
U64C OP462HRUZ
A5VP_ADC

R755 15K 1005/1%
R761 15K 1005/1%
R763 15K 1005/1%
U63D OP462HRUZ
A5VP_ADC

CW & VMON Control register setting : 0100111(0x27)

D3.3VP
U43
PCF8574PW

I2C_SCL	2	SCL	VCC 5 → R437 10K 1005/1% → D3.3VP
I2C_SDA	4	SDA	/INT 1
A0	6	A0	P0 10 VMON_EN
A1	7	A1	P1 11 VMON_A0
A2	9	A2	P2 12 VMON_A1
	3	NC1	P3 14 VMON_A2
	8	NC2	P4 16 VMON_A3
	13	NC3	P5 17
	18	NC4	P6 19
	15	GND	P7 20

C876 100NF 1005/16V/10%

D3.3VP
A0 R9 4.7K 1005/1%
A1 R11 4.7K 1005/1%
A2 R13 4.7K 1005/1%

D3.3VP
C749 100nF 1005/25V/10%
U12
TXS0102DCU

I2C_SCL	3	VCCA	VCCB 7
I2C_SDA	5	A1	B1 8 → C748 100nF 1005/25V/10% → A5VP_ADC
	4	A2	B2 1
	6	OE	GND 2

R168 4.7K 1005/1%
R169 4.7K 1005/1%
A5VP_ADC

VMON_OUT
U44
ADS1000

1	VIN+	VDD	5
3	SCL	VIN-	6 → R10 0 1005/1% → A5VP_ADC
4	SDA	GND	2

C877 100nF 1005/25V/10%
C878 4.7uF 1608/25V/10%
A5VP_ADC

Title	<Title>	
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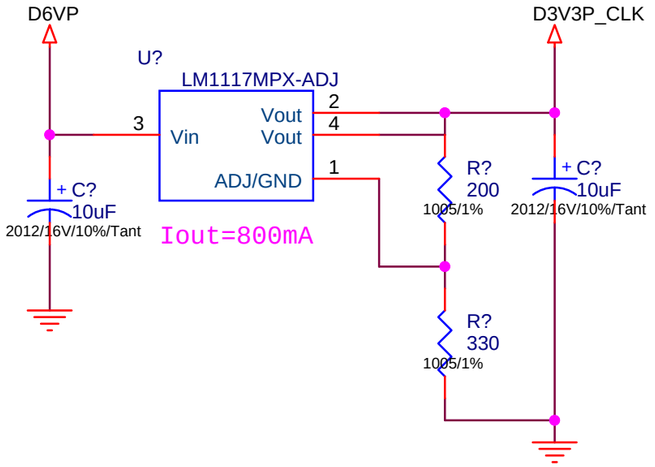

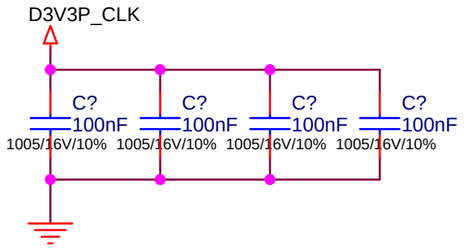

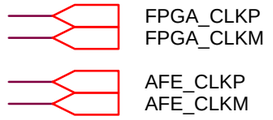

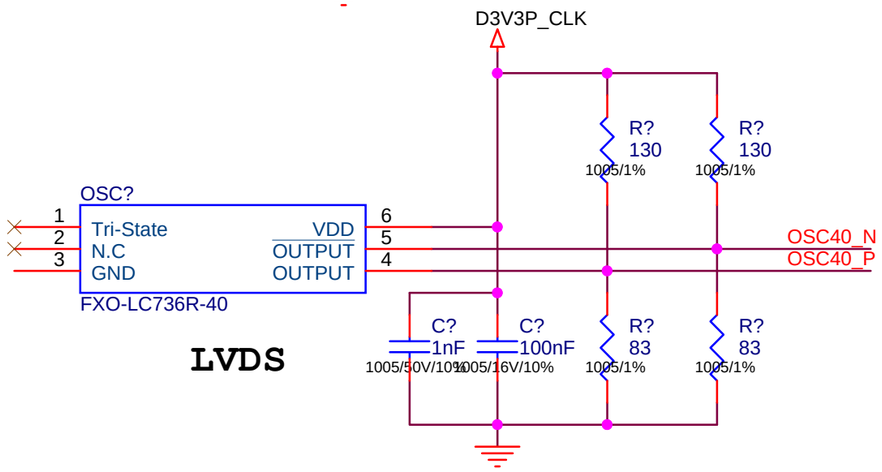

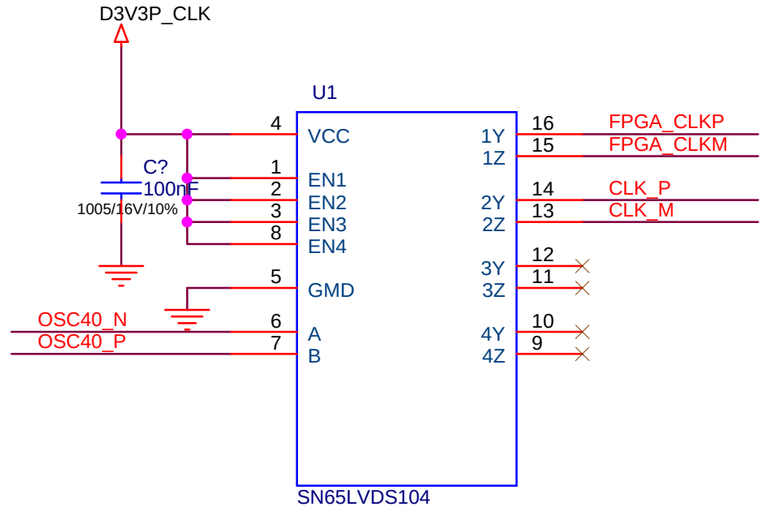

CLOCK Buffer LVDS 1:4

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INIT_B
DONE
GPIO[52]
GPIO[50]

SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#

DQ[0:15]
GPIO[1:5]

FX3_CLK

SPI_SSN
SPI_CLOCK
SPI_MOSI

FLAGA
FLAGB
FLAGC
FLAGD

FPGA_INT

U1A

P - PORT
SEC 1/7
VIO1

DQ0	F10	R2	22 1005/1%	DQ0
DQ1	F9	R61	22 1005/1%	DQ1
DQ2	F7	R62	22 1005/1%	DQ2
DQ3	G10	R63	22 1005/1%	DQ3
DQ4	G9	R64	22 1005/1%	DQ4
DQ5	F8	R65	22 1005/1%	DQ5
DQ6	H10	R66	22 1005/1%	DQ6
DQ7	H9	R67	22 1005/1%	DQ7
DQ8	J10	R68	22 1005/1%	DQ8
DQ9	J9	R69	22 1005/1%	DQ9
DQ10	K11	R70	22 1005/1%	DQ10
DQ11	L10	R71	22 1005/1%	DQ11
DQ12	K10	R72	22 1005/1%	DQ12
DQ13	K9	R73	22 1005/1%	DQ13
DQ14	J8	R74	22 1005/1%	DQ14
DQ15	G8	R75	22 1005/1%	DQ15
PCLK	J6	R76	22 1005/1%	FX3_CLK
CTL0	K8	R77	22 1005/1%	SLCS#
CTL1	K7	R78	22 1005/1%	SLWR#
CTL2	J7	R79	22 1005/1%	SLOE#
CTL3	H7	R80	22 1005/1%	SLRD#
CTL4	G7	R81	22 1005/1%	FLAGA
CTL5	G6	R82	22 1005/1%	FLAGB
CTL6	K6	R83	22 1005/1%	FLAGC
CTL7	H8	R84	22 1005/1%	PKTEND#
CTL8	G5	R85	22 1005/1%	FLGAD
CTL9	H6	R86	22 1005/1%	GPIO_3
CTL10	K5	R87	22 1005/1%	GPIO_4
CTL11	J5	R88	22 1005/1%	A1
CTL12	H5	R89	22 1005/1%	A2
PMODE0	G4	R90	22 1005/1%	PMODE[0]
PMODE1	H4	R91	22 1005/1%	PMODE[1]
PMODE2	L4	R92	22 1005/1%	PMODE[2]
INT_N_CTL15	L8	R35	22 1005/1%	FPGA_INT
RESET_N	C5		/RESET	

FX3_121_BUMP_4

VCC_ARROW
R36
22
1005/1%
FPGA_INT

/RESET
SW1
EVQ-Q2P02W
C49
100nF
1005/16V/10%

U1B

S0 - PORT
SEC 2/7
VIO2

DQ16	K2	R93	22 1005/1%	
DQ17	J4	R94	22 1005/1%	
DQ18	K1	R95	22 1005/1%	
DQ19	J2	R96	22 1005/1%	
DQ20	J3	R97	22 1005/1%	
DQ21	J1	R98	22 1005/1%	
DQ22	H2	R99	22 1005/1%	
DQ23	H3	R100	22 1005/1%	
DQ24	F4	R101	22 1005/1%	
DQ25	G2	R102	22 1005/1%	
DQ26	G3	R103	22 1005/1%	
DQ27	F3	R104	22 1005/1%	
GPIO45	F2		GPIO45	

FX3_121_BUMP_4

U1C

S1 - PORT
SEC 3/7
VIO3
VIO4

DQ28	F5	R105	22 1005/1%	
DQ29	E1	R106	22 1005/1%	
DQ30	E5	R107	22 1005/1%	
DQ31	E4	R108	22 1005/1%	
I2S-CLK	D1	R109	22 1005/1%	GPIO[50]
I2S-SD	D2	R110	22 1005/1%	
I2S-WS	D3	R111	22 1005/1%	GPIO[52]
UART-RTS_SPI-SCK	D4	R112	22 1005/1%	SPI_SCK
UART-CTS_SPI-SSN	C1	R113	22 1005/1%	SPI_SSN
UART-TX_SPI-MISO	C2	R114	22 1005/1%	SPI_MISO
UART-RX_SPI-MOSI	D5	R115	22 1005/1%	SPI_MOSI
I2S-MCLK	C4	R116	22 1005/1%	

FX3_121_BUMP_4

D3.3VP
LED?
LED_BLUE
R?
332
1005/1%

VCC_ARROW
J1
SPI_SCK
SPI_MOSI
SPI_SSN
SPI_MISO
1
2
3
4
5
6
CON6

D1V8P
R?
100K/DNI
1005/1%
SW?
GPIO45
A1
B1
EVQ-PE105K/DNI
C?
100nF/DNI
1005/16V/10%

D3V3P
R? 10K 1005/1% PMODE0
R? 30K/DNI 1005/1%

D3V3P
R? 10K 1005/1% PMODE1
R? 30K/DNI 1005/1%

D3V3P
R? 10K/DNI 1005/1% PMODE2
R? 30K/DNI 1005/1%

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OTG_ID
EN_USB

U1E

XTAL / CLK

SEC 5/7

FSLC0
FSLC1
FSLC2
XTALIN
XTALOUT
CLKIN
CLKIN_32
CVDDQ

B2 FSLC0
B4 FSLC1
E6 FSLC2
C6 XTALIN
C7 XTALOUT
D7
D6

Y1
1 2
19.2MHz
C19 12pF 1005/16V/10%
C18 12pF 1005/16V/10%

FX3_121_BUMP_4

Crystal/Clock Frequency Selection

D3V3P_USB D3V3P_USB D3V3P_USB

R3 10K 1005/1% FSLC0
R5 10K 1005/1% FSLC1
R7 10K 1005/1% FSLC2
R4 10K 1005/1%
R6 10K 1005/1%
R8 10K 1005/1%

0 0 0 19.2MHz Crystal

U1F

MISC

SEC 6/7

I2C-GPIO58_SCL
I2C-GPIO59_SDA
I2C-GPIO60_CHARGER-DETECT
TCK
TDI
TDO
TMS
TRST_N
VIO5

D3V3P_USB

R9 2K 1005/1%
R10 2K 1005/1%

D9 I2C_SCL
D10 I2C_SDA
D11 Charger Detector
F6 TCK
E7 TDI
C10 TDO
E8 TMS
B11 /TRST

FX3_121_BUMP_4

I2C_SCL
I2C_SDA

D3V3P_USB

R11 R12 R13 R14 R15 R16 10K 1005/1%

/TRST
TDI
TMS
TCK
TDO

J1
CON20A

D3V3P_USB

U32

SS_RX_P
SS_RX_M
SS_TX_P
SS_TX_M

D1+ D1- GND D2+ D2-
NC NC GND NC NC

TPD4E05U06 DQA

U1G

POWER

SEC 7/7

D1V2P_USB
A1V2P_USB
D1V2P_USB
D1V2P_USB
D1V2P_USB

H1 C3 L7 E9 F11 VDD1 VDD2 VDD3 VDD4 VDD5
L5 J11 VDD_SRAM_VDD1 VDD_SRAM_VDD2
A7 AVDD
A2 U3RXVDDQ
B5 U3TXVDDQ
B10 VDD_EFVDDQ
G1 L1 E2 L6 D8 G11 L11 K4 L3 K3 L2 A8 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12

VBAT E10
VIO5 C11
VIO2 F1
VIO3 E3
CVDDQ B6
VIO4 B1
VIO1_1 VIO1_2 L9 H11
AVSS B7
U3VSSQ A1
U2AFEVSSQ B9
U2PLLVSSQ B8

D3V3P_USB
D3V3P_USB
D3V3P_USB
D3V3P_USB
D3V3P_USB
D3V3P_USB

FX3_121_BUMP_4

U1D

U - PORT

SEC 4/7

VBUS/VBAT
VBUS
VBUS/VBAT

VBUS E11
OTG_ID C9
SSRXP A4
SSRXM A3
SSTXP A5
SSTXM A6
DP A9
DM A10
NC A11
R_USB2 C8
R_USB3 B3

5VP_USB
OTG_ID
SS_RX_P
SS_RX_M
100nF C78 1005/25V/10%
100nF C80 1005/25V/10%
SS_TX_P
SS_TX_M
DP
DM
R42 0 1005/1%
R43 200 1005/1%

FX3_121_BUMP_4

Micron_B

U31

MIC_SSRX+ MIC_SSRX- MIC_SSTX+ MIC_SSTX- D- D+
VBUS ID SHIELD1 SHIELD2 SHIELD3 SHIELD4 SHIELD5 SHIELD6 GND GND

ZX360D-B-10P

BLM21PG221SN1D FB31
C77 150uF 2012/16V/10%/Tant
C79 100nF 1005/50V/10%
C81 100nF 1005/50V/10%
R122 1M 1005/1%

VBUS

VBUS
U33
DP DM
D2 D1 OUT EN GND IN
EN_USB
5VP_USB
TPD3S044
C16 100nF 1005/16V/10%

1V2P_USB

C2 100nF 1005/16V/10%
C3 100nF 1005/16V/10%
C4 100nF 1005/16V/10%
C5 10nF 1005/16V/10%
C6 10nF 1005/16V/10%
C82 100nF 1005/16V/10%
C83 100nF 1005/16V/10%
C84 10nF 1005/16V/10%
C85 100nF 1005/16V/10%
C86 10nF 1005/16V/10%

AVDD_USB
C87 100nF 1005/16V/10%
C88 2.2uF 1608/16V/10%

U3RX_VDDQ
C89 100nF 1005/16V/10%
C90 2.2uF 1608/16V/10%

U3TX_VDDQ
C91 100nF 1005/16V/10%
C92 2.2uF 1608/16V/10%

AVDD_USB
C93 100nF 1005/16V/10%
C94 2.2uF 1608/16V/10%

CVDDQ (1.8 or 3.3)
C103 100nF 1005/16V/10%
C104 2.2uF 1608/16V/10%

VIO1(1.8 2.5 and 3.3)
C95 100nF 1005/16V/10%
C96 2.2uF 1608/16V/10%

VIO2(1.8 2.5 and 3.3)
C97 100nF 1005/16V/10%
C98 2.2uF 1608/16V/10%

VIO3(1.8 2.5 and 3.3)
C99 100nF 1005/16V/10%
C100 2.2uF 1608/16V/10%

VIO4(1.8 2.5 and 3.3)
C101 100nF 1005/16V/10%
C102 2.2uF 1608/16V/10%

VIO5(1.8 2.5 and 3.3)
C105 100nF 1005/16V/10%
C106 2.2uF 1608/16V/10%

1V2P_USB U3RX_VDDQ
MPZ2012S601A FB32

1V2P_USB U3TX_VDDQ
MPZ2012S601A FB33

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FPGA_CLKP
FPGA_CLKM

ADC_OUT_P[0:15]
ADC_OUT_N[0:15]
ADC_SDOUT
FCLKP
FCLKM
DCLKP
DCLKM
CW_I_DATA
CW_I_FSO
CW_I_SCLK
CW_Q_DATA

FLAGA
FLAGB
FLAGC
FLAGD
FPGA_INT

SD_DQ[0:15]

TR_CH_D[0:15]
PLS_TX_ON
PLS_DATAOUT
PLS_INT

HVMUX_DOUT
THERM_UVLO

SPI_SSN
SPI_CLOCK
SPI_MOSI

TR

FPGA_CLKP
FPGA_CLKM

CLKP_1X
CLKM_1X
CLKP_16X
CLKM_16X

ADC_OUT_P[0:15]
ADC_OUT_N[0:15]
ADC_SDOUT
FCLKP
FCLKM
DCLKP
DCLKM

ADC_SCLK
ADC_SDATA
ADC_SEN
TGC_UP_DN
TGC_SLOPE
TX_TRIG
AFE_RESET
PDN_CLOBAL

TR_CH_D[0:15]

PLS_DATA_P[0:15]
PLS_DATA_N[0:15]

PLS_TX_ON
PLS_DATAOUT
PLS_INT

PLS_SYS_CLKP
PLS_SYS_CLKN
PLS_CLKP
PLS_CLKN
PLS_ENABLE_P
PLS_ENABLE_N
PLS_TRIGER_P
PLS_TRIGER_N
PLS_/RESET

11 FPGA_TR

CONFIG

SPI_SSN
SPI_CLOCK
SPI_MOSI

INIT_B
DONE

13 FPGA_CONFIG

MGT&NC

14 FPGA MGT&NC

EMIF

CW_I_DATA
CW_I_FSO
CW_I_SCLK
CW_Q_DATA

FLAGA
FLAGB
FLAGC
FLAGD
FPGA_INT

SD_DQ[0:15]

HVMUX_DOUT
THERM_UVLO

CW_AD_CLK
CW_AD_SYNC

SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#

DQ[0:15]
GPIO[1:5]
FX3_CLK
OTG_ID
EN_USB

SD_A[0:11]
BA[0:1]
SD_CLK
SD_CKE
/SD_CS
/SD_RAS
/SD_CAS
/SD_WE
SD_DQMH
SD_DQML

TR_CH_D[0:15]
HVMUX_CLK
HVMUX_DIS
HVMUX_CLR
HVMUX_/LE
HVMUX_DIN

12 FPGA_EMIF

POWER&GND

15 FPGA_POWER&GND

CLKP_1X
CLKM_1X
CLKP_16X
CLKM_16X
ADC_SCLK
ADC_SDATA
ADC_SEN
TGC_UP_DN
TGC_SLOPE
TX_TRIG
RESET
PDN_CLOBAL
CW_AD_CLK
CW_AD_SYNC

PLS_DATA_P[0:15]
PLS_DATA_N[0:15]
PLS_SYS_CLKP
PLS_SYS_CLKN
PLS_CLKP
PLS_CLKN
PLS_ENABLE_P
PLS_ENABLE_N
PLS_TRIGER_P
PLS_TRIGER_N
PLS_/RESET

SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#

DQ[0:15]
GPIO[1:5]
FX3_CLK
OTG_ID
EN_USB

SD_A[0:11]
BA[0:1]
SD_CLK
SD_CKE
/SD_CS
/SD_RAS
/SD_CAS
/SD_WE
SD_DQMH
SD_DQML

TR_CH_D[0:15]

HVMUX_CLK
HVMUX_DIS
HVMUX_CLR
HVMUX_/LE
HVMUX_DIN

INIT_B
DONE

Title	FPGA_TOP	
Size A3	Document Number 2014110001	Rev 2.0
Date: Friday, September 22, 2017	Sheet 1 of 1	

TR_CH_D[0:15]

HVMUX_CLK
HVMUX_DIS
HVMUX_CLR
HVMUX_/LE
HVMUX_DIN

PRB_EL_D[0:63]

HVMUX_DOUT
THERM_UVLO

U1A

TR_CH_D0	N1	IN0	IN16	M8	TR_CH_D4
PRB_EL_D0	N2	OUT0	OUT16	M7	PRB_EL_D4
	M2	IN1	IN17	N7	
PRB_EL_D16	M1	OUT1	OUT17	N8	PRB_EL_D20
	L1	IN2	IN18	P10	
PRB_EL_D32	L2	OUT2	OUT18	P9	PRB_EL_D36
	K2	IN3	IN19	N9	
PRB_EL_D48	K1	OUT3	OUT19	N10	PRB_EL_D52
TR_CH_D1	K4	IN4	IN20	M10	TR_CH_D5
PRB_EL_D1	K3	OUT4	OUT20	M9	PRB_EL_D5
	L3	IN5	IN21	L9	
PRB_EL_D17	L4	OUT5	OUT21	L10	PRB_EL_D21
	M4	IN6	IN22	K10	
PRB_EL_D33	M3	OUT6	OUT22	K9	PRB_EL_D37
	N3	IN7	IN23	K12	
PRB_EL_D49	N4	OUT7	OUT23	K11	PRB_EL_D53
TR_CH_D2	P4	IN8	IN24	L11	TR_CH_D6
PRB_EL_D2	P3	OUT8	OUT24	L12	PRB_EL_D6
	P6	IN9	IN25	M12	
PRB_EL_D18	P5	OUT9	OUT25	M11	PRB_EL_D22
	N5	IN10	IN26	N11	
PRB_EL_D34	N6	OUT10	OUT26	N12	PRB_EL_D38
	M6	IN11	IN27	P12	
PRB_EL_D50	M5	OUT11	OUT27	P11	PRB_EL_D54
TR_CH_D3	L5	IN12	IN28	N13	TR_CH_D7
PRB_EL_D3	L6	OUT12	OUT28	N14	PRB_EL_D7
	K6	IN13	IN29	M14	
PRB_EL_D19	K5	OUT13	OUT29	M13	PRB_EL_D23
	K8	IN14	IN30	L13	
PRB_EL_D35	K7	OUT14	OUT30	L14	PRB_EL_D39
	L7	IN15	IN31	K14	
PRB_EL_D51	L8	OUT15	OUT31	K13	PRB_EL_D55

STHV64SW

U1B

TR_CH_D8	B1	IN32	IN48	C8	TR_CH_D12
PRB_EL_D8	B2	OUT32	OUT48	C7	PRB_EL_D12
	C2	IN33	IN49	B7	
PRB_EL_D24	C1	OUT33	OUT49	B8	PRB_EL_D28
	D1	IN34	IN50	A10	
PRB_EL_D40	D2	OUT34	OUT50	A9	PRB_EL_D44
	E2	INT35	IN51	B9	
PRB_EL_D56	E1	OUT35	OUT51	B10	PRB_EL_D60
TR_CH_D9	E4	IN36	IN52	C10	TR_CH_D13
PRB_EL_D9	E3	OUT36	OUT52	C9	PRB_EL_D13
	D3	IN37	IN53	D9	
PRB_EL_D25	D4	OUT37	OUT53	D10	PRB_EL_D29
	C4	IN38	IN54	E10	
PRB_EL_D41	C3	OUT38	OUT54	E9	PRB_EL_D45
	B3	IN39	IN55	E12	
PRB_EL_D57	B4	OUT39	OUT55	E11	PRB_EL_D61
TR_CH_D10	A4	IN40	IN56	D11	TR_CH_D14
PRB_EL_D10	A3	OUT40	OUT56	D12	PRB_EL_D14
	A6	IN41	IN57	C12	
PRB_EL_D26	A5	OUT41	OUT57	C11	PRB_EL_D30
	B5	IN42	IN58	B11	
PRB_EL_D42	B6	OUT42	OUT58	B12	PRB_EL_D46
	C6	IN43	IN59	A12	
PRB_EL_D58	C5	OUT43	OUT59	A11	PRB_EL_D62
TR_CH_D11	D5	IN44	IN60	B13	TR_CH_D15
PRB_EL_D11	D6	OUT44	OUT60	B14	PRB_EL_D15
	E6	IN45	IN61	C14	
PRB_EL_D27	E5	OUT45	OUT61	C13	PRB_EL_D31
	E8	IN46	IN62	D13	
PRB_EL_D43	E7	OUT46	OUT62	D14	PRB_EL_D47
	D7	IN47	IN63	E14	
PRB_EL_D59	D8	OUT47	OUT63	E13	PRB_EL_D63

STHV64SW

HVP1

HVN1

A3V3P_HVMUX

U1C

	F8	VPP	GND	A7	
	F9	VPP	GND	A8	
	G8	VPP	GND	F1	
	G9	VPP	GND	F2	
	H8	VPP	GND	F3	
	H9	VPP	GND	F4	
	J8	VPP	GND	F5	
			GND	F11	
	F6	VNN	GND	F12	
	F7	VNN	GND	F13	
	G6	VNN	GND	F14	
	G7	VNN	GND	G5	
	H6	VNN	GND	H1	
	H7	VNN	GND	H2	
	J7	VNN	GND	H3	
			GND	H4	
	F10	VDDP	GND	H5	
	G10	VDDP	GND	H11	
	G11	VDDP	GND	H12	
	H10	VDDP	GND	H13	
	J10	VDDP	GND	H14	
			GND	J1	
HVMUX_CLK	G14	CLK	GND	J2	
HVMUX_DIS	G1	DIS	GND	J3	
HVMUX_CLR	G2	CLR	GND	J4	
HVMUX_/LE	G3	/LE	GND	J5	
HVMUX_DIN	G4	DIN	GND	J11	
HVMUX_DOUT	G13	DOUT	GND	J12	
THERM_UVLO	G12	THERM_UVLO	GND	J13	
			GND	J14	
	A1	NC		P7	
	A2	NC	RGND	P8	
	A13	NC	RGND		
	A14	NC			
	J6	NC			
	J9	NC			
	P1	NC			
	P2	NC			
	P13	NC			
	P14	NC			

STHV64SW

RGND

HVP1

C9	2.2uF	5750/250V/10%
C10	2.2uF	5750/250V/10%
C1	470nF	4532/200V/10%
C2	470nF	4532/200V/10%
C3	470nF	4532/200V/10%
C4	470nF	4532/200V/10%

HVN1

C15	2.2uF	5750/250V/10%
C16	2.2uF	5750/250V/10%
C11	470nF	4532/200V/10%
C12	470nF	4532/200V/10%
C13	470nF	4532/200V/10%
C14	470nF	4532/200V/10%

A3V3P_HVMUX

C21	100nF	1005/25V/10%
C22	100nF	1005/25V/10%
C23	100nF	1005/25V/10%
C24	100nF	1005/25V/10%
C25	100nF	1005/25V/10%

Title	MOJUK_HVMUX	
Size A3	Document Number 2014120002	Rev 0.1
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CW_I_DATA
CW_I_FSO
CW_I_SCLK
CW_Q_DATA

FLAGA
FLAGB
FLAGC
FLAGD
FPGA_INT

HVMUX_DOUT
THERM_UVLO

SD_DQ[0:15]

D3V3P_FPGA

U1-3

A21	VCCO_14	IO_0_14	K21 CW_I_DATA
C25	VCCO_14	IO_25_14	L23 CW_Q_DATA
D22	VCCO_14	IO_L1P_T0_D00_MOSI_14	B24 CW_I_FSO
F26	VCCO_14	IO_L2P_T0_D02_14	B22 SD_DQ0
G23	VCCO_14	IO_L2N_T0_D03_14	A22 SD_DQ1
L21	VCCO_14	IO_L4P_T0_D04_14	A23 SD_DQ2
		IO_L4N_T0_D05_14	A24 SD_DQ3
		IO_L5P_T0_D06_14	D26 SD_DQ4
		IO_L5N_T0_D07_14	C26 SD_DQ5
		IO_L6P_T0_FCS_B_14	C23 SD_DQ6
		IO_L6N_T0_D08_VREF_14	C24 SD_DQ7
		IO_L7P_T1_D09_14	D21 SD_DQ8
		IO_L7N_T1_D10_14	C22 SD_DQ9
		IO_L8P_T1_D11_14	B20 SD_DQ10
		IO_L8N_T1_D12_14	A20 SD_DQ11
		IO_L9P_T1_DQS_14	E21 SD_DQ12
		IO_L9N_T1_DQS_D13_14	E22 SD_DQ13
		IO_L10P_T1_D14_14	C21 SD_DQ14
		IO_L10N_T1_D15_14	B21 SD_DQ15
		IO_L11P_T1_SRCC_14	D23 SD_DQMH
		IO_L11N_T1_SRCC_14	D24 SD_DQML
		IO_L12P_T1_MRCC_14	F22 SD_CLK
		IO_L12N_T1_MRCC_14	E23 CW_I_SCLK
		IO_L13P_T2_MRCC_14	G22 CW_AD_CLK
		IO_L13N_T2_MRCC_14	F23 CW_AD_SYNC
		IO_L14P_T2_SRCC_14	G24
		IO_L14N_T2_SRCC_14	F24
		IO_L15P_T2_DQS_RDWR_B_14	E25
		IO_L16P_T2_CSI_B_14	G25
		IO_L16N_T2_A15_D31_14	G26 SD_A0
		IO_L17P_T2_A14_D30_14	F25 SD_A1
		IO_L17N_T2_A13_D29_14	E26 SD_A2
		IO_L18P_T2_A12_D28_14	J26 SD_A3
		IO_L18N_T2_A11_D27_14	H26 SD_A4
		IO_L19P_T3_A10_D26_14	H21 SD_A5
		IO_L19N_T3_A09_D25_VREF_14	G21 SD_A6
		IO_L20P_T3_A08_D24_14	H23 SD_A7
		IO_L20N_T3_A07_D23_14	H24 SD_A8
		IO_L21P_T3_DQS_14	J21 SD_A9
		IO_L21N_T3_DQS_A06_D22_14	H22 SD_A10
		IO_L22P_T3_A05_D21_14	J24 SD_A11
		IO_L22N_T3_A04_D20_14	J25 SD_CKE
		IO_L23P_T3_A03_D19_14	L22 /SD_CS
		IO_L23N_T3_A02_D18_14	K22 /SD_RAS
		IO_L24P_T3_A01_D17_14	K23 /SD_CAS
		IO_L24N_T3_A00_D16_14	J23 /SD_WE

BANK14

XC7K70T-FBG676

D3V3P_FPGA

U2-4

B18	VCCO_15	IO_0_15	K15 GPIO2
E19	VCCO_15	IO_25_15	M16 GPIO3
F16	VCCO_15	IO_L1P_T0_AD0P_15	C16 DQ0
H20	VCCO_15	IO_L1N_T0_AD0N_15	B16 DQ1
J17	VCCO_15	IO_L2P_T0_AD8P_15	A18 DQ2
M18	VCCO_15	IO_L2N_T0_AD8N_15	A19 DQ3
		IO_L3P_T0_DQS_AD1P_15	B17 DQ4
		IO_L3N_T0_DQS_AD1N_15	A17 DQ5
		IO_L4P_T0_AD9P_15	C19 DQ6
		IO_L4N_T0_AD9N_15	B19 DQ7
		IO_L5P_T0_AD2P_15	C17 DQ8
		IO_L5N_T0_AD2N_15	C18 DQ9
		IO_L6P_T0_15	D15 DQ10
		IO_L6N_T0_VREF_15	D16 DQ11
		IO_L7P_T1_AD10P_15	H16 DQ12
		IO_L7N_T1_AD10N_15	G16 DQ13
		IO_L8P_T1_AD3P_15	G15 DQ14
		IO_L8N_T1_AD3N_15	F15 DQ15
		IO_L9P_T1_DQS_AD11P_15	J15 GPIO1
		IO_L9N_T1_DQS_AD11N_15	J16 TR_CH_D0
		IO_L10P_T1_AD4P_15	E15 TR_CH_D1
		IO_L10N_T1_AD4N_15	E16 TR_CH_D2
		IO_L11P_T1_SRCC_AD12P_15	G17 TR_CH_D3
		IO_L11N_T1_SRCC_AD12N_15	F18 TR_CH_D4
		IO_L12P_T1_MRCC_AD5P_15	F17 TR_CH_D5
		IO_L12N_T1_MRCC_AD5N_15	E17 TR_CH_D6
		IO_L13P_T2_MRCC_15	E18 FX3_CLK
		IO_L13N_T2_MRCC_15	D18 TR_CH_D7
		IO_L14P_T2_SRCC_15	H17 TR_CH_D8
		IO_L14N_T2_SRCC_15	H18 TR_CH_D9
		IO_L15P_T2_DQS_15	D19 TR_CH_D10
		IO_L15N_T2_DQS_ADV_B_15	D20 TR_CH_D11
		IO_L16P_T2_A28_15	G19 TR_CH_D12
		IO_L16N_T2_A27_15	F20 TR_CH_D13
		IO_L17P_T2_A26_15	F19 TR_CH_D14
		IO_L17N_T2_A25_15	E20 TR_CH_D15
		IO_L18P_T2_A24_15	H19 GPIO4
		IO_L18N_T2_A23_15	G20 OTG_ID
		IO_L19P_T3_A22_15	K20 SLCS#
		IO_L19N_T3_A21_VREF_15	J20 PKTEND#
		IO_L20P_T3_A20_15	J18 A1
		IO_L20N_T3_A19_15	J19 A2
		IO_L21P_T3_DQS_15	L19 SLWR#
		IO_L21N_T3_DQS_A18_15	L20 SLRD#
		IO_L22P_T3_A17_15	K16 SLOE#
		IO_L22N_T3_A16_15	K17 FLAGA
		IO_L23P_T3_FOE_B_15	M17 FLAGB
		IO_L23N_T3_FWE_B_15	L18 FLAGC
		IO_L24P_T3_RS1_15	L17 FLAGD
		IO_L24N_T3_RS0_15	K18 FPGA_INT

BANK15

XC7K70T-FBG676

STATUS_LED0
STATUS_LED1
STATUS_LED2
STATUS_LED3
STATUS_LED4

CW_AD_CLK
CW_AD_SYNC

DQ[0:15]
GPIO[1:5]
FX3_CLK
OTG_ID
EN_USB

SLCS#
PKTEND#
A[1:2]
SLWR#
SLRD#
SLOE#

TR_CH_D[0:15]

HVMUX_CLK
HVMUX_DIS
HVMUX_CLR
HVMUX_/LE
HVMUX_DIN

SD_A[0:11]
BA[0:1]
SD_CLK
SD_CKE
/SD_CS
/SD_RAS
/SD_CAS
/SD_WE
SD_DQMH
SD_DQML

J23
1 PIN HDR
STATUS_LED0
D8
BL-HG036A-AV-TRB
R1377 330 1005/1%

J24
1 PIN HDR
STATUS_LED1
D9
BL-HG036A-AV-TRB
R1378 330 1005/1%

J17
1 PIN HDR
STATUS_LED2
D2
BL-HG036A-AV-TRB
R61 330 1005/1%

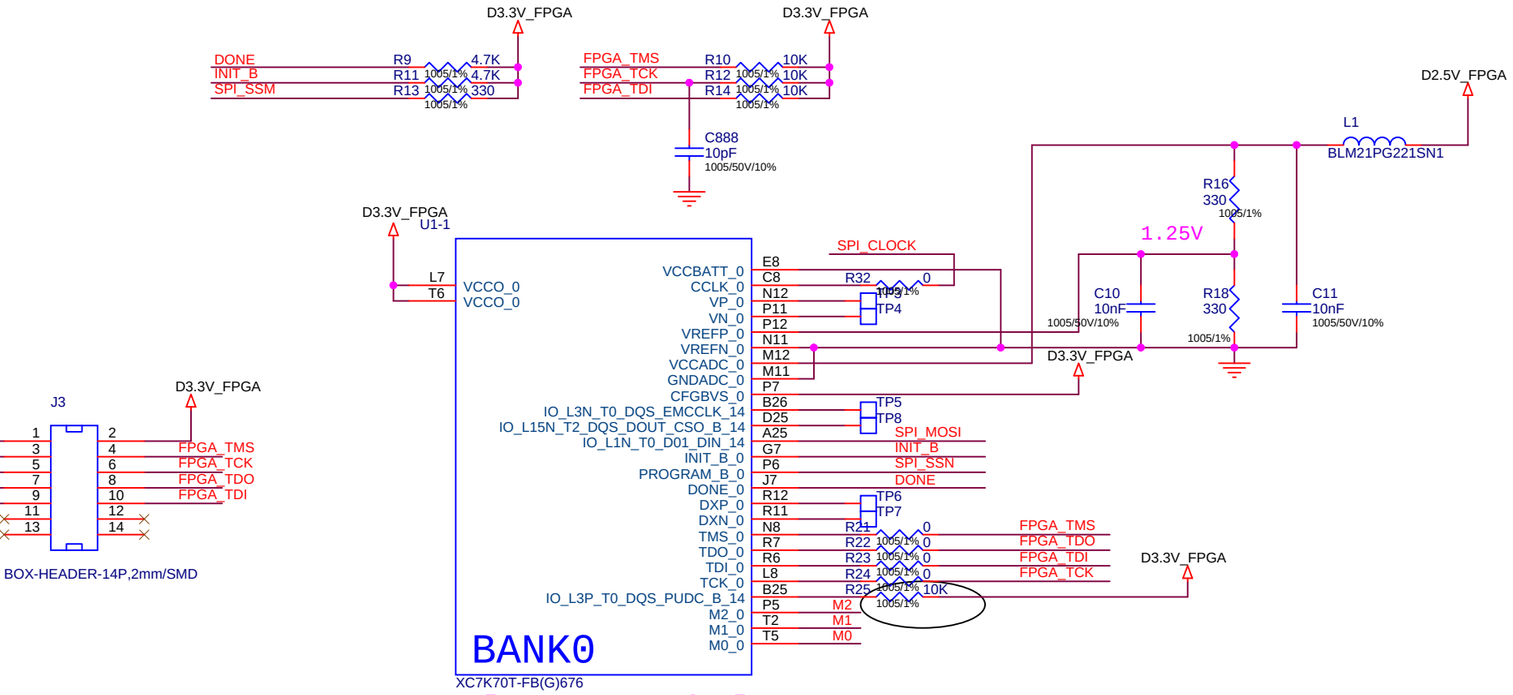
J18
1 PIN HDR
STATUS_LED3
D3
BL-HG036A-AV-TRB
R64 330 1005/1%

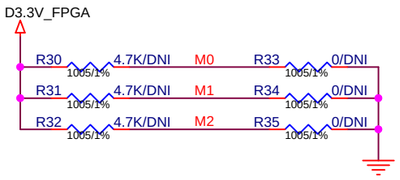
J19
1 PIN HDR
STATUS_LED4
D4
BL-HG036A-AV-TRB
R65 330 1005/1%

Title	FPGA_EMIF	
Size A3	Document Number 2014110001	Rev 2.0
Date: Friday, September 22, 2017	Sheet 1 of 1	

SPI_SSN
SPI_CLOCK
SPI_MOSI

INIT_B
DONE





Slave serial

M[2:0] = 1 1 1 (Default setting --> internal pull up resistors)

FPGA_CFG_CLK은via hole 이 아닌
point to point로연결

Title	FPGA_CONFIG	
Size A3	Document Number 2014110001	Rev 2.0
Date: Thursday, September 21, 2017	Sheet 1 of 1	

PLS_DATA_P[0:15]
PLS_DATA_N[0:15]

PLS_SYS_CLKP
PLS_SYS_CLKN
PLS_CLKP
PLS_CLKN

PLS_ENABLE_P
PLS_ENABLE_N
PLS_TRIGER_P
PLS_TRIGER_N

PLS_/RESET

LVOUT_CH[0:15]
TR_CH_D[0:15]

PLS_INT
PLS_TX_ON
PLS_DATAOUT

HVP0
HVP_CW
HVN0
HVN_CW

U1
STHV1600

CLKSYSN
CLKSYSP
CLKSERN
CLKSERP
DATAIN0N
DATAIN0P
DATAIN1N
DATAIN1P
DATAIN2N
DATAIN2P
DATAIN3N
DATAIN3P
ENSERN
ENSERP
TRIGGERN
TRIGGERP
DATAOUT
INT
RESET
TX_ON
DEVID3
DEVID2
DEVID1
DEVID0
GND
VDDP3V3
VDDM3V3
DGND
IOGND
DVDD
IOVDD

XDCR0 LVOUT0
XDCR1 LVOUT1
XDCR2 LVOUT2
XDCR3 LVOUT3
XDCR4 LVOUT4
XDCR5 LVOUT5
XDCR6 LVOUT6
XDCR7 LVOUT7
XDCR8 LVOUT8
XDCR9 LVOUT9
XDCR10 LVOUT10
XDCR11 LVOUT11
XDCR12 LVOUT12
XDCR13 LVOUT13
XDCR14 LVOUT14
XDCR15 LVOUT15

D1V8P_PLS
A3V3P_PLS
A3V3N_PLS

R1065 10k 1005/1%
R1066 0 1005/1%
C? 100nF 1005/16V/10%
R1067 0 1005/1%
R1068 100 1005/1%
R1069 100 1005/1%
R1070 100 1005/1%
R1071 100 1005/1%
R1072 100 1005/1%
R1073 100 1005/1%
R1074 100 1005/1%
R1064 0 1005/1%
R1060 0 1005/1%
R1061 0 1005/1%

C? 470nF 2012/100V/10%
C? 270pF 2012/100V/10%
C? 50pF 2012/100V/10%

R1022 100 2012/1%
R1023 200 2012/1%
R1024 100 2012/1%
R1025 200 2012/1%
R1026 100 2012/1%
R1027 200 2012/1%
R1028 100 2012/1%
R1029 200 2012/1%
R1031 100 2012/1%
R1032 200 2012/1%
R1033 100 2012/1%
R1034 200 2012/1%
R1037 100 2012/1%
R1038 200 2012/1%
R1039 100 2012/1%
R1040 200 2012/1%
R1041 100 2012/1%
R1042 200 2012/1%
R1043 100 2012/1%
R1044 200 2012/1%
R1045 100 2012/1%
R1046 200 2012/1%
R1047 100 2012/1%
R1048 200 2012/1%
R1051 100 2012/1%
R1052 200 2012/1%
R1053 100 2012/1%
R1054 200 2012/1%
R1055 100 2012/1%
R1056 200 2012/1%
R1057 100 2012/1%
R1058 200 2012/1%

C1894 100nF 2012/100V/10%
C1895 100nF 2012/100V/10%
C1896 100nF 2012/100V/10%
C1897 100nF 2012/100V/10%
C1898 100nF 2012/100V/10%
C1899 100nF 2012/100V/10%
C1901 100nF 2012/100V/10%
C1902 100nF 2012/100V/10%
C1903 100nF 2012/100V/10%
C1904 100nF 2012/100V/10%
C1905 100nF 2012/100V/10%
C1906 100nF 2012/100V/10%
C1908 100nF 2012/100V/10%
C1909 100nF 2012/100V/10%
C1910 100nF 2012/100V/10%
C1911 100nF 2012/100V/10%

TR_CH0 TR_CH1 TR_CH2 TR_CH3 TR_CH4 TR_CH5 TR_CH6 TR_CH7
TR_CH8 TR_CH9 TR_CH10 TR_CH11 TR_CH12 TR_CH13 TR_CH14 TR_CH15

L? 10uH/MLF2012E100KT

Title	PULSER
Size	Custom
Document Number	2014110001
Rev	2.0
Date:	Thursday, September 21, 2017
Sheet	1 of 1

SD_A[0:11]

BA[0:1]

SD_CLK
SD_CKE
/SD_CS
/SD_RAS
/SD_CAS
/SD_WE
SD_DQMH
SD_DQML

D3V3P

U1

1	VDD				
3	VDDQ				
SD_A0	23	A0	DQ15	53	SD_DQ15
SD_A1	24	A1	DQ14	51	SD_DQ14
SD_A2	25	A2	DQ13	50	SD_DQ13
SD_A3	26	A3	DQ12	48	SD_DQ12
SD_A4	29	A4	DQ11	47	SD_DQ11
SD_A5	30	A5	DQ10	45	SD_DQ10
SD_A6	31	A6	DQ9	44	SD_DQ9
SD_A7	32	A7	DQ8	42	SD_DQ8
SD_A8	33	A8	DQ7	13	SD_DQ7
SD_A9	34	A9	DQ6	11	SD_DQ6
SD_A10	22	A10	DQ5	10	SD_DQ5
SD_A11	35	A11	DQ4	8	SD_DQ4
			DQ3	7	SD_DQ3
BA0	20	BA0	DQ2	5	SD_DQ2
BA1	21	BA1	DQ1	4	SD_DQ1
			DQ0	2	SD_DQ0
SD_CLK	38	CLK			
SD_CKE	37	CKE			
/SD_CS	19	/CS			
/SD_RAS	18	/RAS			
/SD_CAS	17	/CAS			
/SD_WE	16	/WE			
SD_DQMH	39	DQMH			
SD_DQML	15	DQML			
54	VSS		NC	36	
52	VSSQ		EPG	55	

IS42/45S16800F

SD_DQ[0:15]

Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
Date: Friday, September 22, 2017		Sheet 1 of 1	

POWER_FILTER

91 POWER_FILTER

POWER_ANALOG

92 POWER_ANALOG

POWER_AFE5816

93 POWER_AFE5808

POWER_DIGITAL

94 POWER_DIGITAL

POWER_CONTROL

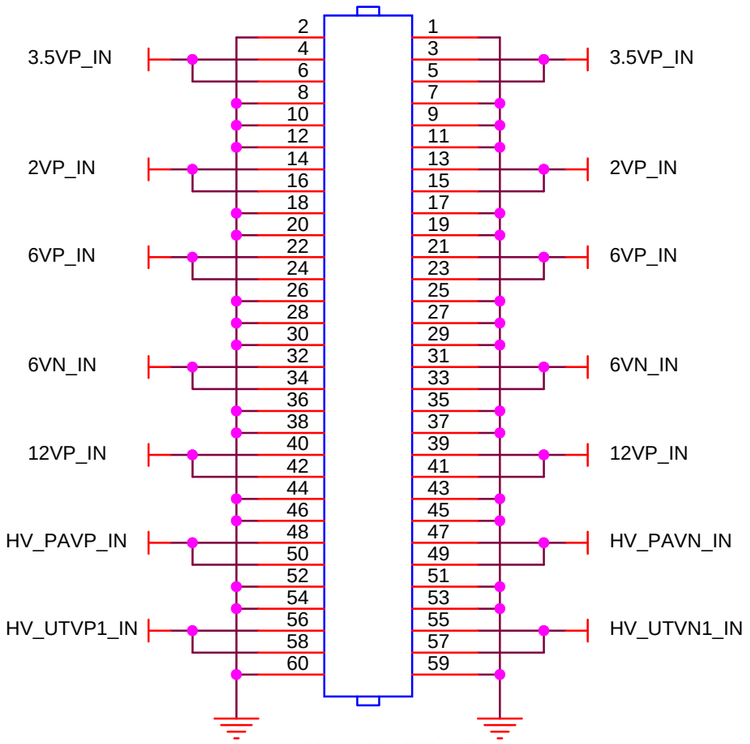
CW_PWR_CTRL[0:3]
THV_CW+
THV_CW-

87 POWER_CONTROL

POWER_FPGA

95 POWER_FPGA

J?

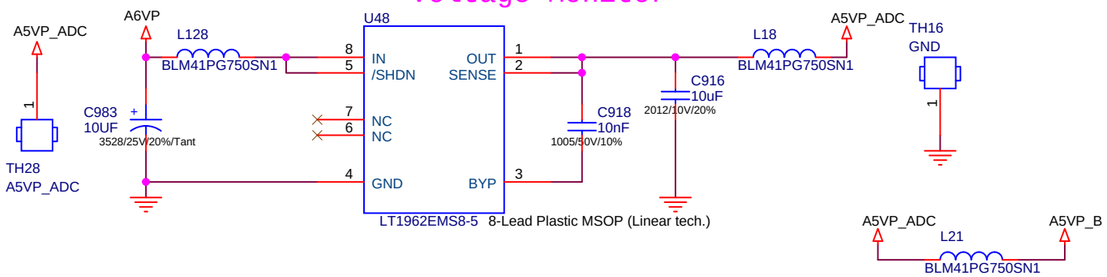


8911-060-178S-A-F

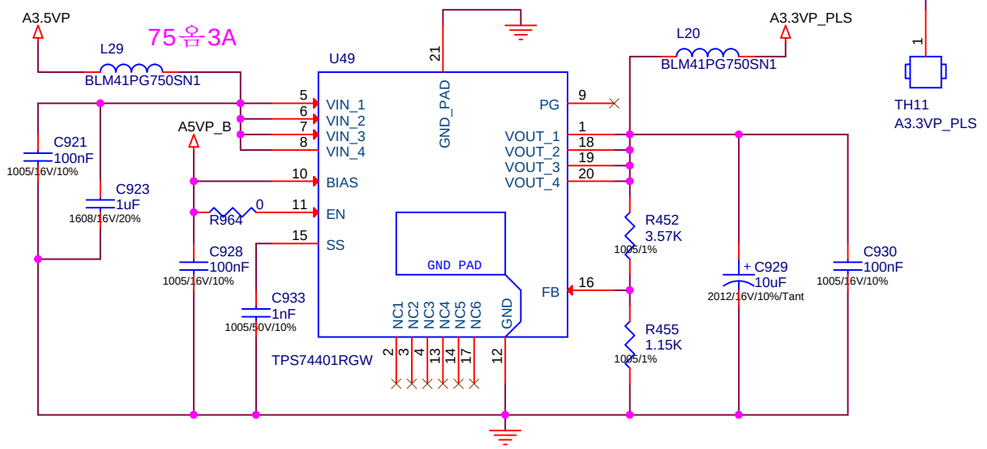
Title: ATTO FE BOARD_POWER		
Size: A4	Document Number: 2015060001	Rev: MP
Date: Friday, September 22, 2017	Sheet 1 of 1	

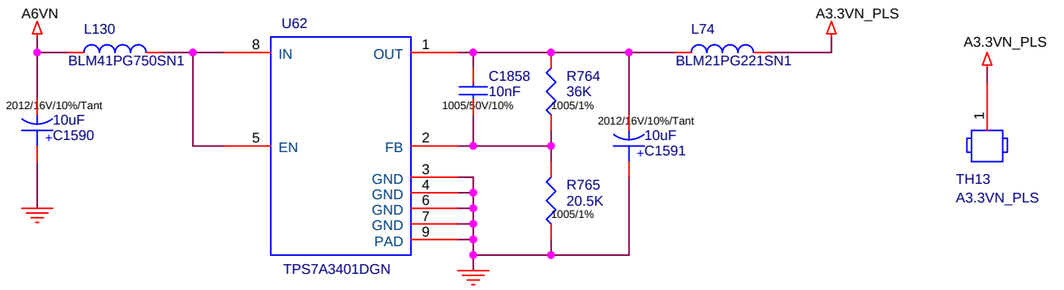
A12VP → A6VP

Voltage Monitor



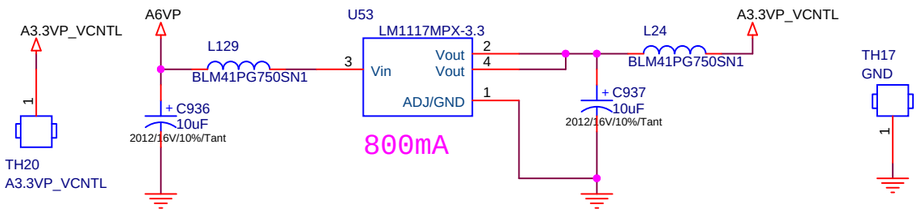
Support Power for Pulser 0 ~ 15 CHIP

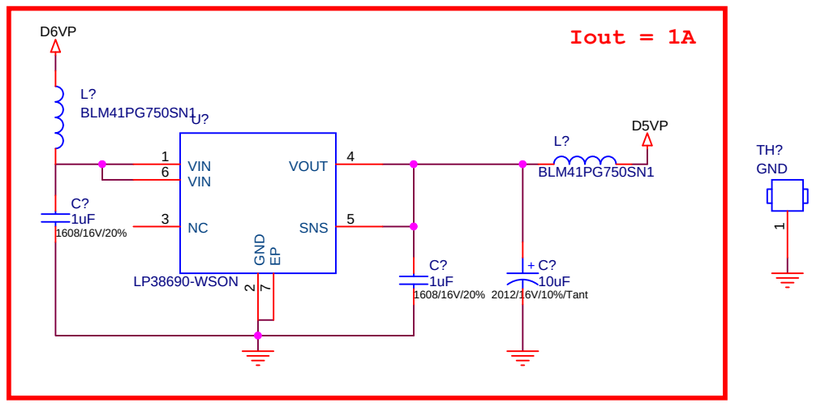




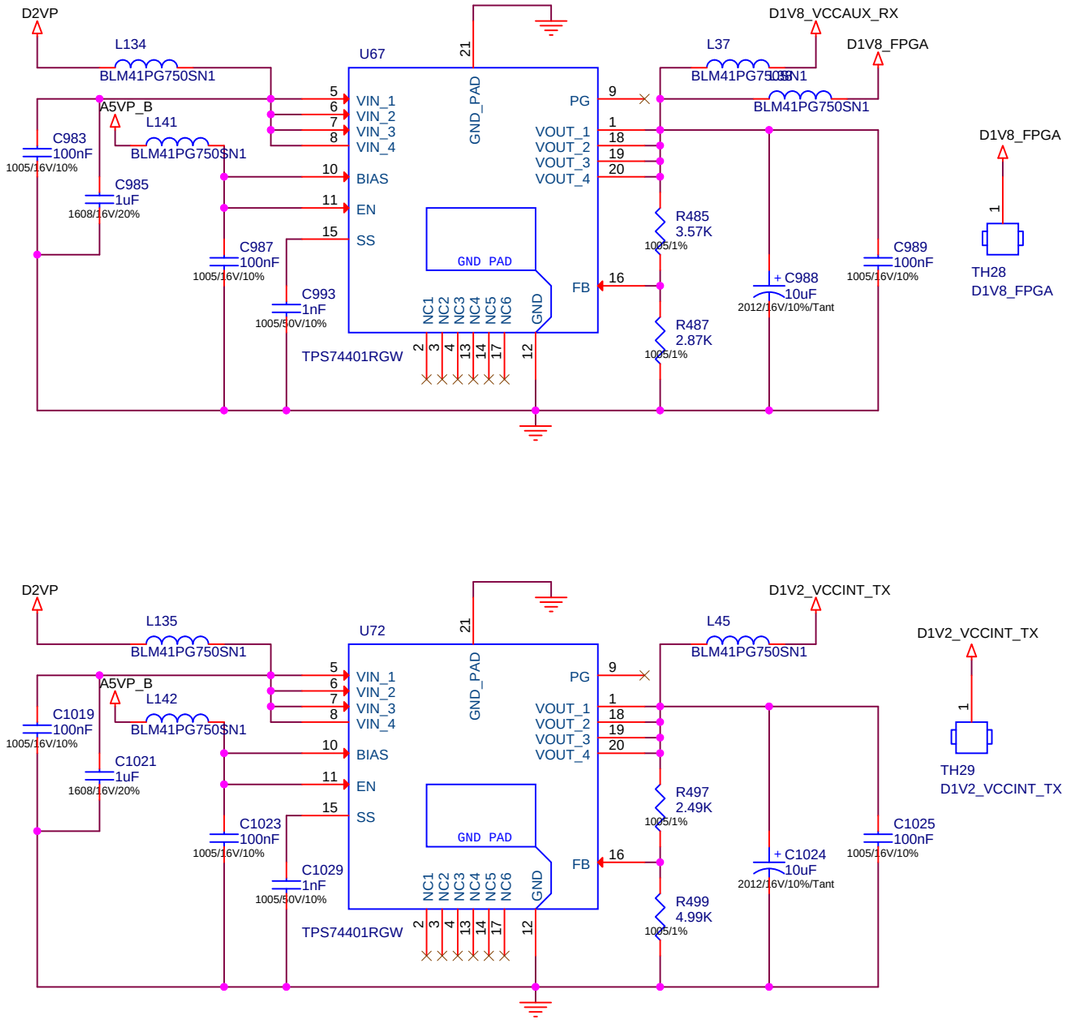
A5VP → A6VP

Support Power for ATGC Module





Title	ATTO FE BOARD_POWER ANALOG	
Size A3	Document Number 2015060001	Rev MP
Date: Friday, September 22, 2017	Sheet 1 of 1	

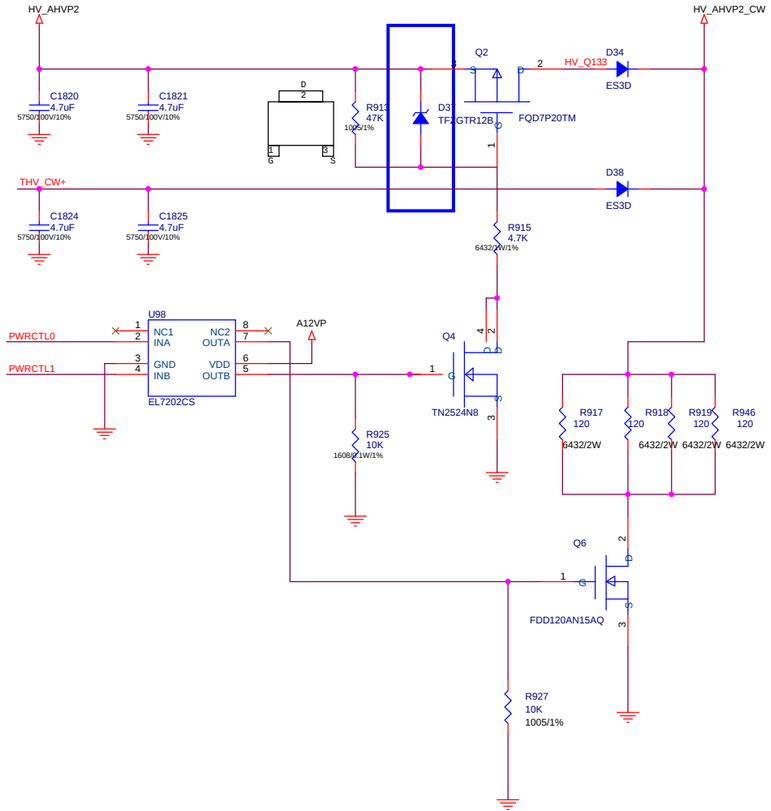


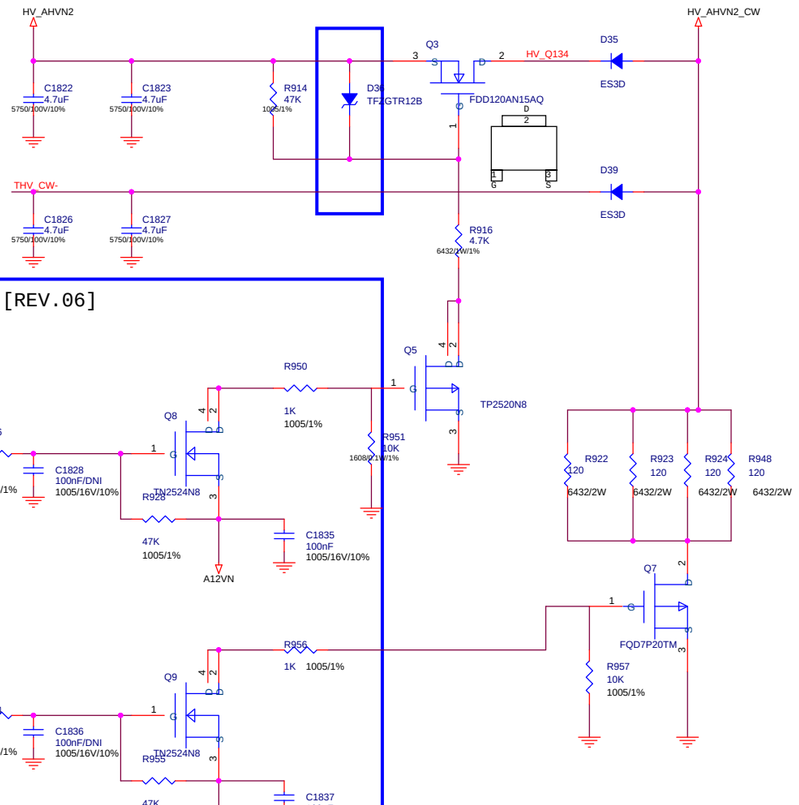
Title	ATTO FE BOARD_POWER FPGA		
Size A3	Document Number 2015060001		Rev MP
Date: Friday, September 22, 2017		Sheet 1 of 1	

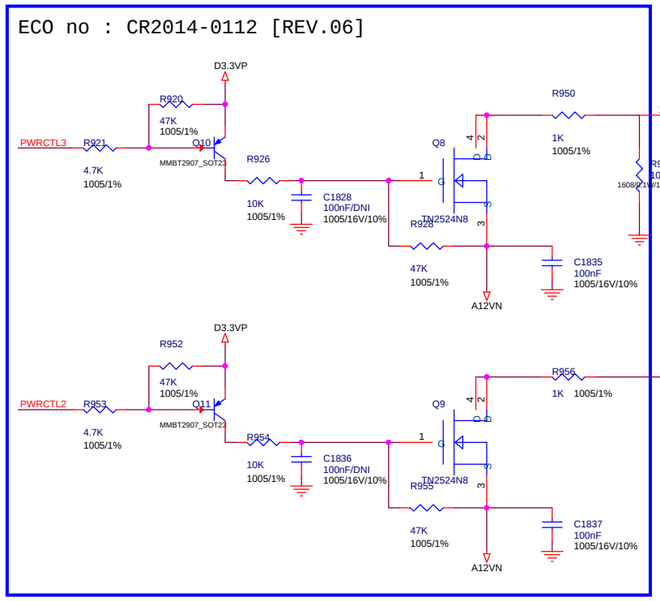
THV_CW+
THV_CW-
CW_PWR_CTRL[0:3]

THV_CW+
THV_CW-
PWRCTL[0:3]

PWRCTL0	PWRCTL1	PWRCTL2	PWRCTL3	Function
0	1	1	0	supply +30/-30V
0	0	1	1	supply CW power
1	0	0	1	+/- High voltage discharge







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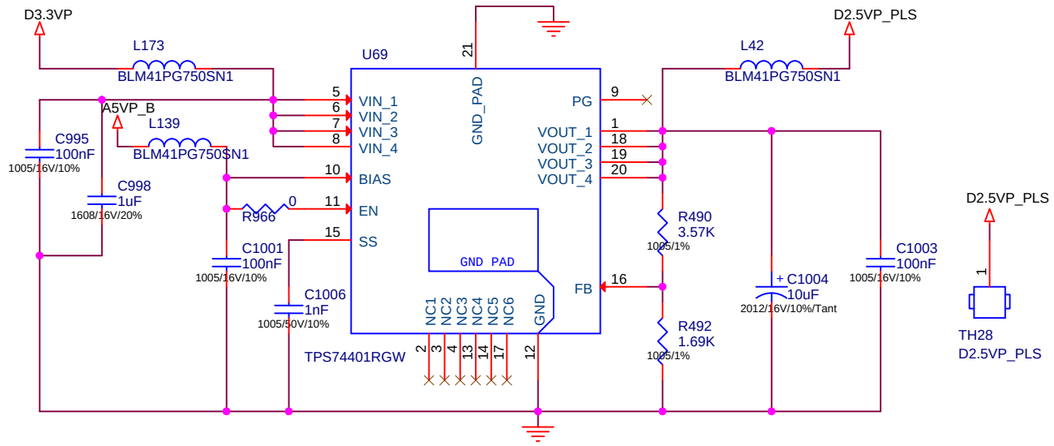
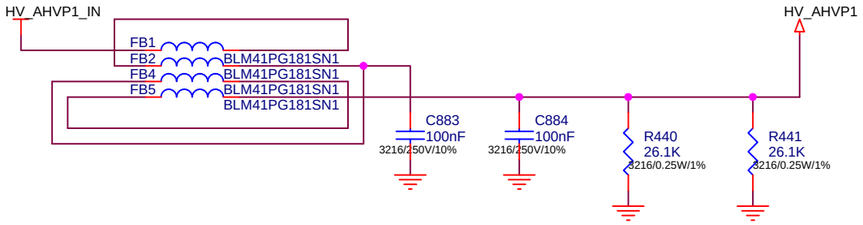
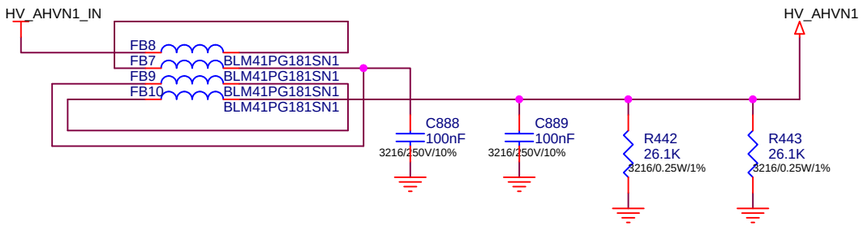
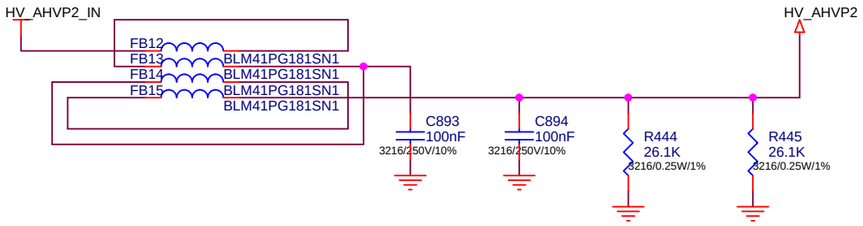
Size A2	Document Number 2015060001	Rev MP
Date: Wednesday, September 20, 2017	Sheet 1 of 1	

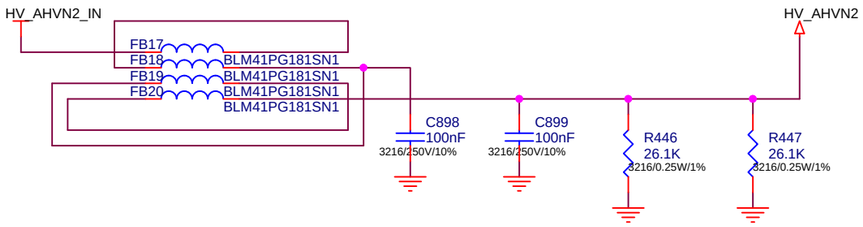


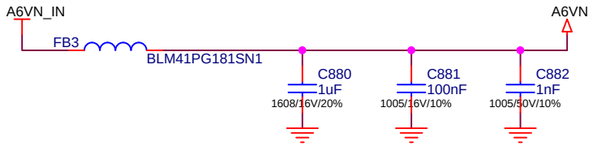
Title: ATTO FE BOARD_POWER DIGITAL		
Size: A3	Document Number: 2015060001	Rev: MP
Date: Friday, September 22, 2017	Sheet 1 of 1	

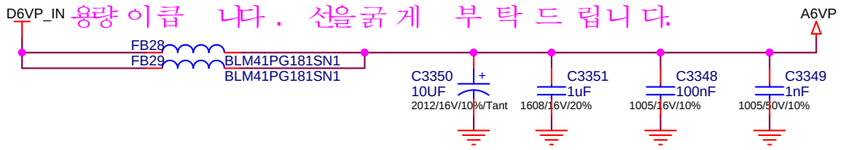


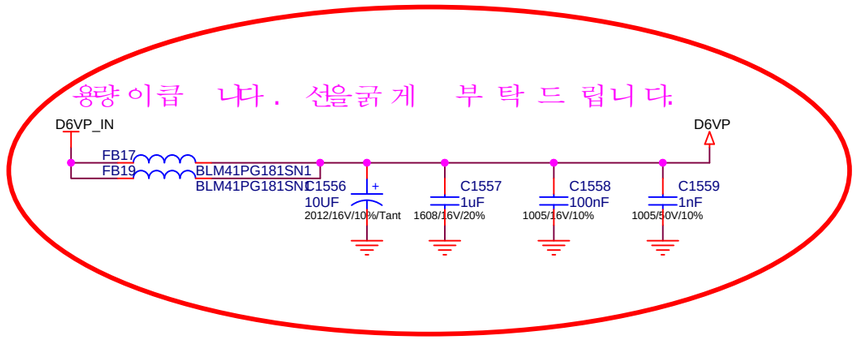


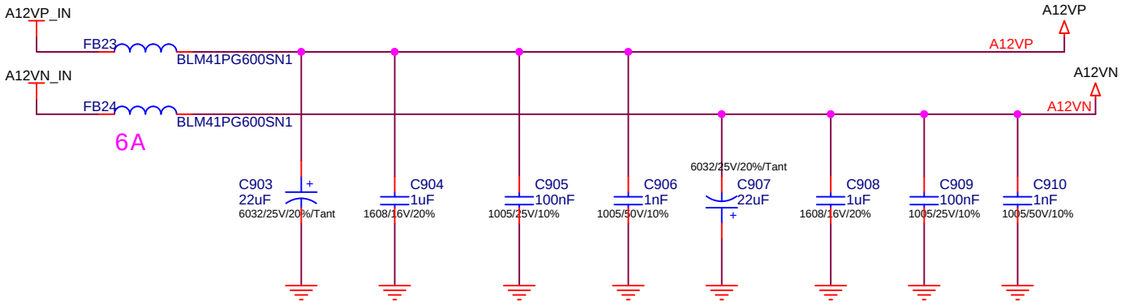


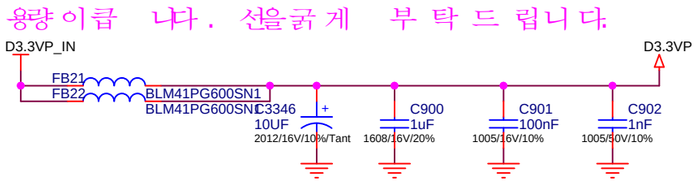


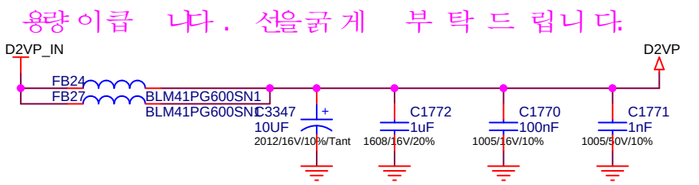


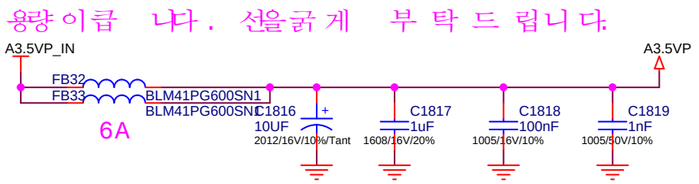


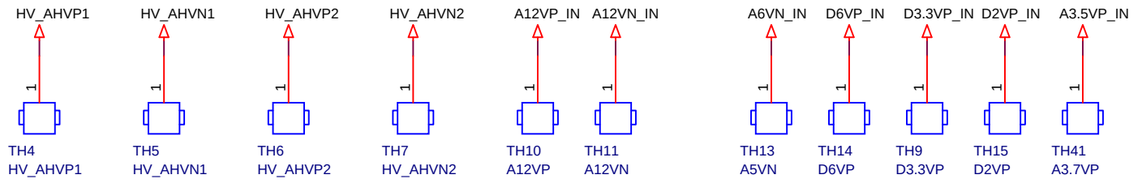


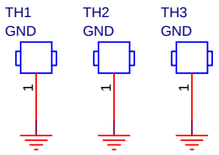






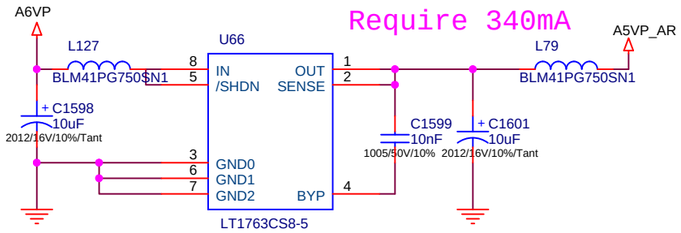


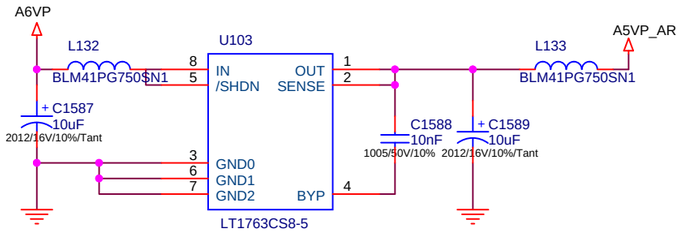


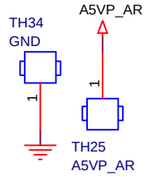


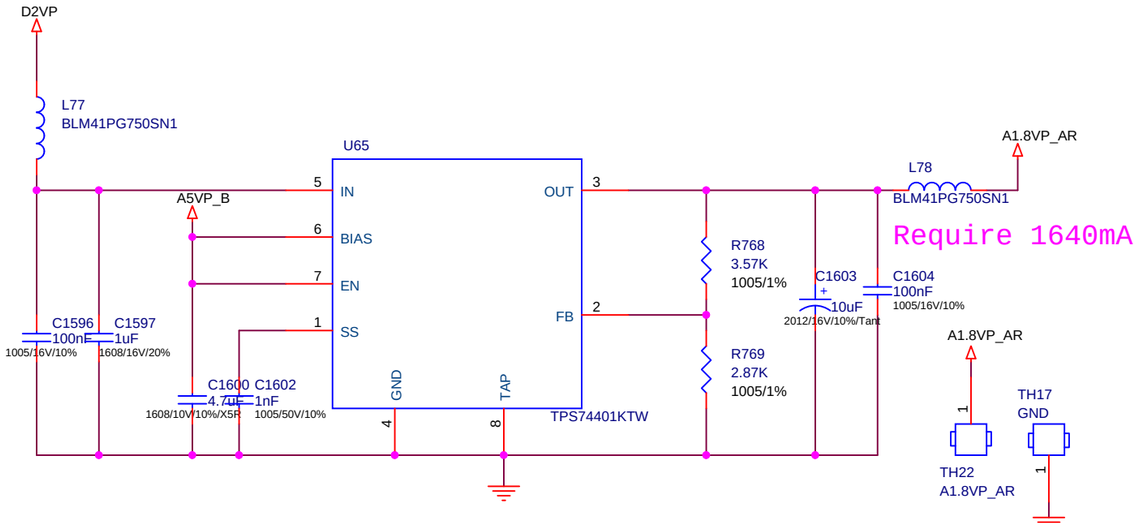
Title: ATTO FE BOARD_POWER FILTER		
Size: A3	Document Number: 2015060001	Rev: MP
Date: Friday, September 22, 2017	Sheet 1 of 1	

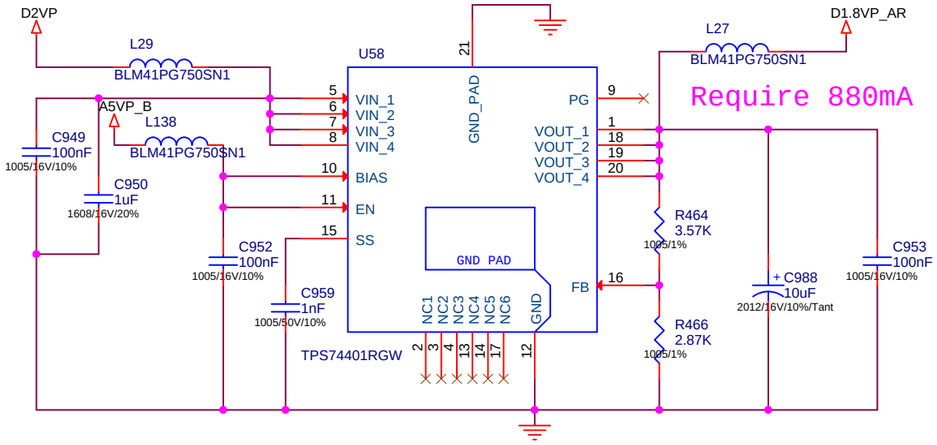
A12VP → A6VP

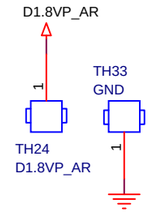


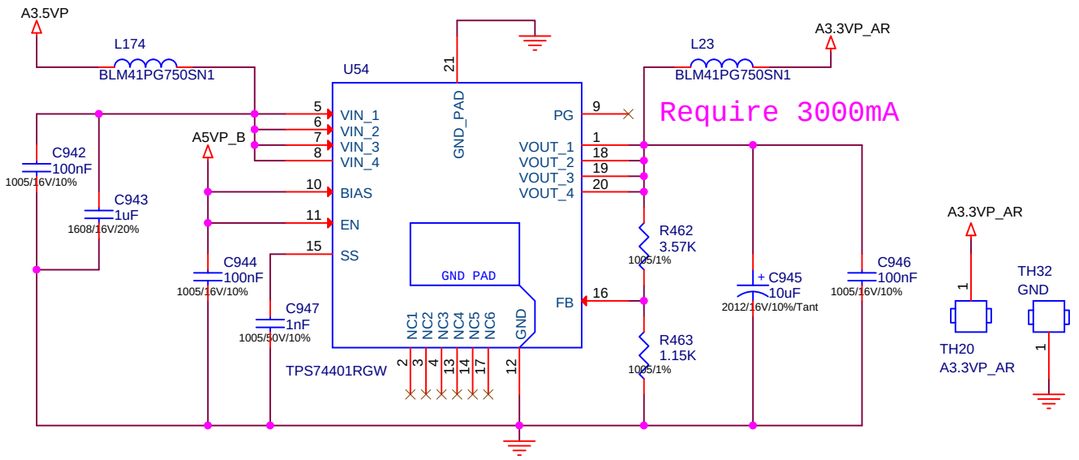












Title	ATTO FE BOARD_AFE5808	
Size A3	Document Number 2015060001	Rev MP
Date: Friday, September 22, 2017	Sheet 1 of 1	

CW_IP_OUTP
CW_IP_OUTM
CW_QP_OUTP
CW_QP_OUTM

CW_AD_CLK
CW_AD_SYNC

CW_I_DATA
CW_I_FSO
CW_I_SCLK

CW_Q_DATA

CW_SUMMING

CW_IP_OUTP
CW_IP_OUTM
CW_QP_OUTP
CW_QP_OUTM

CW_I_OUTP
CW_I_OUTM
CW_Q_OUTP
CW_Q_OUTM

SCW_ISUM
SCW_QSUM

SCW_ISUM
SCW_QSUM

51 CW_SUMMING

CW_ADC DRIVER

SCW_ISUM
SCW_QSUM
CTL_150HZ_HPF_SEL
CTL_150HZ_HPF_SEL

SCW_ISUM
SCW_QSUM
CTL_150HZ_HPF_SEL
CTL_400HZ_HPF_SEL

CW_I_ADINP
CW_I_ADINN
CW_Q_ADINP
CW_Q_ADINN

CW_I_ADINP
CW_I_ADINN
CW_Q_ADINP
CW_Q_ADINN

52 CW_ADC DRIVER

CW_ADC I

CW_I_ADINP
CW_I_ADINN
CW_AD_CLK
CW_AD_SYNC

CW_I_ADINP
CW_I_ADINN
CW_AD_CLK
CW_AD_SYNC

CW_I_DATA
CW_I_FSO
CW_I_SCLK

CW_I_DATA
CW_I_FSO
CW_I_SCLK

53-0 CW_ADC I

CW_ADC Q

CW_Q_ADINP
CW_Q_ADINN
CW_AD_CLK
CW_AD_SYNC

CW_Q_ADINP
CW_Q_ADINN
CW_AD_CLK
CW_AD_SYNC

CW_Q_DATA
CW_Q_FSO
CW_Q_SCLK

CW_Q_DATA

53-1 CW_ADC Q

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, September 22, 2017	Sheet 1 of 1	

CW_I_OUTP
CW_I_OUTM
CW_Q_OUTP
CW_Q_OUTM

amplifier

A5VP_CW
R1032 0 1005/1%
U1
CW_I_OUTP R1028 0 1005/1% 8 Vin+
Vocm 2 Vocm
CW_I_OUTM R1029 0 1005/1% 1 Vin-
NC 7
Vcc+ 3
Vout- 5 CW_I_AMP_OUTM
Vout+ 4 CW_I_AMP_OUTP
EPG 9
Vcc- 6
THS4131CDGNR
R1033 0 1005/1%
A5VN_CW

A5VP_CW
R1036 0 1005/1%
U112
CW_Q_OUTP R1034 0 1005/1% 8 Vin+
Vocm 2 Vocm
CW_Q_OUTM R1035 0 1005/1% 1 Vin-
NC 7
Vcc+ 3
Vout- 5 CW_Q_AMP_OUTM
Vout+ 4 CW_Q_AMP_OUTP
EPG 9
Vcc- 6
THS4131CDGNR
R1037 0 1005/1%
A5VN_CW

A5VP_CW
R1031 10K 1005/1%
Vocm
C1893 100nF 2012/16V/10%
R1030 10K 1005/1%
A5VN_CW

Summing

SCW_ISUM
SCW_QSUM

A5VP_CW
R1027 0 1005/1%
R1022 499 1005/1%
C1882 3.3nF 2012/16V/10%
C1883 1uF 2012/50V/5%/X7R
C1884 100nF 2012/50V/5%/X7R
CW_AMP_OUTM C1894 1uF 2012/50V/5%/X7R R1014 0 1005/1%
CW_AMP_OUTP C1895 1uF 2012/50V/5%/X7R R1015 0 1005/1%
U110A OPA2614D
C1888 100nF 2012/50V/5%/X7R
C1889 1uF 2012/50V/5%/X7R
A5VN_CW
R1026 499 1005/1%
C1891 3.3nF 2012/16V/10%
R1024 49.9 1005/1%
C1887 4.7uF 2012/50V/5%/X7R
TP30 SUMI_IV_0
C1890 150pF 1005/50V/10%/X5R
SCW_ISUM

A5VP_CW
R1042 0 1005/1%
R1038 499 1005/1%
C1901 3.3nF 2012/16V/10%
C1896 1uF 2012/50V/5%/X7R
C1898 100nF 2012/50V/5%/X7R
CW_I_OUTM_INT C1904 1uF 2012/50V/5%/X7R R1040 0 1005/1%
CW_I_OUTP_INT C1905 1uF 2012/50V/5%/X7R R1041 0 1005/1%
U110B OPA2614D
C1899 100nF 2012/50V/5%/X7R
C1900 1uF 2012/50V/5%/X7R
A5VN_CW
R1039 499 1005/1%
C1902 3.3nF 2012/16V/10%
R1043 49.9 1005/1%
C1903 4.7uF 2012/50V/5%/X7R
TP31 CW_SE_QP
C1897 150pF 1005/50V/10%/X5R
SCW_QSUM

Title	<Title>	
Size Custom	Document Number <Doc>	Rev <RevCo
Date: Wednesday, September 20, 2017	Sheet 1 of 1	

LVOUT_CH[0:15]

CLK_M
CLK_P
CLKM_1X
CLKP_1X
CLKM_16X
CLKP_16X

ADC_SCLK
ADC_SDATA
ADC_SEN

TGC_UP_DN
TGC_SLOPE

TX_TRIG
RESET
PDN_CLOBAL

ADC_OUT_P[0:15]
ADC_OUT_N[0:15]
ADC_SDOUT

CW_IP_OUTP
CW_IP_OUTM
CW_QP_OUTP
CW_QP_OUTM

FCLKM
FCLKP
DCLKM
DCLKP

U6-1

LVOUT_CH0	C578 100nF	C579 15nF	A17 C17	INP1 INM1	DOUTP1 DOUTM1	R16 T16	ADC_OUT_P0 ADC_OUT_N0
LVOUT_CH1	C580 100nF	C581 15nF	A16 C16	INP2 INM2	DOUTP2 DOUTM2	R15 T15	ADC_OUT_P1 ADC_OUT_N1
LVOUT_CH2	C582 100nF	C583 15nF	A15 C15	INP3 INM3	DOUTP3 DOUTM3	R14 T14	ADC_OUT_P2 ADC_OUT_N2
LVOUT_CH3	C584 100nF	C585 15nF	A14 C14	INP4 INM4	DOUTP4 DOUTM4	T13 U13	ADC_OUT_P3 ADC_OUT_N3
LVOUT_CH4	C586 100nF	C587 15nF	A13 C13	INP5 INM5	DOUTP5 DOUTM5	T12 U12	ADC_OUT_P4 ADC_OUT_N4
LVOUT_CH5	C588 100nF	C589 15nF	A12 C12	INP6 INM6	DOUTP6 DOUTM6	R12 R11	ADC_OUT_P5 ADC_OUT_N5
LVOUT_CH6	C590 100nF	C591 15nF	A11 C11	INP7 INM7	DOUTP7 DOUTM7	T11 U11	ADC_OUT_P6 ADC_OUT_N6
LVOUT_CH7	C592 100nF	C593 15nF	A10 C10	INP8 INM8	DOUTP8 DOUTM8	T10 U10	ADC_OUT_P7 ADC_OUT_N7
LVOUT_CH8	C594 100nF	C595 15nF	A8 C8	INP9 INM9	DOUTP9 DOUTM9	T8 U8	ADC_OUT_P8 ADC_OUT_N8
LVOUT_CH9	C597 100nF	C596 15nF	A7 C7	INP10 INM10	DOUTP10 DOUTM10	T7 U7	ADC_OUT_P9 ADC_OUT_N9
LVOUT_CH10	C599 100nF	C598 15nF	A6 C6	INP11 INM11	DOUTP11 DOUTM11	R7 R6	ADC_OUT_P10 ADC_OUT_N10
LVOUT_CH11	C600 100nF	C601 15nF	A5 C5	INP12 INM12	DOUTP12 DOUTM12	T6 U6	ADC_OUT_P11 ADC_OUT_N11
LVOUT_CH12	C602 100nF	C603 15nF	A4 C4	INP13 INM13	DOUTP13 DOUTM13	T5 U5	ADC_OUT_P12 ADC_OUT_N12
LVOUT_CH13	C605 100nF	C604 15nF	A3 C3	INP14 INM14	DOUTP14 DOUTM14	R4 T4	ADC_OUT_P13 ADC_OUT_N13
LVOUT_CH14	C607 100nF	C606 15nF	A2 C2	INP15 INM15	DOUTP15 DOUTM15	R3 T3	ADC_OUT_P14 ADC_OUT_N14
LVOUT_CH15	C608 100nF	C609 15nF	A1 C1	INP16 INM16	DOUTP16 DOUTM16	R2 T2	ADC_OUT_P15 ADC_OUT_N15

AFE5816

D1V8P_AFE
R81 0 1005/1%

U6-2

FCLKP	R10	CW_IP_AMPINP	D4 CW_IP_OUTP
FCLKM	R8	CW_IP_AMPINM	D3 CW_IP_OUTM
PDN_CLOBAL	M17 M16	CW_QP_AMPINP	G4 CW_QP_OUTP
		CW_QP_AMPINM	G3 CW_QP_OUTM
ADC_SCLK	J17		
ADC_SDATA	L16		
ADC_SDOUT	H16		
ADC_SEN	K17 K16		
	L1 L2 M1 M2		
R82 0 1005/1% R83 0 1005/1%	J5 H5		
TGC_UP_DN	J4		
TGC_SLOPE	H4		
	J1 J2		
DCLKM	U9		
DCLKP	T9		
TX_TRIG	M15		
RESET	L17		
C617 1uF C622 100nF C623 100nF C624 100nF C625 100nF	D5 G5 F5 K14 D14		

CML8_OUTM U4, CML7_OUTM U2, CML6_OUTM T1, CML5_OUTM P1, CML4_OUTM U14, CML3_OUTM U16, CML2_OUTM T17, CML1_OUTM P17

CML8_OUTP U3, CML7_OUTP U1, CML6_OUTP R1, CML5_OUTP N1, CML4_OUTP U15, CML3_OUTP U17, CML2_OUTP R17, CML1_OUTP N17

CLKP_1X G17, CLKM_1X G16, CLKP_16X E16, CLKM_16X E17

C613 100nF 1005/25V/10% CLKP_1X R? 100 1005/1%
C614 100nF 1005/25V/10% CLKM_1X 1005/1%
C615 100nF 1005/25V/10% CLKP_16X R? 100 1005/1%
C616 100nF 1005/25V/10% CLKM_16X 1005/1%

TR_EN-1 K15, TR_EN-2 J16, TR_EN-3 H15, TR_EN-4 J15

BIAS_2P5, BAND_GAP, LNA_INCM, VREF_IN_REXT, SRC_BIAS

LVDS
R? 100 1005/1% AFE_CLKP AFE_CLKM C611 100nF 1005/25V/10% C612 100nF 1005/25V/10%

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U6-3

AVDD_3P3-7	D12	AVDD_1P8-6	L13
AVDD_3P3-6	D11	AVDD_1P8-5	L12
AVDD_3P3-5	D10	AVDD_1P8-4	L11
AVDD_3P3-4	D9	AVDD_1P8-3	L7
AVDD_3P3-3	D8	AVDD_1P8-2	L6
AVDD_3P3-2	D7	AVDD_1P8-1	L5
AVDD_3P3-1	D6		
		DVDD_1P2-1	N12
		DVDD_1P2-2	N13
		DVDD_1P2-3	N14
		DVDD_1P2-4	N15
		DVDD_1P2-5	N16
AVDD_1P9-1	E6	DVDD_1P2-6	M4
AVDD_1P9-2	E7	DVDD_1P2-7	M5
AVDD_1P9-3	E11	DVDD_1P2-8	N2
AVDD_1P9-4	E12	DVDD_1P2-9	N3
AVDD_1P9-5	E13	DVDD_1P2-10	N4
AVDD_1P9-6	E14	DVDD_1P2-11	N5
AVDD_1P9-7	F11	DVDD_1P2-12	N6
AVDD_1P9-8	F12	DVDD_1P2-13	P15
AVDD_1P9-9	F13	DVDD_1P2-14	P16
AVDD_1P9-10	F14	DVDD_1P2-15	P2
AVDD_1P9-11	F6	DVDD_1P2-16	P3
AVDD_1P9-12	F7	DVDD_1P2-17	L3
AVDD_1P9-13	G11	DVDD_1P2-18	M12
AVDD_1P9-14	G12	DVDD_1P2-19	M13
AVDD_1P9-15	G6	DVDD_1P2-20	M14
AVDD_1P9-16	G7	DVDD_1P2-21	M6
AVDD_1P9-17	H11		
AVDD_1P9-18	H12		
AVDD_1P9-19	H6		
AVDD_1P9-20	H7		
AVDD_1P9-21	J11	DVDD1P8-1	P4
AVDD_1P9-22	J12	DVDD1P8-2	P5
AVDD_1P9-23	J6	DVDD1P8-3	P6
AVDD_1P9-24	J7	DVDD1P8-4	P7
AVDD_1P9-25	K11	DVDD1P8-5	P11
AVDD_1P9-26	K12	DVDD1P8-6	P12
AVDD_1P9-27	K6	DVDD1P8-7	P13
AVDD_1P9-28	K7	DVDD1P8-8	P14

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U6-5

AVSS-1	D15	AVSS-19	H2
AVSS-2	D16	AVSS-20	H3
AVSS-3	D17	AVSS-21	H8
AVSS-4	E8	AVSS-22	H9
AVSS-5	E9	AVSS-23	H10
AVSS-6	E10	AVSS-24	J3
AVSS-7	E15	AVSS-25	J8
AVSS-8	F8	AVSS-26	J9
AVSS-9	F9	AVSS-27	J10
AVSS-10	F10	AVSS-28	K1
AVSS-11	F15	AVSS-29	K2
AVSS-12	F16	AVSS-30	K3
AVSS-13	F17	AVSS-31	K8
AVSS-14	G8	AVSS-32	K9
AVSS-15	G9	AVSS-33	K10
AVSS-16	G10	AVSS-34	L8
AVSS-17	G15	AVSS-35	L9
AVSS-18	H1	AVSS-36	L10
DVSS-1	M3	DVSS-8	N8
DVSS-2	M7	DVSS-9	N9
DVSS-3	M8	DVSS-10	N10
DVSS-4	M9	DVSS-11	N11
DVSS-5	M10	DVSS-12	P8
DVSS-6	M11	DVSS-13	P9
DVSS-7	N7	DVSS-14	P10

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U6-4

NC-1	B1	NC-25	E3
NC-2	B2	NC-31	F4
NC-3	B3	NC-30	F3
NC-4	B4	NC-29	F2
NC-5	B5	NC-28	F1
NC-6	B6	NC-27	E5
NC-7	B7	NC-32	G1
NC-8	B8	NC-33	G2
NC-9	B9	NC-34	G13
NC-10	B10	NC-35	G14
NC-11	B11	NC-36	H13
NC-12	B12	NC-37	H14
NC-13	B13	NC-38	H17
NC-14	B14	NC-39	J13
NC-15	B15	NC-40	J14
NC-16	B16	NC-41	K4
NC-17	B17	NC-42	K5
NC-18	A9	NC-43	K13
NC-19	C9	NC-44	L4
NC-20	D1	NC-45	L14
NC-21	D2	NC-46	L15
NC-22	D13	NC-47	R5
NC-23	E1	NC-48	R9
NC-24	E2	NC-49	R13
NC-26	E4		

AFE5816

A3V3P_AFE
A1V8P_AFE
A1V9P_AFE
A1V9P_AFE
A1V9P_AFE
D1V2P_AFE
D1V2P_AFE
D1V8P_AR

C626 10uF 2012/0805/X5R/6.3V/20% C? 100nF 1005/16V/10%
C481 10uF 2012/0805/X5R/6.3V/20% C? 100nF 1005/16V/10%
C627 10uF 2012/0805/X5R/6.3V/20% C? 100nF 1005/16V/10%
C? 100nF 1005/16V/10%
C? 100nF 1005/16V/10%
C628 10uF 2012/0805/X5R/6.3V/20% C? 100nF 1005/16V/10%
C? 100nF 1005/16V/10%
C629 10uF 2012/0805/X5R/6.3V/20% C? 100nF 1005/16V/10%

D1V8P_AR
A1V8P_AR

Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Thursday, September 21, 2017	Sheet 3 of 10		

FPGA_CLKP
FPGA_CLKM
ADC_OUT_P[0:15]
ADC_OUT_N[0:15]
ADC_SDOUT
FCLKP
FCLKM
DCLKP
DCLKM
TR_CH_D[0:15]
PLS_TX_ON
PLS_DATAOUT
PLS_INT

CLKP_1X
CLKM_1X
CLKP_16X
CLKM_16X
ADC_SCLK
ADC_SDATA
ADC_SEN
TGC_UP_DN
TGC_SLOPE
TX_TRIG
AFE_RESET
PDN_CLOBAL

PLS_DATA_P[0:15]
PLS_DATA_N[0:15]
PLS_SYS_CLKP
PLS_SYS_CLKN
PLS_CLKP
PLS_CLKN
PLS_ENABLE_P
PLS_ENABLE_N
PLS_TRIGER_P
PLS_TRIGER_N
PLS_/RESET

U1-2

K24 VCCO_13
N25 VCCO_13
P22 VCCO_13
R19 VCCO_13
T16 VCCO_13
T26 VCCO_13
D2.5V_FPGA

IO_0_13 N16
IO_25_13 U16
IO_L1P_T0_13 K25
IO_L1N_T0_13 K26
IO_L2P_T0_13 R26
IO_L2N_T0_13 P26
IO_L3P_T0_DQS_13 M25
IO_L3N_T0_DQS_13 L25
IO_L4P_T0_13 P24
IO_L4N_T0_13 N24
IO_L5P_T0_13 N26
IO_L5N_T0_13 M26
IO_L6P_T0_13 R25
IO_L6N_T0_VREF_13 P25
IO_L7P_T1_13 N19
IO_L7N_T1_13 M20
IO_L8P_T1_13 M24
IO_L8N_T1_13 L24
IO_L9P_T1_DQS_13 P19
IO_L9N_T1_DQS_13 P20
IO_L10P_T1_13 M21
IO_L10N_T1_13 M22
IO_L11P_T1_SRCC_13 P23
IO_L11N_T1_SRCC_13 N23
IO_L12P_T1_MRCC_13 N21 CLKP_1X
IO_L12N_T1_MRCC_13 N22 CLKM_1X
IO_L13P_T2_MRCC_13 R21 CLKP_16X
IO_L13N_T2_MRCC_13 P21 CLKM_16X
IO_L14P_T2_SRCC_13 R22
IO_L14N_T2_SRCC_13 R23
IO_L15P_T2_DQS_13 T24
IO_L15N_T2_DQS_13 T25
IO_L16P_T2_13 T20
IO_L16N_T2_13 R20
IO_L17P_T2_13 T22
IO_L17N_T2_13 T23
IO_L18P_T2_13 U19
IO_L18N_T2_13 U20
IO_L19P_T3_13 T18
IO_L19N_T3_VREF_13 T19
IO_L20P_T3_13 P16
IO_L20N_T3_13 N17
IO_L21P_T3_DQS_13 R16
IO_L21N_T3_DQS_13 R17
IO_L22P_T3_13 N18
IO_L22N_T3_13 M19
IO_L23P_T3_13 U17
IO_L23N_T3_13 T17
IO_L24P_T3_13 R18
IO_L24N_T3_13 P18

BANK13
XC7K70T-FB(G)676

U2-5

H10 VCCO_16
G13 VCCO_16
E9 VCCO_16
D12 VCCO_16
C15 VCCO_16
B8 VCCO_16
A11 VCCO_16
D2.5V_FPGA

IO_0_16 J8
IO_25_16 J14
IO_L1P_T0_16 H9
IO_L1N_T0_16 H8
IO_L2P_T0_16 G10
IO_L2N_T0_16 G9
IO_L3P_T0_DQS_16 J13
IO_L3N_T0_DQS_16 H13
IO_L4P_T0_16 J11
IO_L4N_T0_16 J10
IO_L5P_T0_16 H14
IO_L5N_T0_16 G14
IO_L6P_T0_16 H12
IO_L6N_T0_VREF_16 H11
IO_L7P_T1_16 F9
IO_L7N_T1_16 F8
IO_L8P_T1_16 D9
IO_L8N_T1_16 D8
IO_L9P_T1_DQS_16 A9
IO_L9N_T1_DQS_16 A8
IO_L10P_T1_16 C9
IO_L10N_T1_16 B9
IO_L11P_T1_SRCC_16 G11
IO_L11N_T1_SRCC_16 F10
IO_L12P_T1_MRCC_16 E10 FPGA_CLK_P
IO_L12N_T1_MRCC_16 D10 FPGA_CLK_N
IO_L13P_T2_MRCC_16 C12 CLK_RSV_P2
IO_L13N_T2_MRCC_16 C11 CLK_RSV_N2
IO_L14P_T2_SRCC_16 E11
IO_L14N_T2_SRCC_16 D11
IO_L15P_T2_DQS_16 F14
IO_L15N_T2_DQS_16 F13
IO_L16P_T2_16 G12
IO_L16N_T2_16 F12
IO_L17P_T2_16 D14
IO_L17N_T2_16 D13
IO_L18P_T2_16 E13
IO_L18N_T2_16 E12
IO_L19P_T3_16 C14
IO_L19N_T3_VREF_16 C13
IO_L20P_T3_16 B12
IO_L20N_T3_16 B11
IO_L21P_T3_DQS_16 B14
IO_L21N_T3_DQS_16 A14
IO_L22P_T3_16 B10
IO_L22N_T3_16 A10
IO_L23P_T3_16 B15
IO_L23N_T3_16 A15
IO_L24P_T3_16 A13
IO_L24N_T3_16 A12

BANK16
XC7K70T-FB(G)676

D2.5V_FPGA
R343 100 1005/1%
R344 100 1005/1%
FPGA_CLKP
FPGA_CLKM
D2.5V_FPGA
R345 100 1005/1%
R346 100 1005/1%

J23 1 PIN HDR
STATUS_LED0
D8 BL-HG036A-AV-TRB
R1377 330 1005/1%
J24 1 PIN HDR
STATUS_LED1
D9 BL-HG036A-AV-TRB
R1378 330 1005/1%
J17 1 PIN HDR
STATUS_LED2
D2 BL-HG036A-AV-TRB
R61 330 1005/1%
J18 1 PIN HDR
STATUS_LED3
D3 BL-HG036A-AV-TRB
R64 330 1005/1%
J19 1 PIN HDR
STATUS_LED4
D4 BL-HG036A-AV-TRB
R65 330 1005/1%

U3-6

W7 VCCO_33
V10 VCCO_33
AE9 VCCO_33
AD12 VCCO_33
AB8 VCCO_33
AA11 VCCO_33
D1.8V_FPGA

IO_0_VRN_33 U9
IO_25_VRP_33 V12
IO_L1P_T0_33 V11 ADC_OUT_P0
IO_L1N_T0_33 W11 ADC_OUT_N0
IO_L2P_T0_33 V8 ADC_OUT_P1
IO_L2N_T0_33 V7 ADC_OUT_N1
IO_L3P_T0_DQS_33 W10 ADC_OUT_P2
IO_L3N_T0_DQS_33 W9 ADC_OUT_N2
IO_L4P_T0_33 Y8 ADC_OUT_P3
IO_L4N_T0_33 Y7 ADC_OUT_N3
IO_L5P_T0_33 Y11 ADC_OUT_P4
IO_L5N_T0_33 Y10 ADC_OUT_N4
IO_L6P_T0_33 V9 ADC_OUT_P5
IO_L6N_T0_VREF_33 W8 ADC_OUT_N5
IO_L7P_T1_33 AE7 ADC_OUT_P6
IO_L7N_T1_33 AF7 ADC_OUT_N6
IO_L8P_T1_33 AA8 ADC_OUT_P7
IO_L8N_T1_33 AA7 ADC_OUT_N7
IO_L9P_T1_DQS_33 AC8 ADC_OUT_P8
IO_L9N_T1_DQS_33 AD8 ADC_OUT_N8
IO_L10P_T1_33 AB7 ADC_OUT_P9
IO_L10N_T1_33 AC7 ADC_OUT_N9
IO_L11P_T1_SRCC_33 AA9 ADC_SDOUT
IO_L11N_T1_SRCC_33 AB9
IO_L12P_T1_MRCC_33 AC9 DCLKP R347 100 1005/1%
IO_L12N_T1_MRCC_33 AD9 DCLKN
IO_L13P_T2_MRCC_33 AB11 FCLKP R348 100 1005/1%
IO_L13N_T2_MRCC_33 AC11 FCLKN
IO_L14P_T2_SRCC_33 AA10
IO_L14N_T2_SRCC_33 AB10
IO_L15P_T2_DQS_33 AB12 ADC_OUT_P10
IO_L15N_T2_DQS_33 AC12 ADC_OUT_N10
IO_L16P_T2_33 AA13 ADC_OUT_P11
IO_L16N_T2_33 AA12 ADC_OUT_N11
IO_L17P_T2_33 AC13 ADC_OUT_P12
IO_L17N_T2_33 AD13 ADC_OUT_N12
IO_L18P_T2_33 Y13 ADC_OUT_P13
IO_L18N_T2_33 Y12 ADC_OUT_N13
IO_L19P_T3_33 AD11 ADC_OUT_P14
IO_L19N_T3_VREF_33 AE11 ADC_OUT_N14
IO_L20P_T3_33 AD10 ADC_OUT_P15
IO_L20N_T3_33 AE10 ADC_OUT_N15
IO_L21P_T3_DQS_33 AE12 ADC_SCLK
IO_L21N_T3_DQS_33 AF12 ADC_SDATA
IO_L22P_T3_33 AE8 ADC_SEN
IO_L22N_T3_33 AF8 TGC_UP_DN
IO_L23P_T3_33 AE13 TGC_SLOPE
IO_L23N_T3_33 AF13 TX_TRIG
IO_L24P_T3_33 AF10 AFE_RESET
IO_L24N_T3_33 AF9 PDN_CLOBAL

BANK33
XC7K70T-FB(G)676

U3-7

Y4 VCCO_34
U3 VCCO_34
AF6 VCCO_34
AD2 VCCO_34
AC5 VCCO_34
AA1 VCCO_34
D1.8V_FPGA

IO_0_VRN_34 U4
IO_25_VRP_34 T7
IO_L1P_T0_34 U6 PLS_DATA_P0
IO_L1N_T0_34 U5 PLS_DATA_N0
IO_L2P_T0_34 U2 PLS_DATA_P1
IO_L2N_T0_34 U1 PLS_DATA_N1
IO_L3P_T0_DQS_34 W6 PLS_DATA_P2
IO_L3N_T0_DQS_34 W5 PLS_DATA_N2
IO_L4P_T0_34 V3 PLS_DATA_P3
IO_L4N_T0_34 W3 PLS_DATA_N3
IO_L5P_T0_34 U7 PLS_DATA_P4
IO_L5N_T0_34 V6 PLS_DATA_N4
IO_L6P_T0_34 V4 PLS_DATA_P5
IO_L6N_T0_VREF_34 W4 PLS_DATA_N5
IO_L7P_T1_34 Y3 PLS_DATA_P6
IO_L7N_T1_34 Y2 PLS_DATA_N6
IO_L8P_T1_34 V2 PLS_DATA_P7
IO_L8N_T1_34 V1 PLS_DATA_N7
IO_L9P_T1_DQS_34 AB1 PLS_DATA_P8
IO_L9N_T1_DQS_34 AC1 PLS_DATA_N8
IO_L10P_T1_34 W1 PLS_DATA_P9
IO_L10N_T1_34 Y1 PLS_DATA_N9
IO_L11P_T1_SRCC_34 AB2
IO_L11N_T1_SRCC_34 AC2
IO_L12P_T1_MRCC_34 AA3 PLS_SYS_CLKP
IO_L12N_T1_MRCC_34 AA2 PLS_SYS_CLKN
IO_L13P_T2_MRCC_34 AA4 PLS_CLKP
IO_L13N_T2_MRCC_34 AB4 PLS_CLKN
IO_L14P_T2_SRCC_34 AC4
IO_L14N_T2_SRCC_34 AC3
IO_L15P_T2_DQS_34 AA5 PLS_DATA_P10
IO_L15N_T2_DQS_34 AB5 PLS_DATA_N10
IO_L16P_T2_34 AB6 PLS_DATA_P11
IO_L16N_T2_34 AC6 PLS_DATA_N11
IO_L17P_T2_34 Y6 PLS_DATA_P12
IO_L17N_T2_34 Y5 PLS_DATA_N12
IO_L18P_T2_34 AD6 PLS_DATA_P13
IO_L18N_T2_34 AD5 PLS_DATA_N13
IO_L19P_T3_34 AD4 PLS_DATA_P14
IO_L19N_T3_VREF_34 AD3 PLS_DATA_N14
IO_L20P_T3_34 AD1 PLS_DATA_P15
IO_L20N_T3_34 AE1 PLS_DATA_N15
IO_L21P_T3_DQS_34 AF5 PLS_TRIGER_P
IO_L21N_T3_DQS_34 AF4 PLS_TRIGER_N
IO_L22P_T3_34 AE3 PLS_ENABLE_P
IO_L22N_T3_34 AE2 PLS_ENABLE_N
IO_L23P_T3_34 AE6 PLS_/RESET
IO_L23N_T3_34 AE5
IO_L24P_T3_34 AF3
IO_L24N_T3_34 AF2

BANK34
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Title: FPGA_ADC
Size: A2
Document Number: 2014110001
Rev: 2.0
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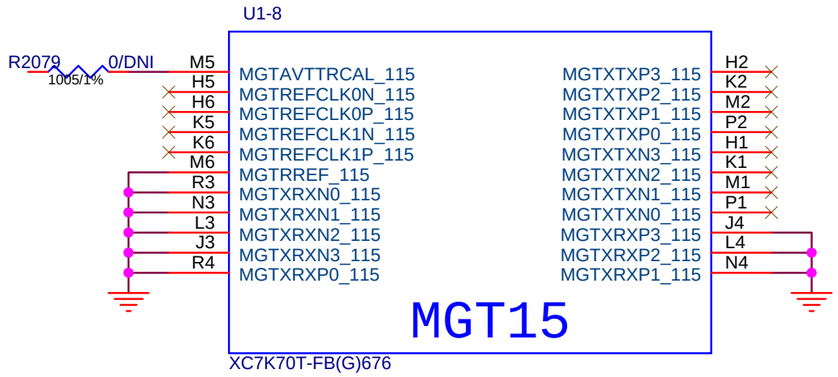

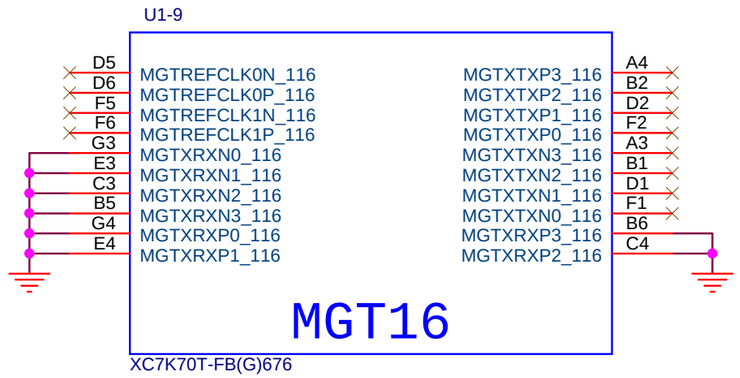

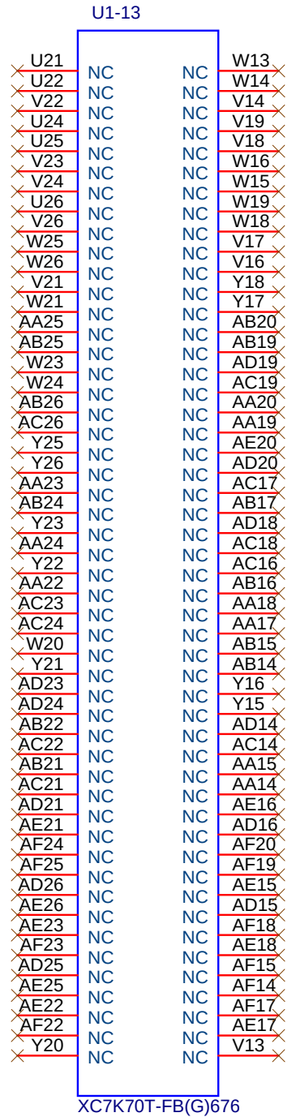

Title: FPGA MGT&NC			
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SCW_ISUM
SCW_QSUM

150Hz HPF

22nF/3216 → 150nF/3225

4.22K → 12.7K

18.2K → 54.9K

SCW_ISUM — R66 0 (1005/1%) — TP17 I_TEST

C84 150nF (3225/16V/2%/X7R) — C88 68NF/DNI (3216/16V/2%/X7R) — R67 9.09K (1005/1%)

U21A AD8674ARZ/AD: A5VP_CW — C81 100nF (1005/16V/10%); A5VN_CW — C91 100nF (1005/16V/10%)

C85 150nF/DNI (3225/16V/2%/X7R) — C86 22nF (3216/50V/2%/X7R) — C90 68nF (3216/16V/2%/X7R)

R72 9.09K (1005/1%) — C93 100pF (3216/25V/5%/NP0) — R74 5.11K (1005/1%)

R85 12.7K (1005/1%) — R89 54.9K (1005/1%)

U15B AD8674ARZ/AD — R71 4.22K (1005/1%) — C92 100pF (3216/25V/5%/NP0)

R68 200 (1005/1%)

400Hz HPF

C95 68nF (3216/16V/2%/X7R) — R77 9.09K (1005/1%)

U17C AD8674ARZ/AD — R78 9.09K (1005/1%) — C101 100pF (3216/25V/5%/NP0) — R83 5.11K (1005/1%)

C97 150nF (3225/16V/2%/X7R) — C100 68NF/DNI (3216/16V/2%/X7R)

C98 22nF (3216/50V/2%/X7R) — R81 21.0K (1005/1%)

U16D AD8674ARZ/AD — R82 4.87K (1003/1%) — C102 100pF (3216/25V/5%/NP0)

R76 4.87K (1003/1%) — R79 200 (1005/1%)

150Hz HPF

value/Size 22nF/3216 → 150nF/3225

4.22K → 12.7K

18.2K → 54.9K

SCW_QSUM — R87 0 (1003/1%) — TP19 Q_TEST

C106 150nF (3225/16V/2%/X7R) — C110 68NF/DNI (3216/16V/2%/X7R) — R88 9.09K (1005/1%)

U22A AD8674/AD: A5VP_CW — C105 100nF (1005/16V/10%); A5VN_CW — C113 100nF (1005/16V/10%)

C107 150nF/DNI (3225/16V/2%/X7R) — C108 22nF (3216/50V/2%/X7R) — C111 68nF (3216/16V/2%/X7R)

R93 9.09K (1005/1%) — C115 100pF (3216/25V/5%/NP0) — R97 5.11K (1005/1%)

R86 12.7K (1005/1%) — R89 54.9K (1005/1%)

U22B AD8674/AD — R92 4.22K (1003/1%) — C114 100pF (3216/25V/5%/NP0)

R90 200 (1005/1%)

400Hz HPF

C121 68nF (3216/16V/2%/X7R) — R99 9.09K (1005/1%)

U22C AD8674/AD — R103 9.09K (1003/1%) — C126 100pF (3216/25V/5%/NP0) — R106 5.11K (1005/1%)

C124 150nF (3225/16V/2%/X7R) — C125 68NF/DNI (3216/16V/2%/X7R)

C122 22nF (3216/50V/2%/X7R) — R102 21.0K (1005/1%)

U22D AD8674/AD — R104 4.87K (1003/1%) — C127 100pF (3216/25V/5%/NP0)

R98 4.87K (1003/1%) — R101 200 (1005/1%)

TP16 Filtered_ISUM — C79 10nF (1005/50V/10%) — R62 200 (1005/1%)

C73 820pF (3216/50V/2%/C0G) — R59 4.02K (1005/1%)

A5VN_CW — C76 +10uF (3528/25V/20%/Tant); C77 100nF (1005/16V/10%)

U14 THS4131CDGN/TI: N_IN, Vocm, P_IN, Vo+, Vo-, V+, V-, PAD, NC

TP15 CW_I_ADP — R61 1K (1005/1%)

R63 24.9 (1005/1%) — C80 390pF (1005/50V/10%/X7R) — CW_I_ADINP

R64 24.9 (1005/1%) — C82 100pF (1005/50V/10%/X5R); C83 100pF (1005/50V/10%/X5R) — CW_I_ADINN

A5VP_CW — C87 +10uF (3528/25V/20%/Tant); C89 100nF (1005/16V/10%)

R70 1K (1005/1%) — TP18 CW_I_ADN

R73 4.02K (1005/1%) — C94 820pF (3216/50V/2%/C0G) — R75 402 (1005/1%)

A5VP_CW — C96 100nF (1005/16V/10%)

U19 ADG1412YRUZ/ADI: VDD, NC, GND, VSS, S1–S4, D1–D4, IN1–IN4

R80 1M (1005/1%) — CTL_150HZ_HPF_SEL — CTL_150HZ_HPF_SEL

C99 100nF (1005/16V/10%)

R84 1M (1005/1%) — CTL_400HZ_HPF_SEL — CTL_400HZ_HPF_SEL

C103 100nF (1005/16V/10%)

INx 1 -> ON & 0 -> OFF

A5VN_CW — C109 100nF (1005/16V/10%)

TP21 Filtered_QSUM — Filtered_QSUM — R94 200 (1005/1%) — C116 10nF (1005/50V/10%)

C104 820pF (3216/50V/2%/C0G) — R85 4.02K (1005/1%)

A5VN_CW — C112 100nF (1005/16V/10%)

TP20 CW_Q_ADP — R91 1K (1005/1%)

U18 THS4131CDGN/TI: N_IN, Vocm, P_IN, Vo+, Vo-, V+, V-, PAD, NC

R95 24.9 (1005/1%) — C117 390pF (1005/50V/10%/X7R) — CW_Q_ADINP

R96 24.9 (1005/1%) — C118 100pF (1005/50V/10%/X5R); C119 100pF (1005/50V/10%/X5R) — CW_Q_ADINN

A5VP_CW — C123 100nF (1005/16V/10%)

R100 1K (1005/1%) — TP23 CW_Q_ADN

R105 4.02K (1005/1%) — C128 820pF (3216/50V/2%/C0G) — R108 402 (1005/1%)

REF_2.5VP — A5VP_CW — C120 100nF (1005/16V/10%)

U20 AD820ARZ/ADI — REF_2.5V — TP22 REF_2.5V

changed net_name at P2

R107 796 (2012/0.1%) — R109 10K/DNI (1005/1%)

Title	fgtg		
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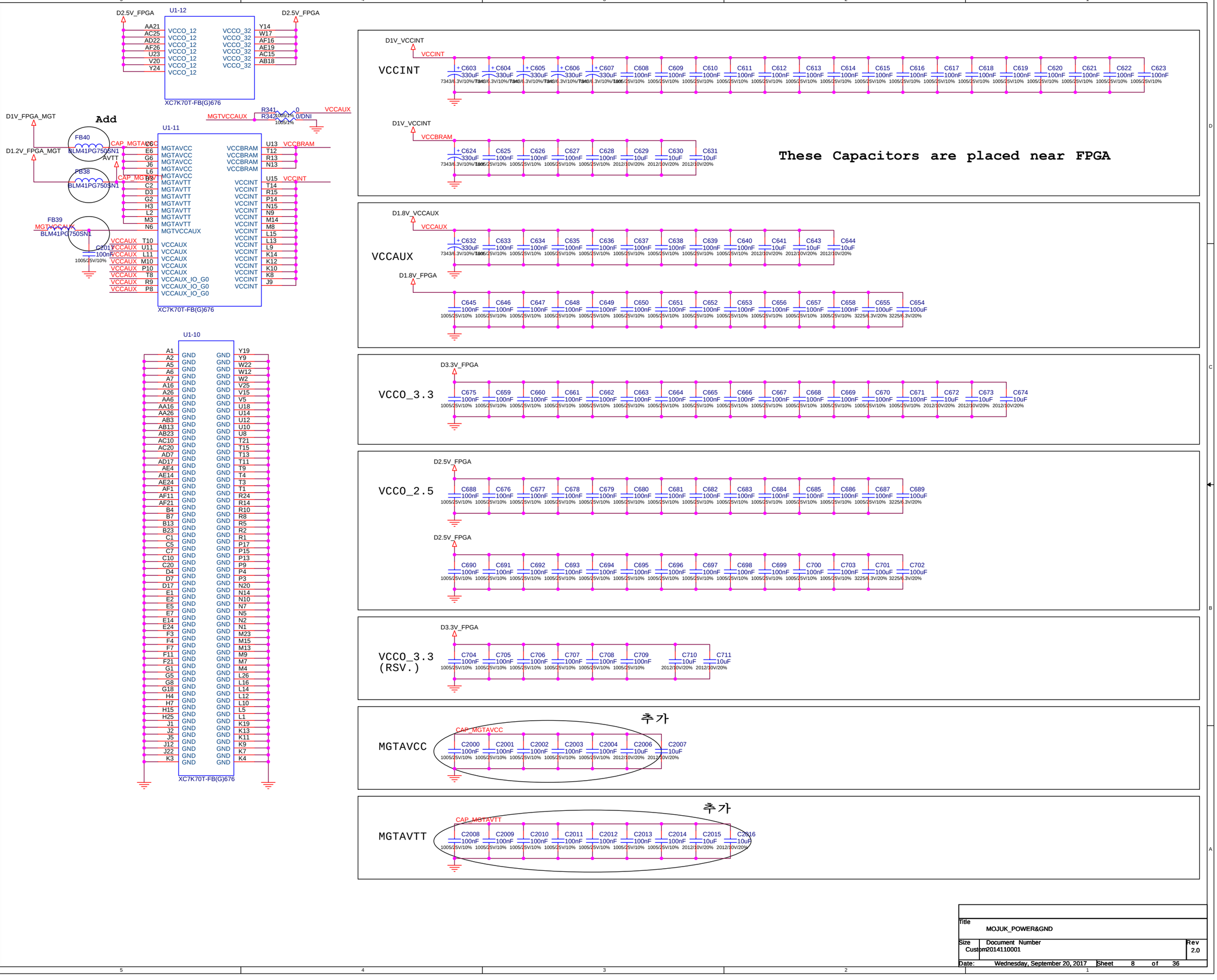

Title	MOJUK_POWER&GND	
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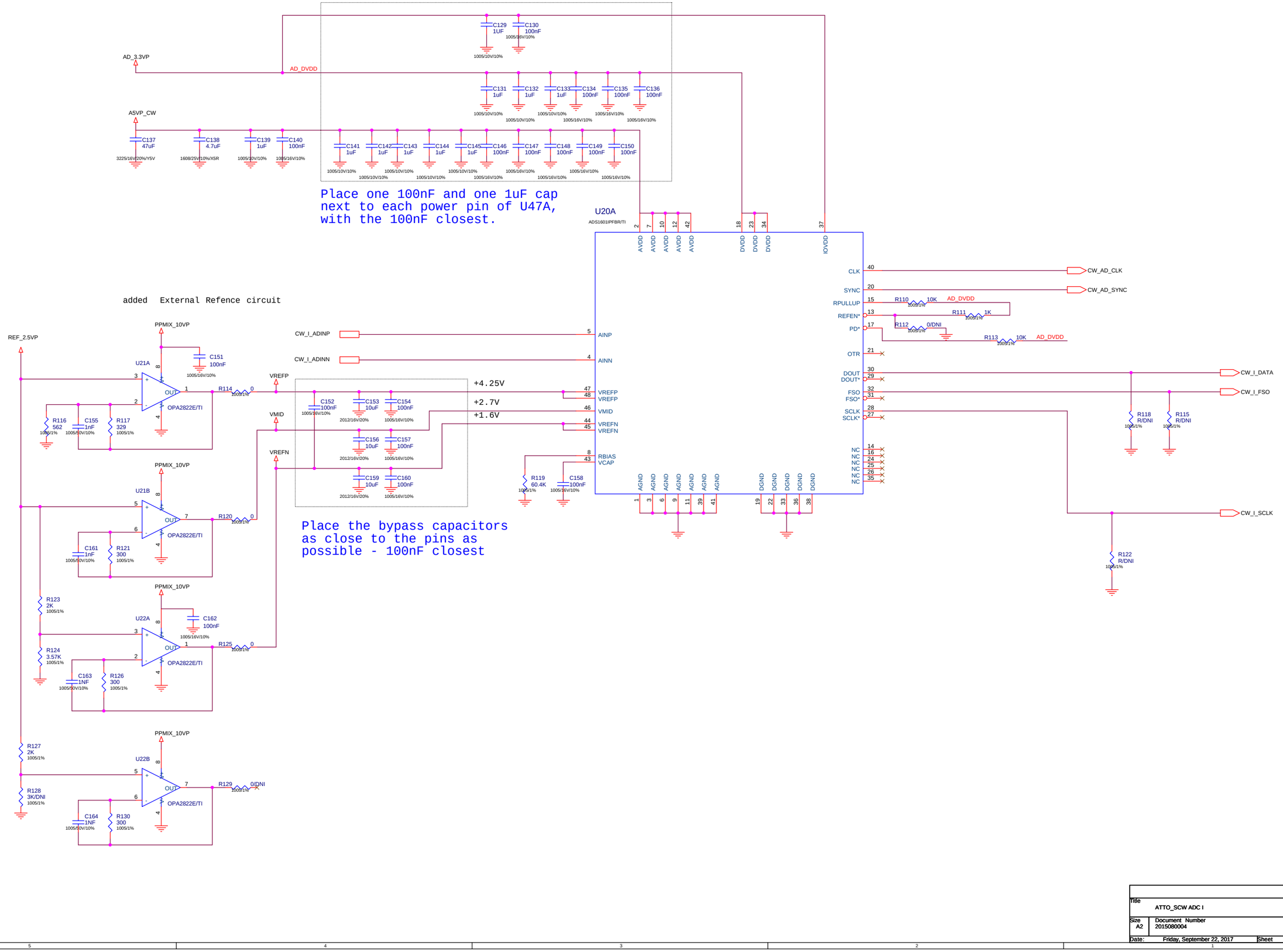
AD_3.3VP
AD_DVDD
A5VP_CW
C129 1UF
C130 100nF
C131 1uF
C132 1uF
C133 1uF
C134 100nF
C135 100nF
C136 100nF
C137 47uF
C138 4.7uF
C139 1uF
C140 100nF
C141 1uF
C142 1uF
C143 1uF
C144 1uF
C145 1uF
C146 100nF
C147 100nF
C148 100nF
C149 100nF
C150 100nF
Place one 100nF and one 1uF cap next to each power pin of U47A, with the 100nF closest.
U20A
ADS1601IPFBR/TI
AVDD
DVDD
IOVDD
CLK
SYNC
RPULLUP
REFEN*
PD*
OTR
DOUT
DOUT*
FSO
FSO*
SCLK
SCLK*
NC
CW_AD_CLK
CW_AD_SYNC
CW_I_DATA
CW_I_FSO
CW_I_SCLK
R110 10K
R111 1K
R112 0/DNI
R113 10K
R118 R/DNI
R115 R/DNI
R122 R/DNI
added External Refence circuit
REF_2.5VP
PPMIX_10VP
U21A
OPA2822E/TI
C151 100nF
R116 562
C155 1nF
R117 329
R114 0
CW_I_ADINP
CW_I_ADINN
AINP
AINN
VREFP
VMID
VREFN
RBIAS
VCAP
+4.25V
+2.7V
+1.6V
C152 100nF
C153 10uF
C154 100nF
C156 10uF
C157 100nF
C159 10uF
C160 100nF
R119 60.4K
C158 100nF
Place the bypass capacitors as close to the pins as possible - 100nF closest
U21B
R120 0
C161 1nF
R121 300
U22A
R123 2K
R124 3.57K
C162 100nF
R125 0
C163 1NF
R126 300
U22B
R127 2K
R128 3K/DNI
R129 0/DNI
C164 1NF
R130 300
AGND
DGND
Title
ATTO_SCW ADC I
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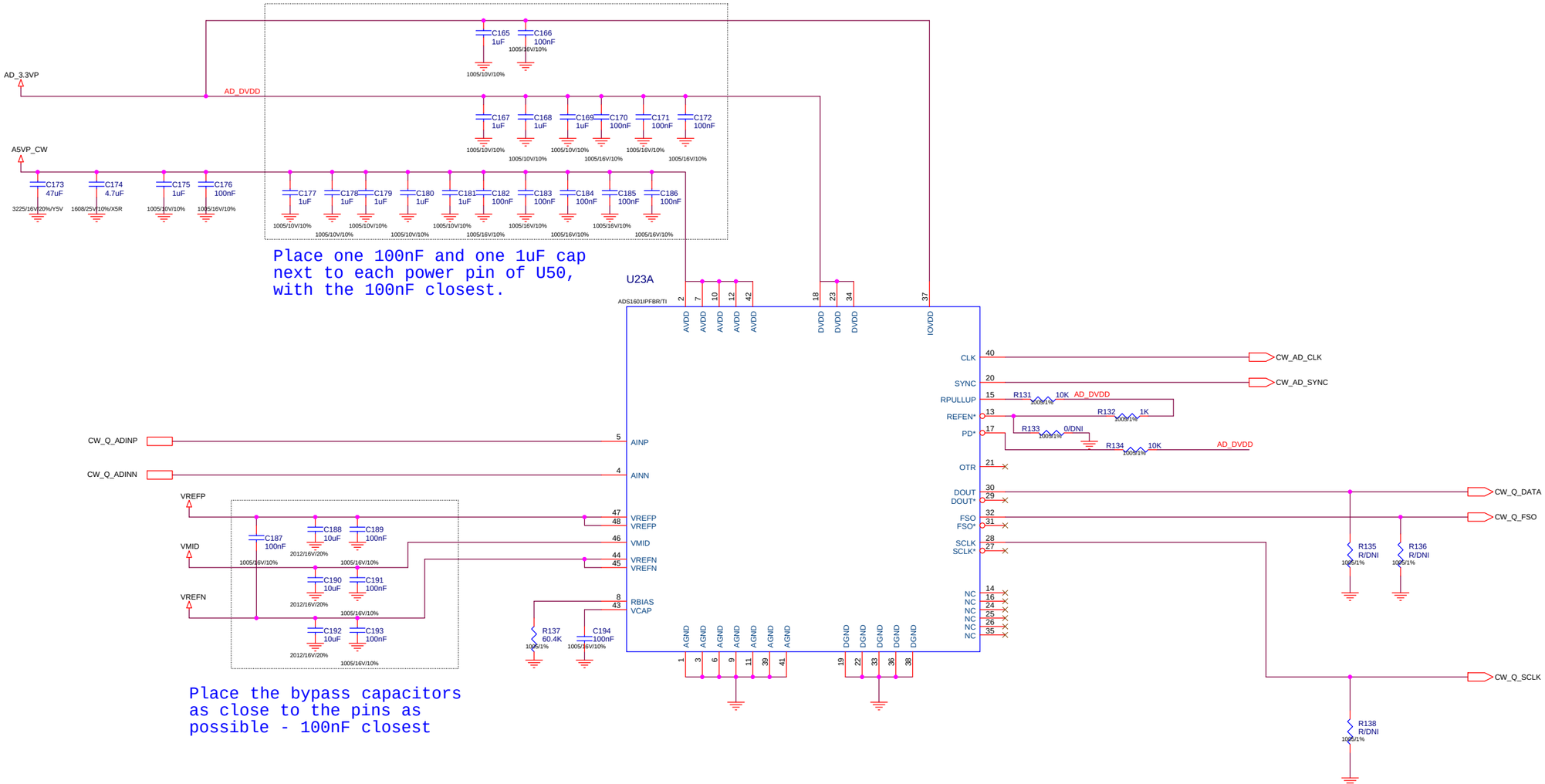

Title	ATTO_SCW ADC Q	
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