AFE5816 16-Channel Ultrasound AFE with 90-mW/Channel Power, 1-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer

1 Features

- 16-Channel, AFE for Ultrasound Applications:
  - Input Attenuator, LNA, LPF, ADC, and CW Mixer
  - Optimized Signal Chains for TGC and CW Modes
  - Digital Time Gain Compensation (DTGC)
  - Total Gain Range: 6 dB to 45 dB
  - Linear Input Range: 1 V_{PP}
- Input Attenuator with DTGC:
  - 8-dB to 0-dB Attenuation with 0.125-dB Step
  - Supports Matched Impedance for:
    - 50-Ω to 800-Ω Source Impedance
- Low-Noise Amplifier (LNA) with DTGC:
  - 14-dB to 45-dB Gain with 0.125-dB Step
  - Low Input Current Noise: 1.2 pA/√Hz
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF):
  - 10 MHz, 15 MHz, 20 MHz, and 25 MHz
- Analog-to-Digital Converter (ADC) with Programmable Resolution:
  - 14-Bit ADC: 75-dBFS Idle Channel SNR at 65 MSPS
  - 12-Bit ADC: 72-dBFS Idle Channel SNR at 80 MSPS
- LVDS Interface with a Maximum Speed Up to 1 GBPS
- Optimized for Noise and Power:
  - 90 mW/Ch at 1 nV/√Hz, 65 MSPS, TGC Mode
  - 55 mW/Ch at 1.45 nV/√Hz, 40 MSPS, TGC Mode
  - 59 mW/Ch, CW Mode
- Excellent Device-to-Device Gain Matching:
  - ±0.5 dB (Typical)
- Low Harmonic Distortion: –60-dBc Level
- Fast and Consistent Overload Recovery
- Continuous Wave (CW) Path with:
  - Passive Mixer
  - Low Close-In Phase Noise of –148 dBc/Hz at 1-kHz frequency
  - Phase Resolution: λ / 16
  - Supports 16X, 8X, 4X, and 1X CW Clocks
  - 12-dB Suppression of 3rd and 5th Harmonics
- Small Package: 15-mm × 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment
- Multichannel, High-Speed Data Acquisition

3 Description

The AFE5816 is a highly-integrated, analog front-end (AFE) solution specifically designed for ultrasound systems where high performance, low power, and small size are required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE5816	nFBGA (289)	15.00 mm x 15.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Block Diagram

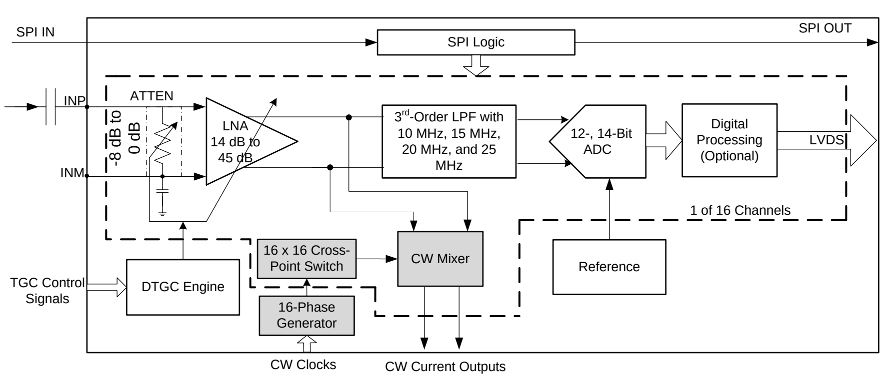


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2015) to Revision D — **Page**

- Released full document to web: added *Device Comparison Table*, *Pin Configuration and Functions* section, *Specifications* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, and *Register Maps* section from custom version of document 1
- Changed *Features* section: added second sub-bullet to first Features bullet, changed *ADC* and *Optimized for Noise and Power* Features bullets, and added first and last sub-bullets to *CW* Features bullet 1
- Changed *Device Information* table and *Simplified Block Diagram* 1
- Changed last paragraph of *Description* section 3
- Added *Community Resources* section 158

Changes from Revision B (June 2015) to Revision C — **Page**

- Removed AFE58JD16 from document 1
- Changed *Functional Block Diagram*: removed references to AFE58JD16 29

Changes from Revision A (April 2015) to Revision B — **Page**

- Changed from product preview to production data 1

5 Description (continued)

The AFE5816 is an integrated analog front-end (AFE) optimized for medical ultrasound application. The AFE5816 is a multichip module (MCM) device with two dies: VCA and ADC_CONV. Each die has total of 16 channels.

Each channel in the VCA die can be configured in two modes: time gain compensation (TGC) mode and continuous wave (CW) mode. In TGC mode, each channel includes an input attenuator (ATTEN), a low-noise amplifier (LNA) with variable-gain, and a third-order, low-pass filter (LPF). The attenuator supports an attenuation range of 8 dB to 0 dB, and the LNA supports gain ranges from 14 dB to 45 dB. The LPF cutoff frequency can be configured at 10 MHz, 15 MHz, 20 MHz, or 25 MHz to support ultrasound applications with different frequencies. In CW mode, each channel includes an LNA with a fixed gain of 18 dB, and a low-power passive mixer with 16 selectable phase delays. Different phase delays can be applied to each analog input signal to perform an on-chip beamforming operation. A harmonic filter in the CW mixer suppresses the third and fifth harmonic to enhance the sensitivity of the CW Doppler measurement. CW mode supports three clock modes: 16X, 8X, and 4X.

Each channel of the ADC_CONV die has a high-performance analog-to-digital converter (ADC) with a programmable resolution of 14 bits or 12 bits. The ADC achieves 75-dBFS signal-to-noise ratio (SNR) in 14-bit mode, and 72-dBFS SNR in 12-bit mode. This ADC provides excellent SNR at low-channel gain. The devices operate at maximum speeds of 65 MSPS and 80 MSPS, providing 14-bit and 12-bit output, respectively. The ADC is designed to scale power with sampling rate. The output interface of the ADC is a low-voltage differential signaling (LVDS) interface that can easily interface with low-cost field-programmable gate arrays (FPGAs).

The AFE5816 also allows various power and noise combinations to be selected for optimizing system performance. Therefore, these devices are suitable ultrasound AFE solutions for systems with strict battery-life requirements. The AFE5816 is available in a 15-mm × 15-mm NFBGA-289 package (ZAV package, S-PBGA-N289) and is specified for operation from –40°C to +85°C. The device is also pin-to-pin compatible with the AFE5818 family.

6 Device Comparison Table

DEVICE	DESCRIPTION	PACKAGE	BODY SIZE (NOM)
AFE5818	16-channel, ultrasound, analog front-end (AFE) with 124-mW/channel, 0.75-nV/√Hz noise, 14-bit, 65-MSPS or 12-bit, 80-MSPS ADC and passive CW mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5812	Fully integrated, 8-channel ultrasound AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 180 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5809	8-channel ultrasound AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5808A	8-channel ultrasound AFE with passive CW mixer, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5807	8-channel ultrasound AFE with passive CW mixer, 1.05 nV/√Hz, 12 bits, 80 MSPS, 117 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5803	8-channel ultrasound AFE, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5805	8-channel ultrasound AFE, 0.85 nV/√Hz, 12 bits, 50 MSPS, 122 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5804	8-channel ultrasound AFE, 1.23 nV/√Hz, 12 bits, 50 MSPS, 101 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5801	8-channel variable-gain amplifier (VGA) with octal high-speed ADC, 5.5 nV/√Hz, 12 bits, 65 MSPS, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
AFE5851	16-channel VGA with high-speed ADC, 5.5 nV/√Hz, 12 bits, 32.5 MSPS, 39 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
VCA5807	8-channel voltage-controlled amplifier for ultrasound with passive CW mixer, 0.75 nV/√Hz, 99 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
VCA8500	8-channel, ultralow-power VGA with low-noise pre-amp, 0.8 nV/√Hz, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
ADS5294	Octal-channel, 14-bit, 80-MSPS ADC, 75-dBFS SNR, 77 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5292	Octal-channel, 12-bit, 80-MSPS ADC, 70-dBFS SNR, 66 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5295	Octal-channel, 12-bit, 100-MSPS ADC, 70.6-dBFS SNR, 80 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5296A	10-bit, 200-MSPS, 4-channel, 61-dBFS SNR, 150-mW/ch and 12-bit, 80-MSPS, 8-channel, 70-dBFS SNR, 65-mW/ch ADC	VQFN (64)	9.00 mm × 9.00 mm

7 Pin Configuration and Functions

ZAV Package
289-Bumps NFBGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	INP16	INP15	INP14	INP13	INP12	INP11	INP10	INP9	NC	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	INM16	INM15	INM14	INM13	INM12	INM11	INM10	INM9	NC	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	NC	NC	CW_IP_OUTM	CW_IP_OUTP	BIAS_2P5	AVDD_3P15	AVDD_3P15	AVDD_3P15	AVDD_3P15	AVDD_3P15	AVDD_3P15	AVDD_3P15	NC	SRC_BIAS	AVSS	AVSS	AVSS
E	NC	NC	NC	NC	NC	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	AVDD_1P9	AVDD_1P9	AVSS	CLKP_16X	CLKM_16X
F	NC	NC	NC	NC	LNA_INCM	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS
G	NC	NC	CW_QP_OUTM	CW_QP_OUTP	BAND_GAP	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	NC	NC	AVSS	CLKM_1X	CLKP_1X
H	AVSS	AVSS	AVSS	TGC_SLOPE	TGC_PROF<2>	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	NC	NC	TR_EN<3>	SDOUT	NC
J	ADC_CLKP	ADC_CLKM	AVSS	TGC_UP_DN	TGC_PROF<1>	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	NC	NC	TR_EN<4>	TR_EN<2>	SCLK
K	AVSS	AVSS	AVSS	NC	NC	AVDD_1P9	AVDD_1P9	AVSS	AVSS	AVSS	AVDD_1P9	AVDD_1P9	NC	NC	TR_EN<1>	NC	SEN
L	NC	NC	DVDD_1P2	NC	AVDD_1P8	AVDD_1P8	AVDD_1P8	AVSS	AVSS	AVSS	AVDD_1P8	AVDD_1P8	AVDD_1P8	NC	NC	SDIN	RESET
M	NC	NC	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	TX_TRIG	PDN_GBL	PDN_FAST
N	NC	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	NC
P	NC	DVDD_1P2	DVDD_1P2	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVSS	DVSS	DVSS	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P2	DVDD_1P2	NC
R	NC	DOUTP16	DOUTP15	DOUTP14	NC	DOUTM11	DOUTP11	FCLKM	NC	FCLKP	DOUTM6	DOUTP6	NC	DOUTP3	DOUTP2	DOUTP1	NC
T	NC	DOUTM16	DOUTM15	DOUTM14	DOUTP13	DOUTP12	DOUTP10	DOUTP9	DCLKP	DOUTP8	DOUTP7	DOUTP5	DOUTP4	DOUTM3	DOUTM2	DOUTM1	NC
U	NC	NC	NC	NC	DOUTM13	DOUTM12	DOUTM10	DOUTM9	DCLKM	DOUTM8	DOUTM7	DOUTM5	DOUTM4	NC	NC	NC	NC

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADC_CLKM	J2	I	Differential clock input pin used for ADC conversion, negative. A single-ended clock is also supported. Connect ADC_CLKM to dc ground when using a single-ended clock.
ADC_CLKP	J1	I	Differential clock input pin used for ADC conversion, positive. A single-ended clock is also supported. Connect the ADC clock to the ADC_CLKP pin when using a single-ended clock.
AVDD_1P8	L5-L7, L11-L13	P	Analog supply pins, 1.8 V (ADC_CONV die)
AVDD_1P9	E6, E7, E11-E14, F6, F7, F11-F14, G6, G7, G11, G12, H6, H7, H11, H12, J6, J7, J11, J12, K6, K7, K11, K12	P	Analog supply pins, 1.9 V (VCA die)(1)
AVDD_3P15	D6-D12	P	Analog supply pins, 3.15 V (VCA die)
AVSS	D15-D17, E8-E10, E15, F8-F10, F15-F17, G8-G10, G15, H1-H3, H8-H10, J3, J8-J10, K1-K3, K8-K10, L8-L10	G	Analog ground pins
BAND_GAP	G5	O	Bypass to analog ground with a 1-µF capacitor.
BIAS_2P5	D5	O	Bypass to analog ground with a 1-µF capacitor.
CLKM_1X	G16	I	Differential clock input for the 1X CW clock, negative. A single-ended clock is also supported. In single-ended clock mode, the CLKM_1X pin is internally pulled to ground. In 1X clock mode, this pin is the negative quadrature-phase clock input for the CW mixer.(2)
CLKP_1X	G17	I	Differential clock input for the 1X CW clock, positive. A single-ended clock is also supported. Connect the 1X CW clock to the CLKP_1X pin when using a single-ended clock. In 1X clock mode, this pin is the positive quadrature-phase clock input for the CW mixer.(2)
CLKM_16X	E17	I	Differential clock input for the 16X, 8X, and 4X CW clocks, negative. A single-ended clock is also supported. In single-ended clock mode, the CLKM_16X pin is internally pulled to ground.(2)
CLKP_16X	E16	I	Differential clock input for the 16X, 8X, and 4X CW clocks, positive. A single-ended clock is also supported. Connect the 16X CW clock to the CLKP_16X pin when using a single-ended clock. In 1X CW clock mode, this pin is the positive in-phase clock input for the CW mixer.(2)
CW_IP_OUTM	D3	O	In-phase CW differential summed current output, negative.(2)
CW_IP_OUTP	D4	O	In-phase CW differential summed current output, positive.(2)
CW_QP_OUTM	G3	O	Quadrature-phase CW differential summed current output, negative.(2)
CW_QP_OUTP	G4	O	Quadrature-phase CW differential summed current output, positive.(2)
DCLKM	U9	O	Low-voltage differential signaling (LVDS) serialized data clock outputs (receiver bit alignment)
DCLKP	T9		
DOUTM1	T16	O	LVDS serialized differential data outputs for channel 1
DOUTP1	R16		
DOUTM2	T15	O	LVDS serialized differential data outputs for channel 2
DOUTP2	R15		
DOUTM3	T14	O	LVDS serialized differential data outputs for channel 3
DOUTP3	R14		
DOUTM4	U13	O	LVDS serialized differential data outputs for channel 4
DOUTP4	T13		
DOUTM5	U12	O	LVDS serialized differential data outputs for channel 5
DOUTP5	T12		
DOUTM6	R11	O	LVDS serialized differential data outputs for channel 6
DOUTP6	R12		
DOUTM7	U11	O	LVDS serialized differential data outputs for channel 7
DOUTP7	T11		
DOUTM8	U10	O	LVDS serialized differential data outputs for channel 8
DOUTP8	T10		
DOUTM9	U8	O	LVDS serialized differential data outputs for channel 9
DOUTP9	T8		

(1) In low-power mode, the typical power supply for AVDD_1P9 is 1.8 V.
(2) When CW mode is not used, this pin can be floated.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DOUTM10	U7	O	LVDS serialized differential data outputs for channel 10
DOUTP10	T7		
DOUTM11	R6	O	LVDS serialized differential data outputs for channel 11
DOUTP11	R7		
DOUTM12	U6	O	LVDS serialized differential data outputs for channel 12
DOUTP12	T6		
DOUTM13	U5	O	LVDS serialized differential data outputs for channel 13
DOUTP13	T5		
DOUTM14	T4	O	LVDS serialized differential data outputs for channel 14
DOUTP14	R4		
DOUTM15	T3	O	LVDS serialized differential data outputs for channel 15
DOUTP15	R3		
DOUTM16	T2	O	LVDS serialized differential data outputs for channel 16
DOUTP16	R2		
DVDD_1P2	L3, M4-M6, M12-M14, N2-N6, N12-N16, P2, P3, P15, P16	P	1.2-V digital supply pins for the ADC digital block
DVDD_1P8	P4-P7, P11-P14	P	1.8-V digital supply pins for the ADC digital, digital I/Os, phase-locked loop (PLL), and LVDS interface blocks
DVSS	M3, M7-M11, N7-N11, P8-P10	G	Digital ground (ADC_CONV die).
FCLKM	R8	O	LVDS serialized differential frame clock outputs (receiver word alignment).
FCLKP	R10		
INM1	C17	I	Complementary analog input for channel 1.(3)
INM2	C16	I	Complementary analog input for channel 2.(3)
INM3	C15	I	Complementary analog input for channel 3.(3)
INM4	C14	I	Complementary analog input for channel 4.(3)
INM5	C13	I	Complementary analog input for channel 5.(3)
INM6	C12	I	Complementary analog input for channel 6.(3)
INM7	C11	I	Complementary analog input for channel 7.(3)
INM8	C10	I	Complementary analog input for channel 8.(3)
INM9	C8	I	Complementary analog input for channel 9.(3)
INM10	C7	I	Complementary analog input for channel 10.(3)
INM11	C6	I	Complementary analog input for channel 11.(3)
INM12	C5	I	Complementary analog input for channel 12.(3)
INM13	C4	I	Complementary analog input for channel 13.(3)
INM14	C3	I	Complementary analog input for channel 14.(3)
INM15	C2	I	Complementary analog input for channel 15.(3)
INM16	C1	I	Complementary analog input for channel 16.(3)
INP1	A17	I	Analog input for channel 1. AC-couple to device input with a 10-nF capacitor.
INP2	A16	I	Analog input for channel 2. AC-couple to device input with a 10-nF capacitor.
INP3	A15	I	Analog input for channel 3. AC-couple to device input with a 10-nF capacitor.
INP4	A14	I	Analog input for channel 4. AC-couple to device input with a 10-nF capacitor.
INP5	A13	I	Analog input for channel 5. AC-couple to device input with a 10-nF capacitor.
INP6	A12	I	Analog input for channel 6. AC-couple to device input with a 10-nF capacitor.
INP7	A11	I	Analog input for channel 7. AC-couple to device input with a 10-nF capacitor.
INP8	A10	I	Analog input for channel 8. AC-couple to device input with a 10-nF capacitor.
INP9	A8	I	Analog input for channel 9. AC-couple to device input with a 10-nF capacitor.
INP10	A7	I	Analog input for channel 10. AC-couple to device input with a 10-nF capacitor.
INP11	A6	I	Analog input for channel 11. AC-couple to device input with a 10-nF capacitor.

(3) The LNA high-pass filter (HPF) response of the channel depends on the capacitor connected at the INMx pin. By default, leave this pin floating. For very low-frequency applications, connect a capacitor > 1 µF.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
INP12	A5	I	Analog input for channel 12. AC-couple to device input with a 10-nF capacitor.
INP13	A4	I	Analog input for channel 13. AC-couple to device input with a 10-nF capacitor.
INP14	A3	I	Analog input for channel 14. AC-couple to device input with a 10-nF capacitor.
INP15	A2	I	Analog input for channel 15. AC-couple to device input with a 10-nF capacitor.
INP16	A1	I	Analog input for channel 16. AC-couple to device input with a 10-nF capacitor.
LNA_INCM	F5	O	Bypass to ground with a 1-µF capacitor.
NC	A9, B1-B17, C9, D1, D2, D13, E1-E5, F1-F4, G1, G2, G13, G14, H13, H14, H17, J13, J14, K4, K5, K13, K14, K16, L1, L2, L4, L14, L15, M1, M2, R5, R9, R13, N1, N17, P1, R1, R17, P17, T1, T17, U1-U4, U14-U17	—	Unused pins; do not connect
PDN_FAST	M17	I	Partial power-down control pin for the entire device with an internal 16-kΩ pulldown resistor; active high.(4)
PDN_GBL	M16	I	Global (complete) power-down control pin for the entire device with an internal 16-kΩ pulldown resistor; active high.(4)
RESET	L17	I	Hardware reset pin with an internal 16-kΩ pull-down resistor; active high.(4)
SCLK	J17	I	Serial programming interface clock pin with an internal 16-kΩ pulldown resistor.(4)
SDIN	L16	I	Serial programming interface data pin with an internal 16-kΩ pulldown resistor.(4)
SDOUT	H16	O	Serial programming interface readout pin. This pin is in tri-state by default.(4)
SEN	K17	I	Serial programming interface enable pin, active low. This pin has a 16-kΩ pullup resistor.(4)
SRC_BIAS	D14	O	Bypass to ground with a 1-µF capacitor.
TGC_PROF<1>	J5	I	Digital TGC profile 1 select pin. This pin has an internal 150-kΩ pulldown resistor; active high.(4)
TGC_PROF<2>	H5	I	Digital TGC profile 2 select pin. This pin has an internal 150-kΩ pulldown resistor; active high.(4)
TGC_SLOPE	H4	I	Digital TGC control pin. This pin has an internal 150-kΩ pulldown resistor.(4)
TGC_UP_DN	J4	I	Digital TGC control pin. This pin has an internal 150-kΩ pulldown resistor.(4)
TR_EN<1>	K15	I	TR enable pin 1; disconnects the LNA HPF from the input pins of channels 1 to 4.(4) This pin has an internal 150-kΩ pullup resistor.
TR_EN<2>	J16	I	TR enable pin 2; disconnects the LNA HPF from the input pins of channels 5 to 8.(4) This pin has an internal 150-kΩ pullup resistor.
TR_EN<3>	H15	I	TR enable pin 3; disconnects the LNA HPF from the input pins of channels 9 to 12.(4) This pin has an internal 150-kΩ pullup resistor.
TR_EN<4>	J15	I	TR enable pin 4; disconnects the LNA HPF from the input pins of channels 13 to 16.(4) This pin has an internal 150-kΩ pullup resistor.
TX_TRIG	M15	I	This pin synchronizes test patterns across devices. This pin has a 20-kΩ pulldown resistor.(4)

(4) A 1.8-V logic level is required.

Table 1. Pin Name to Signal Name Map

SIGNAL NUMBER	PIN NAME	SIGNAL NAME
1	ADC_CLKP – ADC_CLKM	ADC_CLK
2	CLKP_1X – CLKM_1X	CW_CLK1X
3	CLKP_16X – CLKM_16X	CW_CLK_NX
4	CW_IP_OUTP – CW_IP_OUTM	CW_IP_OUT
5	CW_QP_OUTP – CW_QP_OUTM	CW_QP_OUT
6	DOUTPx – DOUTMx	DOUT
7	FCLKP – FCLKM	FCLK
8	DCLKP – DCLKM	DCLK
9	CMLx_OUTP – CMLx_OUTM	CMLx_OUT

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD_1P8	–0.3	2.2	V
	AVDD_1P9	–0.3	2.2	
	AVDD_3P15	–0.3	3.9	
	DVDD_1P2	–0.3	1.35	
	DVDD_1P8	–0.3	2.2	
Voltage at analog inputs		–0.3	Minimum [2.2, (AVDD_1P9 + 0.3)]	V
Voltage at digital inputs		–0.3	Minimum [2.2, (AVDD_1P9 + 0.3), (DVDD_1P8 + 0.3)]	V
Temperature	Maximum junction temperature (T_J), any condition		105	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range, unless otherwise noted

PARAMETER			MIN	TYP	MAX	UNIT
SUPPLIES						
V_{A_1P8}	AVDD_1P8 voltage		1.7	1.8	1.9	V
V_{A_1P9}	AVDD_1P9 voltage	Low-noise mode, medium-power mode	1.8	1.9	2.0	V
		Low-power mode	1.75	1.8	2.0	
V_{A_3P15}	AVDD_3P15 voltage		3	3.15	3.3	V
V_{D_1P2}	DVDD_1P2 voltage		1.15	1.2	1.25	V
V_{D_1P8}	DVDD_1P8 voltage		1.7	1.8	1.9	V
TEMPERATURE						
T_A	Ambient temperature		–40		85	°C
BIAS VOLTAGES						
	Common-mode voltage(1)	ADC_CLKP, ADC_CLKM in differential mode		0.7		V
		CLKP_1X, CLKM_1X, CLKP_16X, CLKM_16X in differential mode		1.5		
		CW_IP_OUTP, CW_IP_OUTM, CW_QP_OUTP, CW_QP_OUTM		0.9		
		(INM1, INP1), (INM2, INP2)…(INM16, INP16)		1		
	Bias voltage(1)	BAND_GAP		1.2		V
		BIAS_2P5		2.5		
		LNA_INCM		1		
		SRC_BIAS		0.5		

(1) Internally set by the device.

Recommended Operating Conditions (continued)

over operating free-air temperature range, unless otherwise noted

PARAMETER				MIN	TYP	MAX	UNIT
ADC CLOCK INPUT: ADC_CLK							
f_{CLKIN}	ADC clock frequency	14-bit ADC resolution		5		65	MHz
		12-bit ADC resolution		5		80	
V_{DEADC}	Differential clock amplitude	Sine-wave, ac-coupled		0.7			V_{PP}
		LVPECL, ac-coupled			1.6		
		LVDS, ac-coupled			0.7		
V_{SEADC}	Single-ended clock amplitude	LVCMOS on ADC_CLKP with ADC_CLKM grounded			1.8		V
D_{ADC}	ADC_CLK duty cycle			40%	50%	60%	
CW CLOCK INPUT: CW_CLK1X, CW_CLK_NX							
CW_{CLK}	CW clock frequency	CW_CLK1X across CW clock modes in relation to CW_CLK1X; see the CW_CLK_MODE register bits in register 192				8	MHz
		CW_CLK_NX across CW clock modes; see the CW_CLK_MODE register bits in register 192	16X mode		16X		CW_ CLK1X
			8X mode		8X		
			4X mode		4X		
V_{DECW}	Differential clock amplitude	CW_CLK1X, CW_CLK_NX. LVDS, ac-coupled			0.7		V_{PP}
V_{SECW}	Single-ended clock amplitude	LVCMOS on CLKP_1X, CLKP_16X with CLKM_1X, CLKM_16X grounded or floating			3.15		V
D_{CW}	CLK duty cycle	CW_CLK1X, CW_CLK_NX		40%	50%	60%	
DIGITAL OUTPUT (LVDS)							
R_L	Differential load resistance				100		Ω

8.4 Thermal Information

THERMAL METRIC[1]		AFE5816 ZAV (NFBGA) 289 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics: TGC Mode

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, and DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), 14-bit ADC resolution, LVDS interface to capture ADC data, and output amplitude V_{OUT} = –1 dBFS. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
GENERAL							
V_{MAX}	Maximum linear input voltage	At INP_SOURCE node; see the *Functional Block Diagram* section			1		V_{PP}
		At INPx node; see the *Functional Block Diagram* section			0.4		
C_{INP}	Input capacitance				35		pF
G_{CODE}	Gain code[1]	Programs the total gain		0		319	
G_{TOT}	Total gain	Low-noise mode and medium-power mode			(6 + 0.125 × G_{CODE})		dB
		Low-power mode			(12 + 0.125 × G_{CODE})		
G_{RANGE}	Gain range				39		dB
G_{SLOPE}	Gain slope				0.125		dB/G_{CODE}
T_{TGC}	TGC response time	G_{CODE} changed from 64 to 319			10		µs
$V_{N,IRN}$	Input voltage noise	R_S = 0 Ω, calculated in band of 4-MHz to 6-MHz frequency	Low-noise mode		1		nV/√Hz
			Medium-power mode		1.3		
			Low-power mode		1.45		
$I_{N,IRN}$	Input-referred current noise	Across low-noise, medium-power, and low-power mode			1.2		pA/√Hz
NF	Noise figure[2]	R_S = 50 Ω	Low-noise mode		3.6		dB
			Medium-power mode		4.5		
			Low-power mode		5.0		
		R_S = 400 Ω	Low-noise mode		1.2		dB
			Medium-power mode		1.5		
			Low-power mode		1.6		

(1) The gain code range from 0 to 63 controls the input attenuation and the gain code range from 64 to 319 controls the LNA gain.
(2) NF is measured as the SNR at the output of the device relative to the SNR at the input resulting from ths noise of source resistance R_S.

Electrical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, and DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), 14-bit ADC resolution, LVDS interface to capture ADC data, and output amplitude V_{OUT} = –1 dBFS. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
GENERAL (continued)							
K_{CORR}	Channel-to-channel noise correlation factor(3)	Without a signal, calculated in a 1-MHz to 10-MHz bandwidth	R_S = 330 Ω		–20		dB
			R_S = 100 Ω		–26		
		With a signal, calculated in a 1-MHz to 10-MHz bandwidth	Total gain = 45 dB		–17		
			Total gain = 26 dB		–14		
		With a signal, calculated in a 1-MHz bandwidth around a 5-MHz input signal frequency	Total gain = 45 dB		–13		
			Total gain = 26 dB		–10		
SNR	Signal-to-noise ratio	SNR calculated in 750 kHz to Nyquist bandwidth	Total gain = 14 dB	65	68		dBFS
			Total gain = 45 dB	55	58		
SNR_{NB}	Narrow-band SNR	SNR calculated in 2-MHz bandwidth around input signal frequency	Total gain = 30 dB	72.5	76		dBFS
LPF	3rd-order, low-pass filter	–3-dB cutoff frequency across LPF_PROG register settings; see register 199	Low-noise and medium-power mode		10		MHz
					15		
					20		
					25		
			Low-power mode		5		
					7.5		
					10		
					12.5		
Δ_{LPF}	LPF bandwidth variation				±5%		
Δ_{Gr}	Channel-to-channel group delay matching	2-MHz to 15-MHz input signal frequency			2		ns
Δ_{φ}	Channel-to-channel phase matching	15-MHz signal			11		Degrees
G_{MATCH}	Gain matching	Device-to-device, average across channels	G_{CODE} < 64		±0.5		dB
			G_{CODE} > 64	–1	±0.5	1	
		Channel-to-channel, same device	G_{CODE} < 64		±0.5		
			G_{CODE} > 64	–1	±0.5	1	
HD2	Second-order harmonic distortion	Output amplitude = –1 dBFS, gain = 45 dB			–65		dBc
		Output amplitude = –1 dBFS, gain = 6 dB			–55		
HD3	Third-order harmonic distortion	Output amplitude = –1 dBFS, gain = 45 dB			–60		dBc
		Output amplitude = –1 dBFS, gain = 6 dB			–60		
THD	Total harmonic distortion	Output amplitude = –1 dBFS, gain = 45 dB			–58		dBc
		Output amplitude = –1 dBFS, gain = 6 dB			–54		
IMD3	Third-order intermodulation distortion	Input frequency 1 = 5 MHz at –1 dBFS, input frequency 2 = 5.01 MHz at –21 dBFS			–75		dBc
XTALK	Fundamental crosstalk	Signal applied to a single channel. Crosstalk measured on neighboring channel.			–55		dBc
PN_{1kHz}	Phase noise	Calculated at 1-kHz offset from 5-MHz input signal frequency			–129		dBc/Hz
V_{ORO}	Output offset				±600		LSB
G_{LNA}	LNA gain range in TGC mode				14 to 45		dB

(3) The noise-correlation factor is defined as 10 × $\log_{10}$[Nc / (Nc + Nu)], where Nc is the correlated noise power in a single channel and Nu is the uncorrelated noise power in a single channel. The noise-correlation factor measurement is described by the equation:

$$\frac{Nc}{(Nu+Nc)} = \frac{N\_16Ch}{(N\_1Ch \times 240)} - \frac{1}{15}$$

where N_16CH is the noise power of the summed 16 channels and N_1CH is the noise power of one channel.

Electrical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, and DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), 14-bit ADC resolution, LVDS interface to capture ADC data, and output amplitude V_{OUT} = –1 dBFS. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
GENERAL (continued)							
HPF_{TGC}	LNA High-pass filter	–1-dB cutoff frequency across LNA_HPF_PROG register settings; see register 199			75		kHz
					150		
					300		
					600		
ADC SPECIFICATIONS							
f_S	Sample rate	14-bit resolution		5		65	MSPS
		12-bit resolution		5		80	
SNR	Signal-to-noise ratio	14-bit resolution	Without a signal		75		dBFS
			With a –1-dBFS signal amplitude		72.5		
		12-bit resolution	Without a signal		72		
			With a –1-dBFS signal amplitude		69.5		
$V_{MAX,ADC}$	ADC input full-scale range				2		V_{PP}
POWER DISSIPATION							
$P_{TGC/Ch}$	Power dissipation per channel: 12-bit ADC resolution and 80-MSPS ADC clock	TGC low-noise mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			94		mW/Ch
		TGC medium-power mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			72		
		TGC low-power mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			62		
I_{A_1P9}	AVDD_1P9 current (1.9 V)(4)	TGC low-noise mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			430		mA
		TGC medium-power mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			240		
		TGC low-power mode, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			160		
I_{A_3P15}	AVDD_3P15 current(4)	TGC low-noise, medium-power, and low-power modes, 500-mV_{PP} input signal up to 1% duty cycle applied to 16 channels			20		mA
I_{A_1P8}	AVDD_1P8 current(4)	For a 12-bit ADC resolution and an 80-MSPS system clock			170		mA
I_{D_1P2}	DVDD_1P2 current(4)	For a 12-bit ADC resolution and an 80-MSPS system clock			110		mA
I_{A_1P8}	DVDD_1P8 current(4)	For a 12-bit ADC resolution and an 80-MSPS system clock			100		mA
AC PERFORMANCE (Power)							
$PSRR_{1\ kHz}$	AC power-supply rejection ratio: tone at output relative to tone on supply	100 mV_{PP}, 1-kHz tone on supply	AVDD_1P9		–65		dBc
			AVDD_3P15		–90		
			AVDD_1P8, DVDD_1P8, and DVDD_1P2		–70		
$PSMR_{1\ kHz}$	AC power-supply modulation ratio: intermodulation tone at output resulting from tones at supply and input measured relative to input tone	100 mV_{PP}, 1-kHz tone on supply and –1-dBFS, 5-MHz tone at input	AVDD_1P9		–45		dBc
			AVDD_3P15		–45		
			AVDD_1P8, DVDD_1P8, and DVDD_1P2		–80		
POWER DOWN							
P_{DOWN}	Power dissipation in power-down mode	Partial power-down when PDN_FAST = high			17		mW/Ch
		Complete power-down when PDN_GBL = high			3		
t_{UP}	Power-up time	Partial power-down when PDN_FAST = high and the device is in partial power-down time for < 500 µs			3		µs
		Complete power-down when PDN_GBL = high			1		ms

(4) Designing the power supply with 2X of the typical current capacity is recommended to take care of current variation across devices, switching current, signal current, and so forth.

8.6 Electrical Characteristics: CW Mode

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 2 MHz, CW_CLK1X = 2-MHz differential clock, and CW_CLK_NX = 32-MHz differential clock. **Device settings:** CW clock mode = 16X, and 1X and 16X clock buffer in differential mode and ADC in power-down mode. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
$V_{MAX,\ CW}$	Maximum input swing				300		mV_{PP}
R_{V2I}	Voltage-to-current resistor at LNA output				500		Ω
I_{OPP}	Peak-to-peak output current per channel				4.8		mA/Ch
$V_{N,IRCW}$	Input voltage noise	1 channel			1.55		nV/√Hz
		16 channels			0.45		
$I_{N,ORCW}$	Output current noise	1 channel			19		pA/√Hz
		16 channels			80		
NF_{CW}	Noise figure(1)	R_S = 100 Ω, 1 channel			4		dB
		R_S = 100 Ω, 16 channels			4.8		
L_{CWM}	CW mixer conversion loss				4		dB
$PN_{1\ kHz,CW}$	Phase noise	16X CW clock mode, calculated at 1-kHz frequency	Signal to 1 channel		–151		dBc/Hz
			Signal to 16 channels		–161		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 5 MHz, f_{IN2} = 5.01 MHz, both tones at –6-dBFS amplitude, input to all the 16 channels.			–60		dBc
		f_{IN1} = 5 MHz, f_{IN2} = 5.01 MHz, both tones at –6-dBFS amplitude, input to single channel			–70		
Δ_{IQG}	I/Q channel gain matching	16X and 8X CW clock mode			±0.06		dB
		4X CW clock mode			±0.08		
Δ_{IQP}	I/Q channel phase matching	16X and 8X CW clock mode			±0.05		Degrees
		4X CW clock mode			±0.15		
IM_{REJ}	Image rejection ratio	16X and 8X CW clock mode			–49		dBc
		4X CW clock mode			–46		
G_{LNACW}	LNA gain in CW mode				18		dB
HPF_{CW}	High-pass filter	–1-dB cutoff frequency across LNA_HPF_PROG register settings; see register 199			75		kHz
					150		
					300		
					600		
POWER DISSIPATION							
$P_{CW/Ch}$	Power dissipation per channel (CW mode)	CW mode, CW_CLK1X = 5 MHz, CW_CLK_NX = 80 MHz	No signal		60		mW/Ch
			300-mV_{PP} input signal to all 16 channels		68		
I_{A_1P9}	AVDD_1P9 current (1.9 V)(2)	CW mode, CW_CLK1X = 5 MHz, CW_CLK_NX = 80 MHz	No signal		385		mA
			300-mV_{PP} input signal to all 16 channels		450		
I_{A_3P15}	AVDD_3P15 current(2)	CW mode, CW_CLK1X = 5 MHz, CW_CLK_NX = 80 MHz	No signal		70		mA
			300-mV_{PP} input signal to all 16 channels		70		

(1) NF is measured as the SNR at the output of the device relative to the SNR at the input resulting from ths noise of source resistance R_S.
(2) Designing the power supply with 2X of the typical current capacity is recommended to take care of current variation across devices, switching current, signal current, and so forth.

Electrical Characteristics: CW Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 2 MHz, CW_CLK1X = 2-MHz differential clock, and CW_CLK_NX = 32-MHz differential clock. **Device settings:** CW clock mode = 16X, and 1X and 16X clock buffer in differential mode and ADC in power-down mode. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE (Power)							
$PSRR_{1\ kHz}$	AC power-supply rejection ratio: tone at output relative to tone on supply	100 mV_{PP}, 1-kHz tone on supply	AVDD_1P9		–60		dBc
			AVDD_3P15		–75		
$PSMR_{1\ kHz}$	AC power-supply modulation ratio: intermodulation tone at output resulting from tones at supply and input measured relative to input tone	100 mV_{PP}, 1-kHz tone on supply and –1-dBFS, 5-MHz tone at input	AVDD_1P9		–50		dBc
			AVDD_3P15		–50		

8.7 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. Typical values are at T_A = 25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, external differential load resistance between the LVDS output pair, and R_{LOAD} = 100 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (PDN_FAST, PDN_GBL, RESET, SCLK, SDIN, SEN, TGC_PROF<1>, TGC_PROF<2>, TGC_SLOPE, TGC_UP_DN, TR_EN<1>, TR_EN<2>, TR_EN<3>, TR_EN<4>, TX_TRIG) (1)						
V_{IH}	High-level input voltage		0.75 × max [AVDD_1P9, DVDD_1P8]			V
V_{IL}	Low-level input voltage				0.25 × min [AVDD_1P9, DVDD_1P8]	V
I_{IH}	High-level input current			150		µA
I_{IL}	Low-level input current			150		µA
C_i	Input capacitance			8		pF
DIGITAL OUTPUTS (SDOUT) (1)						
V_{OH}	High-level output voltage		1.6	1.8 (2)		V
V_{OL}	Low-level output voltage			0	0.2	V
z_o	Output impedance			50		Ω
LVDS DIGITAL OUTPUTS (DOUT) (1)						
$\|V_{OD}\|$	Output differential voltage	100-Ω external load connected differentially across DOUT	320	400	480	mV
V_{OS}	Output offset voltage (common-mode voltage of $DOUTP_I$ and $DOUTM_I$)	100-Ω external load connected differentially across DOUT	0.9	1.03	1.15	V

(1) All digital specifications are characterized across operating temperature range but are not tested at production.
(2) When SDOUT operation is performed in VCA die, typical output voltage of SDOUT is 1.9 V.

8.8 Output Interface Timing Requirements

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, differential ADC clock, LVDS load C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, 14-bit ADC resolution, and sample rate = 65 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C.

			MIN	TYP	MAX	UNIT
GENERAL						
t_{AP}	Aperture delay (1)			1.6		ns
δt_{AP}	Aperture delay variation from device to device (at same temperature and supply)			±0.5		ns
t_{APJ}	Aperture jitter with LVPECL clock as input clock			0.5		ps
ADC TIMING						
C_d	ADC latency	Default after reset (1)		8.5		ADC clocks
		Low-latency mode		4.5		
LVDS TIMING (2)						
f_F	Frame clock frequency (1)			f_{CLKIN}		MHz
D_{FRAME}	Frame clock duty cycle			50%		
N_{SER}	Number of bits serialization of each ADC word		12		16	Bits
f_D	Output rate of serialized data	1X output data rate mode		$N_{SER} \times f_{CLKIN}$	1000	Mbps
		2X output data rate mode		$2 \times N_{SER} \times f_{CLKIN}$	1000	
f_B	Bit clock frequency			f_D / 2	500	MHz
D_{BIT}	Bit clock duty cycle			50%		
t_D	Data bit duration (1)		1	1000 / f_D		ns
t_{PDI}	Clock propagation delay (1)			$6 \times t_D + 5$		ns
δt_{PROP}	Clock propagation delay variation from device to device (at same temperature and supply)			±2		ns
t_{ORF}	DOUT, DCLK, FCLK rise and fall time, transition time between –100 mV and +100 mV			0.2		ns
t_{OSU}	Minimum serial data, serial clock setup time (1)			t_D / 2 – 0.4		ns
t_{OH}	Minimum serial data, serial clock hold time (1)			t_D / 2 – 0.4		ns
t_{DV}	Minimum data valid window (3)(1)			t_D – 0.65		ns
TX_TRIG TIMING						
$t_{TX\_TRIG\_DEL}$	Delay between TX_TRIG and TX_TRIGD (4)		0.5		$0.4 \times t_S$ (5)	ns
$t_{SU\_TX\_TRIGD}$	Setup time related to latching TX_TRIG relative to the rising edge of the system clock			0.6		ns
$t_{H\_TX\_TRIGD}$	Hold time related to latching TX_TRIG relative to the rising edge of the system clock			0.4		ns

(1) See Figure 1.
(2) All LVDS specifications are characterized but are not tested at production.
(3) The specification for the minimum data valid window is larger than the sum of the minimum setup and hold times because there can be a skew between the ideal transitions of the serial output data with respect to the transition of the bit clock. This skew can vary across channels and across devices. A mechanism to correct this skew can therefore improve the setup and hold timing margins. For example, the LVDS_DCLK_DELAY_PROG control can be used to shift the relative timing of the bit clock with respect to the data.
(4) TX_TRIGD is the internally delayed version of TX_TRIG that gets latched on the rising edge of the ADC clock.
(5) t_S is the ADC clock period in nanoseconds (ns).

8.9 Serial Interface Timing Requirements(1)

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C.

		MIN	TYP	MAX	UNIT
t_{SCLK} (2)	SCLK period	50			ns
t_{SCLK_H} (2)	SCLK high time	20			ns
t_{SCLK_L} (2)	SCLK low time	20			ns
t_{DSU} (2)	Data setup time	5			ns
t_{DH} (2)	Data hold time	5			ns
t_{SEN_SU} (2)	SEN falling edge to SCLK rising edge	8			ns
t_{SEN_HO} (2)	Time between last SCLK rising edge to SEN rising edge	8			ns
t_{OUT_DV} (3)	SDOUT delay	12	20	28	ns

(1) All serial interface timing specifications are characterized but are not tested at production.
(2) See Figure 104 for more details.
(3) See Figure 105 for more details.

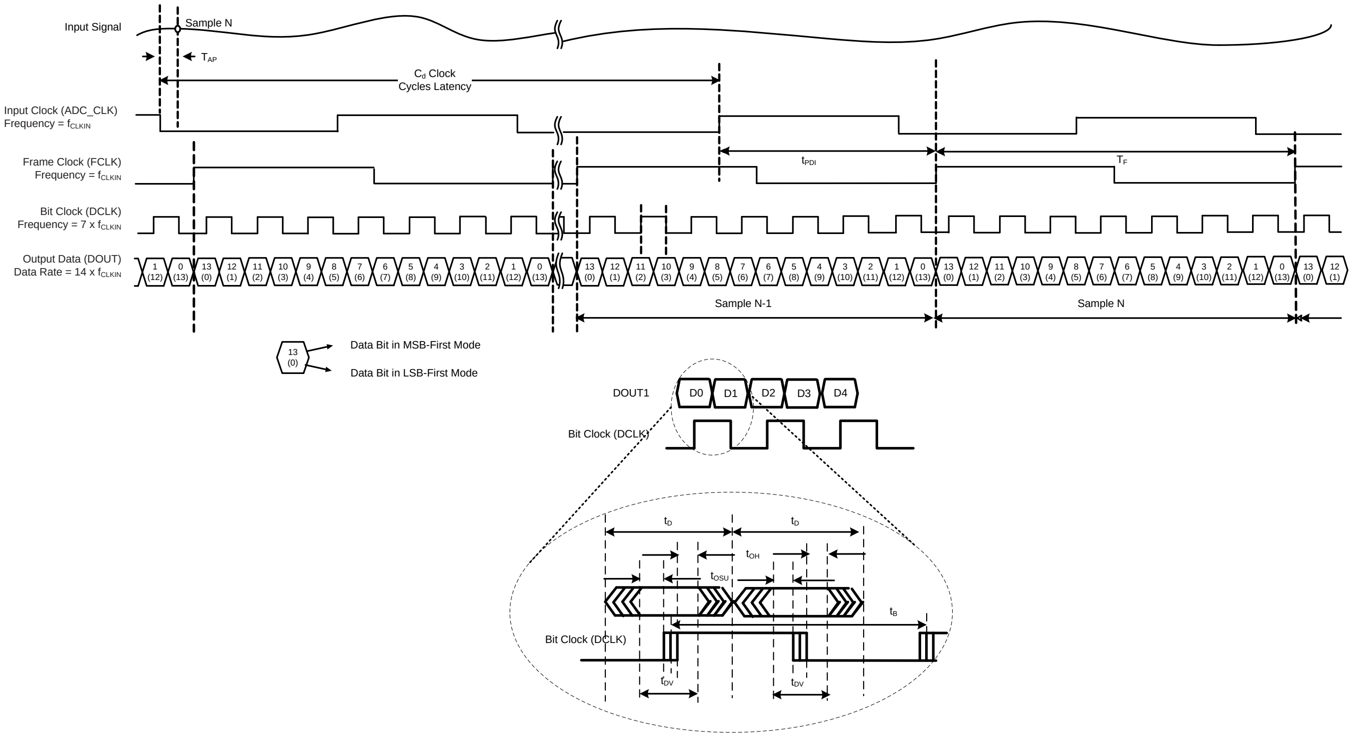
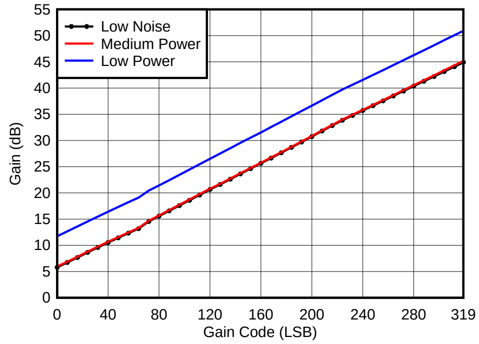


Figure 1. LVDS Output Timing Specification

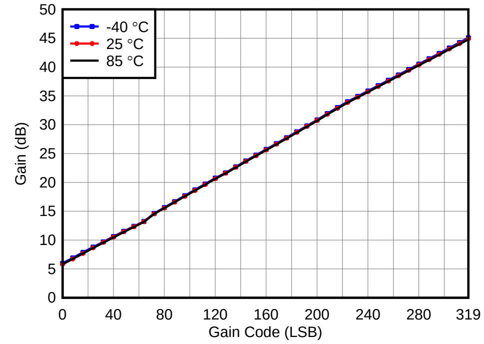
8.10 Typical Characteristics: TGC Mode

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



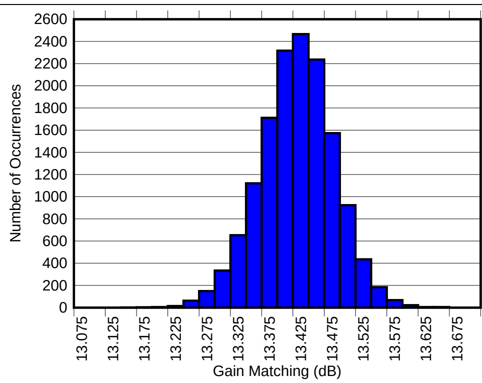
Across power modes

Figure 2. Gain vs Gain Code



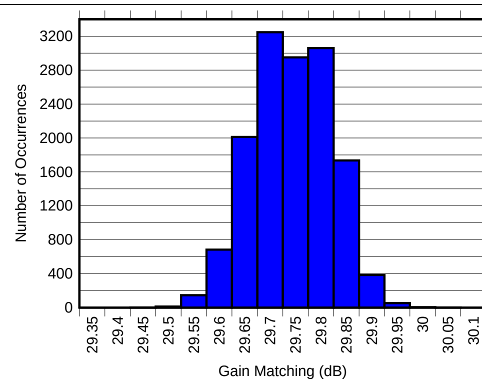
Across temperature

Figure 3. Gain vs Gain Code



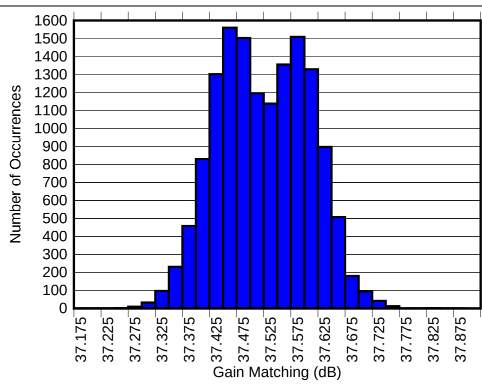
Gain = 14 dB (14288 channels)

Figure 4. Gain Matching Histogram



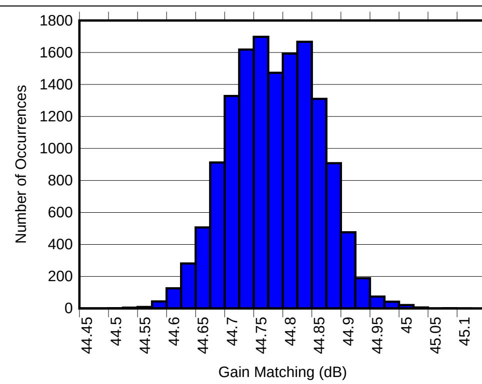
Gain = 30 dB (14288 channels)

Figure 5. Gain Matching Histogram



Gain = 38 dB (14288 channels)

Figure 6. Gain Matching Histogram

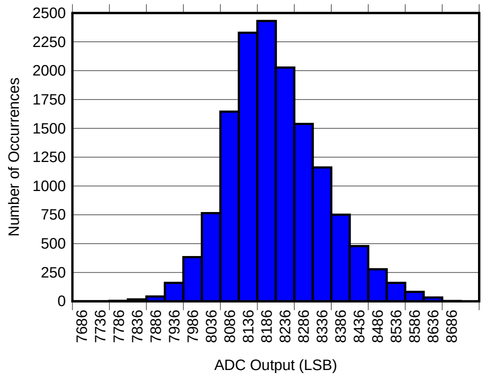


Gain = 45 dB (14288 channels)

Figure 7. Gain Matching Histogram

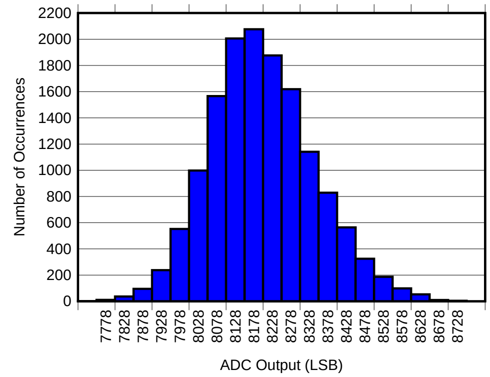
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



Gain = 14 dB (14288 channels)

Figure 8. Output Offset Histogram



Gain = 45 dB (14288 channels)

Figure 9. Output Offset Histogram

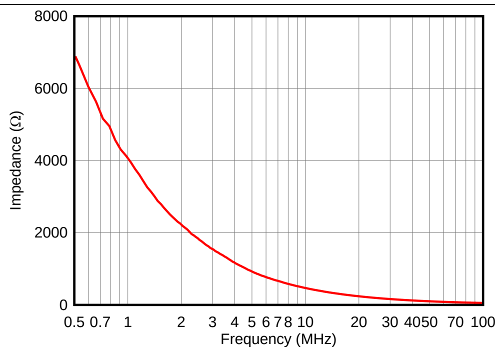


Figure 10. Input Impedance Magnitude vs Frequency

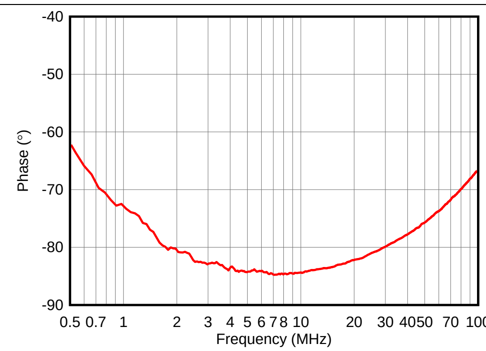
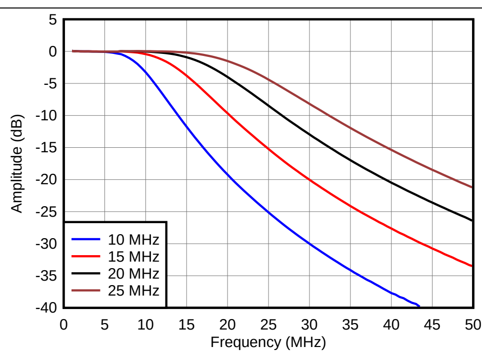
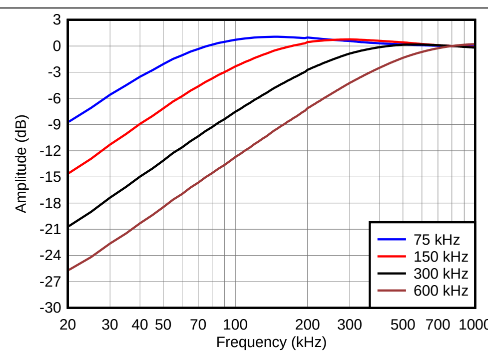


Figure 11. Input Impedance Phase vs Frequency



Across LPF corner settings

Figure 12. Full-Channel, Amplitude Response vs Frequency

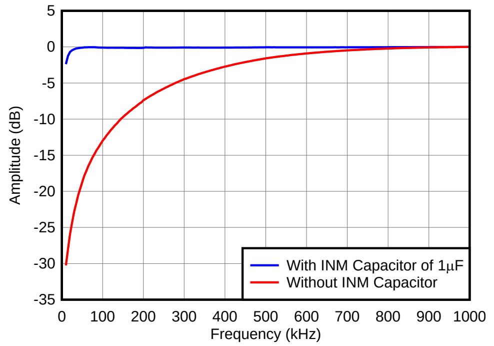


Across LNA HPF corner settings

Figure 13. Full-Channel, Low-Frequency Amplitude Response vs Frequency

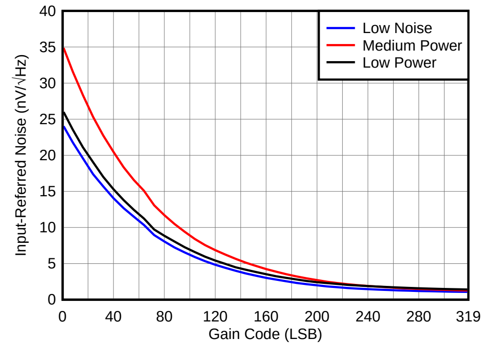
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



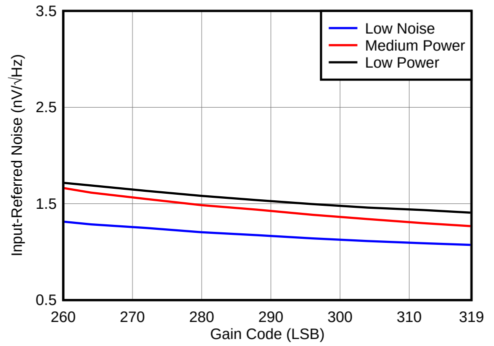
Across INM capacitor

Figure 14. Full-Channel, Low-Frequency Amplitude Response vs Frequency



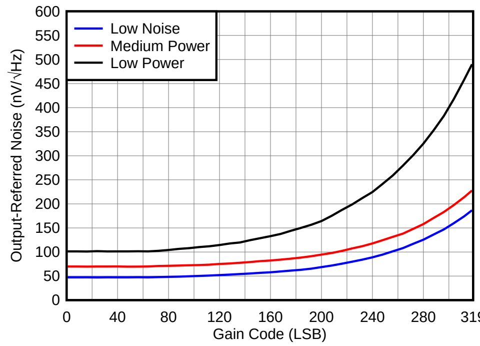
Across power modes

Figure 15. Input-Referred Noise vs Gain Code



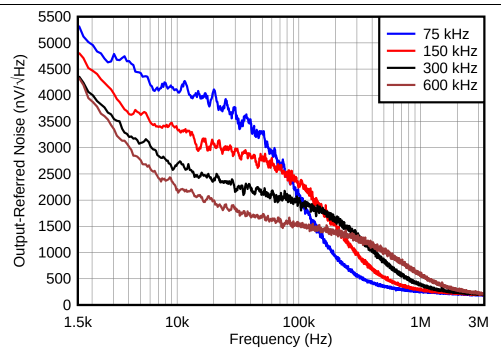
Across power modes

Figure 16. Input-Referred Noise vs Gain Code (Zoomed)



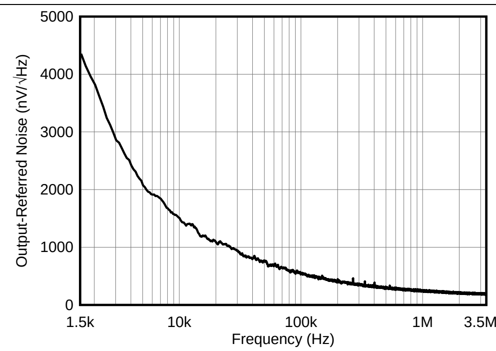
Across power modes

Figure 17. Output-Referred Noise vs Gain Code



Across LNA HPF corner settings

Figure 18. Low-Frequency, Output-Referred Noise vs Frequency



With INMx capacitor = 1 µF

Figure 19. Low-Frequency, Output-Referred Noise vs Frequency

Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.

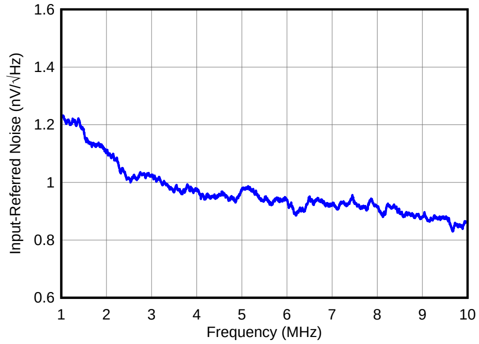


Figure 20. Input-Referred Noise vs Frequency

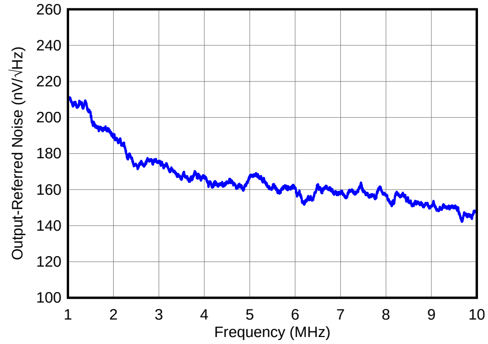
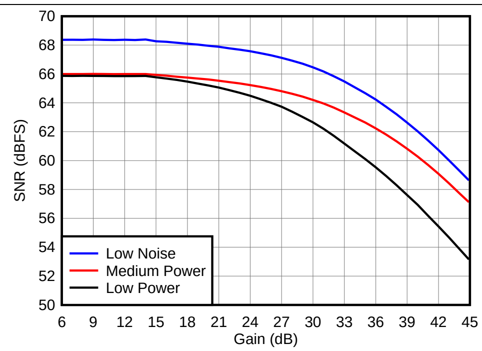
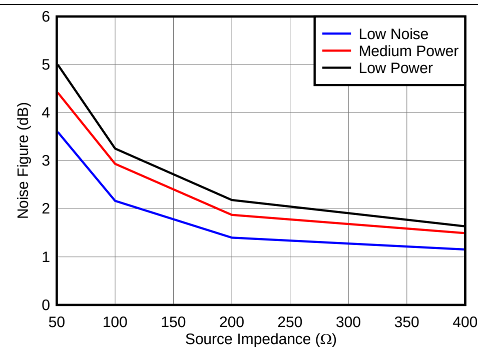


Figure 21. Output-Referred Noise vs Frequency



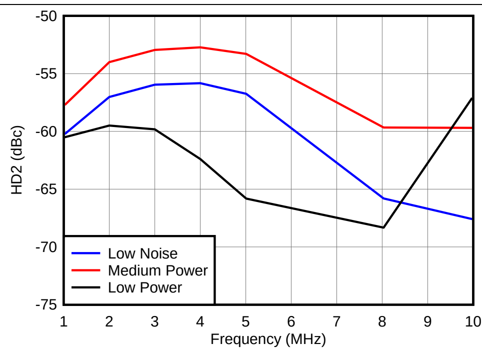
Across power modes

Figure 22. Signal-to-Noise Ratio vs Gain



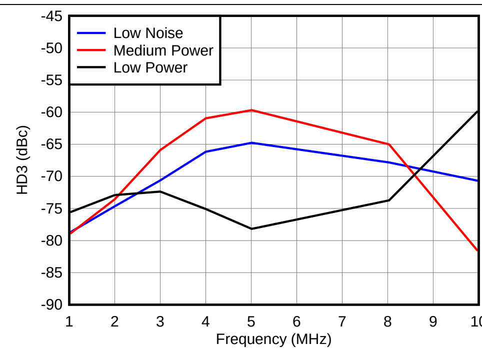
Across power modes

Figure 23. Noise Figure vs Source Impedance



Across power modes

Figure 24. Second-Order Harmonic Distortion vs Frequency

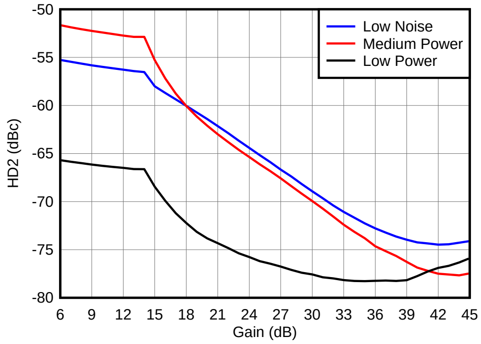


Across power modes

Figure 25. Third-Order Harmonic Distortion vs Frequency

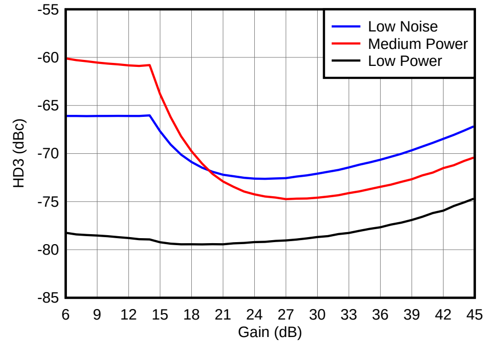
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



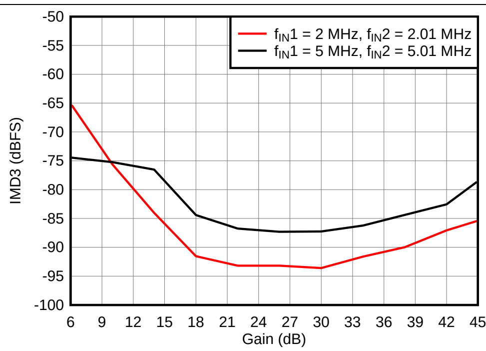
Across power modes

Figure 26. Second-Order Harmonic Distortion vs Gain



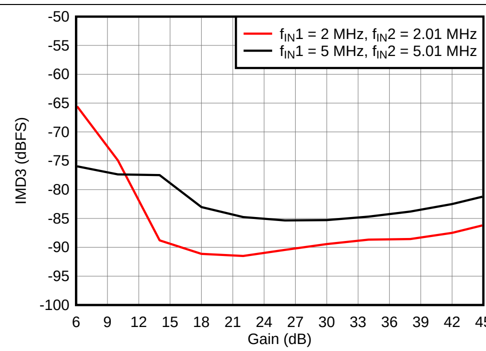
Across power modes

Figure 27. Third-Order Harmonic Distortion vs Gain



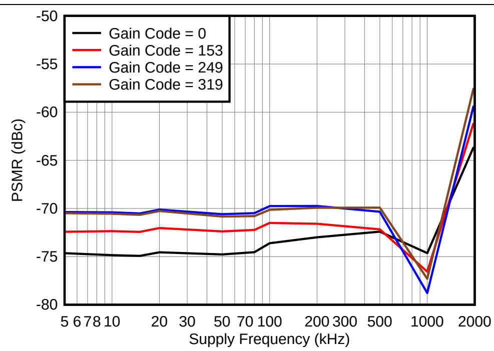
f_{OUT1} = –1 dBFS, f_{OUT2} = –21 dBFS

Figure 28. IMD3 vs Gain



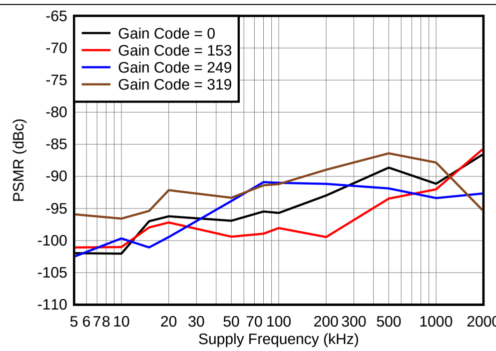
f_{OUT1} = –7 dBFS, f_{OUT2} = –7 dBFS

Figure 29. IMD3 vs Gain



Across gain codes

Figure 30. AVDD_1P9 Power-Supply Modulation Ratio vs 100-mV$_{PP}$ Supply Noise Frequencies

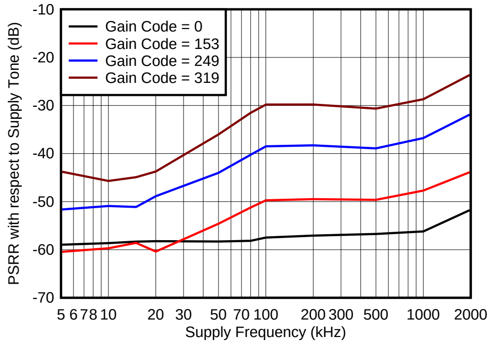


Across gain codes

Figure 31. AVDD_3P15 Power-Supply Modulation Ratio vs 100-mV$_{PP}$ Supply Noise Frequencies

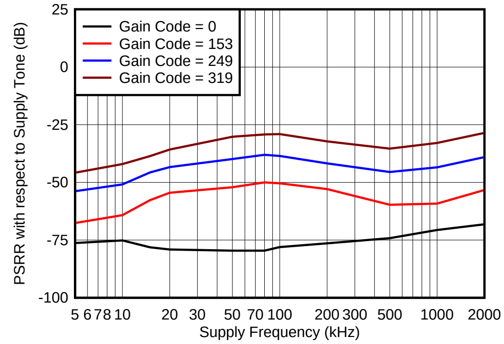
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



Across gain codes

Figure 32. AVDD_1P9 Power-Supply Rejection Ratio vs 100-mV$_{PP}$ Supply Noise Frequencies



Across gain codes

Figure 33. AVDD_3P15 Power-Supply Rejection Ratio vs 100-mV$_{PP}$ Supply Noise Frequencies

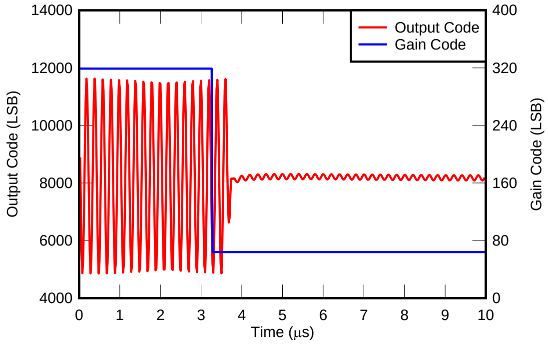


Figure 34. Output and Gain Code Step Response vs Time

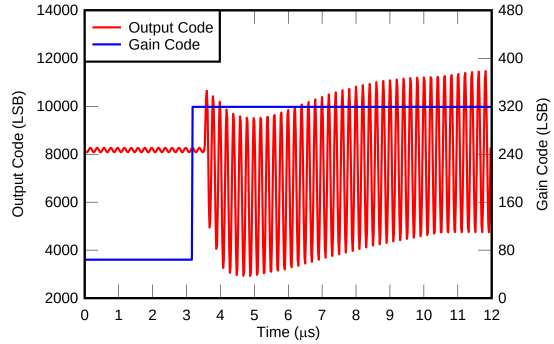
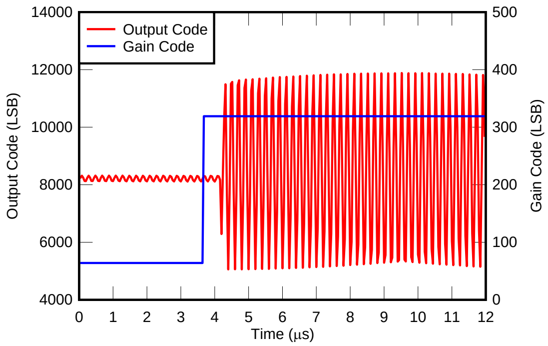


Figure 35. Output and Gain Code Step Response vs Time



With constant-current mode enabled (TGC_CONS register bit = 1)

Figure 36. Output and Gain Code Step Response vs Time

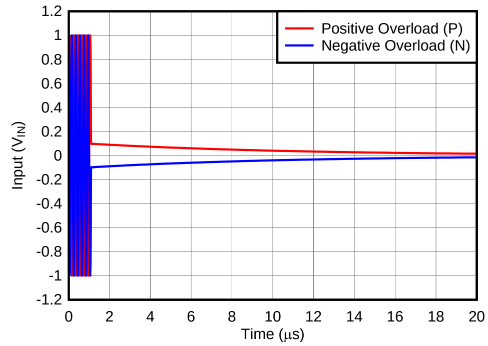
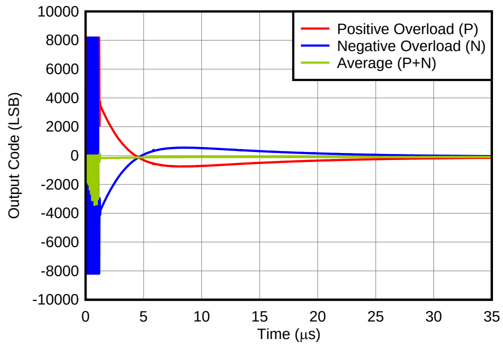


Figure 37. Pulse Inversion Asymmetrical Input vs Time

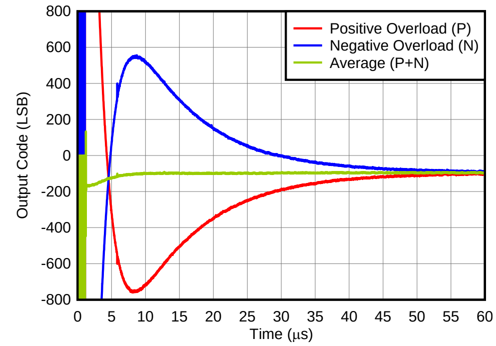
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



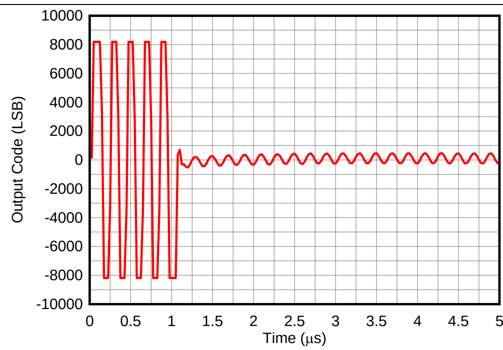
For the input in Figure 37, gain = 21 dB, across positive and negative overload

Figure 38. Device Pulse Inversion Output vs Time



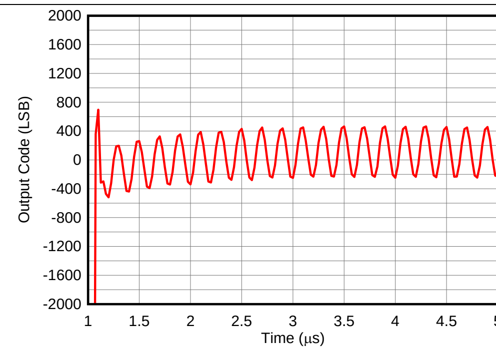
For the input in Figure 37, gain = 21 dB, across positive and negative overload

Figure 39. Device Pulse Inversion Output vs Time (Zoomed)



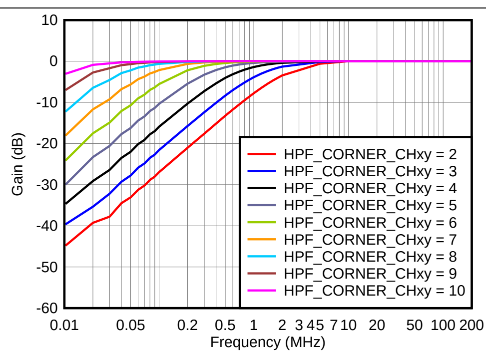
V_{IN} = large amplitude (50 mV_{PP}) followed by small amplitude (500 μV_{PP})

Figure 40. Output Code Overload Recovery vs Time



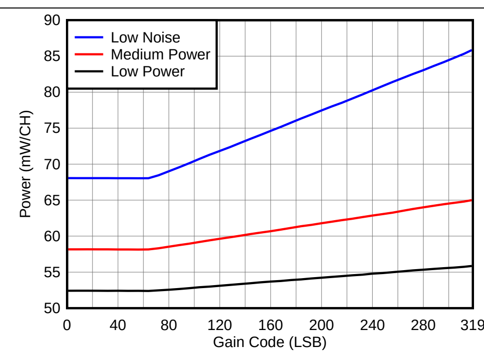
V_{IN} = large amplitude (50 mV_{PP}) followed by small amplitude (500 μV_{PP})

Figure 41. Output Code Overload Recovery vs Time (Zoomed)



Across digital HPF corner settings

Figure 42. Digital High-Pass Filter Gain Response vs Frequency

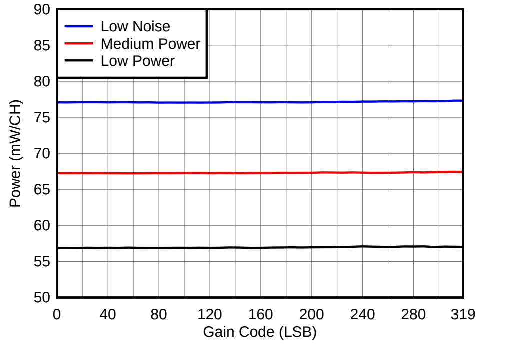


Across power modes

Figure 43. Device Power vs Gain Code

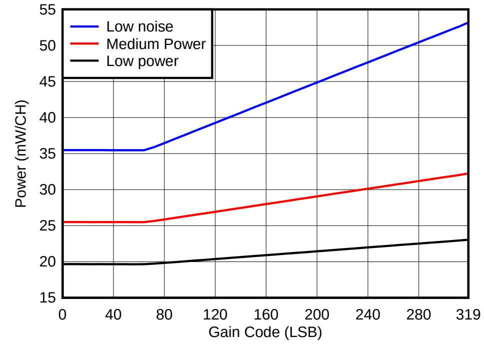
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



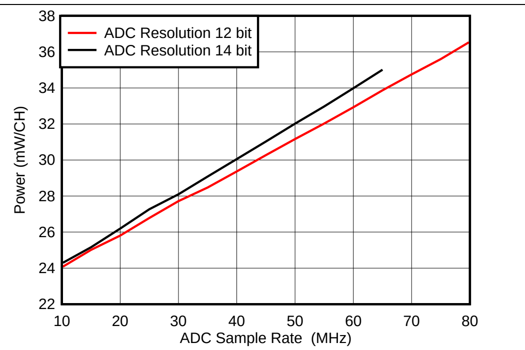
Across power modes with constant-current mode enabled (TGC_CONS register bit = 1)

Figure 44. Device Power vs Gain Code



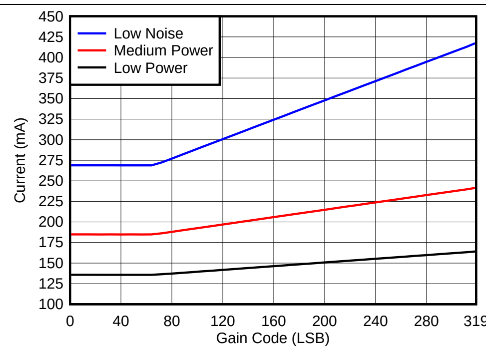
Across power modes

Figure 45. VCA Power vs Gain Code



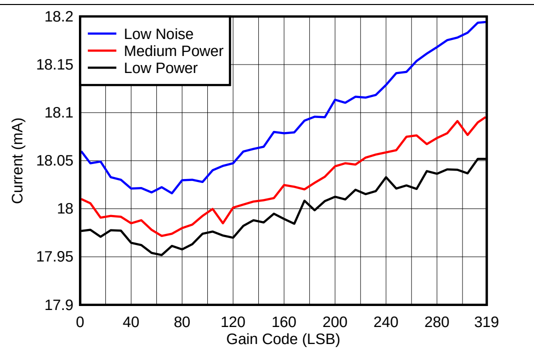
Across ADC resolution

Figure 46. ADC Power vs ADC Sample Rate



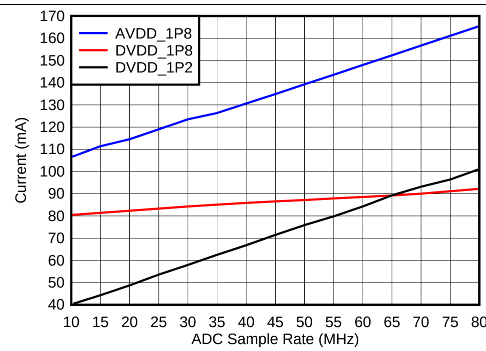
Across power modes

Figure 47. AVDD_1P9 Supply Current vs Gain Code



Across power modes

Figure 48. AVDD_3P15 Supply Current vs Gain Code

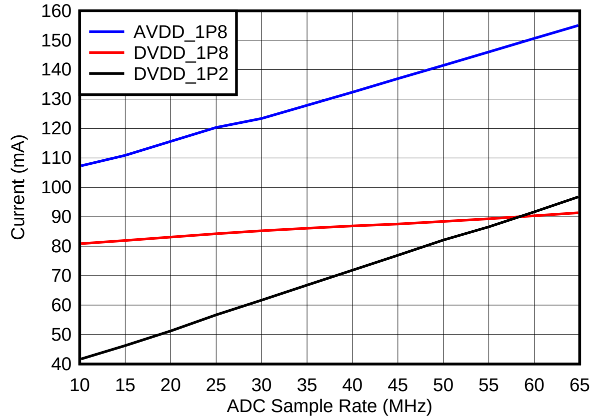


12-bit resolution

Figure 49. AVDD_1P8, DVDD_1P8 and DVDD_1P2 Supply Current vs ADC Sample Rate

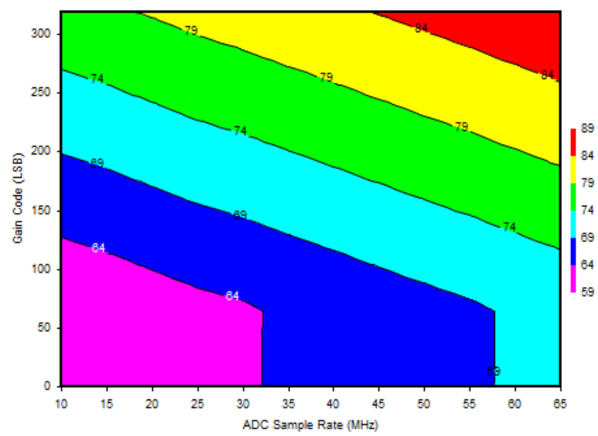
Typical Characteristics: TGC Mode (continued)

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal is ac-coupled to INP with a 10-nF capacitor and is applied with source resistance R_S = 50 Ω at frequency f_{IN} = 5 MHz, and a 50-MHz differential clock is applied on ADC_CLK. **Device settings:** gain code = 319 (total gain = 45 dB), LPF filter cutoff frequency = 15 MHz, low-noise mode, 14-bit ADC resolution, LVDS interface to capture ADC data, output amplitude V_{OUT} = –1 dBFS, and SNR is measured from 750 kHz to Nyquist bandwidth. Minimum and maximum values are specified across the full temperature range.



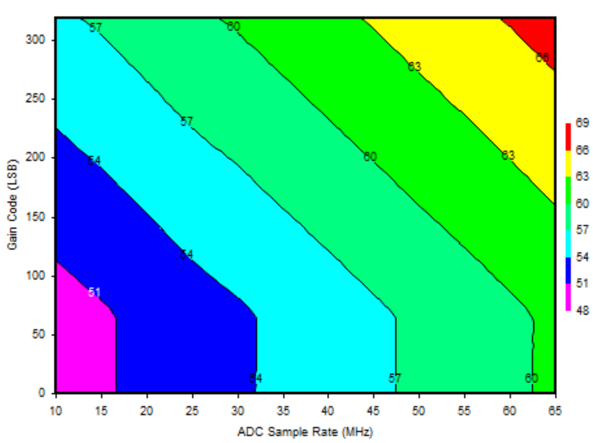
14-bit resolution

Figure 50. AVDD_1P8, DVDD_1P8 and DVDD_1P2 Supply Current vs ADC Sample Rate



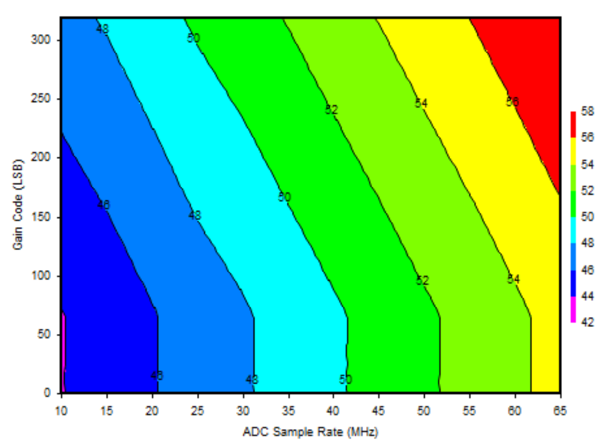
Low-noise mode

Figure 51. Total Power Dissipation (mW/Ch) Contour vs ADC Sample Rate and Gain Code



Medium-power mode

Figure 52. Total Power Dissipation (mW/Ch) Contour vs ADC Sample Rate and Gain Code

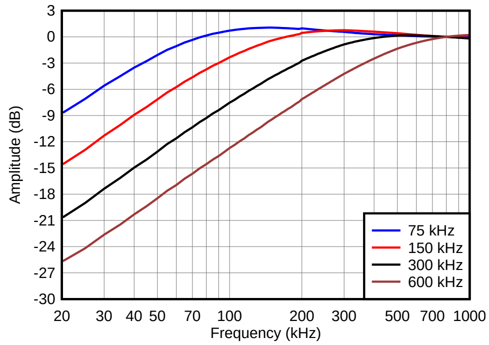


Low-power mode

Figure 53. Total Power Dissipation (mW/Ch) Contour vs ADC Sample Rate and Gain Code

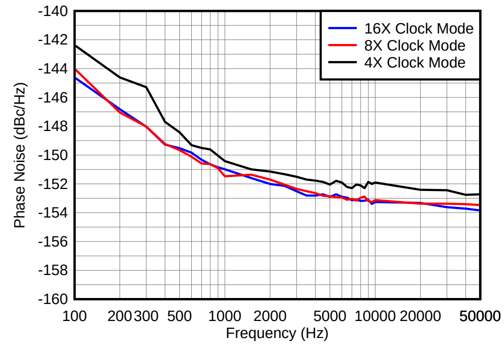
8.11 Typical Characteristics: CW Mode

At T_A = 25°C, unless otherwise noted. **Supply:** AVDD_1P8 = 1.8 V, AVDD_1P9 = 1.9 V, AVDD_3P15 = 3.15 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V. **Input to the device:** input signal = 2 MHz, CW_CLK1X = 2-MHz differential, and CW_CLK_NX = 32-MHz differential. **Device settings:** CW clock mode = 16X, and 1X and 16X clock buffer in differential mode, and ADC in power-down mode. Minimum and maximum values are specified across the full temperature range.



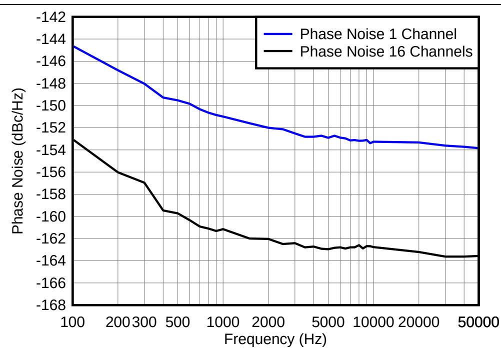
Across LNA HPF corner settings

Figure 54. Full-Channel, Low-Frequency Amplitude Response vs Frequency



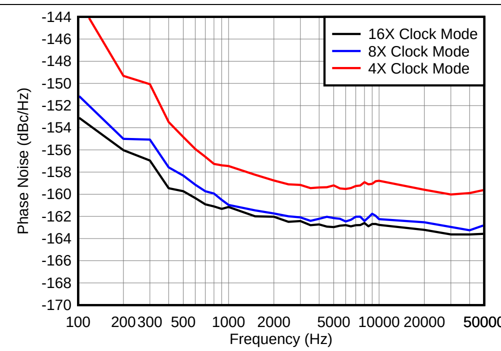
f_{IN} = 2 MHz, one channel across CW clock modes

Figure 55. CW Phase Noise vs Frequency



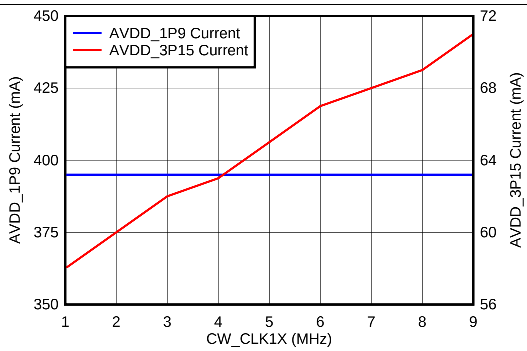
f_{IN} = 2 MHz, across one channel and 16 channels

Figure 56. CW Phase Noise vs Frequency



f_{IN} = 2 MHz, 16 channels across CW clock modes

Figure 57. CW Phase Noise vs Frequency



Across all CW clock modes

Figure 58. AVDD_1P9 and AVDD_3P15 Supply Current vs CW Clock Frequency

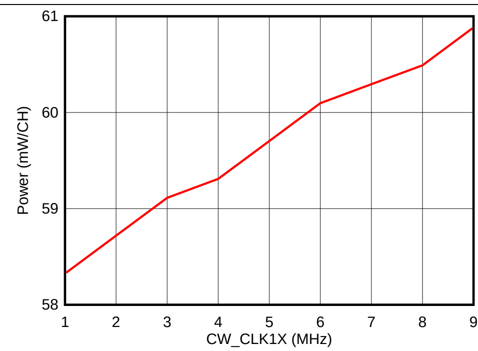


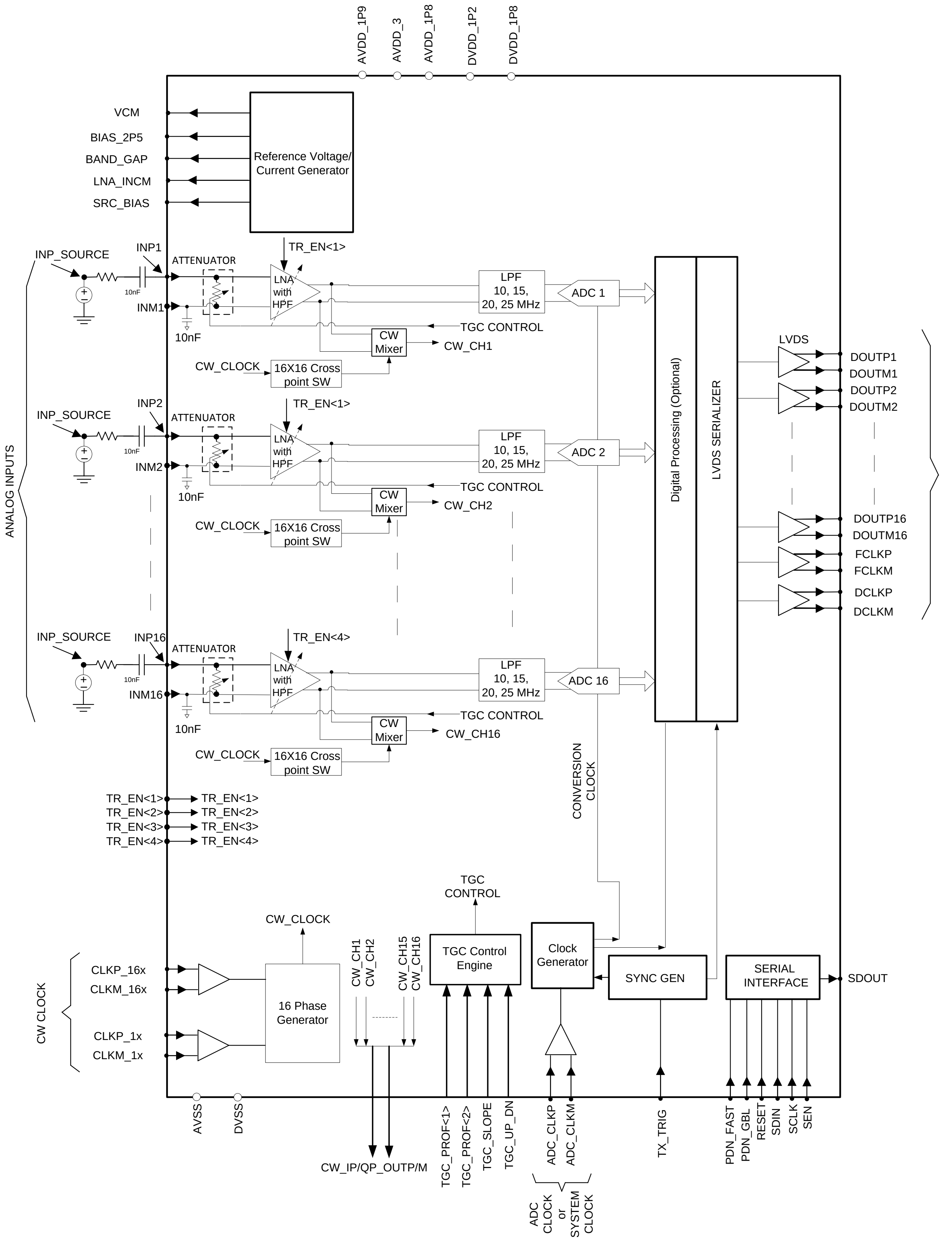
Figure 59. Power vs CW 1X Clock Frequency

9 Detailed Description

9.1 Overview

The AFE5816 is a highly-integrated, analog front-end (AFE) solution specifically designed for ultrasound systems where high performance and higher integration are required. The device integrates a complete time-gain compensation (TGC) imaging path and a continuous-wave Doppler (CWD) path. The device also enables users to select from a variety of power and noise combinations to optimize system performance. The device contains 16 dedicated channels, each comprising an attenuator, low-noise amplifier (LNA), low-pass filter (LPF), and either a 14-bit or 12-bit analog-to-digital converter (ADC). At the output of the 16 ADCs is a low-voltage differential signaling (LVDS) serializer to transfer digital data. In addition, the device also contains a continuous wave (CW) mixer. Multiple features in the device are suitable for ultrasound applications (such as programmable termination, individual channel control, fast power-up and power-down response, fast and consistent overload recovery, and integrated digital processing). Therefore, this device brings premium image quality to ultra-portable, handheld systems all the way up to high-end ultrasound systems. In addition, the signal chain of the device can handle signal frequencies as low as 10 kHz and as high as 25 MHz. This broad analog frequency range enables the device to be used in both sonar and medical applications; see the *Functional Block Diagram* section for a simplified function block diagram.

9.2 Functional Block Diagram



9.3 Feature Description

The device supports two signal chains: TGC mode and CW mode. Table 2 describes the functionality of various blocks in CW and TGC mode.

Table 2. Various Block Functionality in TGC and CW Mode

BLOCK	TGC MODE		CW MODE	
	ENABLED, DISABLED	COMMENT	ENABLED, DISABLED	COMMENT
Attenuator	Enabled	Attenuator supports attenuation range of 8 dB to 0 dB	Disabled	In CW mode, the attenuator is disabled automatically
Attenuator high-pass filter	Enabled	—	Disabled	—
Low-noise amplifier (LNA)	Enabled	LNA supports gain range of 14 dB to 45 dB	Enabled	LNA supports a fixed gain of 18 dB
LNA high-pass filter	Enabled	—	Enabled	—
Low pass filter (LPF)	Enabled	—	Disabled	In CW mode, the LPF is disabled automatically
Digital TGC (DTGC)	Enabled	—	Disabled	In CW mode, the DTGC is disabled automatically
Analog-to-digital converter (ADC)	Enabled	—	Enabled	In CW mode, the ADC remains active. The ADC can be powered down in CW mode using a power-down pin or power-down register bit.

9.3.1 Attenuator

The first stage of the signal chain is an attenuator followed by a low-noise amplifier (LNA). Fundamentally, an attenuator functions as a time-varying passive termination. In ultrasound imaging systems, near-field reflected signals are of very high amplitude. This high-amplitude signal can be attenuated using an attenuator in order to bring the signal amplitude down to within the LNA input amplitude range. The attenuator supports time-gain compensation [that is, the attenuation level is from –8 dB to 0 dB with time in steps of 0.125 dB (64 steps)]. The attenuation level is controlled by the TGC control engine in the device.

9.3.1.1 Implementation

The attenuator is implemented as a resistor divider network that uses the principle of voltage division between a source resistance (R_S) and attenuator resistance (R_{ATTEN}); see Figure 60. At the signal frequency, attenuation provided by this resistor network is given by Equation 1:

$$\text{Attenuation} = \frac{V_{INP}}{V_{INP\_SOURCE}} = \frac{R_{ATTEN}}{R_S + R_{ATTEN}} \quad (1)$$

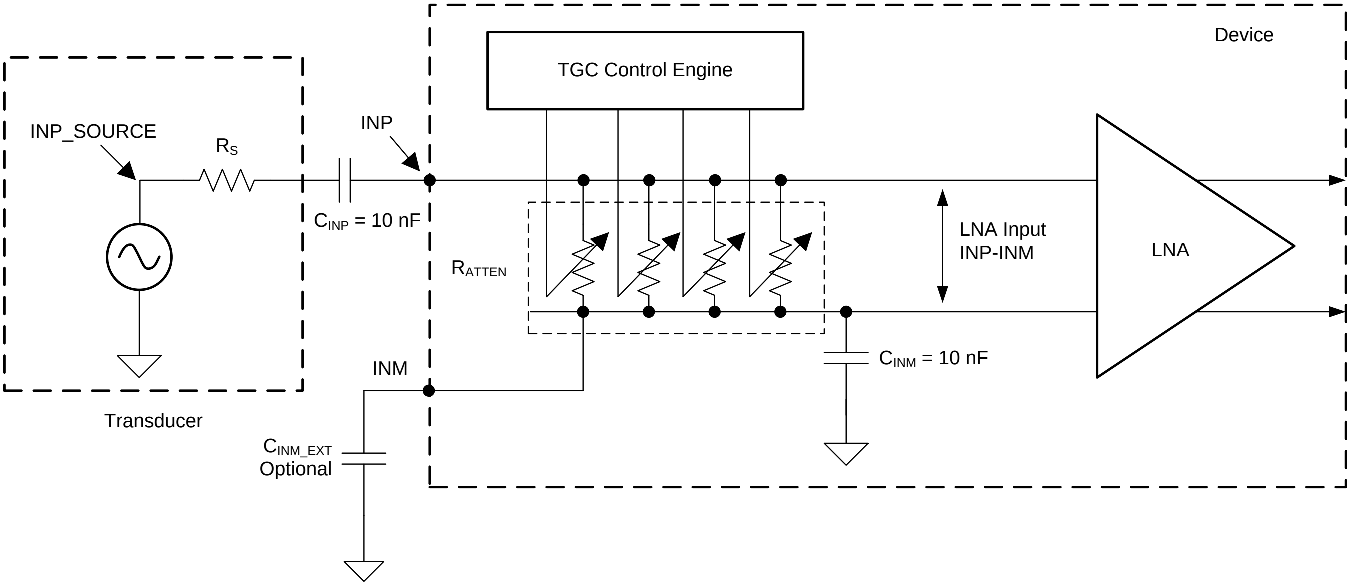


Figure 60. Attenuator Block Diagram

In Equation 1, the value of the R_{ATTEN} resistor is controlled by the TGC control engine. Further details of the TGC control engine are provided in the *Digital TGC (DTGC)* section. The correct R_{ATTEN} network must be selected for a given R_S using the INP_RES_SEL register because attenuation is a function of both source resistance (R_S) and attenuator resistance (R_{ATTEN}). The range of input resistance R_S supported is listed in Table 120.

NOTE

The attenuator block remains active only in TGC mode. The attenuator block is disabled in CW mode.

9.3.1.2 Maximum Signal Amplitude Support

In TGC mode, the maximum input signal amplitude of the low-noise amplifier is approximately 400 mV_{PP}. In Figure 60, the source is modeled as a voltage source at the INP_SOURCE node in series with its (source) impedance R_S. The attenuation is achieved by the voltage division between the series combination of the source impedance R_S and the attenuator resistance a R_{ATTEN}. Therefore, the maximum signal amplitude supported at the INP_SOURCE node is given by 400 mV_{PP} divided by the attenuation. For a given value of source resistance R_S, the attenuator provides the maximum attenuation of 8 dB. Thus, the maximum signal supported at the INP_SOURCE node is 1 V_{PP}.

9.3.1.3 Attenuator High-Pass Filter (ATTEN HPF)

A high-pass filter can be realized through the attenuator. The frequency response of the high-pass filter is governed by the C_{INM} (internal to the device), C_{INM_EXT} (optional and external to the device), and C_{INP} (external ac-coupling capacitor) capacitors, and the source resistance R_S and attenuator resistance R_{ATTEN}.

For the input circuit shown in Figure 60, the LNA input is given by Equation 2:

$$\frac{V_{INP}-V_{INM}}{V_{INP\_SOURCE}}=\frac{R_{ATTEN}}{R_S+R_{ATTEN}}\times\frac{s\times\left(R_S+R_{ATTEN}\right)\times\left(\frac{C_{INP}\times C_{INM\_T}}{C_{INP}+C_{INM\_T}}\right)}{1+s\times\left(R_S+R_{ATTEN}\right)\times\left(\frac{C_{INP}\times C_{INM\_T}}{C_{INP}+C_{INM\_T}}\right)}$$

where

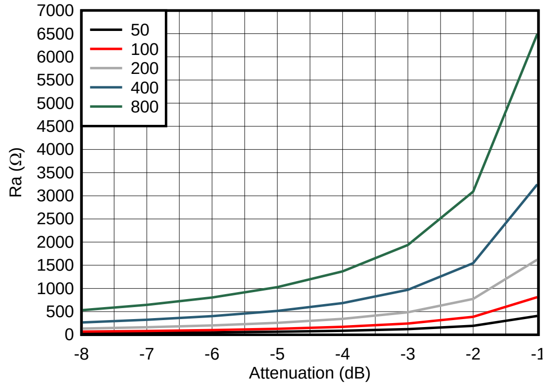
- C_{INM_T} represents the total capacitor (= C_{INM} + C_{INM_EXT}) at the INM node. (2)

Equation 2 describes a high-pass response with a corner frequency given by Equation 3:

$$[1 / (R_S + R_{ATTEN})] \times [(C_{INP} + C_{INM\_T}) / (C_{INP} \times C_{INM\_T})] \quad (3)$$

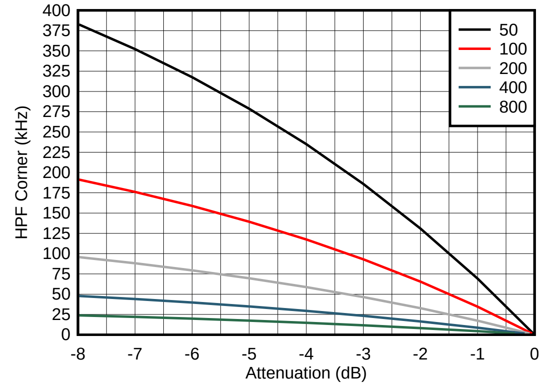
Therefore, when R_{ATTEN} changes with the TGC, the HPF cutoff frequency also changes.

Figure 61 shows typical values of R_{ATTEN} across attenuation and INP_RES_SEL settings. Figure 62 and Figure 63 show the HPF corner frequency across attenuation and INP_RES_SEL settings for C_{INP} = C_{INM_T} = 10 nF and C_{INP} = C_{INM_T} = 1 µF, respectively. For low-frequency application systems (for example, sonar systems that require a very-low, high-pass filter corner), larger value capacitors of C_{INP} and C_{INM_EXT} can be used in order to reduce the HPF corner frequency.



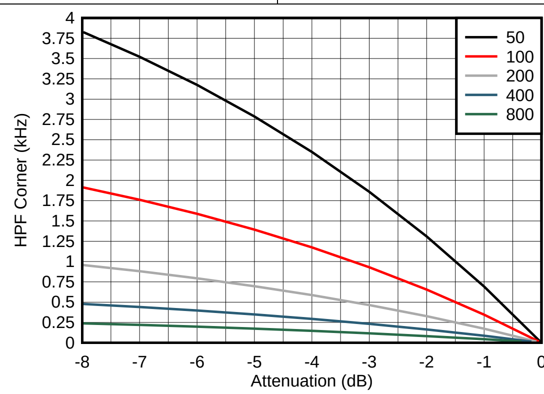
Across INP_RES_SEL register settings

Figure 61. Attenuation Resistance vs Attenuation



Across INP_RES_SEL register settings, C_{INP} = C_{INM_T} = 10 nF

Figure 62. HPF Corner vs Attenuation



Across INP_RES_SEL register settings, C_{INP} = C_{INM_T}= 1 µF

Figure 63. HPF Corner vs Attenuation

9.3.2 Low-Noise Amplifier (LNA)

In many high-gain systems, a LNA is critical to achieve overall performance. The device uses a proprietary architecture and a metal-oxide-semiconductor field-effect transistor (MOSFET) input transistor to achieve exceptional low-noise performance when operating on a low-quiescent current. The LNA takes a single-ended input signal and converts it to a differential output signal.

9.3.2.1 Input Signal Support in TGC Mode

In TGC mode, the LNA supports time-gain compensation [that is, the LNA gain can be changed from 14 dB to 45 dB in steps of 0.125 dB (256 steps total) with time]. Similar to the attenuator, the LNA gain is also controlled by the TGC control engine. The LNA supply current changes with gain; see Figure 41. The device output shows ringing in the gain step response because the LNA supply current changes with gain; see Figure 32. To avoid such ringing, the LNA supply current can be made constant across gain by enabling the constant-current TGC mode using the EN_CONS_CUR register; see Figure 33. Using the constant-current TGC mode is recommended when LNA gain is changed from minimum gain to maximum gain in less than 10 µs (that is, when the rate of change of the LNA gain is greater than 3.1 dB per µs).

In TGC mode, the maximum differential swing supported at the LNA output is 2 V_{PP}. Therefore, the maximum swing supported at the LNA input is given by 2 V_{PP} divided by the LNA gain. For an LNA gain of 14 dB, the maximum swing supported at the LNA input is 400 mV_{PP}.

9.3.2.2 Input Signal Support in CW Mode

In CW mode, the LNA is automatically configured to a 18-dB, fixed-gain mode. In CW mode, the LNA supports a maximum linear input range of 300 mV_{PP}.

9.3.2.3 Input Circuit

In both CW and TGC modes, the LNA input pin (INPx) is internally biased at approximately 1 V. AC-couple the input signal to the INPx pin with an adequately-sized capacitor, C_{INP}; a 10-nF capacitor is recommended. For low-frequency applications, a 1-µF capacitor is recommended for both C_{INP} and C_{INM_EXT}. The electrical interface of the input attenuator and the LNA to the external world is shown in Figure 64.

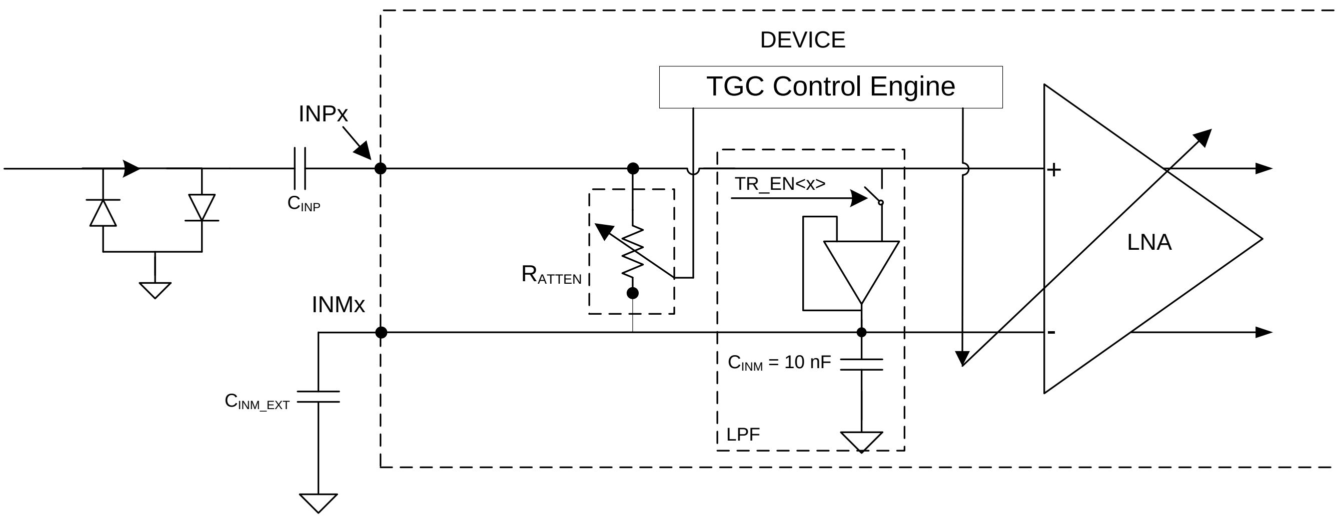


Figure 64. Device Input Circuit

9.3.2.4 LNA High-Pass Filter (LNA HPF)

The LPF circuit in Figure 64 is a low-pass transfer function between the positive and negative inputs of the LNA. The LPF results in a high-pass transfer function between the LNA input and output and can be used to reject unwanted low-frequency leakage signal from the transducer. The high-pass filter in the LNA is active for both CW and TGC mode. The effective corner frequency of the HPF is determined by the capacitor connected at the INMx pin of the device. Internal to the device, a 10-nF capacitor is connected at the INMx node. A large capacitor (such as 1 µF) can be connected externally at the INMx pin for setting the low corner frequency (< 2 kHz) of the LNA dc offset correction circuit. By default, a capacitor is not required to be connected at the INMx pin. To disable this HPF, set the LNA_HPF_DIS register bit to 1. This bit powers down the unity feedback buffer connected between positive and negative input of the LNA shown in Figure 64. For a given INMx capacitor, the corner frequency of the HPF can be programmed using the LNA_HPF_PROG bit. Table 3 lists the HPF corner frequency as a function of the C_{INM_EXT} capacitor connected at the INMx pin across various LNA_HPF_PROG bit settings.

Table 3. HPF Corner Programming Bits

LNA_HPF_PROG	HPF CORNER WITHOUT CONNECTING A CAPACITOR AT THE INMx PIN	HPF CORNER WITH A CINM_EXT CAPACITOR CONNECTED AT THE INMx PIN
00	75 kHz	75 kHz × 10 nF / (10 nF + C_{INM_EXT})
01	150 kHz	150 kHz × 10 nF / (10 nF + C_{INM_EXT})
10	300 kHz	300 kHz × 10 nF / (10 nF + C_{INM_EXT})
11	600 kHz	600 kHz × 10 nF / (10 nF + C_{INM_EXT})

9.3.2.4.1 Disconnecting the LNA HPF During Overload

In ultrasound systems, the device detects a large-amplitude, overloaded signal during transmit phase. The AFE used for such systems is expected to quickly switch from a high overloaded state to a normal state.

To implement a very low LNA high-pass filter corner, the device uses a large capacitor at the INMx node. The INMx node voltage changes as a result of the large overload signal, which ultimately leads to a low-frequency settling at the device output. To avoid any significant disturbance on the INMx node voltage change resulting from an overloaded input signal, the LNA HPF circuit can be disconnected from the INPx pin by using a series switch; see Figure 64. This switch is controlled by the TR_EN<x>pins (TR_EN<1>, TR_EN<2>, TR_EN<3>, and TR_EN<4> control channels 1 to 4, 5 to 8, 9 to 13, and 14 to 16, respectively). Figure 65 shows an example of TR_EN<x> control signals. Figure 66, Figure 67, Figure 68, and Figure 69 illustrate a positive overload input signal, negative overload input signal, and the corresponding device output for both without and with TR_EN<x> pin functionality, respectively. The TR_EN<x> pin functionality refers to using a low-going pulse on TR_EN<x> during an overload input signal to disconnect the LNA HPF. This functionality is useful when there is not a low-frequency signal immediately after an overload signal.

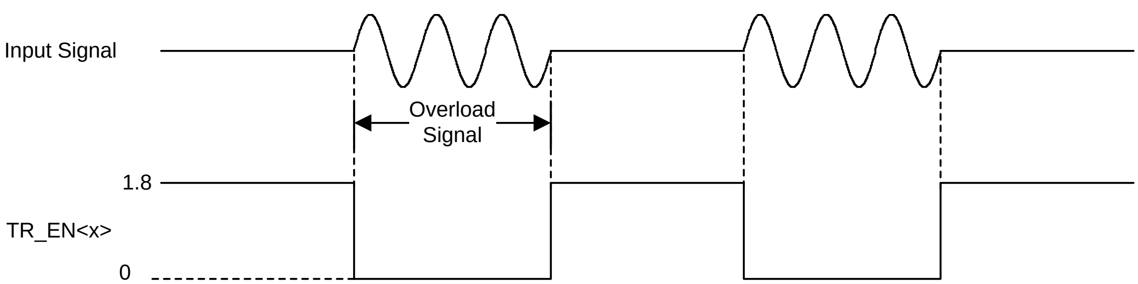


Figure 65. TR_EN Control Signal

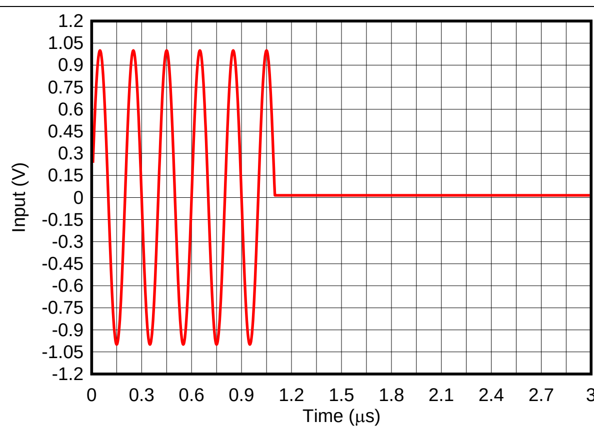


Figure 66. Pulse Inversion Positive Input vs Time

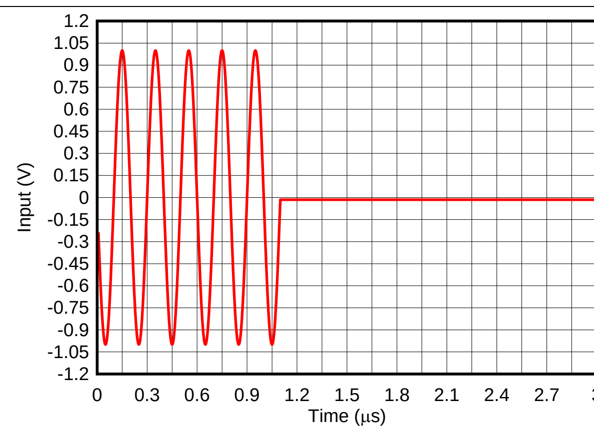


Figure 67. Pulse Inversion Negative Input vs Time

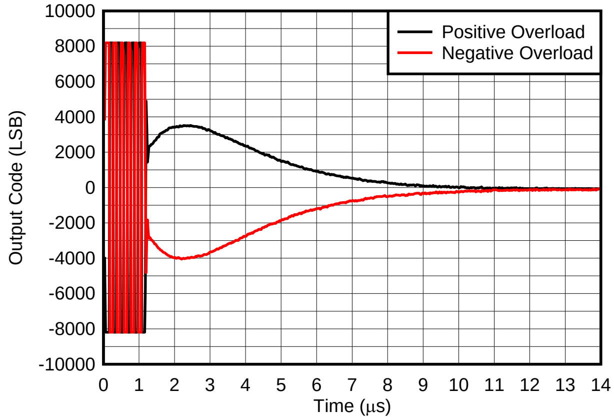


Figure 68. Overload Recovery Output vs Time Without TR_EN Functionality

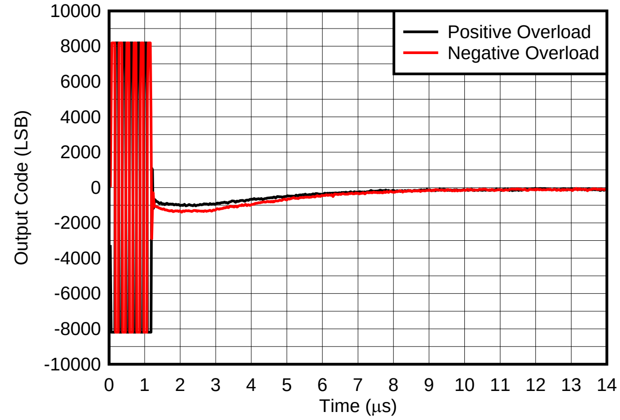


Figure 69. Overload Recovery Output vs Time with TR_EN Functionality

9.3.2.5 LNA Noise Contribution

The noise specification is critical for the LNA and determines the dynamic range of the entire system. The device LNA achieves low power, an exceptionally low-noise voltage of 0.95 nV/√Hz at 45-dB gain, and a low-current noise of 1.2 pA/√Hz in low-noise mode.

Voltage noise is the dominant source of noise; however, the LNA current noise flowing through the source impedance (R_S) generates additional voltage noise. The total LNA noise can be computed with Equation 4.

$$LNA\_Noise_{total} = \sqrt{V^2_{LNAnoise} + R^2_S \times I^2_{LNAnoise}} \quad (4)$$

The device achieves a low noise figure (NF) over a wide range of source resistances; see Figure 23.

9.3.3 High-Pass Filter (HPF)

Two high-pass filters (HPFs) exist in the signal chain. The first high-pass filter is the HPF that is part of the input attenuator and the other filter is the HPF in the low-noise amplifier (LNA). In the preceding sections (see the *LNA High-Pass Filter (LNA HPF)* and *Attenuator High-Pass Filter (ATTEN HPF)* sections) the HPF corner expression of the attenuator and LNA is explained, assuming only a single HPF is active at a time. If both HPFs are enabled at the same time, the overall HPF corner is approximately given by the maximum of the two corner frequencies. For instance, if the HPF corner of the attenuator is (f_{ATTEN}) Hz and the HPF corner of the LNA is (f_{LNA}) Hz, the overall HPF corner is given by the maximum of (f_{ATTEN}, f_{LNA}) Hz. In CW mode, the attenuator HPF is disabled and the LNA HPF remains active so the overall HPF corner is given by f_{LNA}.

9.3.4 Low-Pass Filter (LPF)

In TGC mode, the LNA output is fed to a low-pass filter (LPF). The LPF is designed as a differential, active, third-order filter with Butterworth characteristics and a typical 18 dB per octave roll-off. Programmable through the serial interface, the –3-dB corner frequency can be set to different combinations across power modes, as shown in Table 4. The filter bandwidth is set for all channels simultaneously.

Note that in CW mode, the LPF is automatically disabled.

Table 4. LPF Corner Frequency Combinations

POWER MODE	LPF CORNER FREQUENCY (MHz)
Low noise	10, 15, 20, 25
Medium power	10, 15, 20, 25
Low power	5, 7.5, 10, 12.5

9.3.5 Digital TGC (DTGC)

This section discusses the operation of the digital TGC control engine. The DTGC is relevant only in TGC mode; see the *DTGC Register Map* for register settings and descriptions.

9.3.5.1 DTGC Overview

As described previously, the device consists of a programmable attenuator, a variable-gain LNA, and a TGC control engine that controls the gain of the device, as shown in Figure 70. In combination, these blocks can be used to implement a digital time gain control (DTGC) scheme. The attenuator block attenuation can be changed from 8 dB to 0 dB in 0.125-dB steps (64 steps) and the LNA gain can be changed from 14 dB to 45 dB in 0.125-dB steps (256 steps). Thus, the total channel gain can be varied from 6 dB to 45 dB in 0.125-dB steps (320 steps). These gain settings are controlled as a function of time based on the different profile settings of the TGC control engine. The TGC control engine operates on the same clock as the ADC_CLK.

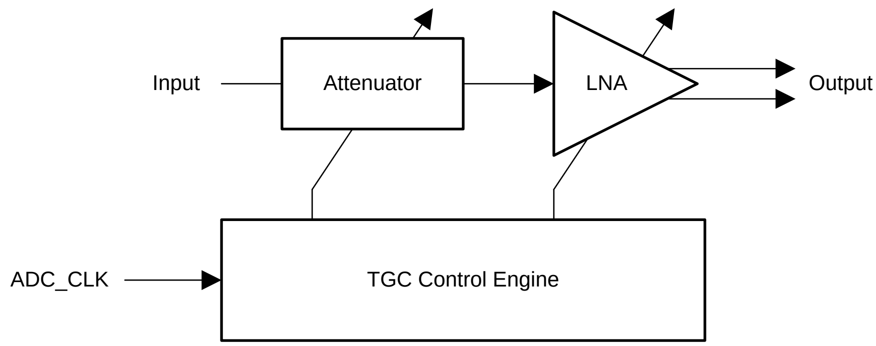


Figure 70. Digital TGC

9.3.5.2 DTGC Programming

Various functions of the digital TGC operation can be programmed using the registers listed in the *DTGC Register Map*. To program register settings in the DTGC register map, set the DTGC_WR_EN bit to 1.

9.3.5.2.1 DTGC Profile

The TGC engine supports four different modes (programmable fixed-gain, up, down ramp, external non-uniform, and internal non-uniform mode) to change the device gain with time. The gain versus time curve for each mode is set using a set of combined parameters referred to as a *profile*. Four such profiles can be programmed in advance, which enables a given mode to switch between one of four profiles based on either a pin control or based on a single register control. Table 5 shows the profile mapping with register bits.

Table 5. Profile Registers Address

PROFILE	REGISTER BITS IN THE DTGC REGISTER MAP
0	Registers 161 (bits 15-0), 162 (bits 15-0), 163 (bits 15-0), 164 (bits 15-0), 165 (bits 15-0), and 185 (bits 15-8)
1	Registers 166 (bits 15-0), 167 (bits 15-0), 168 (bits 15-0), 169 (bits 15-0), 170 (bits 15-0), and 185 (bits 7-0)
2	Registers 171 (bits 15-0), 172 (bits 15-0), 173 (bits 15-0), 174 (bits 15-0), 175 (bits 15-0), and 186 (bits 15-8)
3	Registers 176 (bits 15-0), 177 (bits 15-0), 178 (bits 15-0), 179 (bits 15-0), 180 (bits 15-0), and 186 (bits 7-0)

9.3.5.2.1.1 Profile Selection

When programmed, there are two ways that any one of the four profiles can be selected and switched to program the settings in the TGC mode: either with the device pin or by register settings.

1. Device pin. To select the profile using pin control, set the PROFILE_EXT_DIS bit to 0. Then, the different combinations of logic level at the TGC_PROF<2> and TGC_PROF<1> pins listed in Table 6 dictate which profile is selected.
2. Register settings. To select the profile with register settings, set the PROFILE_EXT_DIS bit to 1. Then, the different combinations of the PROFILE_REG_SEL bits listed in Table 6 dictate which profile must be used to program the corresponding TGC mode.

Table 6. Profile Selection Using the Device Pin or the PROFILE_REG_SEL Bits

PIN CONTROL (PROFILE_EXT_DIS = 0)		REGISTER CONTROL (PROFILE_EXT_DIS = 1)	SELECTED PROFILE
TGC_PROF<2>	TGC_PROF<1>	PROFILE_REG_SEL	
0	0	00	Profile 0
0	1	01	Profile 1
1	0	10	Profile 2
1	1	11	Profile 3

9.3.5.3 DTGC Modes

The device supports four schemes to change the device gain. These schemes are referred to as the four DTGC modes. The device can be programmed in any of these modes by using the MODE_SEL register bit, as shown in Table 7.

Table 7. DTGC Modes

MODE_SEL REGISTER BITS SETTING	DTGC MODE
10	Programmable fixed-gain
01	Up, down ramp
00	External non-uniform
11	Internal non-uniform

9.3.5.3.1 Programmable Fixed-Gain Mode

In this mode, the device gain is set directly by writing a gain code in the MANUAL_GAIN_DTGC register. See Figure 2 for a description of device gain versus gain code across power modes. Note that the allowed value of the gain code is from 0 to 319. The gain codes from 0 to 63 control the attenuator and the codes from 64 to 319 control the LNA. If the gain code is programmed outside the 0 to 319 range, then the gain code value automatically becomes 0.

For Low-Noise or Medium-Power mode: Gain = 6 + Gain code × 0.125

For Low-Power mode: Gain = 12 + Gain code × 0.125

9.3.5.3.2 Up, Down Ramp Mode

Figure 71 shows the change in device gain with time in the up, down ramp mode. This mode generates an ascending gain ramp followed by a descending gain ramp.

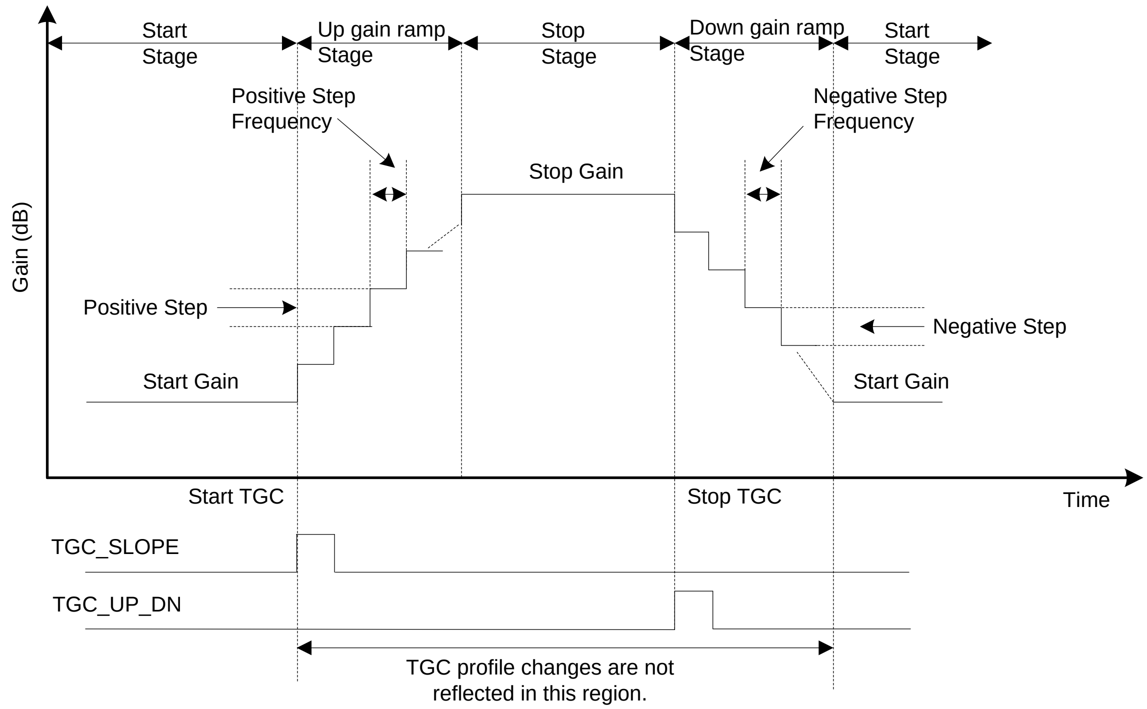


Figure 71. Up, Down Ramp Mode

The different stages of the up, down ramp mode are:

1. Start: At device reset or a DTGC mode change (that is, when changing the DTGC mode to any other mode and returning to up, down ramp mode), the device gain is equal to the start gain.
2. Up gain ramp. The up gain ramp stage starts when the TGC_SLOPE pin voltage level goes high. During the up gain ramp stage, the device gain increases by a positive step at the rate of the positive step frequency.
3. Stop gain. Any device gain in the up gain ramp stage keeps increasing until a stop gain stage is reached. Any pules given at the TGC_SLOPE or TGC_UP_DN pins during the up gain ramp stage are ignored.
4. Down gain ramp. The down gain ramp stage starts when the TGC_UP_DN pin voltage level goes high. During the down gain ramp stage, the device gain decreases by a negative step at the rate of the negative step frequency. Any device gain in the down gain ramp stage keeps decreasing until a gain reaches the value specified by start gain. Thereafter, the TGC curve proceeds to the start stage.
5. Profile. Different parameters (such as start gain, positive step, positive step frequency, and so forth) of different gain stages are programmed with profile registers. A single profile consists of five 16-bit registers and one 8-bit register that can be programmed with the serial interface registers. The functions of these registers in up, down ramp mode are listed in Table 8. Note that changing the profile number updates the parameters only during the start gain stage.
6. Timing requirement. See the section for timing requirements on the TGC_SLOPE and TGC_UP_DN pins with respect to the ADC clock.

Table 8. Profile Description for Up, Down Ramp Mode

REGISTER CONTROL				NAME	NOTATION IN REGISTER MAP	DESCRIPTION	DEFAULT VALUE	ALLOWED RANGE
PROFILE 0	PROFILE 1	PROFILE 2	PROFILE 3					
161 (bits 15-8)	166 (bits 15-8)	171 (bits 15-8)	176 (bits 15-8)	Start gain	START_GAIN_x [15:8]	These bits set the gain code for the start gain. For an *N* value (in decimal), these bits set the start gain stage to (6 + *N* × 0.25) dB.(1)	0	0 to 159
161 (bits 7-0)	166 (bits 7-0)	171 (bits 7-0)	176 (bits 7-0)	Stop gain	STOP_GAIN_x[7:0]	These bits set the gain code for the stop gain. For an *N* value, these bits set the stop gain stage to (6 + *N* × 0.25) dB.(1)	159	0 to 159
162 (bits 15-11)	167 (bits 15-11)	172 (bits 15-11)	177 (bits 15-11)	Positive step	POS_STEP_x[7:3]	For an *N* value, these bits set the positive step to (*N* + 1) × 0.125 dB.	0	0 to 31
162 (bits 10-8)	167 (bits 10-8)	172 (bits 10-8)	177 (bits 10-8)	Positive step frequency	POS_STEP_x[2:0]	For an *N* value, gain steps at a periodicity of [$f_S / 2^{(7 - N)}$]. Where f_S is the ADC clock frequency.(1)	0	0 to 7
162 (bits 7-3)	167 (bits 7-3)	172 (bits 7-3)	177 (bits 7-3)	Negative step	NEG_STEP_x[7:3]	For an *N* value, these bits set the negative step to (*N* + 1) × 0.125 dB.(1)	31	0 to 31
162 (bits 2-0)	167 (bits 2-0)	172 (bits 2-0)	177 (bits 2-0)	Negative step frequency	NEG_STEP_x[2:0]	For an *N* value, gain steps at a periodicity of [$f_S / 2^{(7 - N)}$]. Note that f_S is ≥ the ADC clock frequency.(1)	7	0 to 7
163 to 165 (bits 15-0)	168 to 170 (bits 15-0)	173 to 175 (bits 15-0)	178 to 180 (bits 15-0)	—	—	—	—	N/A
185 (bit 15)	185 (bit 7)	186 (bit 15)	186 (bit 7)	—	FIX_ATTEN_x	0 = Default 1 = Enable fixed attenuation mode	0	0 to 1
185 (bits 14-8)	185 (bits 6-0)	186 (bits 14-8)	186 (bits 6-0)	—	ATTENUATION_x	When the FIX_ATTEN_EN_x bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_0 bits. A value of *N* written in the ATTENUATION_x register sets the attenuation level at –8 + *N* × 0.125 dB.(1)	0	0 to 64

(1) N refers to the decimal equivalent of the multi-bit word.

9.3.5.3.3 External Non-Uniform Mode

Figure 72 shows the change in device gain with time in external non-uniform mode. This mode generates an ascending gain ramp followed by a descending gain ramp. This mode can be made to generate a non-uniform gain profile using appropriate controls on the TGC_SLOPE and TGC_UP_DN pins.

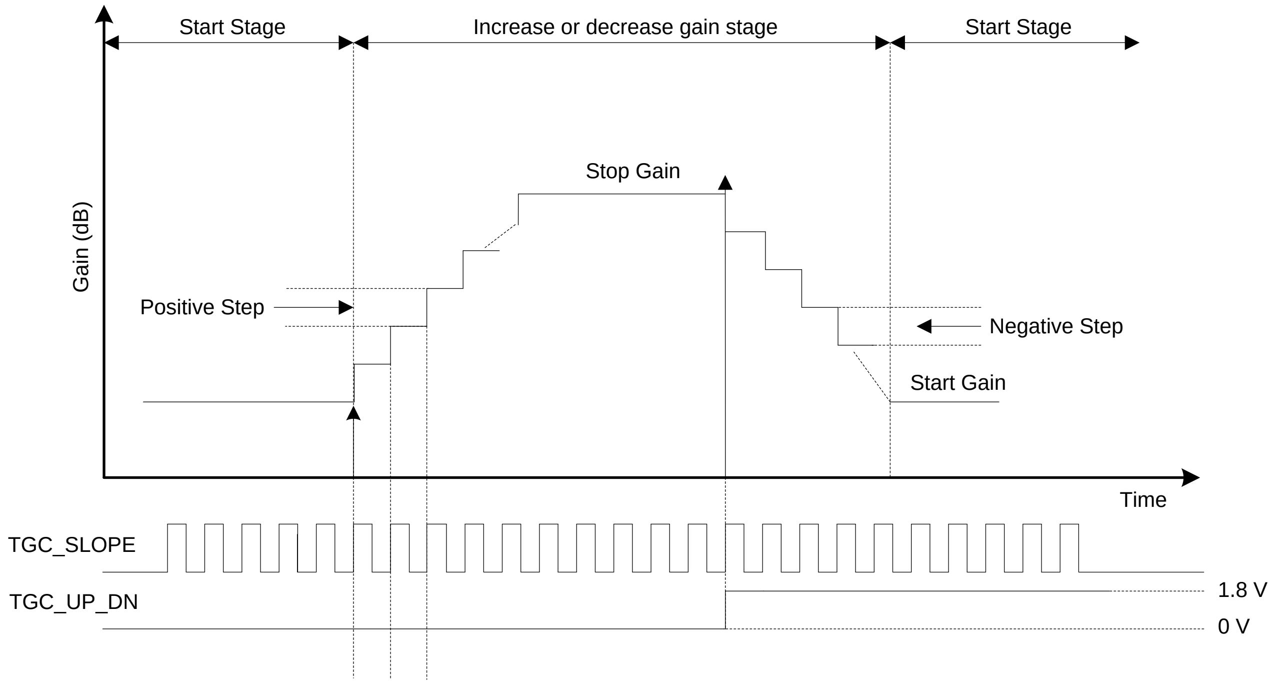


Figure 72. External Non-Uniform Mode

The different stages of the external non-uniform mode are:

1. Start: At device reset or a DTGC mode change (that is, when changing the DTGC mode to any other mode and returning to external non-uniform mode), the device gain is equal to the start gain.
2. Increase or decrease gain. When a positive edge transition is received on the device TGC_SLOPE pin, the device gain increases or decreases by either a positive step or negative step based on the TGC_UP_DN pin voltage level. If the TGC_UP_DN pin is set to a level 0, device gain increases and if the TGC_UP_DN pin is set to 1, device gain decreases. The signal frequency at the TGC_SLOPE pin must be less than or equal to the ADC clock.
3. Profile. Different parameters (such as start gain, positive step, negative step, and so forth) of different gain stages are programmed with profile registers. A single profile consists of five 16-bit registers and one 8-bit register that can be programmed with the serial programming interface (SPI). The functions of these registers in external non-uniform mode are listed in Table 9. Note that changing the profile number updates the parameters at any stage of the gain curve.
4. Timing requirement. See the section for timing requirements on the TGC_SLOPE and TGC_UP_DN pins with respect to the ADC clock.

Table 9. Profile Description for External Non-Uniform Mode

REGISTER CONTROL				NAME	BIT IN REGISTER MAP	DESCRIPTION	DEFAULT VALUE	ALLOWED RANGE
PROFILE 0	PROFILE 1	PROFILE 2	PROFILE 3					
161 (bits 15-8)	166 (bits 15-8)	171 (bits 15-8)	176 (bits 15-8)	Start gain	START_GAIN_x [15:8]	These bits set the gain code for the start gain stage. For an *N* value (in decimal), these bits set the start gain stage to (6 + *N* × 0.25) dB.(1)	0	0 to 159
161 (bits 7-0)	166 (bits 7-0)	171 (bits 7-0)	176 (bits 7-0)	Stop gain	STOP_GAIN_x	These bits set the gain code for the stop gain stage. For an *N* value, these bits set the stop gain stage to (6 + *N* × 0.25) dB.(1)	159	0 to 159
162 (bits 15-8)	167 (bits 15-8)	172 (bits 15-8)	177 (bits 15-8)	Positive step	POS_STEP_x	For an *N* value, these bits set the positive step to (*N* + 1) × 0.125 dB.(1)	0	0 to 255
162 (bits 7-0)	167 (bits 7-0)	172 (bits 7-0)	177 (bits 7-0)	Negative step	NEG_STEP_x	For an *N* value, these bits set the negative step to (*N* + 1) × 0.125 dB.(1)	255	0 to 255
163 to 165 (bits 15-0)	168 to 170 (bits 15-0)	173 to 175 (bits 15-0)	178 to 180 (bits 15-0)	—	—	—	—	—
185 (bit 15)	185 (bit 7)	186 (bit 15)	186 (bit 7)	—	FIX_ATTEN_x	0 = Default 1 = Enable fixed attenuation mode	0	0 to 1
185 (bits 14-8)	185 (bits 6-0)	186 (bits 14-8)	186 (bits 6-0)	—	ATTENUATION_x	When the FIX_ATTEN_EN_x bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_0 bits. A value of *N* written in the ATTENUATION_x register sets the attenuation level at –8 + *N* × 0.125 dB.(1)	0	0 to 64

(1) N refers to the decimal equivalent of the multi-bit word.

9.3.5.3.4 Internal Non-Uniform Mode

Figure 73 shows the change in device gain with time in internal non-uniform mode. A gain profile is completely user defined by programming a set of profile registers and a bank of memory consisting of 160 16-bit registers. Programming the profile register is covered in the *DTGC Profile* section. Memory architecture and other information are explained in detail in the *Memory* section.

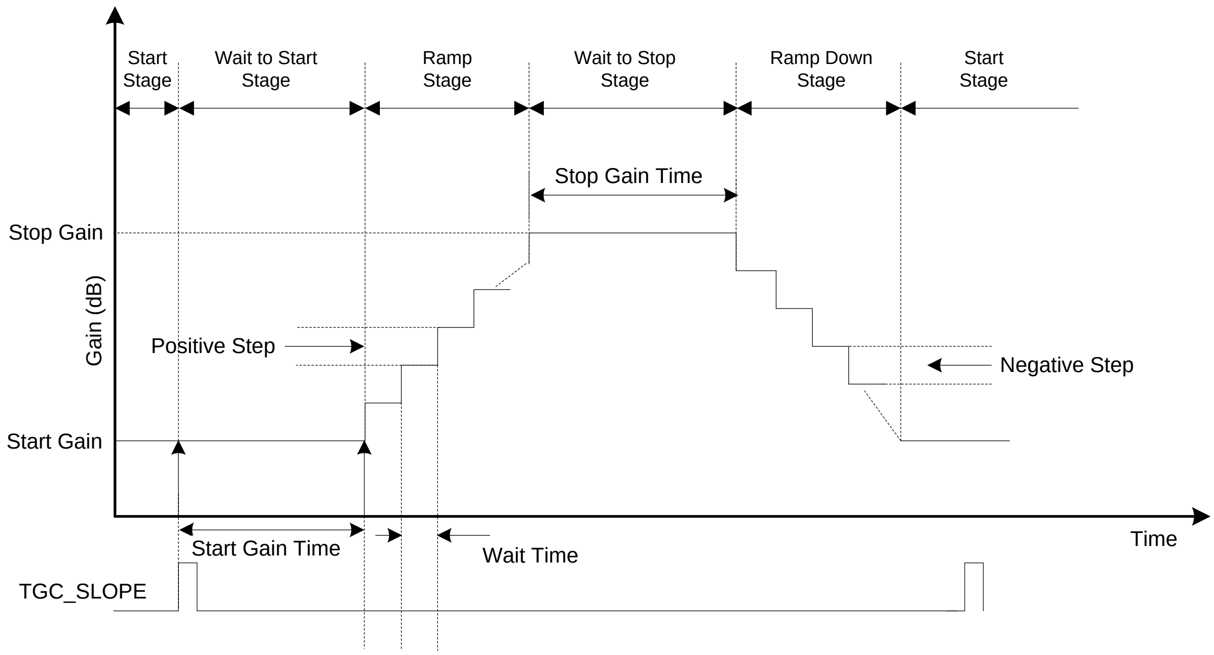


Figure 73. Internal Non-Uniform Mode

9.3.5.3.4.1 Memory

In the device are a total of four memory banks (bank 0 to bank 3), with each bank containing 160 rows and each row is 16 bits in length, as shown in Figure 74. Each memory bank contains the information of the non-uniform gain curve for a particular profile.

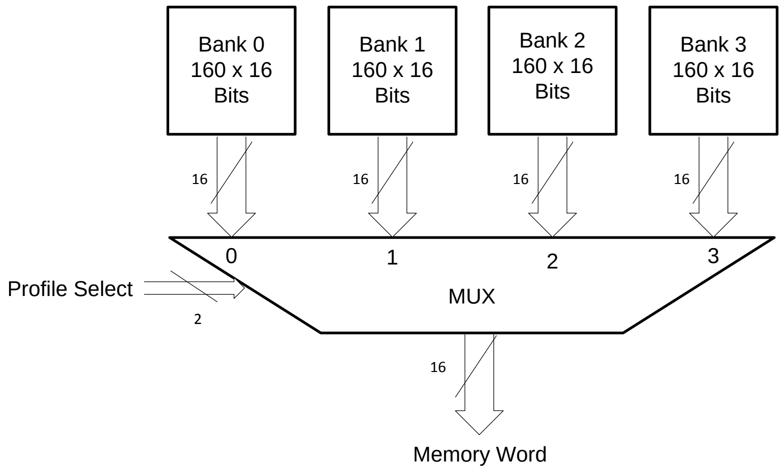


Figure 74. Memory Bank

9.3.5.3.4.1.1 Write Operation for the Memory

The device supports two write operation modes: normal write mode and burst write mode. The following steps describe the memory write operation in normal write mode:

1. Select the memory bank whose contents must be programmed using the MEM_BANK_SEL register bit. Table 10 shows the mapping of the MEM_BANK_SEL and memory bank.

Table 10. Memory Bank Selection

MEM_BANK_SEL	MEMORY BANK
00	0
01	1
10	2
11	3

2. After selecting the memory bank, any memory bank word can be programmed by writing the MEM_WORD_0 to MEM_WORD_159 registers. For example, to program word 1 to word 160 of memory bank 0, first write MEM_BANK_SEL = 00 and write the memory content at the MEM_WORD_0 to MEM_WORD_159 registers.

The following steps describe the memory write operation in burst write mode:

1. Select the memory bank whose contents must be programmed using the MEM_BANK_SEL register bit. Table 10 shows the mapping of the MEM_BANK_SEL and memory bank.
2. After selecting the memory bank, any memory bank word can be programmed in burst by giving the register address only one time. After giving the register address, provide continuous data on the SDIN pin and keep the SEN signal low. The device automatically internally increments the register address and writes the data to the next memory word.

Figure 75 shows the normal and burst write mode operations.

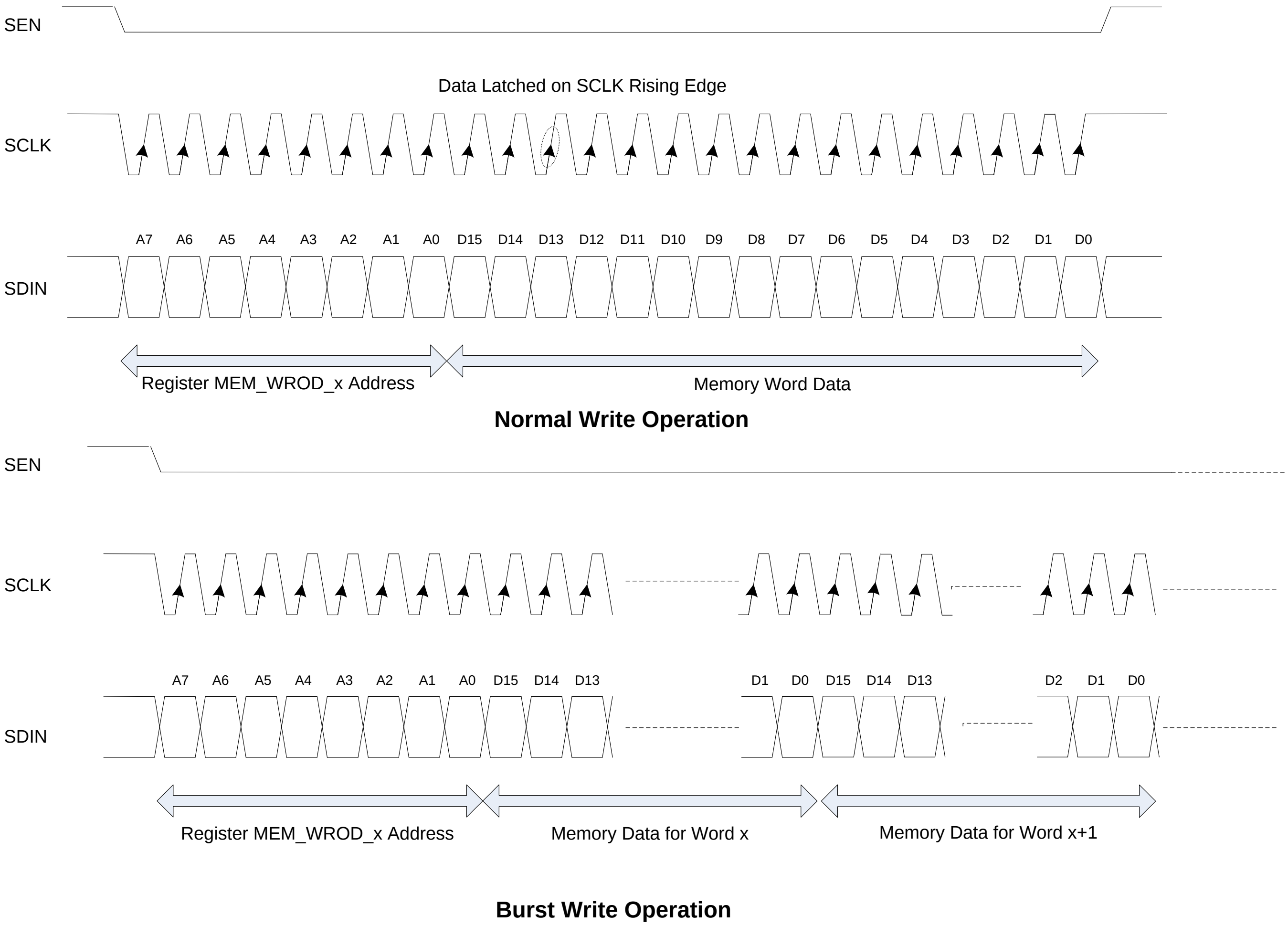


Figure 75. Memory Write Mode

9.3.5.3.4.1.2 Read Operation for the Memory

The memory bank content can be read back in the same manner by reading the registers of the DTGC register map; see the *Register Readout* section. To read the content of memory banks 0, 1, 2, or 3, first set the MEM_BANK_SEL to 00, 01, 10, or 11 respectively, then place the device in DTGC register read mode and read the MEM_WORD_x register to read word x on the SDOUT pin.

NOTE

Simultaneous memory read and write operation is not supported.

9.3.5.3.4.2 Gain Curve Description for the Internal Non-Uniform Mode

The internal non-uniform mode operation is described in Figure 76 via a flow chart.

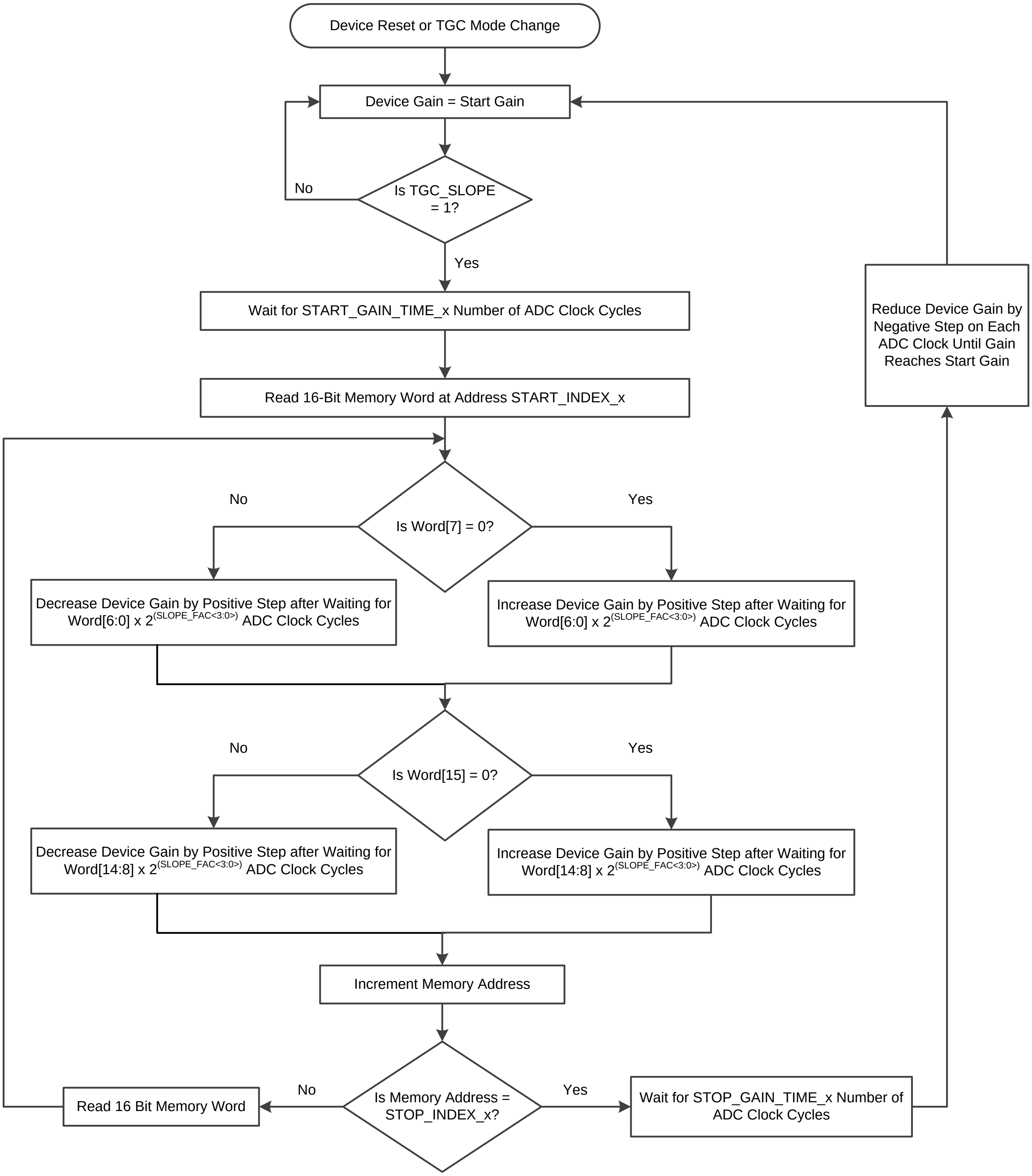


Figure 76. Internal Non-Uniform Mode Operation

The different stages of the internal non-uniform mode are:

1. Start: At device reset or a DTGC mode change (that is, when changing the DTGC mode to any other mode and returning to internal non-uniform mode), the device gain is equal to the start gain.
2. Wait to start: When the TGC_SLOPE pin voltage level goes high, the device gain remains at the start gain stage for the number of ADC clock cycles defined in the START_GAIN_TIME_x register (x is the profile number).
3. Ramp:
   (a) After waiting for START_GAIN_TIME_x number of ADC clock cycles, the TGC engine reads a 16-bit memory word (word[15:0]) at the START_INDEX_x address and performs the following operation:
      (a) If memory word[7] = 0, the device gain increases by a positive step gain after waiting for the word[6:0] × $2^{SLOPE_FAC<3:0>}$number of ADC clock cycles. If memory word[7] = 1, the device gain decreases by a negative step gain after waiting for the word[6:0] × $2^{SLOPE_FAC<3:0>}$number of ADC clock cycles.
      (b) If memory word[15] = 0, the device gain increases by a positive step gain after waiting for the word[14:8] × $2^{SLOPE_FAC<3:0>}$number of ADC clock cycles. If memory word[15] = 1, the device gain decreases by a negative step gain after waiting for the word[14:8] × $2^{SLOPE_FAC<3:0>}$number of ADC clock cycles.
   (b) The TGC engine increases the memory address by 1. If the new address is less than STOP_INDEX_x, the TGC engine reads a 16-bit memory word at the new address and repeats steps i and ii.
4. Wait to stop: The TGC engine increases the memory address by 1. If the new memory address is equal to STOP_INDEX_x, then the device waits for the STOP_GAIN_TIME_x number of ADC clock cycles.
5. Ramp down: After waiting for the STOP_GAIN_TIME_x number of ADC clock cycles, the device gain starts reducing by a negative step gain on each ADC clock until the gain reaches the start gain stage.
6. Profile: Different parameters (such as start gain, positive step, positive step frequency, and so forth) of different gain stages are programmed with profile registers. A single profile consists of five 16-bit registers and one 8-bit register that can be programmed with the serial programming interface (SPI). The functions of these registers in internal non-uniform mode are listed in Table 11. Note that changing the profile number updates the parameters only during the start gain stage.
7. Timing requirement. See the *Timing Specifications* section for timing requirements on the TGC_SLOPE pin with respect to the ADC clock.

Table 11. Internal Non-Uniform Mode Profile Definition

REGISTER CONTROL				NAME	BIT IN REGISTER MAP	DESCRIPTION	DEFAULT VALUE	ALLOWED RANGE
PROFILE 0	PROFILE 1	PROFILE 2	PROFILE 3					
161 (bits 15-8)	166 (bits 15-8)	171 (bits 15-8)	176 (bits 15-8)	Start gain	START_GAIN_x [15:8]	These bits set the gain code for the start gain stage. For an *N* value (in decimal), these bits set the start gain stage to (6 + *N* × 0.25) dB.	0	0 to 159
161 (bits 7-0)	166 (bits 7-0)	171 (bits 7-0)	176 (bits 7-0)	—	STOP_GAIN_x[7:0]	Always write 159	159	0 to 159
162 (bits 15-8)	167 (bits 15-8)	172 (bits 15-8)	177 (bits 15-8)	Positive step	POS_STEP_x[7:0]	For an *N* value, these bits set the positive step to (*N* + 1) × 0.125 dB.	0	0 to 255
162 (bits 7-0)	167 (bits 7-0)	172 (bits 7-0)	177 (bits 7-0)	Negative step	NEG_STEP_x[7:0]	For an *N* value, these bits set the negative step to (*N* + 1) × 0.125 dB.	255	0 to 255
163 (bits 15-8)	168 (bits 15-8)	173 (bits 15-8)	178 (bits 15-8)	Memory start index	START_INDEX_x	Memory start index	0	0 to 159
163 (bits 7-0)	168 (bits 7-0)	173 (bits 7-0)	178 (bits 7-0)	Memory stop index	STOP_INDEX_x	Memory stop index	159	0 to 159
164 (bits 15-0)	169 (bits 15-0)	174 (bits 15-0)	179 (bits 15-0)	Start gain time	START_GAIN_ TIME_x	For an N value, these bits set the start gain time to *N* × ADC clock cycles.	0	0 to (2^{16-1})
165 (bits 15-0)	170 (bits 15-0)	175 (bits 15-0)	180 (bits 15-0)	Stop gain time	STOP_GAIN_ TIME_x	For an N value, these bits set the stop gain time to *N* × ADC clock cycles.	0	0 to (2^{16-1})
185 (bit 15)	185 (bit 7)	186 (bit 15)	186 (bit 7)	—	FIX_ATTEN_x	0 = Default 1 = Enable fixed attenuation mode	0	0 to 1
185 (bits 14-8)	185 (bits 6-0)	186 (bits 14-8)	186 (bits 6-0)	—	ATTENUATION_x	When the FIX_ATTEN_EN_x bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_0 bits. A value of *N* written in the ATTENUATION_x register sets the attenuation level at –8 + *N* × 0.125 dB.	0	0 to 64

9.3.5.4 Timing Specifications

For all DTGC modes, a signal applied on the TGC_SLOPE and TGC_UP_DN pins must meet the timing constraints with respect to the ADC clock signal, as shown in Figure 77.

NOTE

Failure to meet the timing constraints in the up, down ramp mode results in a locked state. To come out of a locked start state, change MODE_SEL to another mode and return to up, down ramp mode or reset the device.

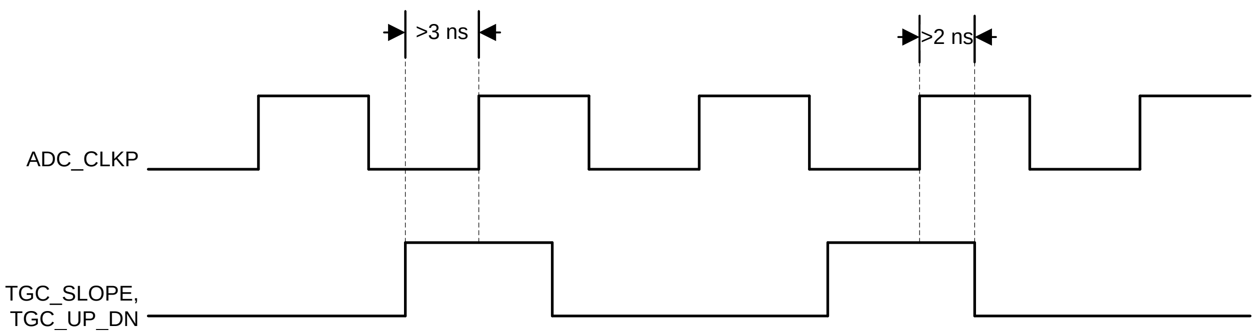


Figure 77. TGC Timing Diagram

No timing constraints are required on signals applied at the TGC_PROF<2> and TGC_PROF<1> pins.

9.3.6 Continuous-Wave (CW) Beamformer

The continuous-wave Doppler (CWD) is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path must handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in the analog domain because of these strict requirements. Multiple beamforming methods are implemented in ultrasound systems, including a passive delay line, active mixer, and passive mixer. Among these approaches, the passive mixer achieves optimized power and noise. This mixer satisfies the CW processing requirements (such as wide dynamic range, low phase noise, and accurate gain and phase matching).

The output signal in the CW path is a current output unlike the TGC path that has a voltage output. The down-converted and phase-shifted currents of all the channels are summed and given to a single node; see Figure 78. Connect this node to the virtual ground of an external differential amplifier for correct operation; see Figure 79.

NOTE

The local oscillator inputs of the passive mixer are cos (ωt) for the I channel and sin (ωt) (where ω is local oscillator frequency) for the Q channel, respectively. Depending on the application-specific CWD complex FFT processing, swapping the I and Q channels in either the field-programmable gate array (FPGA) or digital signal processor (DSP) can be required in order to obtain correct blood flow direction.

All blocks include well-matched, in-phase, quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is excellent, which is desired in ultrasound systems.

NOTE

The TGC path in the device is automatically disabled when the CW path is enabled. The device does not support both TGC and CW modes simultaneously. However though not used, the ADC remains powered up by default in the CW mode. The ADC can be powered down using register bit GLOBAL_PDN.

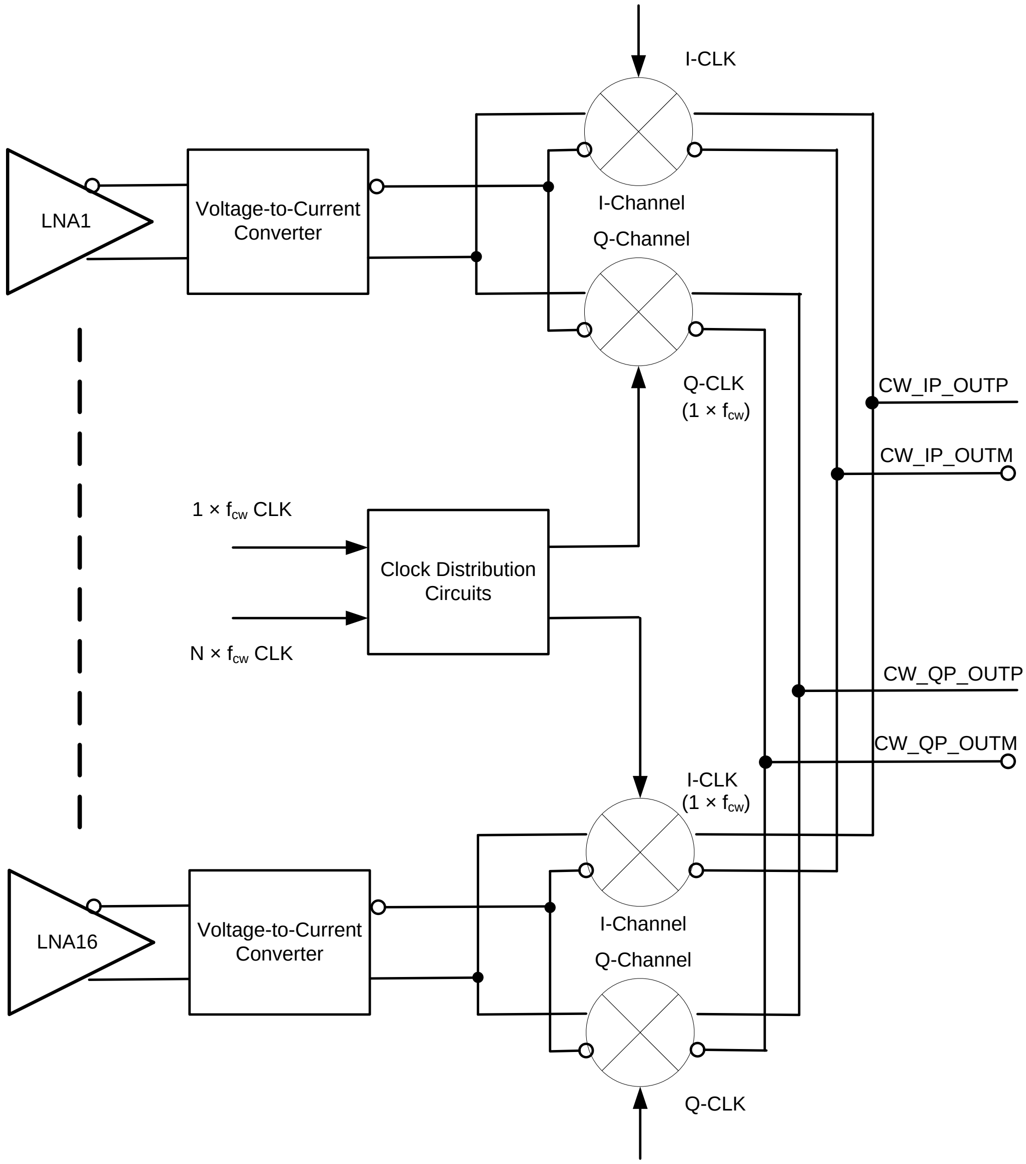
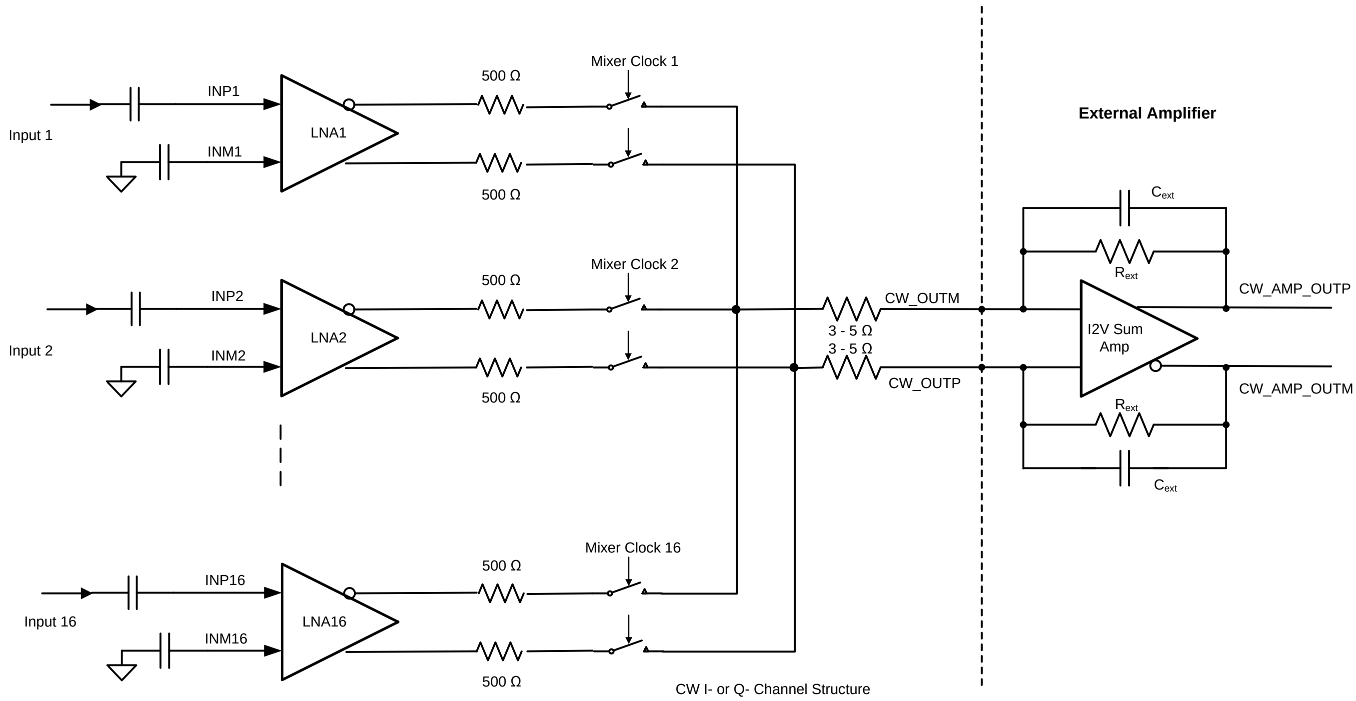


Figure 78. Simplified Block Diagram of the CW Path



NOTE: The 3-Ω to 6-Ω resistors at CW_OUTP and CW_OUTM result from the internal device routing and can create a slight attenuation in the signal.

Figure 79. A Circuit Representation of a In-Phase or Quadrature-Phase Channel

The CW mixing operation attempts to down-convert the signal band to approximately dc such that the Doppler frequency is translated to a low-frequency signal. This process is done by a complex mixing of the signal with a clock that is at the same frequency as the center frequency of the signal. The complex mixing of the signal requires the I- and Q- version of the clock. Furthermore, different channels can have different phase delays in the path of their analog inputs. Thus, the programmability of the phase of the I- and Q- clock is essential to have. The CW mixer uses two clocks; a high speed clock (16X, 8X, or 4X of the mixing clock) that is used to generate multiple phases of a 1X clock, which is at the frequency of the mixing clock.

The CW mixer in the device is passive and switch based; the passive mixer adds less noise than active mixers. The CW mixer achieves good performance at low power. Figure 80, Table 12, and the calculations of Equation 5 describe the principles of the mixer operation. LO(t) is square-wave based and includes odd harmonic components.

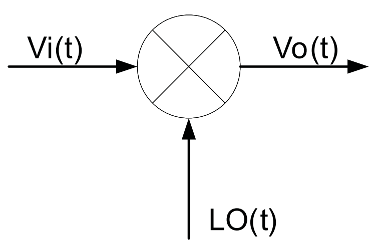


Figure 80. CW Mixer Operation Block Diagram

Table 12. Symbol Definition for CW Mixing

SYMBOL	DEFINITION
Vi(t)	Input signal to the mixer
Vo(t)	Output of the mixer
LO(t)	Local oscillator signal (1X clock) with appropriate phase
ω_0	Input signal center frequency in radians per second
f_0	Input signal center frequency in Hz
ω_d	Doppler shift frequency in radians per second
t	Time
φ	Input signal phase relative to the phase of LO(t)

$$Vi(t) = \sin(\omega_0 t + \omega_d t + \varphi)$$
$$LO(t) = \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t)...\right] - \text{Fourier series of square wave}$$
$$Vo(t) = \frac{2}{\pi}\left[\cos(\omega_d t + \varphi) - \cos(2\omega_0 t + \omega_d t + \varphi) + ...\right] \quad (5)$$

All the symbol definitions for Equation 5 are given in Table 12.

The first term in Equation 5 represents the ideal down-connected Doppler frequency component desired from the CW mixer. However the third- and fifth-order harmonics from LO(t) can either mix with the third- and fifth-order harmonic of the Vi(t) signal or the noise around the third- and fifth-order harmonics of Vi(t). This higher-order mixing can result in additional undesired down-converted components that lead to degraded mixer performance. In order to eliminate this side-effect resulting from the square-wave demodulation, a proprietary harmonic-suppression circuit is implemented in the device. The third- and fifth-order harmonic components from the LO can be suppressed by over 12 dB. Thus, the LNA output noise around the third- and fifth-order harmonic bands are not down-converted to base band. Thus, a better noise figure is achieved. The conversion loss of the mixer is approximately –4 dB, ($20\log_{10} 2 / \pi$).

The mixed current output of the 16 channels must be summed externally; see Figure 79. The external differential amplifier converts the current signal to differential voltage and can also provide a filtering action for the higher frequency components in Equation 5. The common-mode voltage at the CW_OUT nodes is 0.9 V. Setting the output common-mode of the external amplifier to 0.9 V is recommended to avoid common-mode loading. The amplifier must be able to support the maximum output current of the device, which is 80 mA_{PP}. The amplifier noise and matching have a direct impact on the I/Q channel performance and therefore must be selected cautiously. Amplifiers with input-referred voltage noise lower than 2 nV/$\sqrt{Hz}$ can be selected. The OPA1632 and THS4130 for are recommended as external amplifiers, both of which satisfy the above criteria.

The CW I/Q channels are well-matched internally to suppress image frequency components in the Doppler spectrum. Use low-tolerance (0.1%) components and precise operational amplifiers to achieve good matching in the external circuits as well. The circuit illustrated in Figure 79 achieves a first-order filter with a corner frequency of f_C, as given by Equation 6:

$$f_C = \frac{1}{2 \times \pi \times R_{ext} \times C_{ext}} \quad (6)$$

The CW path gain (see Figure 79) for an in-band signal (frequency less than f_C) at one of the channels is given by the combination of LNA gain, mixer loss, and gain provided by the external amplifier. The LNA gain is 18 dB and the mixer attenuation is 4 dB. The gain of the external amplifier is determined by the ratio of the external resistor (Rext) and the internal resistor (500 Ω). The CW gain is given by Equation 7.

$$\text{Gain}(dB) = 18 - 4 + 20 \times \log 10\left(\frac{R_{ext}}{500}\right) \quad (7)$$

The 3-Ω to 5-Ω resistors shown in Figure 79 create a small loss. Multiple clock options are supported in the device CW path. Two CW clock inputs are required: an N × f_{cw} clock and a 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N can be 16, 8, 4, or 1. The most convenient system clock solution can be selected for the device. In the 16 × f_{cw} and 8 × f_{cw} modes, the third- and fifth-order harmonic suppression feature is supported. Thus, the 16 × f_{cw} and 8 × f_{cw} modes achieve better performance than the 4 × f_{cw} and 1 × f_{cw} modes.

9.3.6.1 16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to the other modes. This mode is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16 × f_{cw} generates the 16 × f_{cw} LO signals with 16 accurate phases. Multiple devices can be synchronized by the 1 × f_{cw} (that is, LO signals in multiple AFEs can have the same starting phase). The phase noise specification is critical only for the 16X clock. The 1X clock is for synchronization only and does not require low phase noise.

The top-level clock distribution diagram is shown in Figure 81. Each mixer clock is distributed through a 16 × 16 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1X clock. Synchronizing the 1 × f_{cw} and 16 × f_{cw} clocks is recommended; see Figure 82.

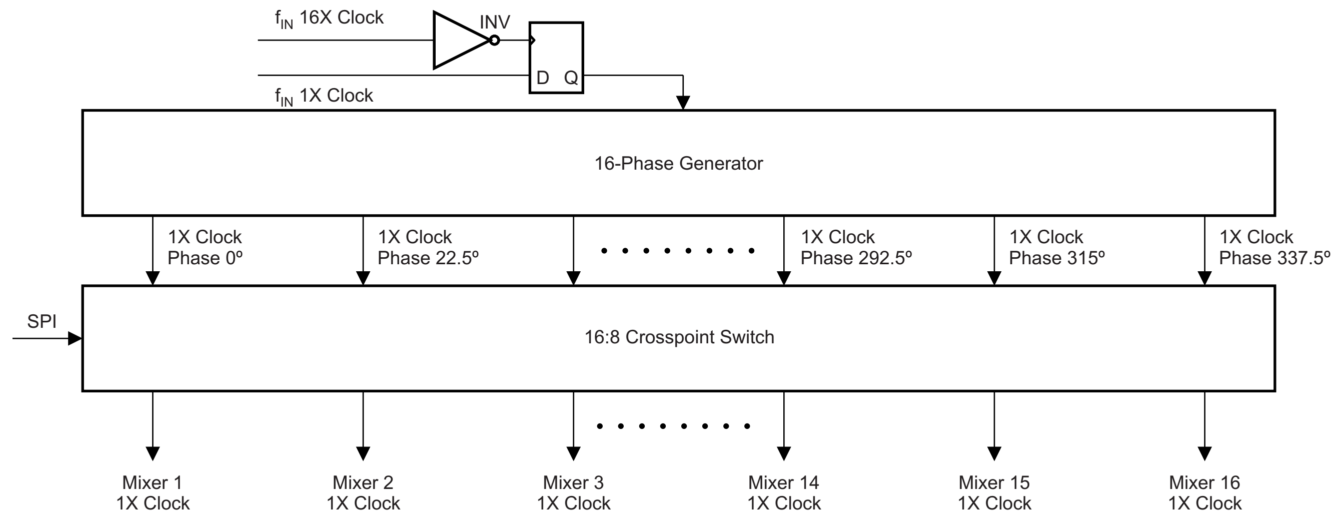


Figure 81. CW Clock Distribution Scheme

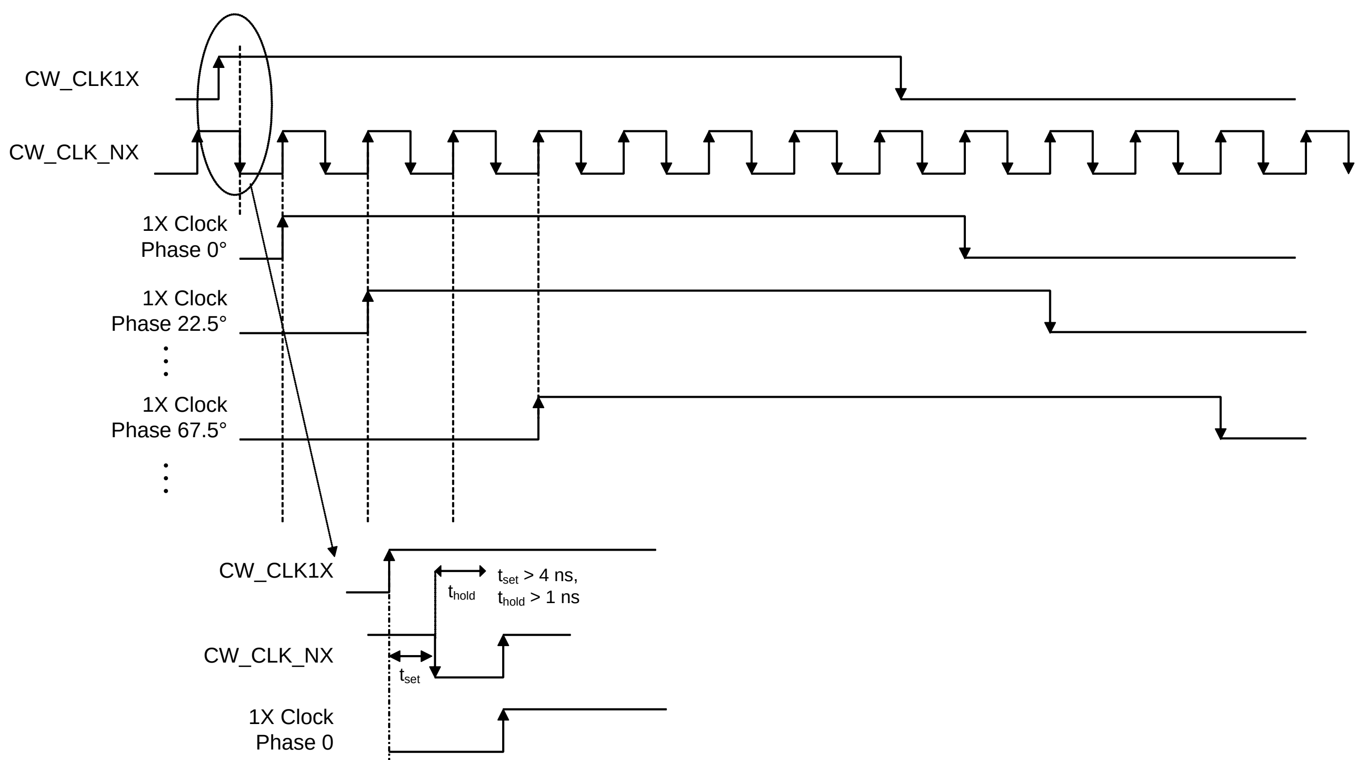


Figure 82. 1X and 16X CW Clock Timing Diagram

The cross-point switch distributes the clocks with an appropriate phase delay to each mixer. The mixer phase delay is used to compensate for the delay in the input signal. For instance, if a received signal Vi(t) is delayed with a time of 1 / (16 × f_o) (where f_o is the input signal frequency in Hz), apply a delayed LO(t) to the mixer in order to compensate for the 1 / (16 × f_o) delay. Thus, a 22.5º delayed clock (that is, 2π / 16) is selected for this channel. The mathematical calculation is expressed in Equation 8. Therefore, after the I/Q mixers, the phase delay in the received signals is compensated. The mixer outputs from all channels are aligned and added linearly to improve the signal-to-noise ratio.

$$Vi(t) = \sin[\omega_0(t - \frac{1}{16 f_0}) + \omega_d t] = \sin[\omega_0 t - 22.5° + \omega_d t]$$

$$LO(t) = \frac{4}{\pi}\sin[\omega_0(t - \frac{1}{16 f_0})] = \frac{4}{\pi}\sin[\omega_0 t - 22.5°]$$

$$Vo(t) = \frac{2}{\pi}\cos(\omega_d t) + f(\omega_n t) \tag{8}$$

This feature enables a beamforming operation to be supported when in CW mode. Here, f(ω_nt) represents all high-frequency components that are filtered out using a low-pass filter implemented in the external amplifier.

9.3.6.2 8 × f_{cw} and 4 × f_{cw} Modes

The 8 × f_{cw} and 4 × f_{cw} modes are alternative modes when a higher frequency clock solution (that is, a 16 × f_{cw} clock) is not available in the system. The block diagram of these two modes is shown in Figure 83.

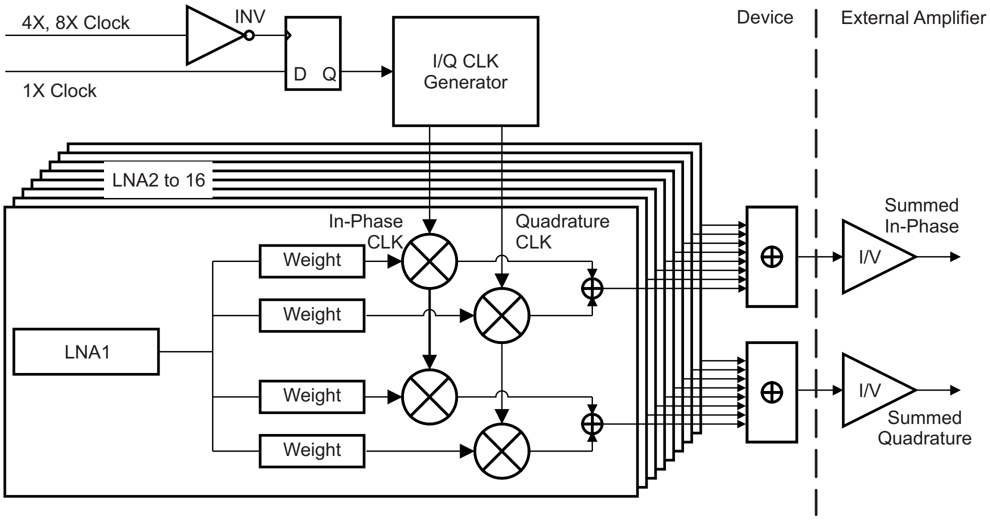


Figure 83. 8 × f_{cw} and 4 × f_{cw} Block Diagram

Good phase accuracy and matching are also maintained in these modes. The quadrature clock generator is used to create in-phase and quadrature clocks with exactly a 90° phase difference. The difference between the 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the third- and fifth-order harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. Although the phases of the 1X clock that can be directly ensured in the 8 × f_{cw} and 4 × f_{cw} modes are fewer than in the 16 × f_{cw} mode, the intermediate phases can be generated by appropriate weighting and combination of I- and Q- signals. For example, if a delay of 1 / (16 × f_o) or 22.5° is targeted corresponding to LO(t), the weighting coefficients must follow Equation 9 (assuming I_{in} and Q_{in} are sin (ω_0t) and cos (ω_0t), respectively).

$$I_{delayed}(t) = I_{in}\cos\left(-\frac{2\pi}{16}\right) + Q_{in}\sin\left(-\frac{2\pi}{16}\right) = I_{in}\left(t - \frac{1}{16 f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(-\frac{2\pi}{16}\right) - I_{in}\sin\left(-\frac{2\pi}{16}\right) = Q_{in}\left(t - \frac{1}{16 f_0}\right) \quad (9)$$

NOTE

The timing requirements for the 4 × f_{cw} clock relative to the 1 × f_{cw} clock are illustrated in Figure 84. A similar timing requirement (t_{set} and t_{hold}) is also applicable for the 8 × f_{cw} clock.

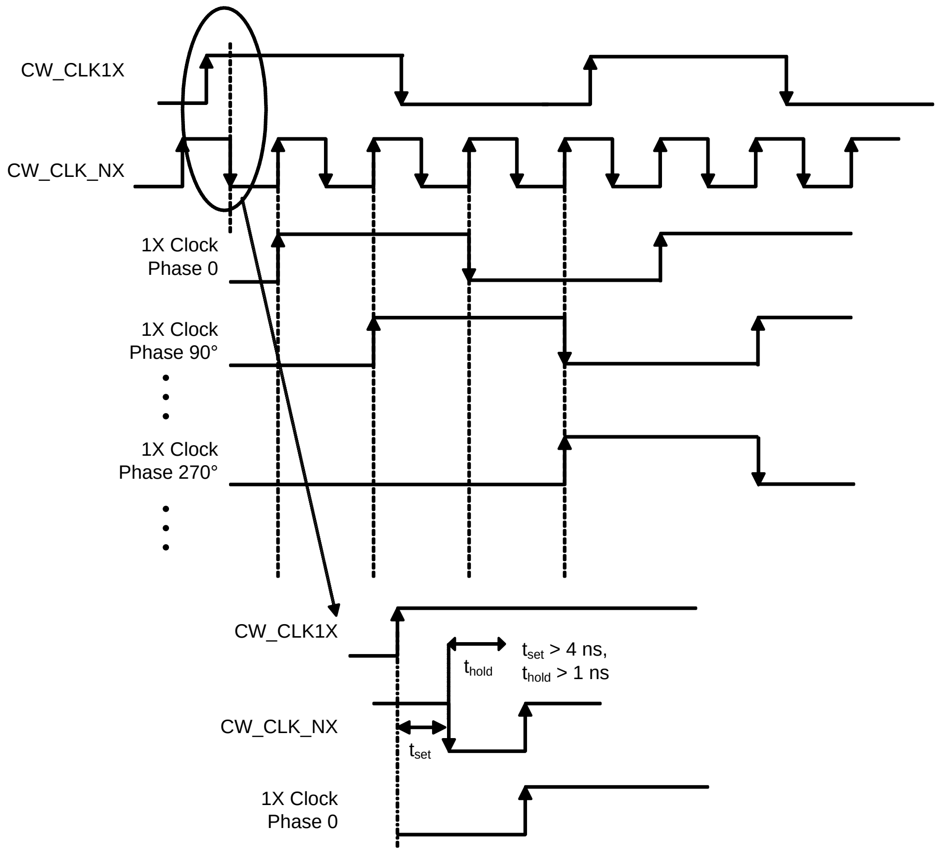


Figure 84. 8 × f_{cw} and 4 × f_{cw} Timing Diagram

9.3.6.3 1 × f_{cw} Mode

The 1 × f_{cw} mode requires in-phase and quadrature clocks with low-phase noise specifications. A block diagram for this mode is shown in Figure 85. Here again, the intermediate phases can be obtained through appropriate weighting and combining of the I- and Q- signals, as described in the *8 × f_{cw} and 4 × f_{cw} Modes* section.

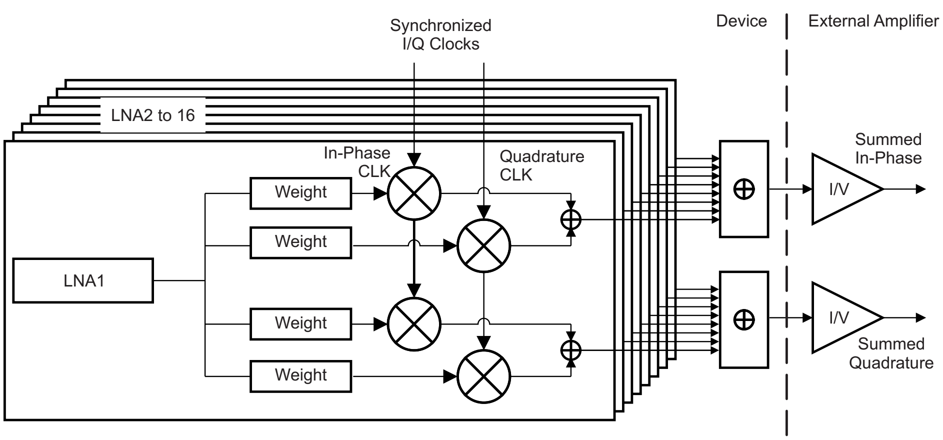


Figure 85. 1 × f_{cw} Mode Block Diagram

9.3.6.4 CW Clock Selection

For the CW clocks, the device can accept differential LVDS, LVPECL, and other differential clock inputs as well as a single-ended CMOS clock. An internally-generated V_{CM} of 1.5 V is applied to CW clock inputs (that is, CW_CLK_NX and CW_CLK1X). Because this 1.5-V V_{CM} is different from the one used in standard LVDS or LVPECL clocks, ac coupling is required between clock drivers and the device CW clock inputs. When the CMOS clock is used, tie CLKM_1X and CLKM_16X either to ground or leave CLKM_1X floating. Common clock configurations are shown in Figure 86. Appropriate termination is recommended to achieve good signal integrity.

NOTE

The configurations shown in Figure 86 can also be used as a reference for the ADC clock input.

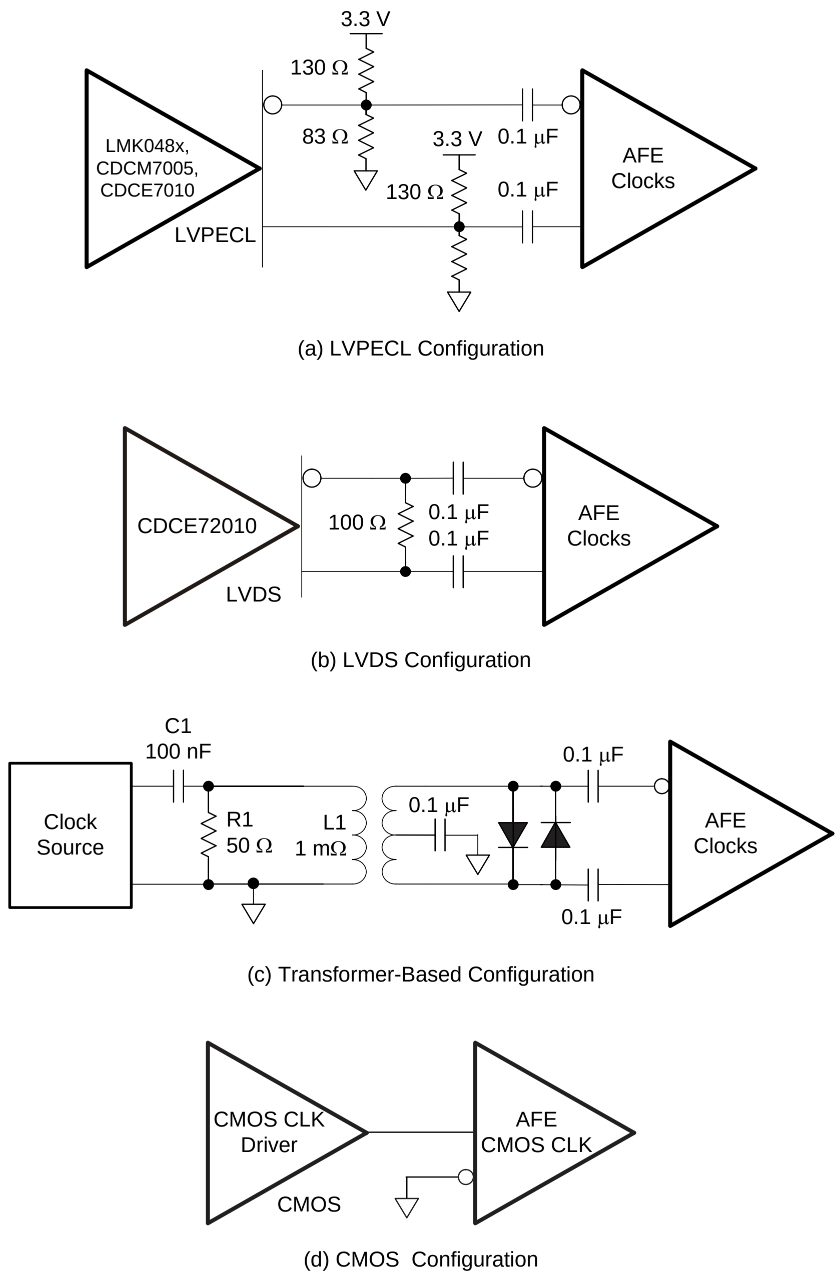


Figure 86. Clock Configurations

The combination of the clock noise and the CW path noise can degrade CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the mixer clock inputs must be better than the phase noise of the CW path.

In the 16, 8, and 4 × f_{cw} operation modes, a low-phase noise clock is required for the 16, 8, and 4 × f_{cw} clocks (that is, the CW_CLK_NX) in order to maintain good CW phase noise performance. The 1 × f_{cw} clock is only used to synchronize multiple device chips and is not used for demodulation. Thus, the 1 × f_{cw} clock phase noise is not a concern. However, in the 1 × f_{cw} operation mode, low-phase noise clocks are required for both the CLKP_16X, CLKM_16X and CLKP_1X, CLKM_1X pins because both pins are used for mixer demodulation. In general, a higher slew rate clock has lower phase noise. Thus, clocks with high amplitude and fast slew rate are preferred in CW operation.

Internal to the device, there is a division of the Nx clock (for example, N = 16, 8, or 4) to generate LO(t). A clock division results in improvement of the phase noise. The phase noise of a divided clock can be improved approximately by a factor of 20logN dB, where N is the dividing factor of 16, 8, or 4. If the target phase noise of the mixer LO clock 1 × f_{cw} is 160 dBc/Hz at a 1-kHz off the carrier, the 16 × f_{cw} clock phase noise must be greater than (160 – 20log16 = 136 dBc/Hz). TI’s jitter cleaners (LMK048x, CDCM7005, and CDCE72010) exceed this requirement and can be selected to work with the device. In the 4X and 1X modes, higher-quality input clocks are expected to achieve the same performance because *N* is smaller. Thus, the 16X mode is a preferred mode because this mode reduces the phase noise requirement for the system clock design.

Note that in the 16X operation mode, the CW operation range is limited to 8 MHz as a result of the 16X clock. The maximum clock frequency for the 16X clock is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with a degradation in performance. For example, the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz.

As the channel number in a system increases, clock distribution becomes more complex. Using one clock driver output is not preferred to drive multiple AFEs because the clock buffer load capacitance increases by a factor of *N* (N is the number of AFEs in a system). See the *System Clock Configuration for Multiple Devices* section for further details of the system clock configuration. When clock phase noise is not a concern (for example, the 1 × f_{cw} clock in the 16, 8, and 4 × f_{cw} operation modes), one clock driver output can excite more than one device. Nevertheless, special considerations must be applied for such a clock distribution network design. Preferably, all clocks are generated from the same clock source in typical ultrasound systems (such as 16 × f_{cw} and 1 × f_{cw} clocks, audio ADC clocks, RF ADC clocks, pulse repetition frequency signals, frame clocks, and so on). By using the same clock source, interference resulting from clock asynchronization can be minimized.

9.3.6.5 CW Supporting Circuits

As a general practice in the CW circuit design, in-phase and quadrature channels must be strictly symmetrical by using well-matched layout and high-accuracy components. Additional high-pass wall filters (20 Hz to 500 Hz) and low-pass audio filters (10 kHz to 100 kHz) with multiple poles are usually required in ultrasound systems. Noise under this range is critical because the CW Doppler signal ranges from 20 Hz to 20 kHz. Consequently, low-noise audio operational amplifiers are suitable to build these active filters for CW post-processing (that is, the OPA1632, OPA2211, or THS4131). More filter design techniques can be found at www.ti.com. The TI active filter design tool is the WEBENCH® Filter Designer. The filtered audio CW I/Q signals are sampled by audio ADCs and processed by the DSP or PC. Although the CW signal frequency is from 20 Hz to 20 KHz, higher sampling-rate ADCs are still preferred for further decimation and SNR enhancement. Because of the large dynamic range of CW signals, high-resolution ADCs (≥ 16 bits) are required [such as the ADS8413 (2 MSPS, 16 bits, 92-dBFS SNR) and the ADS8472 (1 MSPS, 16 bits, 95-dBFS SNR)]. ADCs for in-phase and quadrature-phase channels must be strictly matched, not only for amplitude matching but also for phase matching in order to achieve the best I/Q matching. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

9.3.7 Analog-to-Digital Converter (ADC)

The device supports a high-performance, 14-bit ADC that achieves 72-dBFS SNR. This ADC ensures excellent SNR at low-chain gain. The ADC can operate at maximum speeds of 65 MSPS and 80 MSPS, providing a 14-bit and a 12-bit output, respectively. The low-voltage differential signaling (LVDS) outputs of the ADC enable a flexible system integration that is desirable for miniaturized systems. In the following sections, a full description of all inputs and outputs of the ADC with different configurations are provided along with suitable examples.

NOTE

The ADC is part of the TGC signal chain. An ADC is not used in CW mode and can be powered down in this mode using the appropriate register controls.

9.3.7.1 System Clock Input

The 16 channels on the device operate from a single clock input. To ensure that the aperture delay and jitter are the same for all channels, the device uses a clock tree network to generate individual sampling clocks for each channel. The clock lines for all channels are matched from the source point to the sampling circuit for each of the 16 internal ADCs. The delay variation is described by the aperture delay parameter of the *Output Interface Timing Characteristics* table. Variation over time is described by the aperture jitter parameter of the *Output Interface Timing Characteristics* table.

This system clock input can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). The device clock input has an internal buffer and clock amplifier (as shown in Figure 87) that are enabled or disabled automatically, depending on the type of clock provided (auto-detect feature).

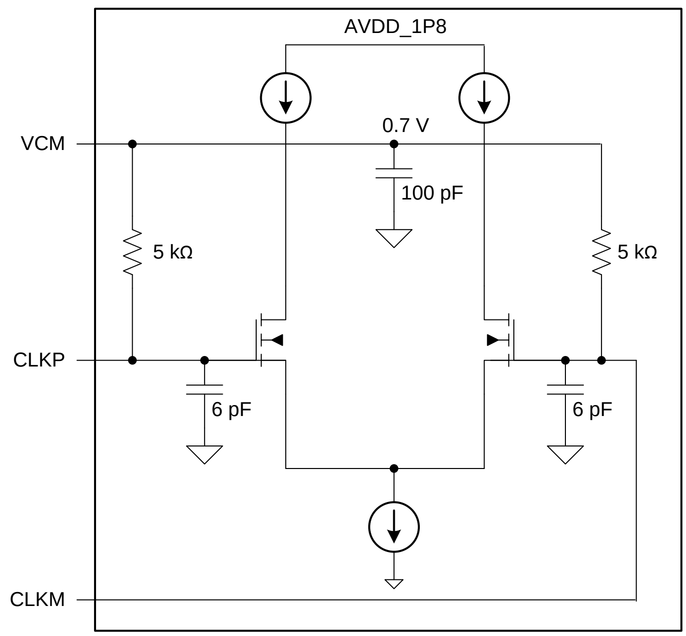


Figure 87. Internal Clock Buffer for Differential Clock Mode

If the preferred clocking scheme for the device is single-ended, connect the single-ended clock to ADC_CLKP and connect the ADC_CLKM pin to ground (in other words, short ADC_CLKM directly to AVSS, as shown in Figure 88). In this case, the auto-detect feature shuts down the internal clock buffer and the device automatically goes into a single-ended clock mode. Connect the single-ended clock source directly (without decoupling) to the ADC_CLKP pin. Low-jitter, square signals (LVCMOS levels, 1.8-V amplitude) are recommended to drive the ADC in single-ended clock mode (refer to technical brief SLYT075 for further details).

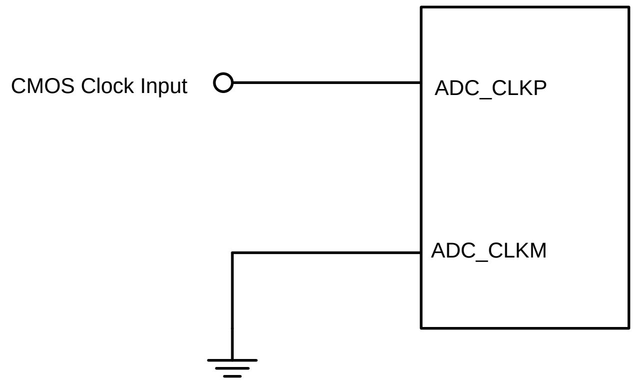


Figure 88. Single-Ended Clock Driving Circuit

For single-ended sinusoidal clocks, or for differential clocks (such as differential sine wave, LVPECL, LVDS, and so forth), enable the clock amplifier with the connection scheme shown in Figure 89. The 10-nF capacitor used to ac-couple the clock input is as shown in Figure 89.

If a transformer is used with the secondary coil floating (for instance, to convert from single-ended to differential), the transformer can be connected directly to the clock inputs without requiring the 10-nF series capacitors, provided that center tap of the transformer is either floating or ac-grounded.

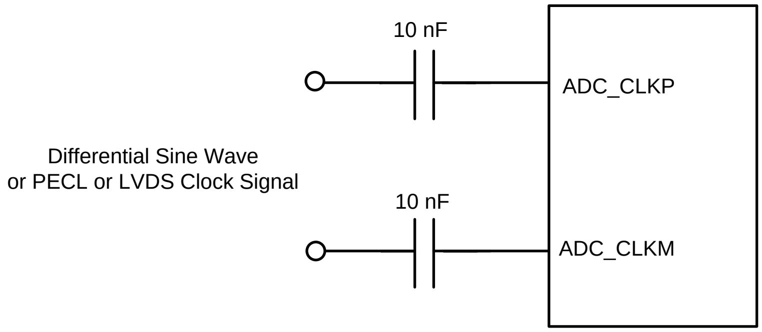


Figure 89. Differential Clock Driving Circuit

9.3.7.2 System Clock Configuration for Multiple Devices

To ensure that the aperture delay and jitter are the same for all channels, the device uses a clock tree network to generate individual sampling clocks for each channel. For all channels, the clock is matched from the source point to the sampling circuit of each of the eight internal devices. The variation on this delay is described in the *Aperture Delay* parameter of the *Output Interface Timing Characteristics* table. Variation is described by the aperture jitter parameter of the *Output Interface Timing Characteristics* table.

Figure 90 shows a clock distribution network.

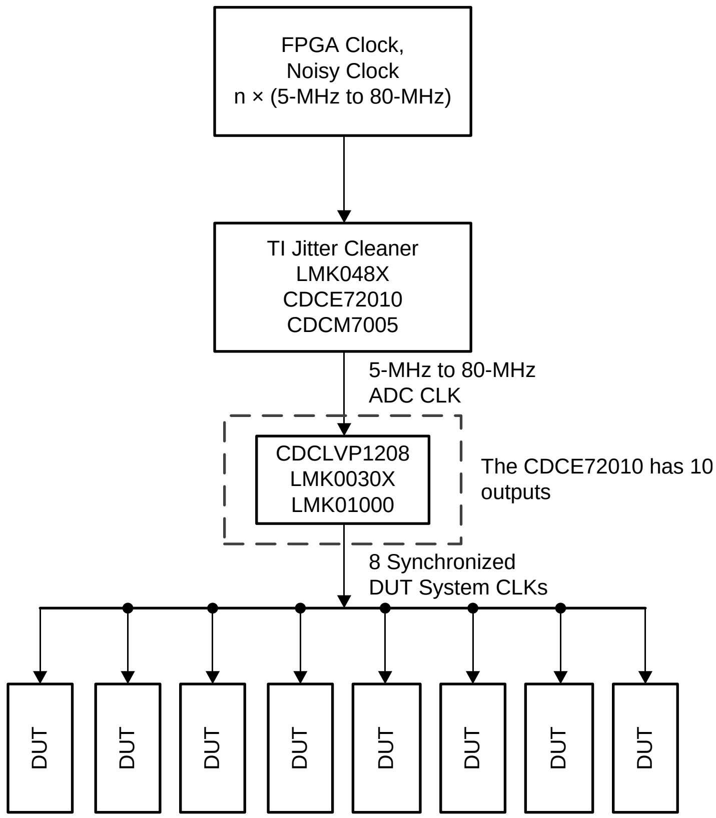


Figure 90. System Clock Distribution Network

9.3.7.3 LVDS Interface

The device supports an LVDS output interface in order to transfer device digital data serially to an FPGA. The device has a total of 18 LVDS output lines. One of these pairs is a serial data clock, another pair is a data framing clock, and the remaining 16 pairs are dedicated for data transfer. A graphical representation of the LVDS output is shown in Figure 91.

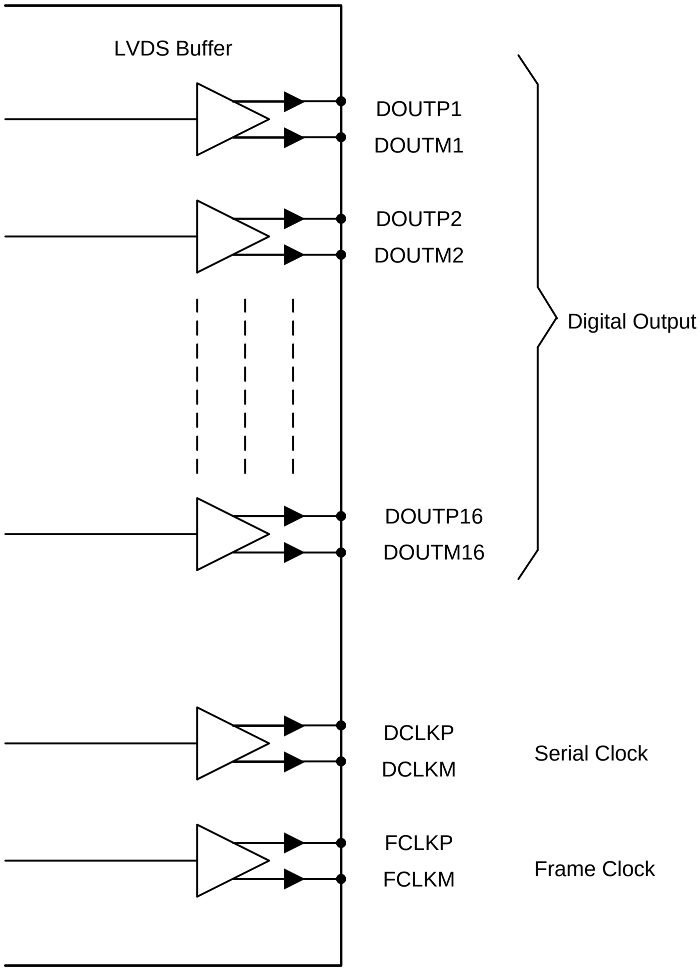


Figure 91. LVDS Output

9.3.7.3.1 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 92. The buffer is designed for a normal output impedance of 100 Ω (R_{OUT}). Terminate the differential outputs at the receiver end by a 100-Ω termination. The buffer output impedance functions like a source-side series termination. By absorbing reflections from the receiver end, the buffer output impedance helps improve signal integrity. Note that this internal termination cannot be disabled nor can its value be changed.

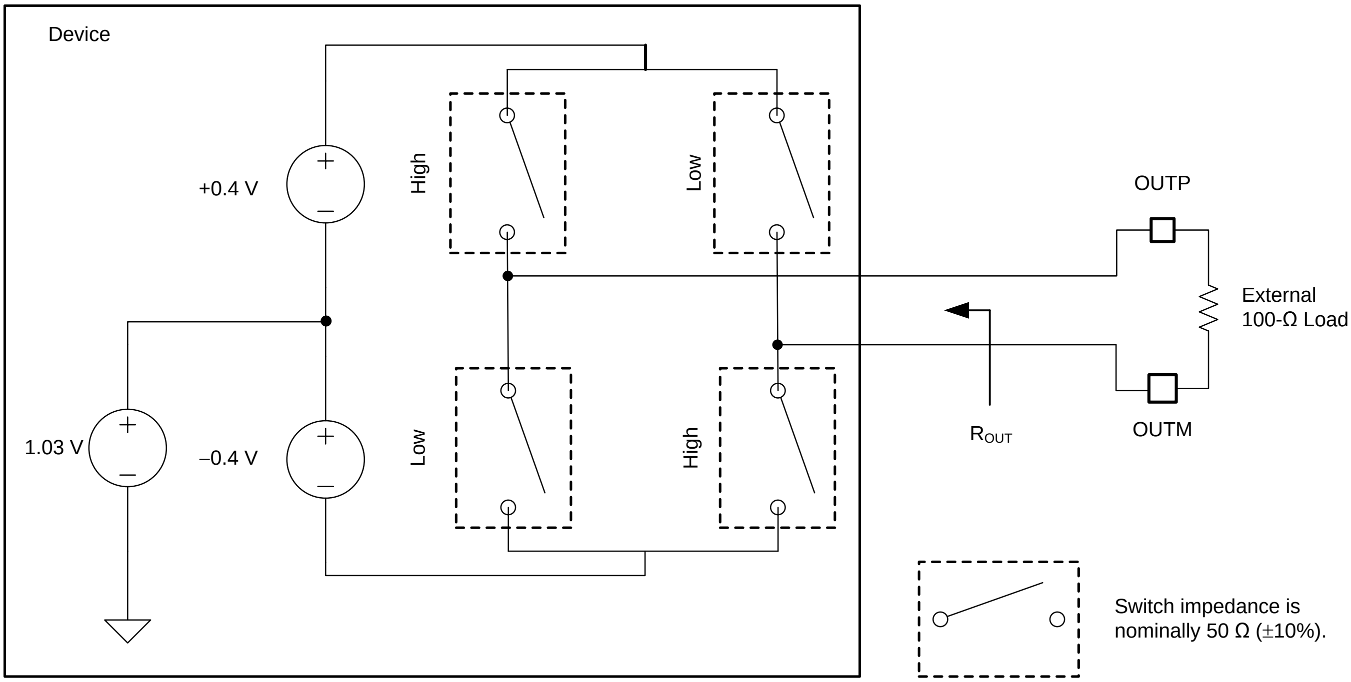


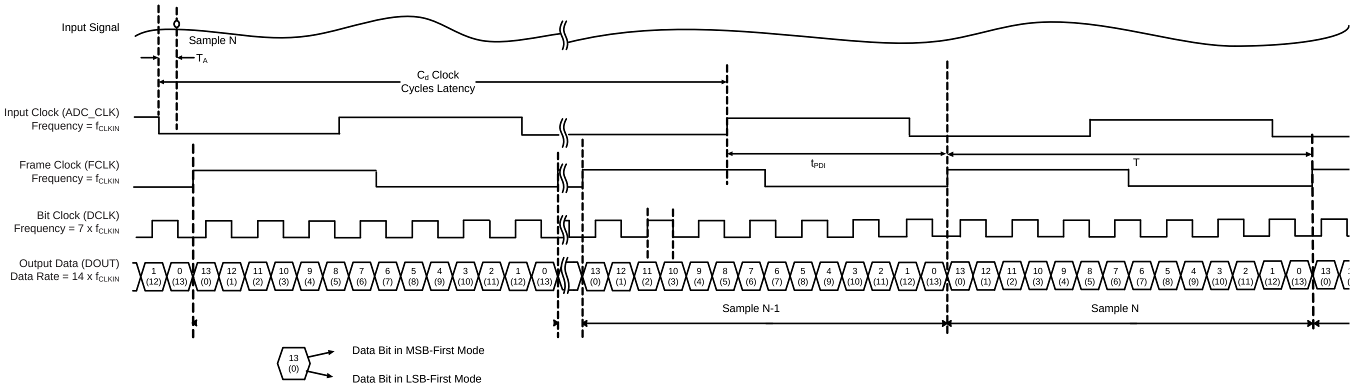
Figure 92. LVDS Output Circuit

9.3.7.3.2 LVDS Data Rate Modes

The LVDS interface supports two data rate modes, as described in this section.

9.3.7.3.2.1 1X Data Rate Mode

In 1X data rate mode, each LVDS output carries data from a single ADC. Figure 93 and Figure 94 show the output data, serial clock, and frame clock LVDS lines for the 14-bit and 12-bit 1X mode, respectively.



(1) K = ADC resolution.

Figure 93. 14-Bit, 1X Data Rate Output Timing Specification

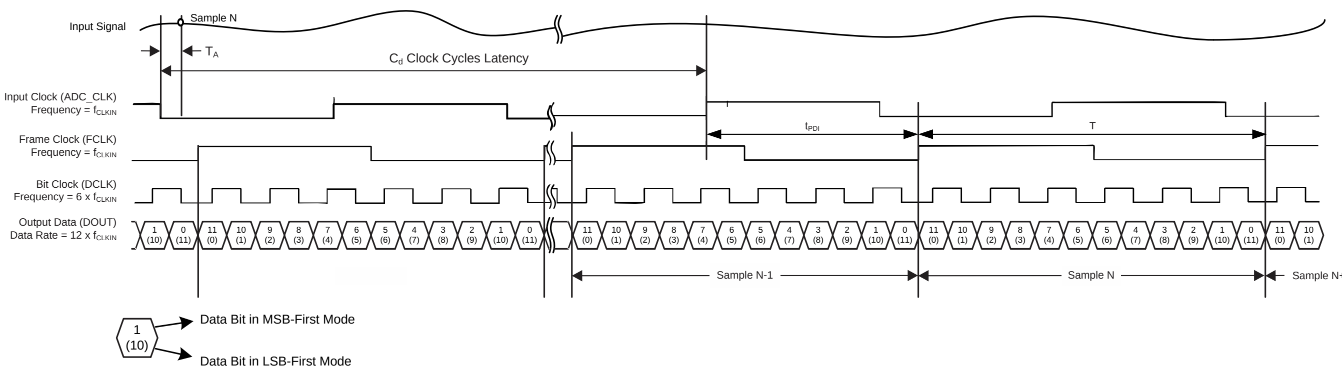


Figure 94. 12-Bit, 1X Data Rate Output Timing Specification

9.3.7.3.2.2 2X Data Rate Mode

In 2X data rate mode, only half of the LVDS lines are used to transfer data. Thus, this mode is useful for saving power when lower sampling frequency ranges permit. This mode is enabled with the LVDS_RATE_2X register bit (register 1, bit 14). After enabling this mode, the digital data from two ADCs are transmitted with a single LVDS lane. When compared to the 1X data rate mode, the 2X data rate mode serial clock frequency is doubled, but the frame clock frequency remains the same (for the same serialization factor and ADC resolution).

When the frame clock is high, data on DOUT1 correspond to channel 1, data on DOUT2 correspond to channel 3, and so forth. When the frame clock is low, DOUT1 transmits channel 2 data, DOUT2 transmits channel 4 data, and so forth.

Figure 95 and Figure 96 show a timing diagram for the 14-bit and 12-bit 2X mode, respectively. Channel and LVDS data line mapping for this mode are listed in Table 13. Note that idle LVDS lines are not powered down by default. To save power, these lines can be powered down using the corresponding power-down bits (PDN_LVDSx).

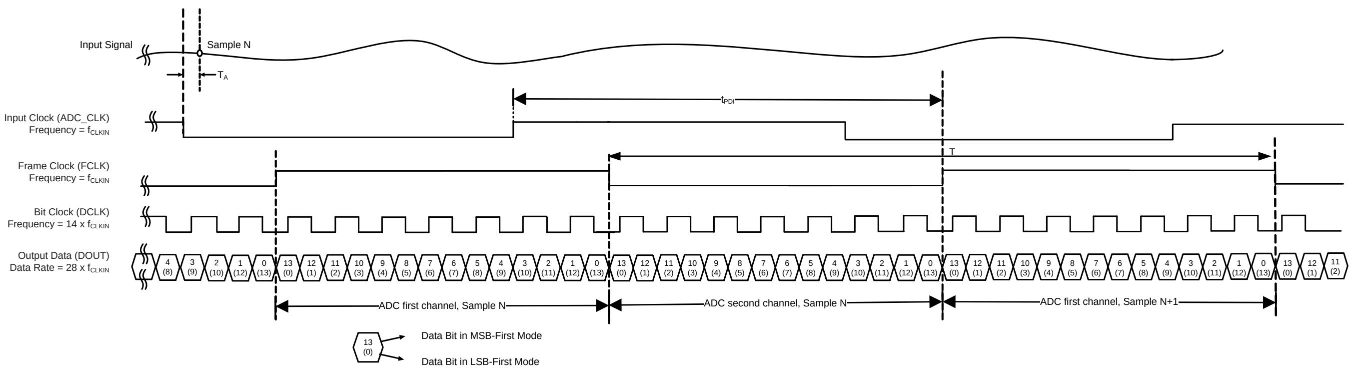


Figure 95. 14-Bit, 2X Data Rate Output Timing Specification

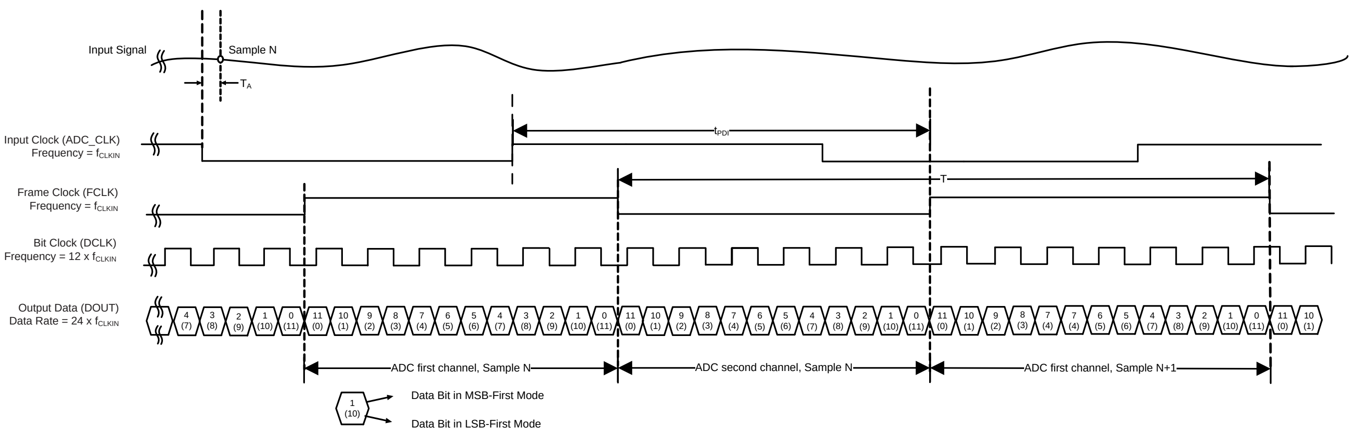


Figure 96. 12-Bit, 2X Data Rate Output Timing Specification

Table 13 illustrates which LVDS output lines are active in 2X data rate mode. The idle channels can be powered down using appropriate register controls.

Table 13. Channel and ADC Data Line Mapping (2X Rate)

CHANNELS	MAPPING
DOUT1	ADC data for channels 1 and 2
DOUT2	ADC data for channels 3 and 4
DOUT3	ADC data for channels 5 and 6
DOUT4	ADC data for channels 7 and 8
DOUT5	Idle
DOUT6	Idle
DOUT7	Idle
DOUT8	Idle
DOUT9	ADC data for channels 9 and 10
DOUT10	ADC data for channels 11 and 12
DOUT11	ADC data for channels 13 and 14
DOUT12	ADC data for channels 15 and 16
DOUT13	Idle
DOUT14	Idle
DOUT15	Idle
DOUT16	Idle

9.3.7.4 ADC Register, Digital Processing Description

The ADC has extensive digital processing functionalities that can be used to enhance ADC output performance. The digital processing blocks are arranged as shown in Figure 97.

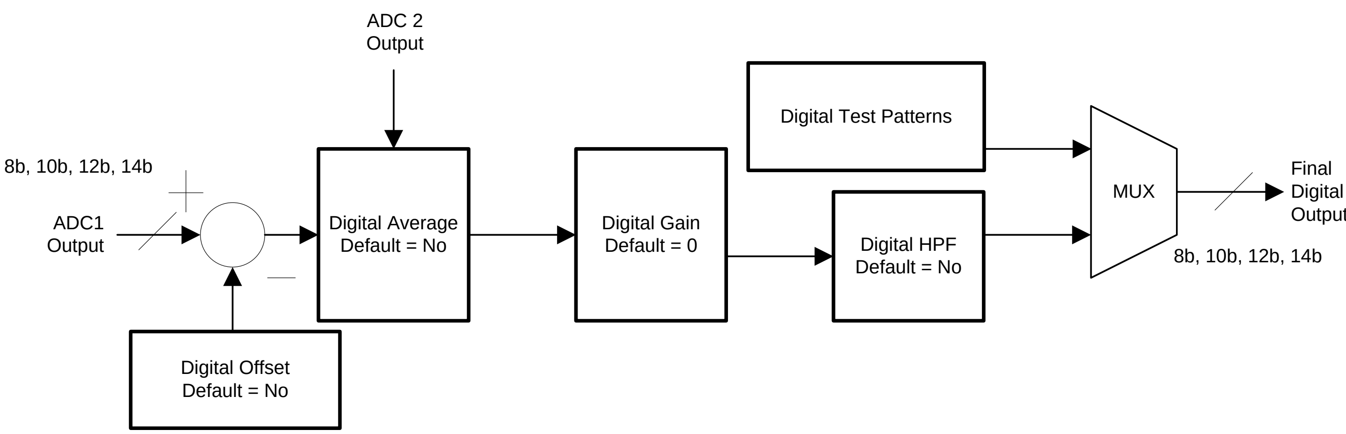


Figure 97. ADC Digital Block Diagram

9.3.7.4.1 Digital Offset

Digital functionality provides for channel offset correction. Setting the DIG_OFFSET_EN bit to 1 enables the subtraction of the offset value from the ADC output. There are two offset correction modes, as shown in Figure 98.

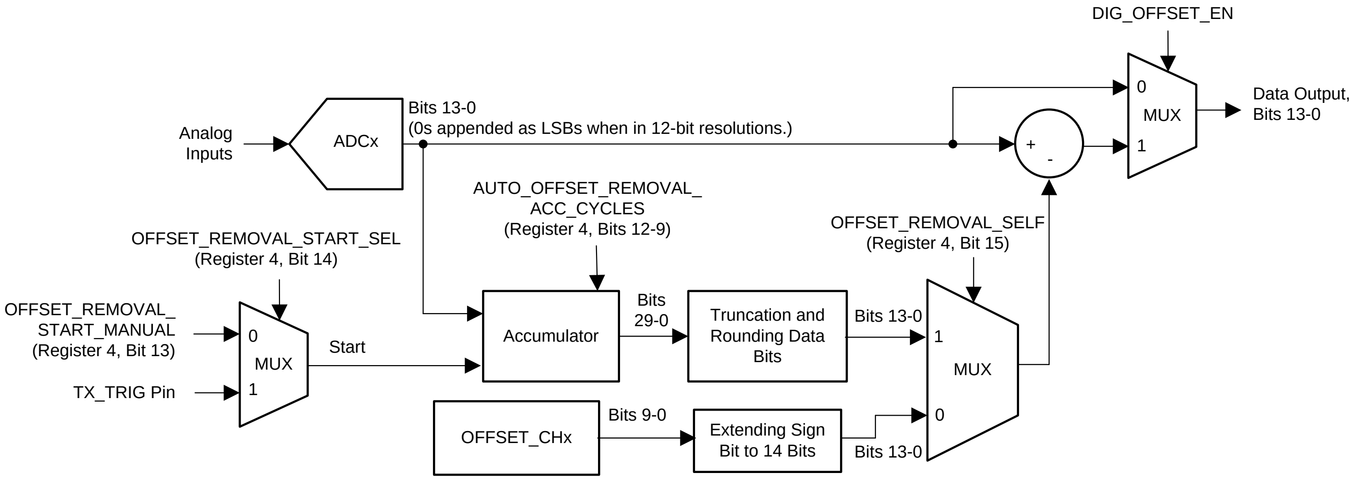


Figure 98. Digital Offset Correction Block Diagram

9.3.7.4.1.1 Manual Offset Correction

If the channel offset is known, the appropriate value can be written in the OFFSET_CHx register for channel x. The offset value programmed in the OFFSET_CHx register subtracts out from the ADC output. The offset of each of the 16 ADC output channels can be independently programmed. The same offset value must be programmed into two adjacent offset registers. For instance, when programming the channel 1 offset value 0000011101, write the same offset value of 0000011101 in registers 13 (bits 9-0) and 14 (bits 9-0). The offset values are to be written in twos complement format.

9.3.7.4.1.2 Auto Offset Correction Mode (Offset Correction using a Built-In Offset Calculation Function)

The auto offset calculation module can be used to calculate the channel offset that is then subtracted from the ADC output. To enable the auto offset correction mode, set the OFFSET_REMOVAL_SELF bit to 0.

In auto offset correction mode, the dc component of the ADC output (assumed to be the channel offset) is estimated using a digital accumulator. The ADC output sample set used by the accumulator is determined by a start time or by the first sample and number of samples to be used. Figure 98 illustrates the options available to determine the accumulator sample set. A high pulse on the TX_TRIG pin or setting the OFFSET_REMOVAL_START_MANUAL register can be used to determine the accumulator first sample. To set the number of samples, the AUTO_OFFSET_REMOVAL_ACC_CYCLES register (bits 12-9) must be programmed according to Table 14.

If a pulse on the TX_TRIG pin is used to set the first sample, additional flexibility in setting the first sample is provided. A programmable delay between the TX_TRIG pulse and first sample can be set by writing to the OFFSET_CORR_DELAY_FROM_TX_TRIG register.

The determined offset value can be read out channel-wise. Set the channel number in the AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL register and read the offset value for the corresponding channel in the AUTO_OFFSET_REMOVAL_VAL_RD register.

Table 14. Auto Offset Removal Accumulator Cycles

AUTO_OFFSET_REMOVAL_ACC_CYCLES (Bits 3-0)	NUMBER OF SAMPLES USED FOR OFFSET VALUE EVALUATION
0	2047
1	127
2	255
3	511
4	1023
5	2045
6	4095
7	8191
8	16383
9	32767
10 to 15	65535

9.3.7.4.2 Digital Average

The signal-to-noise ratio (SNR) of the signal chain can be improved by providing the same input signal to two channels and averaging their output digitally. To enable averaging, set the AVG_EN register bit (register 2, bit 11). The way that data are transmitted on the digital output lines in this mode is described in Table 15.

Table 15. Channel and ADC Data Line Mapping (Averaging Enabled)

CHANNELS	MAPPING
DOUT1	Average of channels 1 and 2
DOUT2	Average of channels 3 and 4
DOUT3	Average of channels 5 and 6 (1)
DOUT4	Average of channels 7 and 8 (1)
DOUT5	Idle
DOUT6	Idle
DOUT7	Idle
DOUT8	Idle
DOUT9	Average of channels 9 and 10
DOUT10	Average of channels 11 and 12
DOUT11	Average of channels 13 and 14 (1)
DOUT12	Average of channels 15 and 16 (1)
DOUT13	Idle
DOUT14	Idle
DOUT15	Idle
DOUT16	Idle

(1) Idle when AVG_EN = 1 and when the LVDS data rate is set to 2X mode.

NOTE

Idle LVDS lines are not powered down by default. To save power, these lines can be powered down using the corresponding power-down bits (PDN_LVDSx).

The serialization factor must be greater than the ADC resolution to obtain SNR improvement after averaging in 12b resolution.

9.3.7.4.3 Digital Gain

To enable the digital gain block, set DIG_GAIN_EN (register 3, bit 12) to 1. When enabled, the gain value for channel x (where x is from 1 to 16) can be set with the 4-bit register control for the corresponding channel (GAIN_CHx). Gain is given as (0 dB + 0.2 dB × GAIN CHx). For instance, if GAIN_CH5 = 3 (decimal equivalent of the 4-bit word), then channel 5 is increased by a 0.6-dB gain. GAIN_CHx = 31 produces the same effect as GAIN_CHx = 30, which sets the gain of channel x to 6 dB.

9.3.7.4.4 Digital HPF

To enable the digital high-pass filter (HPF) of channels 1 to 4, 5 to 8, 9 to 12, and 13 to 16, set the DIG_HPF_EN_CH1-4, DIG_HPF_EN_CH5-8, DIG_HPF_EN_CH9-12, and DIG_HPF_EN_CH13-16, respectively.

The HPF_CORNER_CHxy register bits (where xy are 1-4, 5-8, 9-12, or 13-16) control the characteristics of a digital high-pass transfer function applied to the output data, based on Equation 10. These bits correspond to bits 4-1 in registers 21, 33, 45, and 57, respectively (these register settings describe the value of K). The valid values of K are 2 to 10. The digital HPF can be used to suppress low-frequency noise. Table 16 describes the cutoff frequency versus K.

$$Y(n) = \frac{2^k}{2^k + 1}\,[x(n) - x(n-1) + y(n-1)] \tag{10}$$

Table 16. Digital HPF, –1-dB Corner Frequency versus K and f_S

CORNER FREQUENCY (k) (HPF_CORNER_CHxy Register)	CORNER FREQUENCY (kHz)		
	f_S = 40 MSPS	f_S = 50 MSPS	f_S = 65 MSPS
2	2780	3480	4520
3	1490	1860	2420
4	738	230	1200
5	369	461	600
6	185	230	300
7	111	138	180
8	49	61	80
9	25	30	40
10	12.	15	20

The HPF output is mapped to the ADC resolution bits either by truncation or a round-off operation. By default, the HPF output is truncated to map to the ADC resolution. To enable the rounding operation to map the HPF output to the ADC resolution, set the HPF_ROUND_ENABLE register bit (register 21, bit 5) to 1.

9.3.7.5 LVDS Synchronization Operation

Different test patterns can be synchronized on the LVDS serialized output lines to help set and program the FPGA timing that receives the LVDS serial output. Of these test patterns, the ramp, toggle, and pseudo-random sequence (PRBS) test patterns can be reset or synchronized by providing a synchronization pulse on the TX_TRIG pin or by setting and resetting a specific register bit. The synchronization pulse on the TX_TRIG pin must meet the setup and hold time constraints with respect to the system clock, as shown in Figure 99. Parameter values are listed in the *Output Interface Timing Requirements* table.

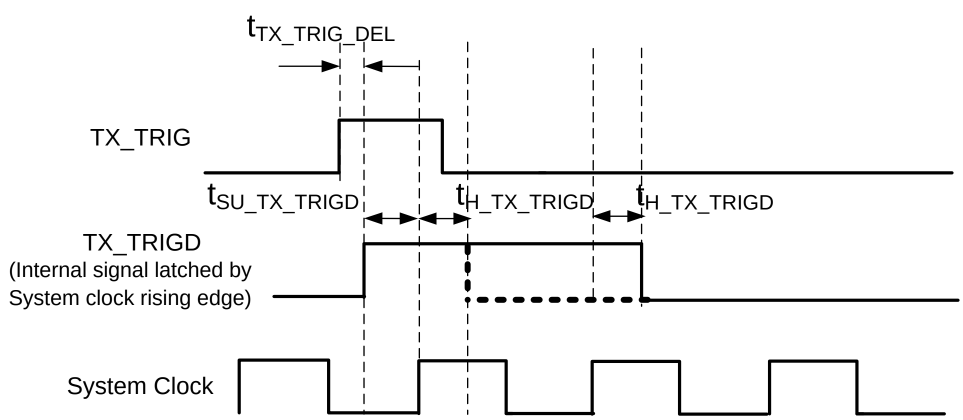


Figure 99. Setup and Hold Time Constraint for the TX_TRIG Signal

ADC data may be corrupted for four to six clocks immediately after applying TX_TRIG. The phase reset from TX_TRIG can be disabled using MASK_TX_TRIG.

9.3.8 Power Management

Power management plays a critical role to extend battery life and to ensure a long operation time. The device has a fast and flexible power-up and power-down control that can maximize battery life. The device can be either powered down or up through external pins or internal registers.

This section describes the functionality of different power-down pins and register bits available in the device. The device can be divided in two major blocks: the VCA and ADC; see Figure 100 and Figure 101.

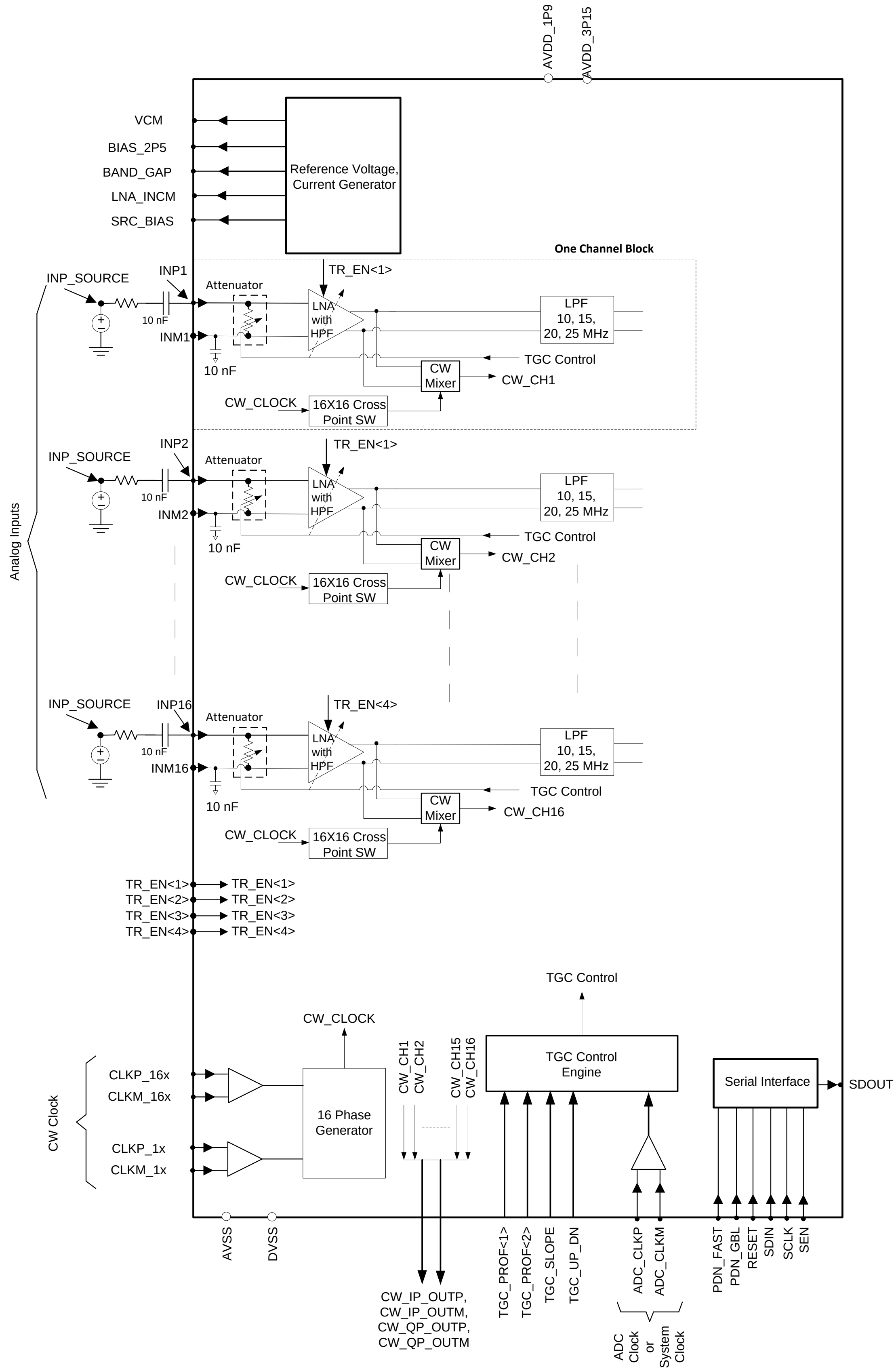


Figure 100. VCA Block Diagram

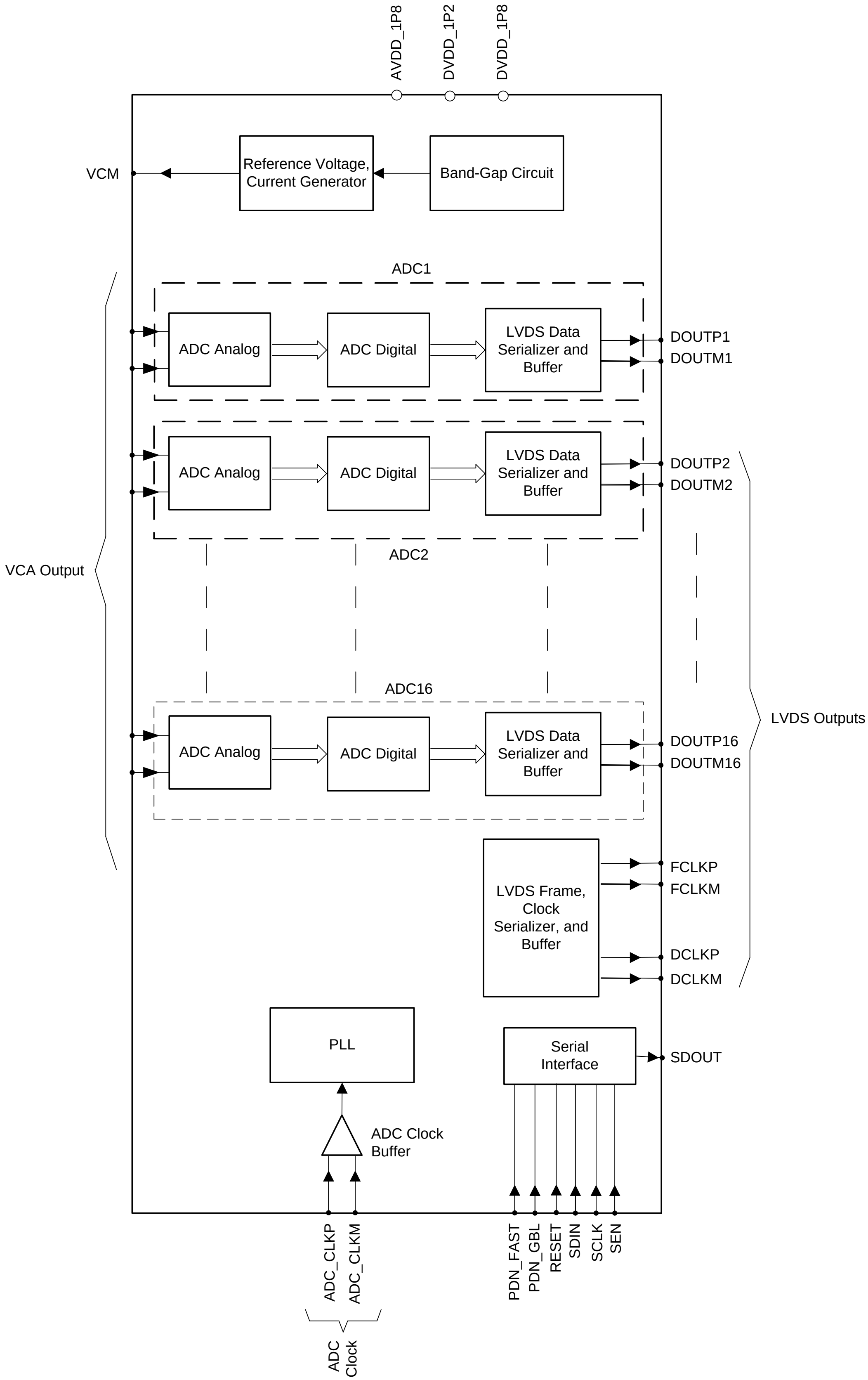


Figure 101. ADC Block Diagram

9.3.8.1 Voltage-Controlled Attenuator (VCA) Power Management

The VCA consists of the following blocks:

- Band-gap circuit,
- Serial interface,
- Reference voltage and current generator,
- A total of 16 channel blocks (each channel block includes an attenuator, LNA, LPF, CW mixer, and a 16 × 16 cross-point switch),
- TGC control engine, and
- Phase generator for CW mode.

Of these VCA blocks, the band-gap, attenuator, and serial interface block cannot be powered down by using power-down pins or bits. Table 17 lists all the VCA blocks that are powered down using various pin and bit settings.

Table 17. VCA Power-Down Mode Descriptions

NAME	TYPE (Pin or Register)	LNA	LPF	CW MIXER	16 × 16 CROSS-POINT SWITCH	TGC CONTROL ENGINE	REFERENCE	PHASE GENERATOR	CHANNEL
PDN_GBL	Pin	Yes(1)	Yes	Yes	Yes	Yes	Yes	Yes	All(2)
GBL_PDWN	Register	Yes	Yes	Yes	Yes	Yes	Yes	Yes	All
PDN_FAST	Pin	Yes	Yes	Yes	Yes	No	No	Yes	All
FAST_PDWN	Register	Yes	Yes	Yes	Yes	No	No	Yes	All
PDCHxx	Register	Yes	Yes	Yes	Yes	No	No	No	Individual
PDWN_LNA	Register	Yes	No	No	No	No	No	No	All
PDWN_FILTER	Register	No	Yes	No	No	No	No	No	All

(1) Yes = powered down; no = active.
(2) All = all channels are powered down; individual = only a single channel is powered down, depending upon the corresponding bit.

If more than one bit is simultaneously enabled, then all blocks listed as *Yes* for each bit setting are powered down.

9.3.8.2 Analog-to-Digital Converter (ADC) Power Management

The ADC consists of the following blocks:

- Band-gap circuit,
- Serial interface,
- Reference voltage and current generator,
- ADC analog block that performs a sampling and conversion,
- ADC digital block that includes all the digital post processing blocks (such as the offset, gain, digital HPF, and so forth),
- LVDS data serializer and buffer that converts the ADC parallel data to a serial stream,
- LVDS frame and clock serializer and buffer, and
- PLL (phase-locked loop) that generates a high-frequency clock for both the ADC and serializer.

Of all these blocks, only the band-gap and serial interface block cannot be powered down using power-down pins or bits. Table 18 lists which blocks in the ADC are powered down using different pins and bits.

Table 18. Power-Down Modes Description for the ADC

NAME	TYPE (Pin or Register)	ADC ANALOG	ADC DIGITAL	LVDS DATA SERIALIZER, BUFFER	LVDS FRAME AND CLOCK SERIALIZER, BUFFER	REFERENCE + ADC CLOCK BUFFER	PLL	CHANNEL
PDN_GBL	Pin	Yes(1)	Yes	Yes	Yes	Yes	Yes	All(2)
GLOBAL_PDN	Register	Yes	Yes	Yes	Yes	Yes	Yes	All
PDN_FAST	Pin	Yes	Yes	Yes	No	No	No	All
DIS_LVDS	Register	No	No	Yes	Yes	No	No	All
PDN_ANA_CHx	Register	Yes	No	No	No	No	No	Individual
PDN_DIG_CHx	Register	No	Yes	No	No	No	No	Individual
PDN_LVDSx	Register	No	No	Yes	No	No	No	Individual

(1) Yes = powered down; no = active.
(2) All = all channels are powered down; individual = only a single channel is powered down, depending upon the corresponding bit.

9.4 Device Functional Modes

9.4.1 ADC Test Pattern Mode

9.4.1.1 Test Patterns

9.4.1.1.1 LVDS Test Pattern Mode

The ADC data coming out of the LVDS outputs can be replaced by different kinds of test patterns. The different test patterns are described in Table 19.

Table 19. Description of LVDS Test Patterns

TEST PATTERN MODE	PROGRAMMING THE MODE: THE SAME PATTERN MUST BE COMMON TO ALL DATA LINES (DOUT)	PROGRAMMING THE MODE: THE PATTERN IS SELECTIVELY REQUIRED ON ONE OR MORE DATA LINE (DOUT)	TEST PATTERNS REPLACE(1)
All 0s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	Zeros in all bits (00000000000000)
All 1s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	Ones in all bits (11111111111111)
Deskew	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The ADC data is replaced by alternate 0s and 1s (01010101010101)
Sync	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	ADC data are replaced by half 1s and half 0s (11111110000000)
Custom	Set the mode using PAT_MODES[2:0]. Set the desired custom pattern using the CUSTOM_PATTERN register control.	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The word written in the CUSTOM_PATTERN control (taken from the MSB side) replaces ADC data. (For instance, CUSTOM_PATTERN = 1100101101011100 and ADC data = 11001011010111 when the serialization factor is 14.)

(1) Shown for a serialization factor of 14.

Device Functional Modes (continued)

Table 19. Description of LVDS Test Patterns (continued)

TEST PATTERN MODE	PROGRAMMING THE MODE: THE SAME PATTERN MUST BE COMMON TO ALL DATA LINES (DOUT)	PROGRAMMING THE MODE: THE PATTERN IS SELECTIVELY REQUIRED ON ONE OR MORE DATA LINE (DOUT)	TEST PATTERNS REPLACE(1)
Ramp	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The ADC data are replaced by a word that increments by 1 LSB every conversion clock starting at negative full-scale, increments until positive full-scale, and wraps back to negative full-scale. Step size of RAMP pattern is function of ADC resolution (N) and serialization factor (S) and given by $2^{(S-N)}$.
Toggle	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0]	The ADC data alternate between two words that are all 1s and all 0s. At each setting of the toggle pattern, the start word can either be all 0s or all 1s. (Alternate between 11111111111111 and 00000000000000.)
PRBS	Set SEL_PRBS_PAT_GBL = 1. Select either custom or ramp pattern with PAT_MODES[2:0]. Enable PRBS mode using PRBS_EN. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	Set PAT_SELECT_IND = 1. Select either custom or ramp pattern with PAT_LVDSx[2:0]. Enable PRBS mode on DOUTx with the PAT_PRBS_LVDSx control. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	A 16-bit pattern is generated by a 23-bit (or 9-bit) PRBS pattern generator (taken from the MSB side) and replaces the ADC data.

All patterns listed in Table 19 (except the PRBS pattern) can also be forced on the frame clock output line by using PAT_MODES_FCLK[2:0]. To force a PRBS pattern on the frame clock, use the SEL_PRBS_PAT_FCLK, PRBS_EN, and PAT_MODES_FCLK register controls.

The ramp, toggle, and pseudo-random sequence (PRBS) test patterns can be reset or synchronized by providing a synchronization pulse on the TX_TRIG pin or by setting and resetting a specific register bit. A block diagram for the test patterns is provided in Figure 102.

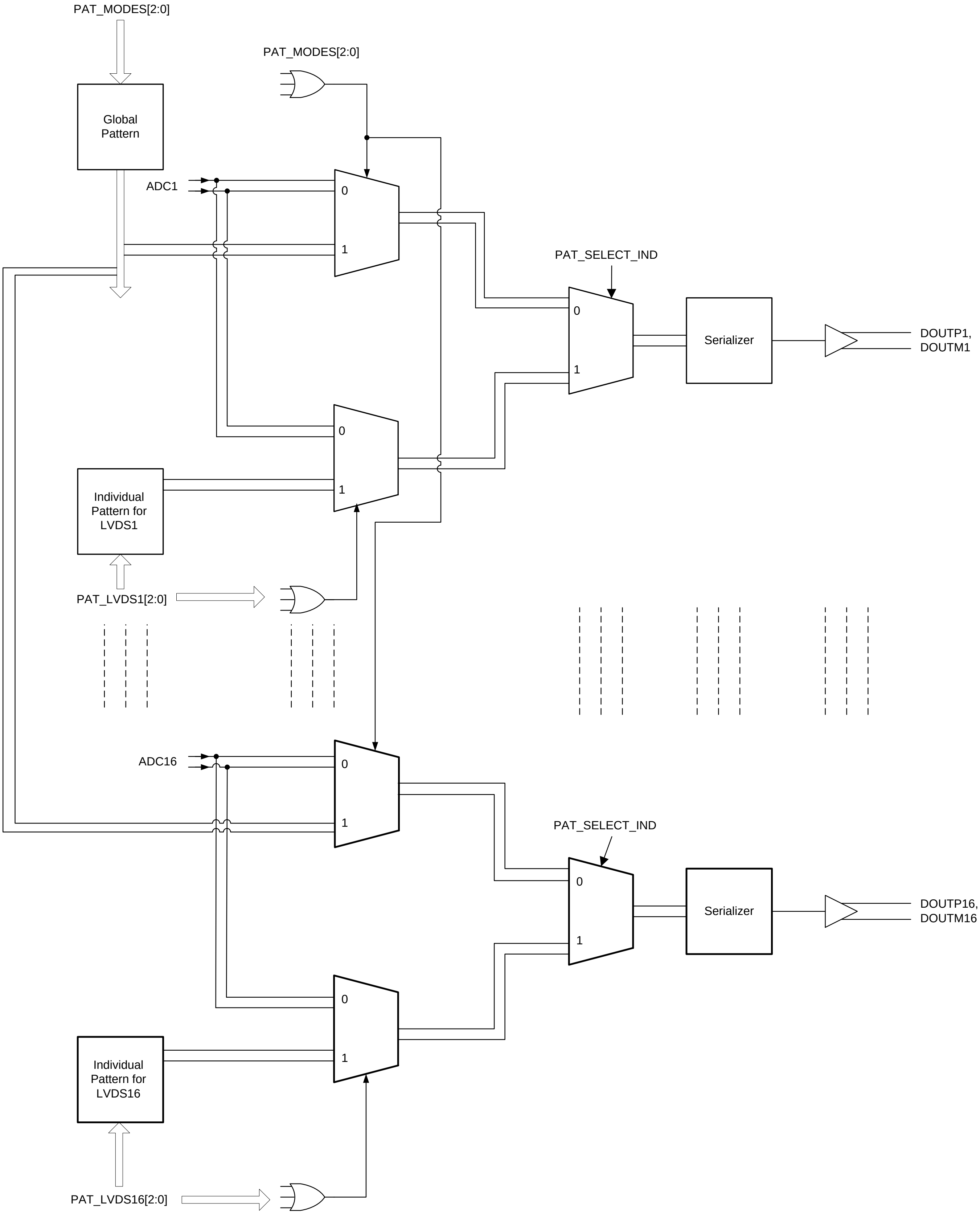


Figure 102. Test Pattern Block Diagram

9.4.2 Partial Power-Up and Power-Down Mode

The partial power-up and power-down mode is also called *fast power-up and power-down mode*. The VCA can be programmed in partial power-down mode either by setting the PDN_FAST pin high or setting the FAST_PDWN register bit to 1. Similarly, the ADC can be programmed in this mode by setting the PDN_FAST pin high. In this mode, many blocks in the signal path are powered down. However, the internal reference circuits, LVDS frame, and data clock buffers remain active. The partial power-down function allows the device to quickly wake-up from a low-power state. This configuration ensures that the external capacitors are discharged slowly; thus, a minimum wake-up time is required as long as the charges on these capacitors are restored. The longest wake-up time depends on the capacitors connected at INP and INM, because the wake-up time is the time required to recharge the capacitors to the desired operating voltages. For larger capacitors, this time is longer. The ADC wake-up time is approximately 1 µs. Thus, the device wake-up time is more dependent on the VCA wake-up time with the assumption that the ADC clock is running for at least 50 µs before the normal operating mode resumes. The power-down time is instantaneous, less than 2 µs. This fast wake-up response is desired for portable ultrasound applications where power savings is critical. The pulse repetition frequency (PRF) of an ultrasound system can vary from 50 kHz to 500 Hz, and the imaging depth (that is, the active period for a receive path) varies from tens of µs to hundreds of µs. The power savings can be quite significant when a system PRF is low. In some cases, only the VCA is powered down when the ADC runs normally to ensure minimal interference to the FPGAs; see the *Electrical Characteristics: TGC Mode* table to determine device power dissipation in partial power-down mode.

9.4.3 Global Power-Down Mode

To achieve the lowest power dissipation, the device can be placed into a complete power-down mode. This mode is controlled through the GBL_PDWN (for the VCA) or GLOBAL_PDN (for the ADC) registers or the PDN_GBL pin (for both the VCA and ADC). In complete power-down mode, all circuits (including reference circuits within the device) are powered down and the capacitors connected to the device are discharged. The wake-up time depends on the time that the device spends in shutdown mode. A 0.01-µF capacitor at INP without a capacitor at INM provides a wake-up time of approximately 1 ms.

9.4.4 TGC Configuration

By default, the VCA is configured in TGC mode after reset. Depending upon the system requirements, the device can be programmed in a suitable power mode using the MEDIUM_POW (register 206, bit 14) and LOW_POW (register 200, bit 12) register bits.

9.4.5 Digital TGC Test Modes

The available test mode bits in the TGC engine are: ENABLE_INT_START, NEXT_CYCLE_WAIT_TIME, MANUAL_START, FLIP_ATTEN, and DIS_ATTEN.

9.4.5.1 ENABLE_INT_START and NEXT_CYCLE_WAIT_TIME

In internal non-uniform digital TGC mode, the device gain starts changing after the TGC_SLOPE pin level goes high. Instead of applying a signal on the TGC_SLOPE pin, the device generates a signal to start the device gain. To generate a signal internally, set the ENABLE_INT_START bit (register 181, bit 14) to 1. When a complete cycle of the gain curve completes and the device gain returns to the start gain stage, the next start pulse is generated after the NEXT_CYCLE_WAIT_TIME (register 183, bits 15-0) number of ADC clock cycles, as shown in Figure 103.

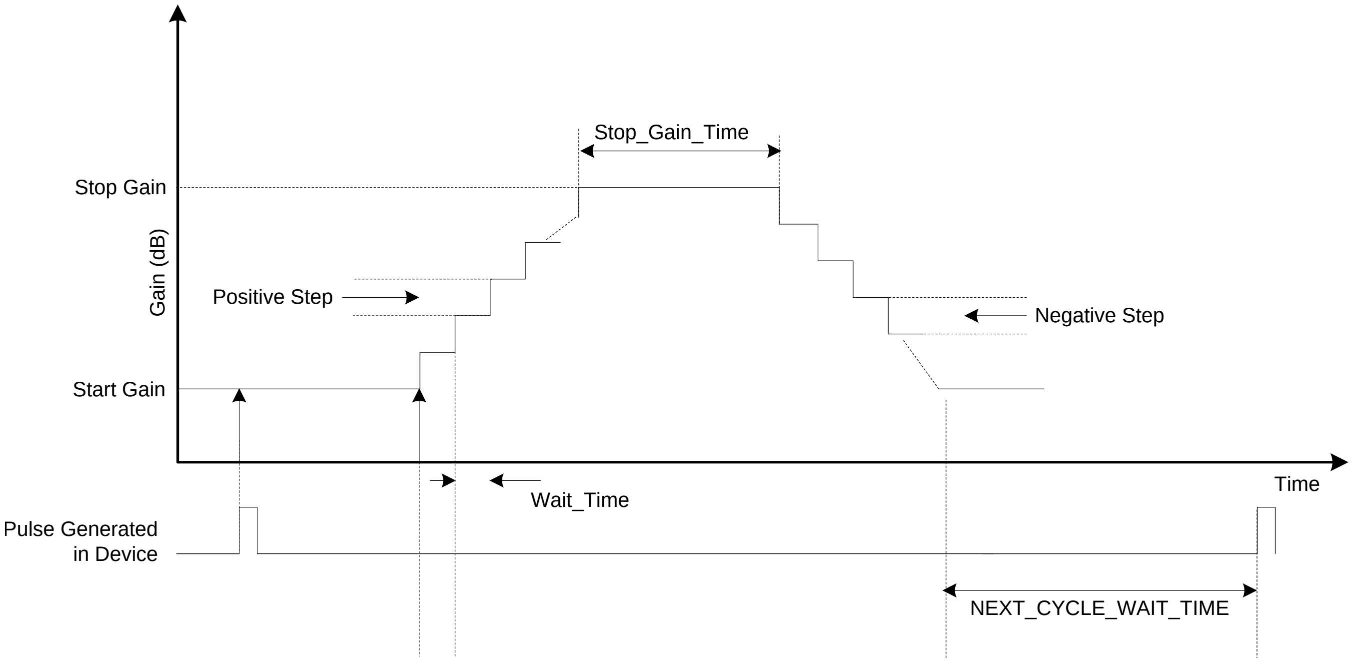


Figure 103. Internal Non-Uniform Test Mode

9.4.5.2 MANUAL_START

In up, down ramp mode and internal non-uniform mode, a single TGC start pulse provided on the TGC_SLOPE pin can be generated by the device when the MANUAL_START bit is enabled. In up, down ramp mode, the MANUAL_START bit also generates a pulse that performs the same functionality that applying a pulse on the TGC_UP_DOWN pin does (that is, reduces the signal gain from stop gain to start gain).

9.4.5.3 FLIP_ATTEN

By default, the attenuation of an attenuator block is varied and followed by an LNA gain variation in all TGC modes. When the FLIP_ATTEN bit (register 182, bit 6) is enabled, the LNA gain is varied first and then followed by the attenuation of an attenuator block.

9.4.5.4 DIS_ATTEN

When the DIS_ATTEN bit is set to 1, the attenuation block is disabled.

9.4.5.5 Fixed Attenuation Mode

The attenuator block can be programmed in fixed attenuation mode (that is, the attenuation does not change with time by enabling the FIX_ATTEN_x (x is the profile number) bit in the *DTGC Register Map*). When the FIX_ATTEN_x bit is set to 1, the attenuation value is set using the ATTENUATION_x register bits. A value of N written in the ATTENUATION_x register sets the attenuation level at $-8 + N \times 0.125$ dB.

9.4.6 CW Configuration

To configure the device in CW mode, set the CW_TGC_SEL register bit (register 192, bit 0) to 1. To save power, the ADC can be powered down completely using the GLOBAL_PDN bit (register 1, bit 0). Usually only half the number of channels in a system are active in the CW mode. Thus, the individual channel control can power-down unused channels and save power; see Table 17 and Table 18. Enabling CW mode automatically configures the LNA from TGC mode to CW mode and disables the LPF stage.

9.4.7 TGC + CW Mode

This device does not support TGC and CW mode simultaneously. Only one mode can remain active at a time.

9.5 Programming

9.5.1 Serial Peripheral Interface (SPI) Operation

This section discusses the read and write operations of the SPI interface.

9.5.1.1 Serial Register Write Description

Several different modes can be programmed with the serial peripheral interface (SPI). This interface is formed by the SEN (serial interface enable), SCLK (serial interface clock), SDIN (serial interface data), and RESET pins. The SCLK, SDIN, and RESET pins have a 16-kΩ pulldown resistor to ground. SEN has a 16-kΩ pullup resistor to supply. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low). SDIN serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse (an internal counter counts the number of 24 clock groups after the SEN falling edge). Data are divided into two main portions: the register address (8 bits) and data (16 bits). Figure 104 shows the timing diagram for serial interface write operation.

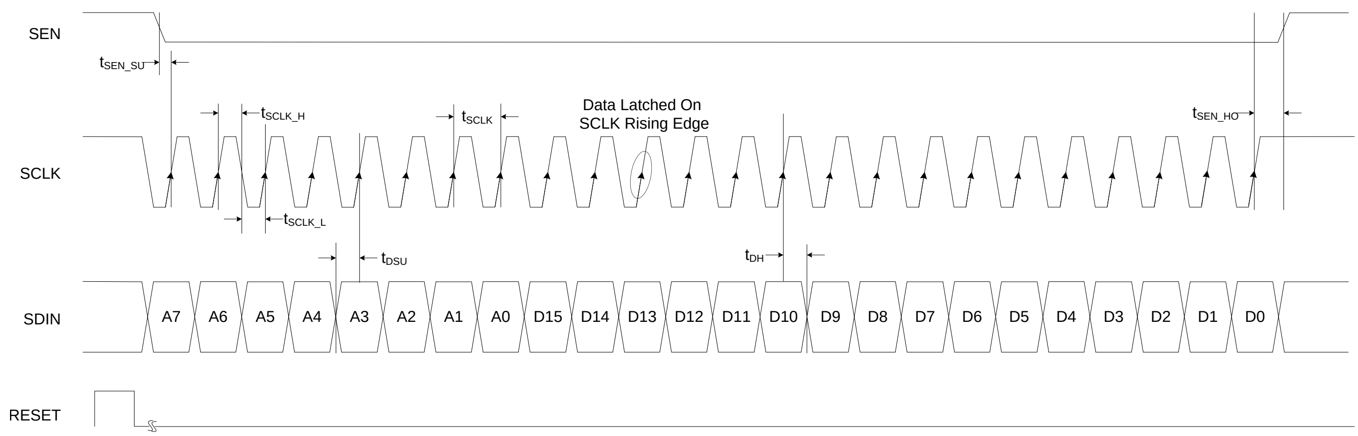


Figure 104. Serial Interface Timing

Programming (continued)

9.5.1.2 Register Readout

The device includes an option where the contents of the internal registers can be read back. This readback can be useful as a diagnostic test to verify the serial interface communication between the external controller and AFE. First, the REG_READ_EN bit must be set to 1. Then, initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read. The data bits are *don't care*. The device outputs the contents (D[15:0]) of the selected register on the SDOUT pin. For lower-speed SCLKs, SDOUT can be latched on the SCLK rising edge. For higher-speed SCLKs, latching SDOUT at the next SCLK falling edge is preferable. The read operation timing diagram is shown in Figure 105. In readout mode, the REG_READ_EN bit can be accessed with SDIN, SCLK, and SEN. To enable serial register writes, set the REG_READ_EN bit back to 0.

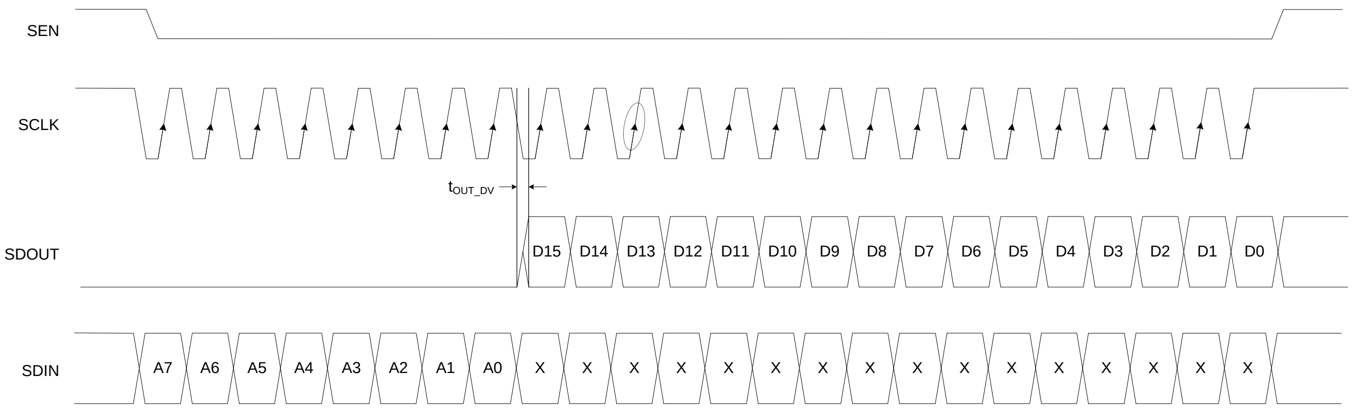


Figure 105. Serial Interface Register, Read Operation

The device SDOUT buffer is 3-stated and is only enabled when the REG_READ_EN bit is enabled. SDOUT pins from multiple devices can therefore be tied together without any pullup resistors. The SN74AUP1T04 level shifter can be used to convert 1.8-V logic to 2.5-V or 3.3-V logic, if necessary.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The device supports a wide-frequency bandwidth signal in the range of several kHz to several MHz. The device is a highly-integrated solution that includes an attenuator, low-noise amplifier (LNA), an antialiasing filter, an analog-to-digital converter (ADC), and a continuous-wave (CW) mixer. As a result of the device functionality, the device can be used in various applications (such as in medical ultrasound imaging systems, sonar imaging equipment, radar, and other systems that require a very large dynamic range).

10.2 Typical Application

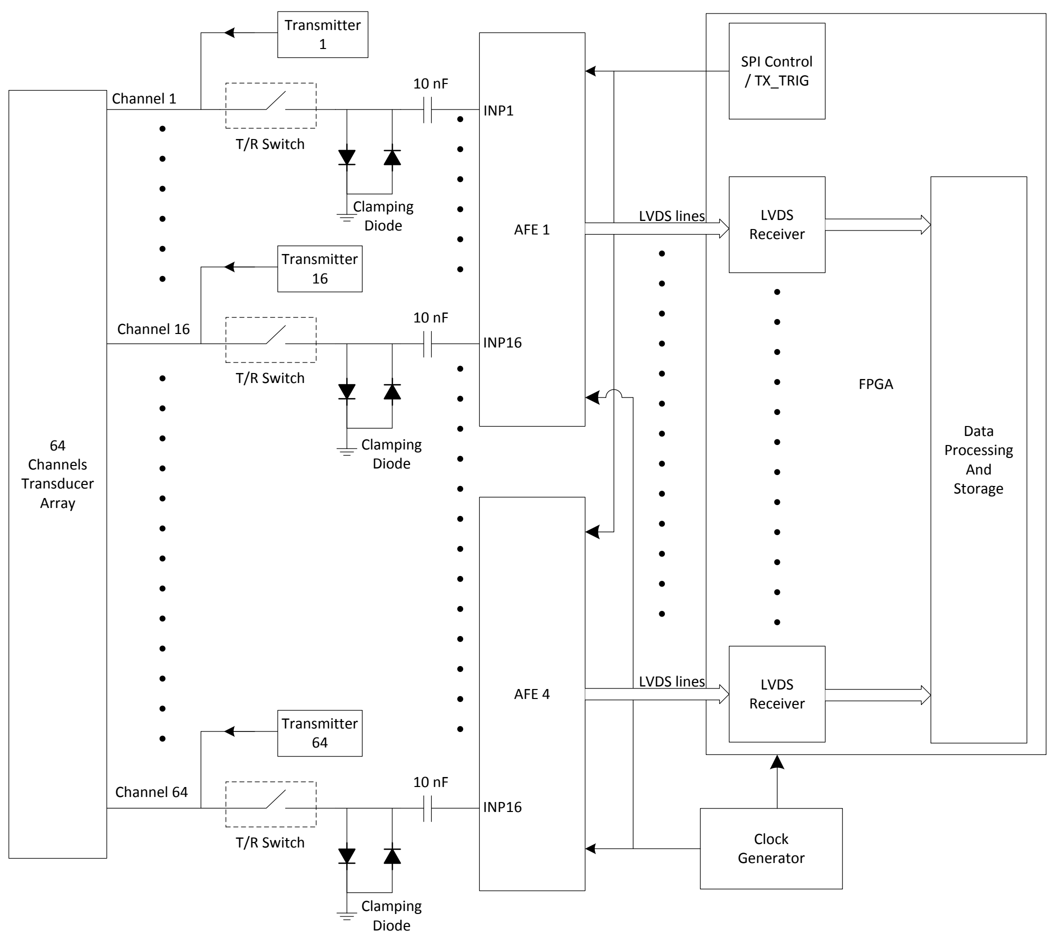


Figure 106. Simplified Schematic for a Medical Ultrasound Imaging System

Typical Application (continued)

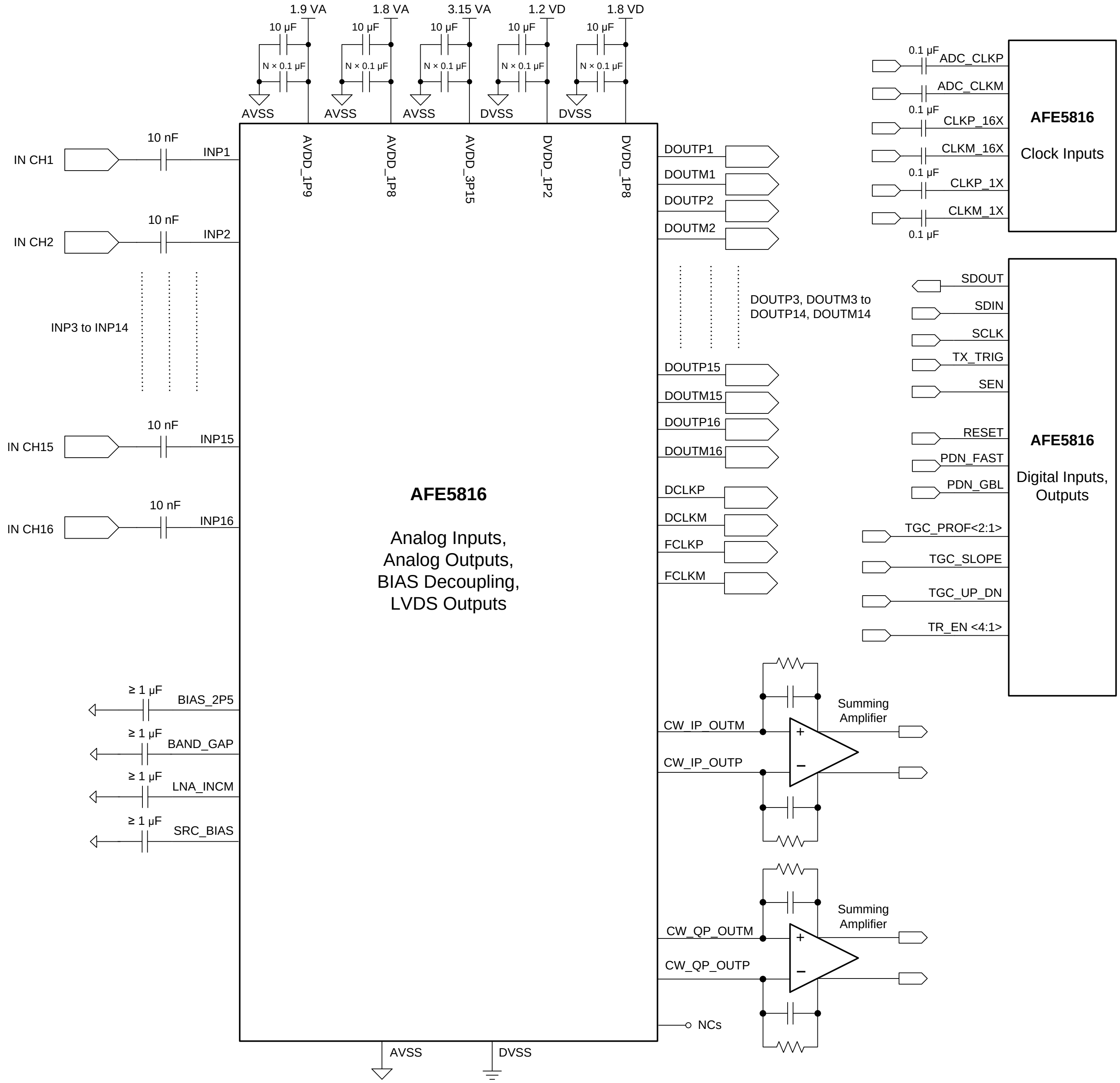


Figure 107. Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

Typical requirements for a medical ultrasound imaging system are listed in Table 20.

Table 20. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Signal center frequency	5 MHz
Signal bandwidth	2 MHz
Maximum overloaded signal	1 V_{PP}
Maximum input signal amplitude	100 mV_{PP}
Transducer noise level	1 $nV/\sqrt{Hz}$
Dynamic range	151 dBc/Hz
Time-gain compensation range	40 dB
Total harmonic distortion	40 dBc

10.2.2 Detailed Design Procedure

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. The concept of focal imaging provides the ability to focus on a single point in the scan region. By subsequently focusing at different points, an image is assembled.

See Figure 106 for a simplified schematic of a 64-channel ultrasound imaging system. When initiating an ultrasound image, a pulse is generated and transmitted from each of the 64 transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1 MHz to 15 MHz.

The sound waves weaken rapidly as they travel through the objects being imaged, falling off as the square of the distance traveled. As the signal travels, portions of the wave front energy are reflected. Signals that are reflected immediately after transmission are very strong because they are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because they are reflecting from deep in the body. As a result of the limitations on the amount of energy that can be put into the imaging object, the industry developed extremely sensitive receive electronics. Receive echoes from focal points close to the surface require little, if any, amplification. This region is referred to as the *near field*. However, receive echoes from focal points deep in the body are extremely weak and must be amplified by a factor of 100 or more. This region is referred to as the *far field*. In the high-gain (far field) mode, the limit of performance is the sum of all noise sources in the receive chain.

In high-gain (far field) mode, system performance is defined by its overall noise level, which is limited by the noise level of the transducer assembly and the receive low-noise amplifier (LNA). However, in the low-gain (near field) mode, system performance is defined by the maximum amplitude of the input signal that the system can handle. The ratio between noise levels in high-gain mode and the signal amplitude level in low-gain mode is defined as the dynamic range of the system.

The high integration and high dynamic range of the device make the AFE5816 ideally-suited for ultrasound imaging applications. The device includes an integrated attenuator, an LNA (with variable gain that can be changed with enough time to handle both near- and far-field systems), a low-pass antialiasing filter to limit the noise bandwidth, an ADC with high SNR performance, and a CW mixer. Figure 107 illustrates an application circuit of the device.

The following steps detail how to design medical ultrasound imaging systems:

1. Use the signal center frequency and signal bandwidth to select an appropriate ADC sampling frequency.
2. Use the time-gain compensation range to select the range of the LNA gain.
3. Use the transducer noise level and maximum input signal amplitude to select the appropriate LNA gain. The device input-referred noise level reduces with higher LNA gain. However, higher LNA gain leads to lower input signal swing support.
4. See Figure 107 to select different passive components for different device pins.
5. See the *CW Clock Selection* section to select the clock configuration for the ADC and CW clocks.

10.2.3 Application Curves

Figure 108 and Figure 109 show the FFT of a device output for gain code = 64 and gain code = 319, respectively, with an input signal at 5 MHz captured at a sample rate of 50 MHz. Figure 108 shows the spectrum for a far-field imaging scenario with the full Nyquist band, default device settings, and gain code = 319. Figure 109 shows the spectrum for a near-field imaging scenario for the full Nyquist band with default device settings and gain code = 64.

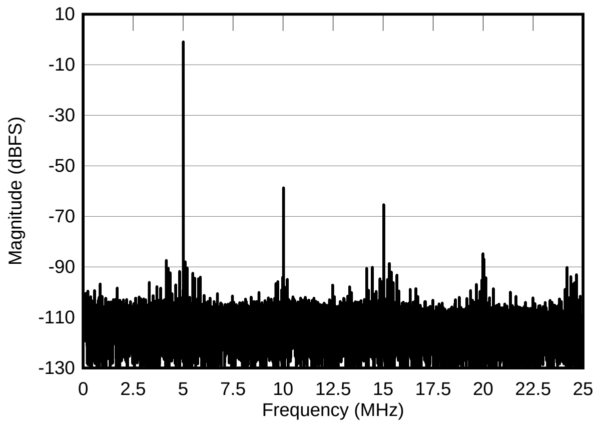


Figure 108. FFT for Gain Code = 14 dB

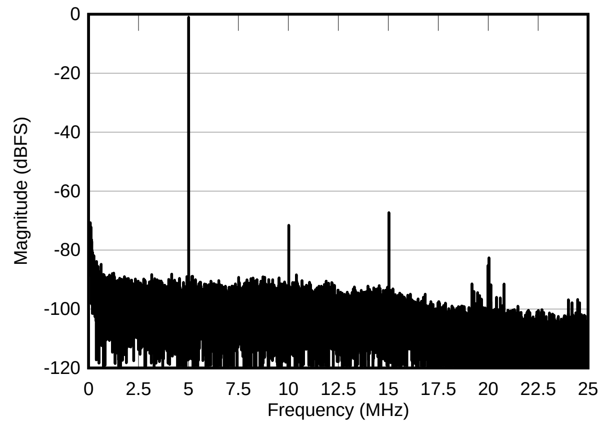


Figure 109. FFT for Gain Code = 45 dB

10.3 Do's and Don'ts

Driving the inputs (analog or digital) beyond the power-supply rails. For device reliability, an input must not go more than 300 mV below the ground pins or 300 mV above the supply pins, as suggested in the *Absolute Maximum Ratings* table. Exceeding these limits, even on a transient basis, can cause faulty or erratic operation and can impair device reliability.

Driving the device signal input with an excessively high-level signal. The device offers consistent and fast overload recovery with a 6-dB overloaded signal. For very large overload signals (> 6 dB of the linear input signal range), TI recommends back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal.

Not meeting timing requirements on the TGC_SLOPE and TGC_UP_DN pins. If timing is not met between the TGC_SLOPE and TGC_UP_DN signals and the ADC clock signal, then the TGC engine is placed into a locked state. See the *Timing Specifications* section for more details.

Using a clock source with excessive jitter, an excessively long input clock signal trace, or having other signals coupled to the ADC or CW clock signal trace. These situations cause the sampling interval to vary, causing an excessive output noise and a reduction in SNR performance. For a system with multiple devices, the clock tree scheme must be used to apply an ADC or CW clock. See the *System Clock Configuration for Multiple Devices* section for clock mismatch between devices, which can lead to latency mismatch and reduction in SNR performance.

LVDS routing length mismatch. The routing length of all LVDS lines routed to the FPGA must be matched to avoid any timing-related issues. For systems with multiple devices, the LVDS serialized data clock (DCLKP, DCLKM) and the frame clock (FCLKP, FCLKM) of each individual device must be used to deserialize the corresponding LDVS serialized data (DOUTP, DOUTM).

Failure to provide adequate heat removal. Use the appropriate thermal parameter listed in the *Thermal Information* table and an ambient, board, or case temperature in order to calculate device junction temperature. A suitable heat removal technique must be used to keep the device junction temperature below the maximum limit of 105°C.

Incorrect register programming. After resetting the device, write register 1, bit 2 = 1 and register 1, bit 4 = 1. If these bits are not set as specified, the device does not function properly.

10.4 Initialization Set Up

After bringing up all the supplies, follow these steps to initialize the device:

1. Apply a hardware reset pulse on the RESET pin with a minimum pulse duration of 100 ns. Note that after powering up the device, a hardware reset is required.
2. After applying a hardware reset pulse, wait for a minimum time of 100 ns.
3. Set register 1, bit 2 and bit 4 to 1 using SPI signals.
4. Write any other register settings as required.

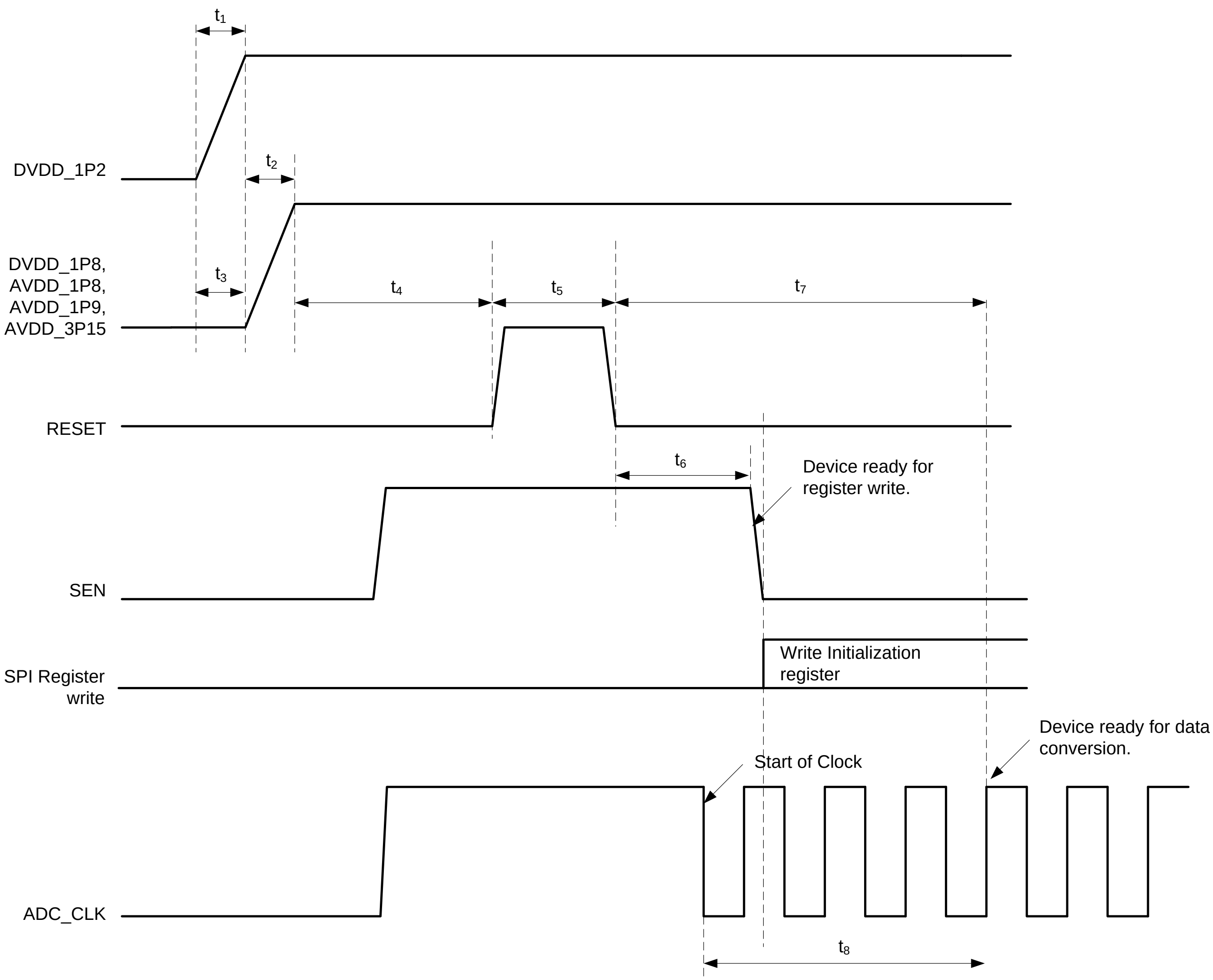
11 Power Supply Recommendations

The device requires a total of five supplies in order to operate properly. These supplies are: AVDD_3P15, AVDD_1P9, AVDD_1P8, DVDD_1P8, and DVDD_1P2. See the *Recommended Operating Conditions* table for detailed information regarding the minimum and maximum operating voltage specifications of different supplies.

11.1 Power Sequencing and Initialization

11.1.1 Power Sequencing

Figure 110 shows the suggested power-up sequencing and reset timing for the device. Note that the DVDD_1P2 supply must rise before the AVDD_1P8 supply. If the AVDD_1P8 supply rises before the DVDD_1P2 supply, the AVDD_1P8 supply current is several times larger than the normal current until the DVDD_1P2 supply reaches a 1.2-V level.



NOTE: 10 µs < t_1 < 50 ms, 10 µs < t_2 < 50 ms, t_3 > t_1, t_4 > 10 ms, t_5 > 100 ns, t_6 > 100 ns, t_7 > 4 ADC clock cycles, and t_8 > 100 µs.

Figure 110. Recommended Power-Up Sequencing and Reset Timing Diagram

12 Layout

12.1 Layout Guidelines

12.1.1 Power Supply, Grounding, and Bypassing

In a mixed-signal system design, the power-supply and grounding design play a significant role. The device distinguishes between two different grounds: AVSS (analog ground) and DVSS (digital ground). In most cases, designing the printed circuit board (PCB) to use a single ground plane is adequate, but in high-frequency or high-performance systems care must be taken so that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital supply set consisting of the DVDD_1P8, DVDD_1P2, and DVSS pins can be placed on separate power and ground planes. For this configuration, tie the AVSS and DVSS grounds together at the power connector in a star layout. In addition, optical or digital isolators (such as the ISO7240) can completely separate the analog portion from the digital portion. Consequently, such isolators prevent digital noise from contaminating the analog portion. Table 21 lists the related circuit blocks for each power supply.

Table 21. Supply versus Circuit Blocks

POWER SUPPLY	GROUND	CIRCUIT BLOCKS(1)
AVDD_3P15	AVSS	Reference voltage and current generator, LNA, VCNTRL, CW mixer, CW clock buffer, 16 × 16 cross-point switch, and 16-phase generator blocks
AVDD_1P9	AVSS	Band-gap circuit, reference voltage and current generator, LNA, PGA, LPF, and VCA SPI blocks
AVDD_1P8	AVSS	ADC analog, reference voltage and current generator, band-gap circuit, ADC clock buffer
DVDD_1P8	DVSS	LVDS serializer and buffer, and PLL blocks
DVDD_1P2	DVSS	ADC digital and serial interface blocks

(1) See Figure 100 and Figure 101 for further details.

Reference all bypassing and power supplies for the device to their corresponding ground planes. Bypass all supply pins with 0.1-µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2 µF to 10 µF, effective at lower frequencies) can also be used on the main supply pins. These components can be placed on the PCB in close proximity (< 0.5 inch or 12.7 mm) to the device itself.

The device has a number of reference supplies that must be bypassed, such as BIAS_2P5, LNA_INCM, BAND_GAP, and SRC_BIAS. Bypass these pins with at least a 1-µF capacitor; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 µF) placed as close as possible to the device pins.

12.1.2 Board Layout

High-speed, mixed-signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer and drivers. For the device, care must be taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each supply and ground connection; smaller effective inductances of the supply and ground pins result in better noise suppression. For this reason, multiple pins are used to connect each supply and ground set. Low inductance properties must be maintained throughout the design of the PCB layout by the use of proper planes and layer thickness.

To avoid noise coupling through supply pins, keep sensitive input pins (such as the INM and INP pins) away from the AVDD_3P15 and AVDD_1P9 planes. For example, do not route the traces or vias connected to these pins across the AVDD_3P15 and AVDD_1P9 planes. That is, avoid the power planes under the INM and INP pins.

In order to maintain proper LVDS timing, all LVDS traces must follow a controlled impedance design. In addition, all LVDS trace lengths must be equal and symmetrical; keep trace length variations less than 150 mil (0.150 inch or 3.81 mm).

In addition, appropriate delay matching must be considered for the CW clock path, especially in systems with a high channel count. For example, if the clock delay is half of the 16X clock period, a phase error of 22.5°C can exist. Thus, the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on the NFBGA PCB layout techniques can be found in the Texas Instruments application report SSYZ015 that can be downloaded from www.ti.com.

12.2 Layout Example

Figure 111 and Figure 112 illustrate example layouts for the top and bottom layers, respectively.

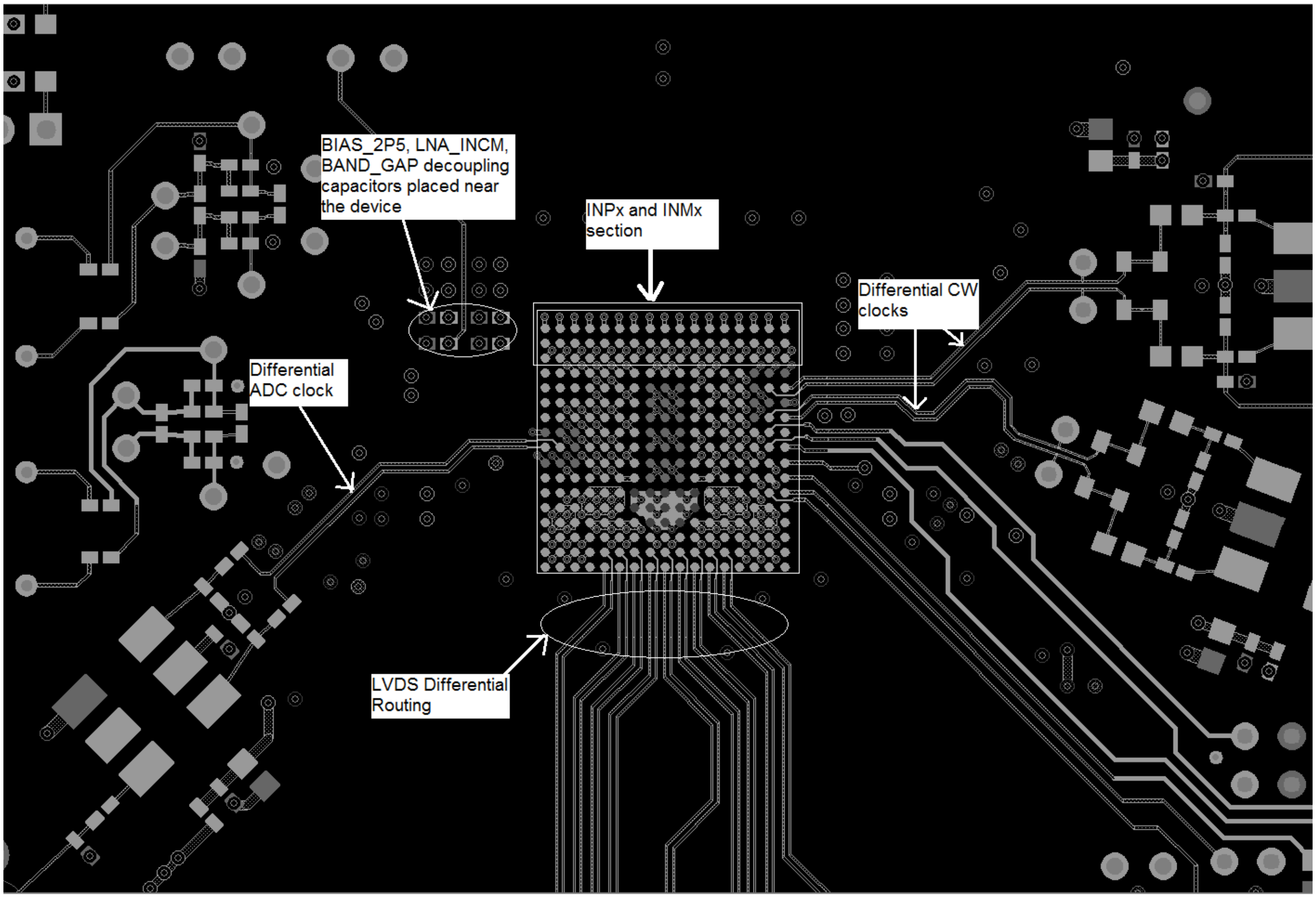


Figure 111. Top Layer

Layout Example (continued)

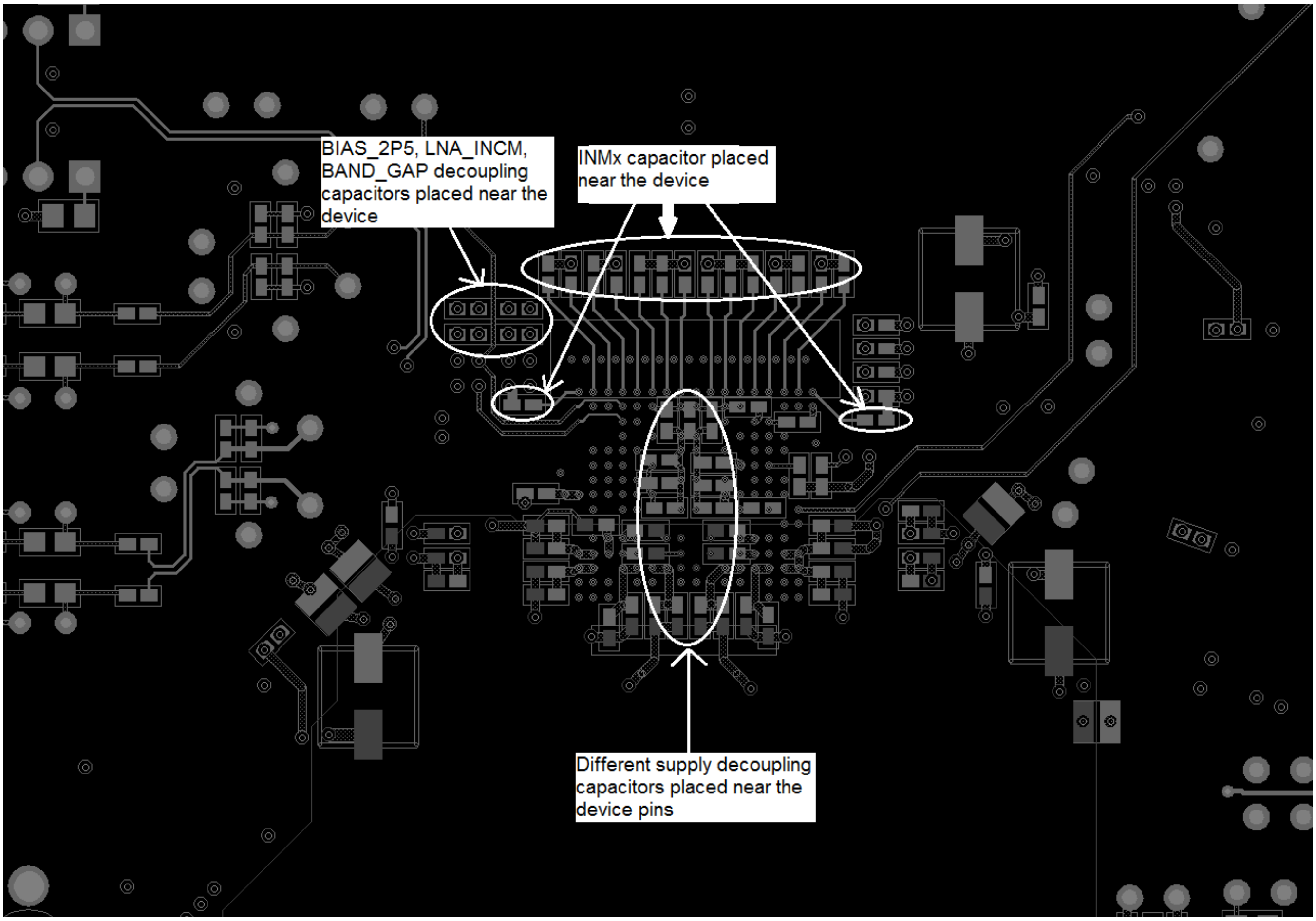


Figure 112. Bottom Layer

Layout Example (continued)

Figure 113 shows the routing of input traces and differential CW outputs.

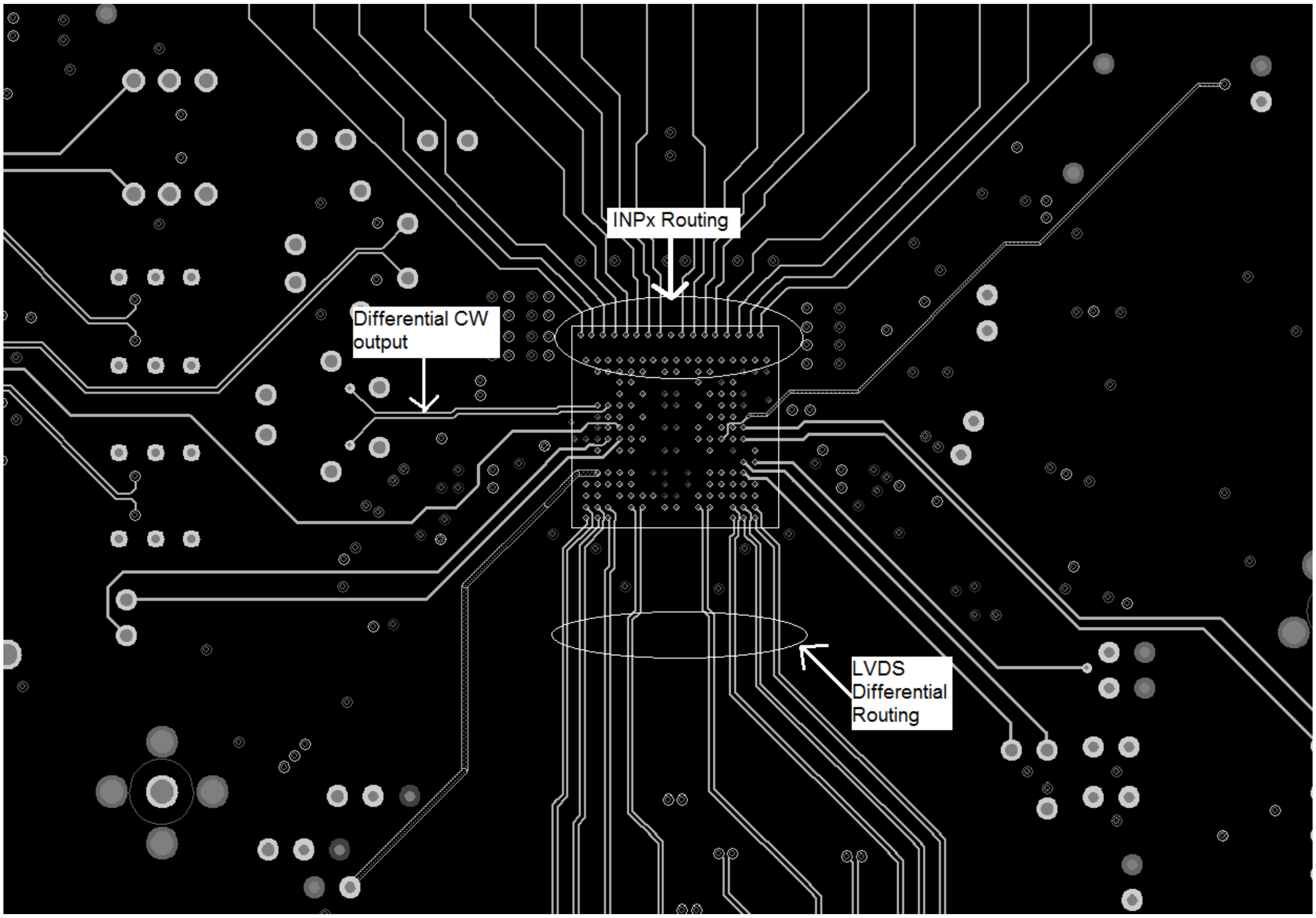


Figure 113. Input Routing

Layout Example (continued)

Figure 114 shows routing examples for different power planes.

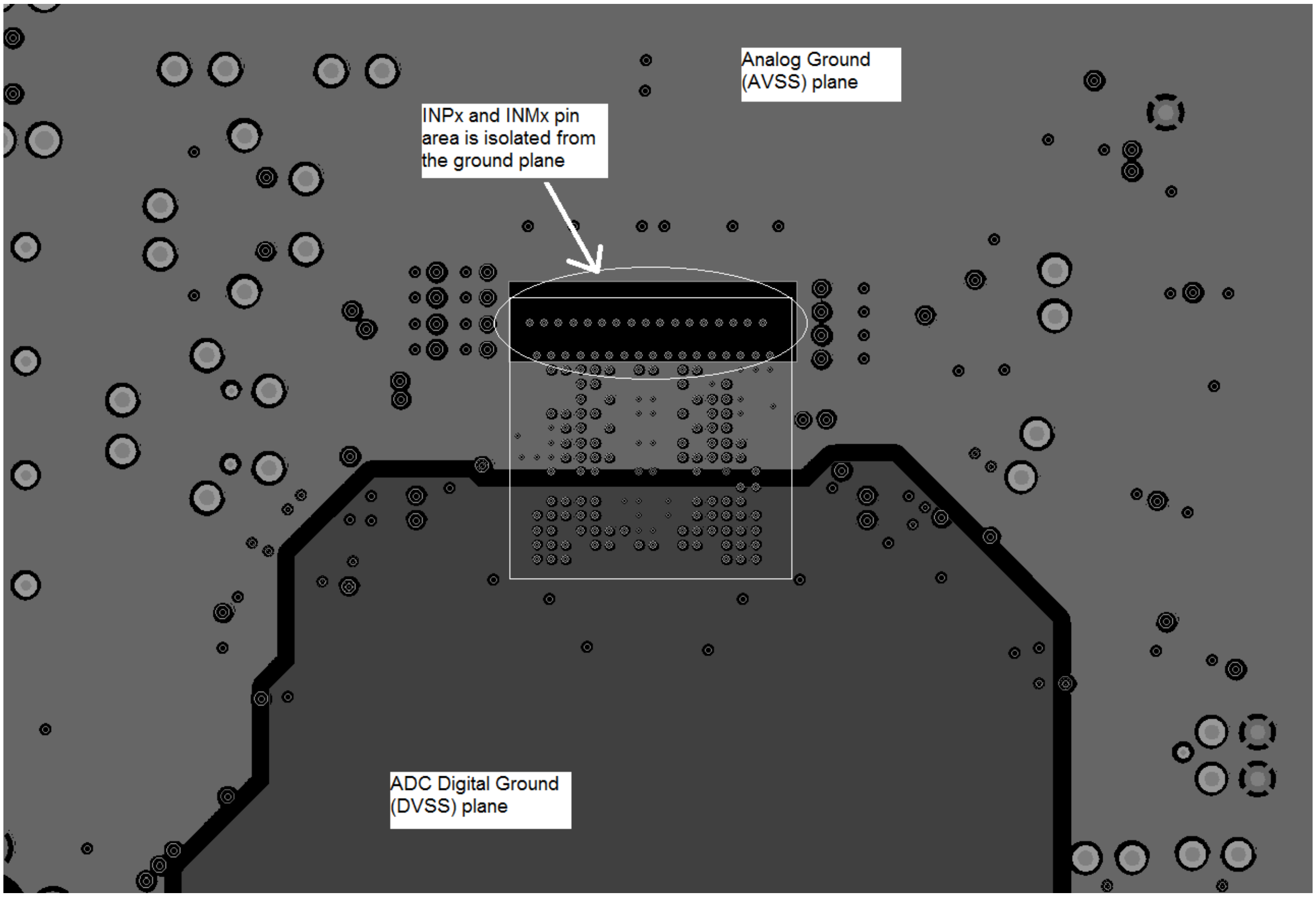


Figure 114. Ground Plane

Layout Example (continued)

Figure 115, Figure 116, and Figure 117 illustrate routing examples for different power planes.

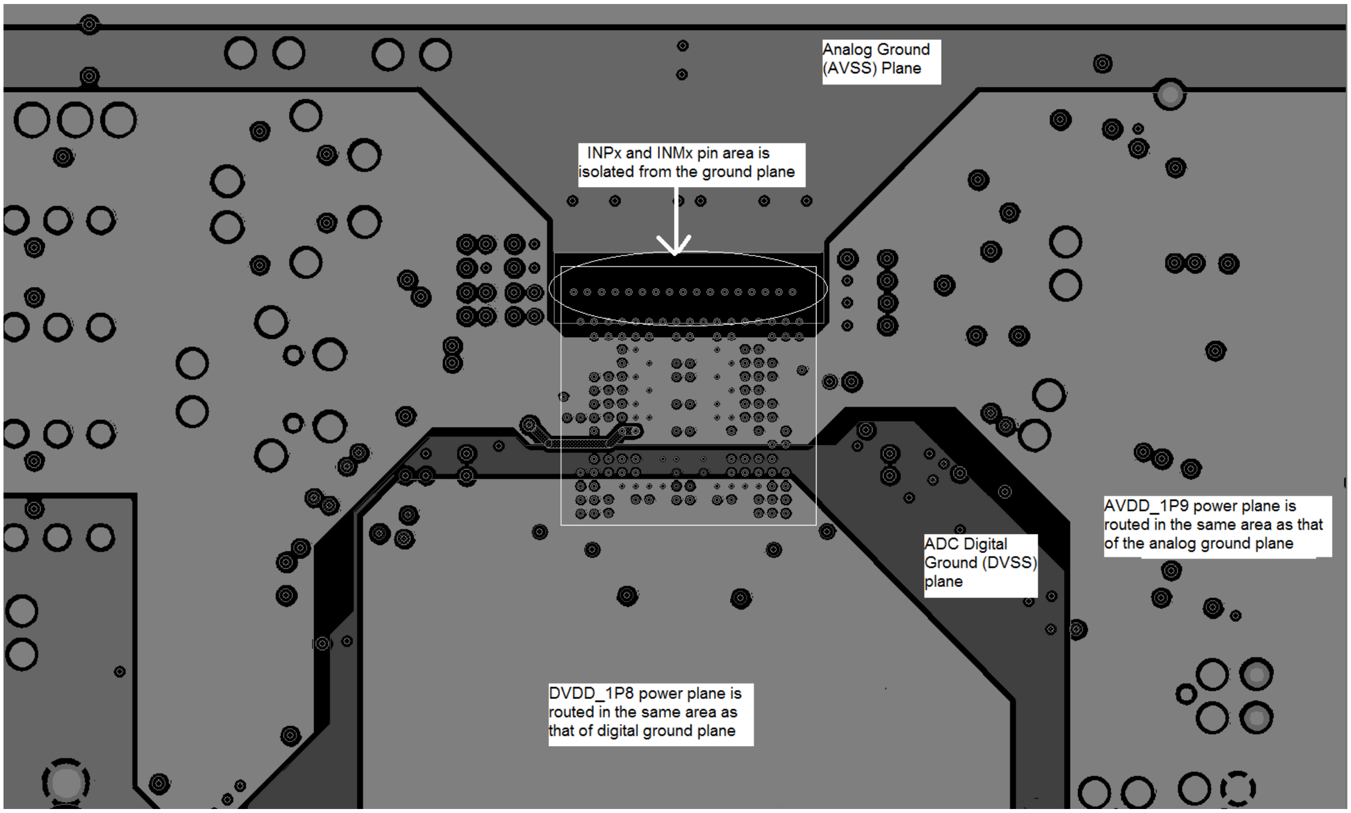


Figure 115. AVDD_1P9 and DVDD_1P8 Power Plane

Layout Example (continued)

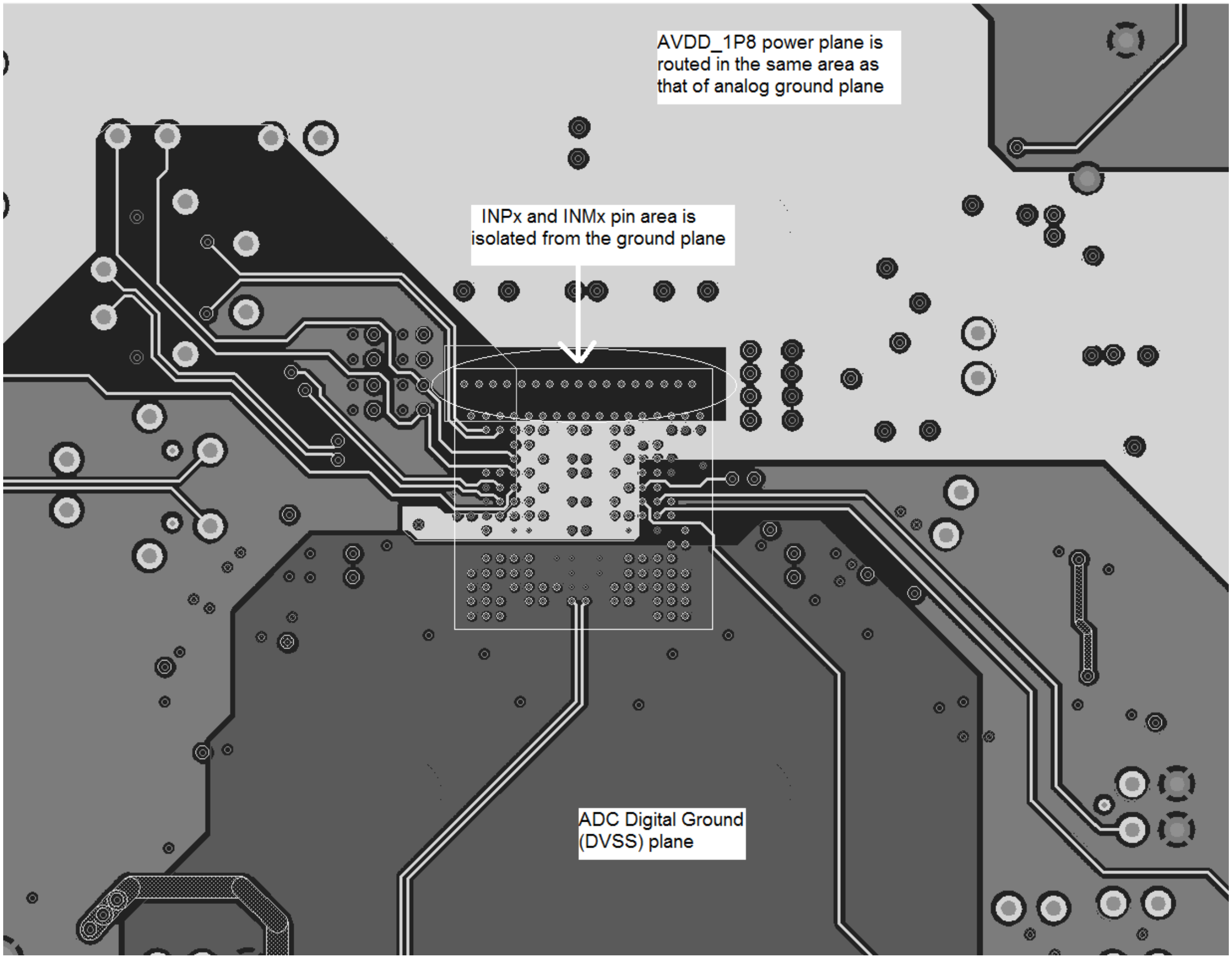


Figure 116. AVDD_1P8 Power Plane

Layout Example (continued)

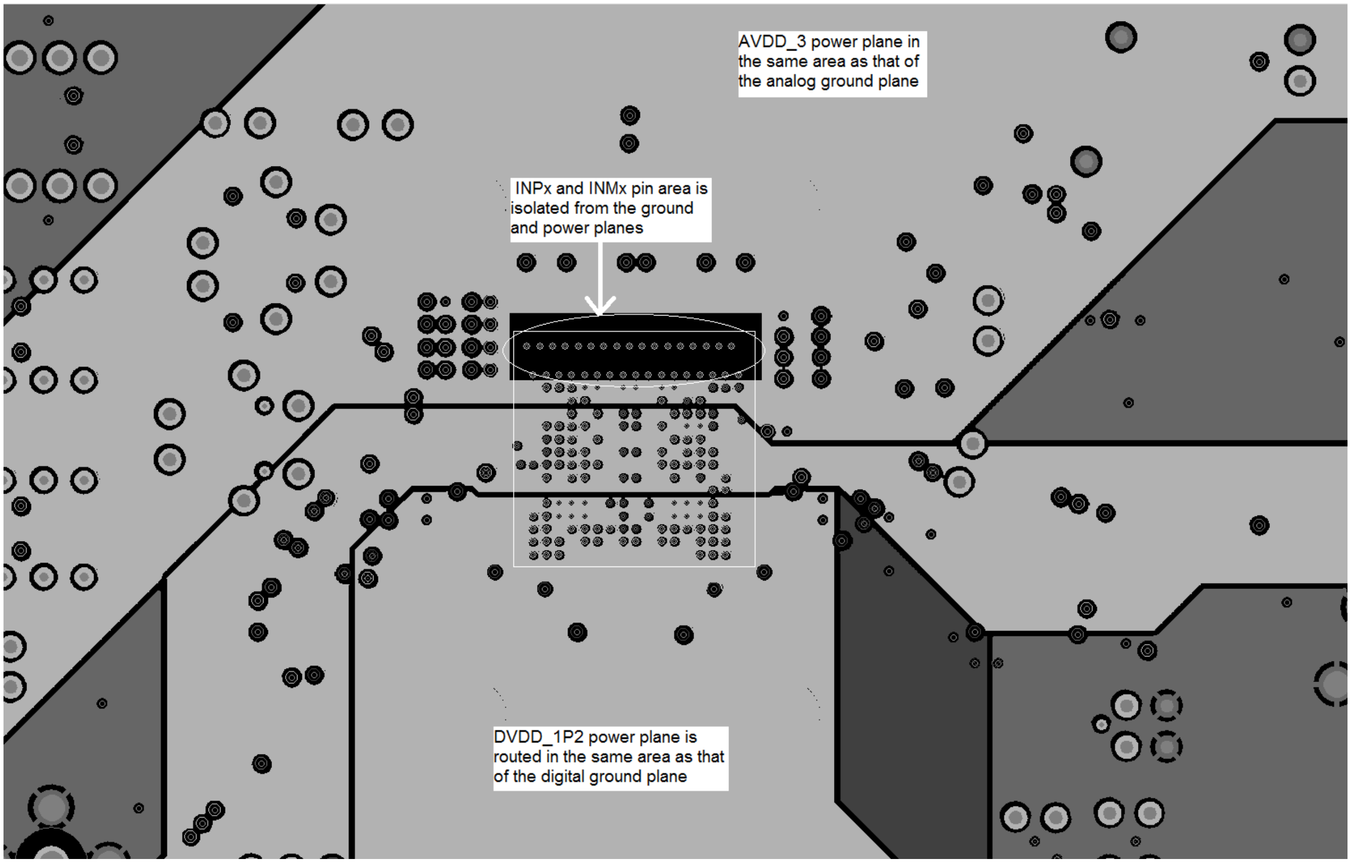


Figure 117. AVDD_3P15 and DVDD_1P2 Power Plane

13 Register Maps

13.1 Serial Register Map

The device is a multichip module (MCM) with two dies: the VCA die and the ADC_CONV die, as shown in Figure 118. Figure 118 also describes the channel mapping of the VCA die to the input pins. Both dies share the same SPI control signals (SCLK, SDIN, and SEN).

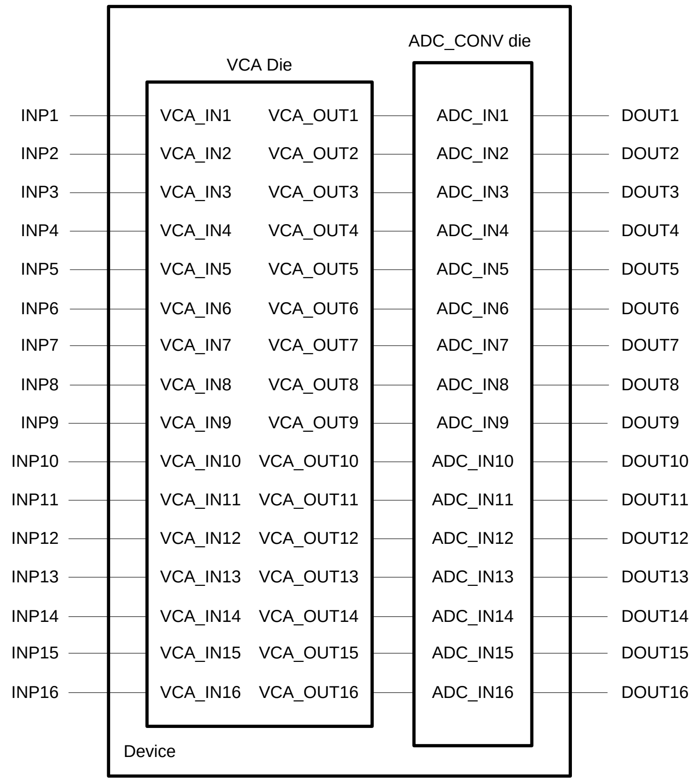


Figure 118. Channel Mapping: VCA Dies

A reset process is required at the device initialization stage.

NOTE

Initialization can be accomplished with a hardware reset by applying a positive pulse to the RESET pin. After reset, all ADC and VCA registers are set to default values. Note that during register programming, all unnamed register bits must be set to 0 for the register that is being programmed.

The device consists of the following register maps:

1. Global register map. This register map is common to both the ADC_CONV and VCA dies. The global register map consists of register 0. To program the global register map, set the DTGC_WR_EN bit to 0.
2. ADC register map. This register map programs the ADC die. The ADC register map consists of register 1 to register 67. To program the ADC register map, set the DTGC_WR_EN bit to 0.
3. VCA register map. This register map contains register 192 to register 230 and programs all VCA blocks except the DTGC engine. To program the VCA register map, set the DTGC_WR_EN bit to 0.
4. DTGC register map. This register map contains register 1 to register 186 and programs the TGC control engine of the VCA die. To program the DTGC register map, set the DTGC_WR_EN bit to 1.

Serial Register Map (continued)

Because these register maps share the same address space, the DTGC_WR_EN bit is used to program the different register maps, as listed in Table 22.

Table 22. Register Configuration

REGISTER MAP	ADDRESS	DTGC_WR_EN BIT
Global register map	0	0
ADC register map	1 to 67	0
VCA register map	192 to 230	0
DTGC register map	1 to 186	1

13.1.1 Global Register Map

This section discusses the global register. This register map is shown in Table 23.

DTGC_WR_EN must be set to 0 before programming other bits of the global register map.

Table 23. Global Register Map

REGISTER ADDRESS		REGISTER DATA(1)															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	DTGC_ WR_EN	0	0	REG_READ_ EN	SOFTWARE_ RESET

(1) The default value of all registers is 0.

13.1.1.1 Description of Global Register

13.1.1.1.1 Register 0 (address = 0h)

Figure 119. Register 0

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	DTGC_WR_EN	0	0	REG_READ_ EN	SOFTWARE_ RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value

Table 24. Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	W	0h	Must write 0
4	DTGC_WR_EN	W	0h	0 = Enables programming of the global, ADC, and VCA register maps 1 = Enables programming of the DTGC register map
3-2	0	W	0h	Must write 0
1	REG_READ_EN	W	0h	0 = Register readout mode disabled 1 = Register readout mode enabled
0	SOFTWARE_RESET	W	0h	0 = Disabled 1 = Enabled (this setting returns the device to a reset state). This bit is a self-clearing register bit.

13.1.2 ADC Register Map

This section discusses the ADC register map. A register map is available in Table 25.

DTGC_WR_EN must be set to 0 before programming the ADC register map.

Table 25. ADC Register Map

REGISTER ADDRESS		REGISTER DATA(1)															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	LVDS_RATE_2X	0	0	0	0	0	0	0	0	DIS_LVDS	1	0	1	0	GLOBAL_PDN
2	2	PAT_MODES_FCLK[2:0]			LOW_LATENCY_EN	AVG_EN	SEL_PRBS_PAT_FCLK	PAT_MODES[2:0]			SEL_PRBS_PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
3	3	SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]		DIG_OFFSET_EN	0	0	0	0	0	0	0	0
4	4	OFFSET_REMOVAL_SELF	OFFSET_REMOVAL_START_SEL	OFFEST_REMOVAL_START_MANUAL	AUTO_OFFSET_REMOVAL_ACC_CYCLES[3:0]				PAT_SELECT_IND	PRBS_SYNC	PRBS_MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
5	5	CUSTOM_PATTERN[15:0]															
7	7	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL[4:0]					0	0	0	0	0	0	0	0	0	0	CHOPPER_EN
8	8	0	0	AUTO_OFFSET_REMOVAL_VAL_RD[13:0]													
11	B	0	0	0	0	EN_DITHER	0	0	0	0	0	0	0	0	0	0	0
13	D	GAIN_CH1					0	OFFSET_CH1									
14	E	0					0	OFFSET_CH1									
15	F	GAIN_CH2					0	OFFSET_CH2									
16	10	0					0	OFFSET_CH2									
17	11	GAIN_CH3					0	OFFSET_CH3									
18	12	0					0	OFFSET_CH3									
19	13	GAIN_CH4					0	OFFSET_CH4									
20	14	0					0	OFFSET_CH4									
21	15	PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1[2:0]			PAT_LVDS2[2:0]			HPF_ROUND_EN	HPF_CORNER_CH1-4[3:0]				DIG_HPF_EN_CH1-4
23	17	0	0	0	0	0	0	0	0	PAT_LVDS3[2:0]			PAT_LVDS4[2:0]			0	0
24	18	PDN_DIG_CH4	PDN_DIG_CH3	PDN_DIG_CH2	PDN_DIG_CH1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1	PDN_ANA_CH4	PDN_ANA_CH3	PDN_ANA_CH2	PDN_ANA_CH1	INVERT_CH4	INVERT_CH3	INVERT_CH2	INVERT_CH1
25	19	GAIN_CH5					0	OFFSET_CH5									
26	1A	0					0	OFFSET_CH5									
27	1B	GAIN_CH6					0	OFFSET_CH6									
28	1C	0					0	OFFSET_CH6									
29	1D	GAIN_CH7					0	OFFSET_CH7									

(1) Default value of all registers is 0.

Table 25. ADC Register Map (continued)

REGISTER ADDRESS		REGISTER DATA[(1)]															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30	1E	0					0	OFFSET_CH7									
31	1F	GAIN_CH8					0	OFFSET_CH8									
32	20	0					0	OFFSET_CH8									
33	21	PAT_PRBS_LVDS5	PAT_PRBS_LVDS6	PAT_PRBS_LVDS7	PAT_PRBS_LVDS8	PAT_LVDS5[2:0]			PAT_LVDS6[2:0]			0	HPF_CORNER_CH5-8[3:0]				DIG_HPF_EN_CH5-8
35	23	0	0	0	0	0	0	0	0	PAT_LVDS7[2:0]			PAT_LVDS8[2:0]			0	0
36	24	PDN_DIG_CH8	PDN_DIG_CH7	PDN_DIG_CH6	PDN_DIG_CH5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5	PDN_ANA_CH8	PDN_ANA_CH7	PDN_ANA_CH6	PDN_ANA_CH5	INVERT_CH8	INVERT_CH7	INVERT_CH6	INVERT_CH5
37	25	GAIN_CH9					0	OFFSET_CH9									
38	26	0					0	OFFSET_CH9									
39	27	GAIN_CH10					0	OFFSET_CH10									
40	28	0					0	OFFSET_CH10									
41	29	GAIN_CH11					0	OFFSET_CH11									
42	2A	0					0	OFFSET_CH11									
43	2B	GAIN_CH12					0	OFFSET_CH12									
44	2C	0					0	OFFSET_CH12									
45	2D	PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9[2:0]			PAT_LVDS10[2:0]			0	HPF_CORNER_CH9-12[3:0]				DIG_HPF_EN_CH9-12
47	2F	0	0	0	0	0	0	0	0	PAT_LVDS11[2:0]			PAT_LVDS12[2:0]			0	0
48	30	PDN_DIG_CH12	PDN_DIG_CH11	PDN_DIG_CH10	PDN_DIG_CH9	PDN_LVDS12	PDN_LVDS11	PDN_LVDS10	PDN_LVDS9	PDN_ANA_CH12	PDN_ANA_CH11	PDN_ANA_CH10	PDN_ANA_CH9	INVERT_CH12	INVERT_CH11	INVERT_CH10	INVERT_CH9
49	31	GAIN_CH13					0	OFFSET_CH13									
50	32	0					0	OFFSET_CH13									
51	33	GAIN_CH14					0	OFFSET_CH14									
52	34	0					0	OFFSET_CH14									
53	35	GAIN_CH15					0	OFFSET_CH15									
54	36	0					0	OFFSET_CH15									
55	37	GAIN_CH16					0	OFFSET_CH16									
56	38	0					0	OFFSET_CH16									
57	39	PAT_PRBS_LVDS13	PAT_PRBS_LVDS14	PAT_PRBS_LVDS15	PAT_PRBS_LVDS16	PAT_LVDS13[2:0]			PAT_LVDS14[2:0]			0	HPF_CORNER_CH13-16[3:0]				DIG_HPF_EN_CH13-16
59	3B	0	0	0	0	0	0	0	0	PIN_PAT_LVDS15[2:0]			PAT_LVDS16[2:0]			0	0
60	3C	PDN_DIG_CH16	PDN_DIG_CH15	PDN_DIG_CH14	PDN_DIG_CH13	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13	PDN_ANA_CH16	PDN_ANA_CH15	PDN_ANA_CH14	PDN_ANA_CH13	INVERT_CH16	INVERT_CH15	INVERT_CH14	INVERT_CH13
67	43	0	0	0	0	0	0	0	0	0	0	0	LVDS_DCLK_DELAY_PROG[3:0]				0

13.1.2.1 Description of ADC Registers

13.1.2.1.1 Register 1 (address = 1h)

Figure 120. Register 1

15	14	13	12	11	10	9	8
0	LVDS_RATE_2X	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	DIS_LVDS	1	0	1	0	GLOBAL_PDN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 26. Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
15	0	R/W	0h	Must write 0
14	LVDS_RATE_2X	R/W	0h	0 = 1X rate; normal operation (default) 1 = 2X rate. This setting combines the data of two LVDS pairs into a single LVDS pair. This feature can be used when the ADC clock rate is low; see the *LVDS Interface* section for further details.
13-6	0	R/W	0h	Must write 0
5	DIS_LVDS	R/W	0h	0 = LVDS interface is enabled (default) 1 = LVDS interface is disabled
4	1	R/W	0h	Must write 1
3	0	R/W	0h	Must write 0
2	1	R/W	0h	Must write 1
1	0	R/W	0h	Must write 0
0	GLOBAL_PDN	R/W	0h	0 = Device operates in normal mode (default) 1 = ADC enters complete power-down mode

13.1.2.1.2 Register 2 (address = 2h)

Figure 121. Register 2

15	14	13	12	11	10	9	8
PAT_MODES_FCLK[2:0]			LOW_LATENCY_EN	AVG_EN	SEL_PRBS_PAT_FCLK	PAT_MODES[2:0]	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_MODES[2:0]	SEL_PRBS_PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 27. Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	PAT_MODES_FCLK[2:0]	R/W	0h	These bits enable different test patterns on the frame clock line; see Table 28 for bit descriptions and the *Test Patterns* section for further details.
12	LOW_LATENCY_EN	R/W	0h	0 = Default latency with digital features supported 1 = Low latency with digital features bypassed
11	AVG_EN	R/W	0h	0 = No averaging 1 = Enables averaging of two channels to improve signal-to-noise ratio (SNR); see the *LVDS Interface* section for further details.
10	SEL_PRBS_PAT_FCLK	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated on f_{CLK}; see the *Test Patterns* section for further details
9-7	PAT_MODES[2:0]	R/W	0h	These bits enable different test patterns on the LVDS data lines; see Table 28 for bit descriptions and the *Test Patterns* section for further details.
6	SEL_PRBS_PAT_GBL	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated; see the *Test Patterns* section for further details
5-0	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]	R/W	0h	This 8-bit register initiates an offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining two MSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6] bits (bits 10-9) in register 3.

Table 28. Pattern Mode Bit Description

PAT_MODES[2:0]	DESCRIPTION
000	Normal operation
001	Sync (half frame 0, half frame 1)
010	Alternate 0s and 1s
011	Custom pattern(1)
100	All 1s
101	Toggle mode
110	All 0s
111	Ramp pattern(1)

(1) Either the custom or the ramp pattern setting is required for PRBS pattern selection.

13.1.2.1.3 Register 3 (address = 3h)

Figure 122. Register 3

15	14	13	12	11	10	9	8
SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]		DIG_OFFSET_EN
R/W-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 29. Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	SER_DATA_RATE	R/W	0h	These bits control the LVDS serialization rate. 000 = 12X 001 = 14X 100 = 16X 101, 110, 111, 010, 011 = Unused
12	DIG_GAIN_EN	R/W	0h	0 = Digital gain disabled 1 = Digital gain enabled
11	0	R/W	0h	Must write 0
10-9	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]	R/W	0h	This 8-bit register initiates an offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining six LSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0] bits (bits 5-0) in register 2.
8	DIG_OFFSET_EN	R/W	0h	0 = Digital offset subtraction disabled 1 = Digital offset subtraction enabled
7-0	0	R/W	0h	Must write 0

13.1.2.1.4 Register 4 (address = 4h)

Figure 123. Register 4

15	14	13	12	11	10	9	8
OFFSET_REMOVAL_SELF	0	0	0	0	0	0	PAT_SELECT_IND
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
PRBS_SYNC	PRBS_MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 30. Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
15	OFFSET_REMOVAL_SELF	R/W	0h	0 = Auto offset correction mode is enabled 1 = Offset correction via register is enabled
14	OFFSET_REMOVAL_START_SEL	R/W	0h	0 = Auto offset correction is initiated when the OFFSET_REMOVAL_START_MANUAL bit is set to 1 1 = Auto offset correction is initiated with a pulse on the TX_TRIG pin
13	OFFSET_REMOVAL_START_MANUAL	R/W	0h	This bit initiates an offset correction manually instead of with a TX_TRIG pulse
12-9	AUTO_OFFSET_REMOVAL_ACC_CYCLES	R/W	0h	These bits define the number of samples required to generate an offset in auto offset correction mode
8	PAT_SELECT_IND	R/W	0h	0 = All LVDS output lines have the same pattern, as determined by the PAT_MODES[2:0] bits 1 = Different test patterns can be sent on different LVDS lines, depending upon the channel and register; see the *Test Patterns* section for further details
7	PRBS_SYNC	R/W	0h	0 = Normal operation 1 = PRBS generator is in a reset state
6	PRBS_MODE	R/W	0h	0 = 23-bit PRBS generator 1 = 9-bit PRBS generator
5	PRBS_EN	R/W	0h	0 = PRBS sequence generation block disabled 1 = PRBS sequence generation block enabled; see the *Test Patterns* section for further details
4	MSB_FIRST	R/W	0h	0 = The LSB is transmitted first on serialized output data 1 = The MSB is transmitted first on serialized output data
3	0	R/W	0h	Must write 0
2	0	R/W	0h	Must write 0
1-0	ADC_RES	R/W	0h	These bits control the ADC resolution. 00 = 12-bit resolution 01 = 14-bit resolution 10, 11 = Unused

13.1.2.1.5 Register 5 (address = 5h)

Figure 124. Register 5

15	14	13	12	11	10	9	8
CUSTOM_PATTERN[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
CUSTOM_PATTERN[13:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 31. Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CUSTOM_PATTERN[15:0]	R/W	0h	If the pattern mode is programmed to a custom pattern mode, then the custom pattern value can be provided by programming these bits; see the *Test Patterns* section for further details.

13.1.2.1.6 Register 7 (address = 7h)

Figure 125. Register 7

15	14	13	12	11	10	9	8
AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CHOPPER_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 32. Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL	R/W	0h	Write the channel number to read the offset value in auto offset correction mode for a corresponding channel number (read the offset value in register 8, bits 13-0)
10-1	0	R/W	0h	Must write 0
0	CHOPPER_EN	R/W	0h	The chopper can be used to move low-frequency, 1 / f noise to an f_S / 2 frequency. 0 = Chopper disabled 1 = Chopper enabled

13.1.2.1.7 Register 8 (address = 8h)

Figure 126. Register 8

15	14	13	12	11	10	9	8
0	0	AUTO_OFFSET_REMOVAL_VAL_RD[13:0]					
R/W-0h	R/W-0h	R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AUTO_OFFSET_REMOVAL_VAL_RD[13:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 33. Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must write 0
13-0	AUTO_OFFSET_REMOVAL_VAL_RD	R/W	0h	Read the offset value applied in auto offset correction mode for a specific channel number as defined in the AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL[4:0] register bit.

13.1.2.1.8 Register 11 (address = Bh)

Figure 127. Register 11

15	14	13	12	11	10	9	8
0	0	0	0	EN_DITHER	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 34. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	EN_DITHER	R/W	0h	Dither can be used to remove higher-order harmonics. 0 = Dither disabled 1 = Dither enabled Note: Enabling the dither converts higher-order harmonics power in noise. Thus, enabling this mode removes harmonics but degrades SNR.
10-0	0	R/W	0h	Must write 0

13.1.2.1.9 Register 13 (address = Dh)

Figure 128. Register 13

15	14	13	12	11	10	9	8
GAIN_CH1					0	OFFSET_CH1	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 35. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH1	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 1 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH1	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 1 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 14, bits 9-0.

13.1.2.1.10 Register 14 (address = Eh)

Figure 129. Register 14

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH1	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 36. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH1	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, then the offset value for channel 1 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 13, bits 9-0.

13.1.2.1.11 Register 15 (address = Fh)

Figure 130. Register 15

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">GAIN_CH2</td><td>0</td><td colspan="2">OFFSET_CH2</td></tr>
<tr><td colspan="5">R/W-0h</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OFFSET_CH2</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Table 37. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH2	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 2 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH2	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 2 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 16, bits 9-0.

13.1.2.1.12 Register 16 (address = 10h)

Figure 131. Register 16

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">OFFSET_CH2</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OFFSET_CH2</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Table 38. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH2	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 2 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 15, bits 9-0.

13.1.2.1.13 Register 17 (address = 11h)

Figure 132. Register 17

15	14	13	12	11	10	9	8
GAIN_CH3					0	OFFSET_CH3	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 39. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH3	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 3 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH3	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 3 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 18, bits 9-0.

13.1.2.1.14 Register 18 (address = 12h)

Figure 133. Register 18

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH3	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 40. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH3	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 3 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 17, bits 9-0.

13.1.2.1.15 Register 19 (address = 13h)

Figure 134. Register 19

15	14	13	12	11	10	9	8
GAIN_CH4					0	OFFSET_CH4	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 41. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH4	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 4 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH4	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 4 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 20, bits 9-0.

13.1.2.1.16 Register 20 (address = 14h)

Figure 135. Register 20

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH4	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 42. Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH4	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 4 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 19, bits 9-0.

13.1.2.1.17 Register 21 (address = 15h)

Figure 136. Register 21

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1[2:0]			PAT_LVDS2[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_LVDS2[2:0]		HPF_ROUND_EN	HPF_CORNER_CH1-4[3:0]				DIG_HPF_EN_CH1-4
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 43. Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS1	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 1 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS2	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 2 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS3	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 3 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS4	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 4 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS1[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 1 can be programmed with these bits; see Table 44 for bit descriptions.
8-6	PAT_LVDS2[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 2 can be programmed with these bits; see Table 44 for bit descriptions.
5	HPF_ROUND_EN	R/W	0h	0 = Rounding in the ADC HPF is disabled. HPF output is truncated to be mapped to the ADC resolution bits. 1 = HPF output is mapped to the ADC resolution bits by the round-off operation.
4-1	HPF_CORNER_CH1-4[3:0]	R/W	0h	When the DIG_HPF_EN_CH1-4 bit is set to 1, the digital HPF characteristic for the corresponding channels can be programmed by setting the value of *k* with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of *k* is defined by: $Y(n) = \frac{2^k}{2^k + 1}[x(n) - x(n-1) + y(n-1)]$ Note that the value of *k* can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH1-4	R/W	0h	0 = Digital HPF disabled for channels 1 to 4 (default) 1 = Enables digital HPF for channels 1 to 4

Table 44. Pattern Mode Bit Description

PAT_MODES[2:0]	DESCRIPTION
000	Normal operation
001	Sync (half frame 0, half frame 1)
010	Alternate 0s and 1s
011	Custom pattern
100	All 1s
101	Toggle mode
110	All 0s
111	Ramp pattern

13.1.2.1.18 Register 23 (address = 17h)

Figure 137. Register 23

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_LVDS3[2:0]			PAT_LVDS4[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 45. Register 23 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS3[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 3 can be programmed with these bits; see Table 44 for bit descriptions.
4-2	PAT_LVDS4[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 4 can be programmed with these bits; see Table 44 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.19 Register 24 (address = 18h)

Figure 138. Register 24

15	14	13	12	11	10	9	8
PDN_DIG_CH4	PDN_DIG_CH3	PDN_DIG_CH2	PDN_DIG_CH1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDN_ANA_CH4	PDN_ANA_CH3	PDN_ANA_CH2	PDN_ANA_CH1	INVERT_CH4	INVERT_CH3	INVERT_CH2	INVERT_CH1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 46. Register 24 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH4	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 4
14	PDN_DIG_CH3	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 3
13	PDN_DIG_CH2	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel2
12	PDN_DIG_CH1	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 1
11	PDN_LVDS4	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 4
10	PDN_LVDS3	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 3
9	PDN_LVDS2	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 2
8	PDN_LVDS1	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 1
7	PDN_ANA_CH4	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 4
6	PDN_ANA_CH3	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 3
5	PDN_ANA_CH2	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 2
4	PDN_ANA_CH1	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 1
3	INVERT_CH4	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 4 (1)
2	INVERT_CH3	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 3 (1)
1	INVERT_CH2	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 2 (1)
0	INVERT_CH1	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 1 (1)

(1) Has no effect on test patterns.

13.1.2.1.20 Register 25 (address = 19h)

Figure 139. Register 25

15	14	13	12	11	10	9	8
GAIN_CH5					0	OFFSET_CH5	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH5							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 47. Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH5	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 5 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH5	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 5 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 26, bits 9-0.

13.1.2.1.21 Register 26 (address = 1Ah)

Figure 140. Register 26

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH5	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH5							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 48. Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH5	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 5 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 25, bits 9-0.

13.1.2.1.22 Register 27 (address = 1Bh)

Figure 141. Register 27

15	14	13	12	11	10	9	8
GAIN_CH6					0	OFFSET_CH6	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH6							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 49. Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH6	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 6 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH6	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 6 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 28, bits 9-0.

13.1.2.1.23 Register 28 (address = 1Ch)

Figure 142. Register 28

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH6	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH6							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 28 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH6	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 6 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 27, bits 9-0.

13.1.2.1.24 Register 29 (address = 1Dh)

Figure 143. Register 29

15	14	13	12	11	10	9	8
GAIN_CH7					0	OFFSET_CH7	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH7							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH7	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 7 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH7	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 7 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 30, bits 9-0.

13.1.2.1.25 Register 30 (address = 1Eh)

Figure 144. Register 30

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH7	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH7							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 52. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH7	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 7 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 29, bits 9-0.

13.1.2.1.26 Register 31 (address = 1Fh)

Figure 145. Register 31

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">GAIN_CH8</td><td>0</td><td colspan="2">OFFSET_CH8</td></tr>
<tr><td colspan="5">R/W-0h</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OFFSET_CH8</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Table 53. Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH8	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 8 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH8	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 8 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 32, bits 9-0.

13.1.2.1.27 Register 32 (address = 20h)

Figure 146. Register 32

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">OFFSET_CH8</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="2">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OFFSET_CH8</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH8	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 16 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 31, bits 9-0.

13.1.2.1.28 Register 33 (address = 21h)

Figure 147. Register 33

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>PAT_PRBS_LVDS5</td><td>PAT_PRBS_LVDS6</td><td>PAT_PRBS_LVDS7</td><td>PAT_PRBS_LVDS8</td><td colspan="3">PAT_LVDS5[2:0]</td><td>PAT_LVDS6[2:0]</td></tr>
<tr><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td>R/W-0h</td><td colspan="3">R/W-0h</td><td>R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PAT_LVDS6[2:0]</td><td>0</td><td colspan="4">HPF_CORNER_CH5-8[3:0]</td><td>DIG_HPF_EN_CH5-8</td></tr>
<tr><td colspan="2">R/W-0h</td><td>R/W-0h</td><td colspan="4">R/W-0h</td><td>R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; -n = value after reset

Table 55. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS5	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 5 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS6	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 6 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS7	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 7 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS8	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 8 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS5[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 5 can be programmed with these bits; see Table 44 for bit descriptions.
8-6	PAT_LVDS6[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 6 can be programmed with these bits; see Table 44 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH5-8[3:0]	R/W	0h	When the DIG_HPF_EN_CH5-8 bit is set to 1, the digital HPF characteristic for the corresponding channels can be programmed by setting the value of *k* with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of *k* is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)]$ Note that the value of *k* can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH5-8	R/W	0h	0 = Digital HPF disabled for channels 5 to 8 (default) 1 = Enables digital HPF for channels 5 to 8

13.1.2.1.29 Register 35 (address = 23h)

Figure 148. Register 35

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
PAT_LVDS7[2:0]			PAT_LVDS8[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 56. Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS7[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 7 can be programmed with these bits; see Table 44 for bit descriptions.
4-2	PAT_LVDS8[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 8 can be programmed with these bits; see Table 44 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.30 Register 36 (address = 24h)

Figure 149. Register 36

15	14	13	12	11	10	9	8
PDN_DIG_CH8	PDN_DIG_CH7	PDN_DIG_CH6	PDN_DIG_CH5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDN_ANA_CH8	PDN_ANA_CH7	PDN_ANA_CH6	PDN_ANA_CH5	INVERT_CH8	INVERT_CH7	INVERT_CH6	INVERT_CH5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 57. Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH8	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 8
14	PDN_DIG_CH7	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 7
13	PDN_DIG_CH6	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 6
12	PDN_DIG_CH5	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 5
11	PDN_LVDS8	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 8
10	PDN_LVDS7	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 7
9	PDN_LVDS6	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 6
8	PDN_LVDS5	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 5
7	PDN_ANA_CH8	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 8
6	PDN_ANA_CH7	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 7
5	PDN_ANA_CH6	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 6
4	PDN_ANA_CH5	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 5
3	INVERT_CH8	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 8 (1)
2	INVERT_CH7	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 7 (1)
1	INVERT_CH6	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 6 (1)
0	INVERT_CH5	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 5 (1)

(1) Has no effect on test patterns.

13.1.2.1.31 Register 37 (address = 25h)

Figure 150. Register 37

15	14	13	12	11	10	9	8
GAIN_CH9					0	OFFSET_CH9	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH9							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 58. Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH9	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 9 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH9	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 9 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 38, bits 9-0.

13.1.2.1.32 Register 38 (address = 26h)

Figure 151. Register 38

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH9	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH9							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH9	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 9 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 37, bits 9-0.

13.1.2.1.33 Register 39 (address = 27h)

Figure 152. Register 39

15	14	13	12	11	10	9	8
GAIN_CH10					0	OFFSET_CH10	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH10							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH10	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 10 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH10	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 10 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 40, bits 9-0.

13.1.2.1.34 Register 40 (address = 28h)

Figure 153. Register 40

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH10	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH10							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 61. Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH10	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 10 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 39, bits 9-0.

13.1.2.1.35 Register 41 (address = 29h)

Figure 154. Register 41

15	14	13	12	11	10	9	8
GAIN_CH11					0	OFFSET_CH11	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH11							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 62. Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH11	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 11 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH11	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 11 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 42, bits 9-0.

13.1.2.1.36 Register 42 (address = 2Ah)

Figure 155. Register 42

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH11	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH11							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 63. Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH11	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 11 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 41, bits 9-0.

13.1.2.1.37 Register 43 (address = 2Bh)

Figure 156. Register 43

15	14	13	12	11	10	9	8
GAIN_CH12					0	OFFSET_CH12	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH12							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 64. Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH12	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 12 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH12	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 12 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 44, bits 9-0.

13.1.2.1.38 Register 44 (address = 2Ch)

Figure 157. Register 44

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH12	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH12							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 65. Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH12	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 12 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 43, bits 9-0.

13.1.2.1.39 Register 45 (address = 2Dh)

Figure 158. Register 45

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9[2:0]			PAT_LVDS10[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_LVDS10[2:0]		0	HPF_CORNER_CH9-12[3:0]				DIG_HPF_EN_CH9-12
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 66. Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS9	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 9 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS10	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 10 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS11	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 11 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS12	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 12 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS9[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 9 can be programmed with these bits; see Table 44 for bit descriptions.
8-6	PAT_LVDS10[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 10 can be programmed with these bits; see Table 44 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH9-12[3:0]	R/W	0h	When the DIG_HPF_EN_CH9-12 bit is set to 1, the digital HPF characteristic for the corresponding channels can be programmed by setting the value of *k* with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of *k* is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n - 1) + y(n - 1)]$ Note that the value of *k* can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH9-12	R/W	0h	0 = Digital HPF disabled for channels 9 to 12 (default) 1 = Enables digital HPF for channels 9 to 12

13.1.2.1.40 Register 47 (address = 2Fh)

Figure 159. Register 47

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_LVDS11[2:0]			PAT_LVDS12[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 67. Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS11[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 11 can be programmed with these bits; see Table 44 for bit descriptions.
4-2	PAT_LVDS12[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 12 can be programmed with these bits; see Table 44 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.41 Register 48 (address = 30h)

Figure 160. Register 48

15	14	13	12	11	10	9	8
PDN_DIG_CH12	PDN_DIG_CH11	PDN_DIG_CH10	PDN_DIG_CH9	PDN_LVDS12	PDN_LVDS11	PDN_LVDS10	PDN_LVDS9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDN_ANA_CH12	PDN_ANA_CH11	PDN_ANA_CH10	PDN_ANA_CH9	INVERT_CH12	INVERT_CH11	INVERT_CH10	INVERT_CH9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 68. Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH12	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 12
14	PDN_DIG_CH11	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 11
13	PDN_DIG_CH10	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 10
12	PDN_DIG_CH9	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 9
11	PDN_LVDS12	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 12
10	PDN_LVDS11	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 11
9	PDN_LVDS10	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 10
8	PDN_LVDS9	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 9
7	PDN_ANA_CH12	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 12
6	PDN_ANA_CH11	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 11
5	PDN_ANA_CH10	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 10
4	PDN_ANA_CH9	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 9
3	INVERT_CH12	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 12 (1)
2	INVERT_CH11	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 11 (1)
1	INVERT_CH10	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 10 (1)
0	INVERT_CH9	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 9 (1)

(1) Has no effect on test patterns.

13.1.2.1.42 Register 49 (address = 31h)

Figure 161. Register 49

15	14	13	12	11	10	9	8
GAIN_CH13					0	OFFSET_CH13	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH13							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 69. Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH13	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 13 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH13	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 13 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 50, bits 9-0.

13.1.2.1.43 Register 50 (address = 32h)

Figure 162. Register 50

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH13	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH13							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 70. Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH13	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 13 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 49, bits 9-0.

13.1.2.1.44 Register 51 (address = 33h)

Figure 163. Register 51

15	14	13	12	11	10	9	8
GAIN_CH14					0	OFFSET_CH14	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH14							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 71. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH14	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 14 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH14	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 14 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 52, bits 9-0.

13.1.2.1.45 Register 52 (address = 34h)

Figure 164. Register 52

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH14	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH14							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 72. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH14	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 14 can be obtained with this 10-bit register. The offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 51, bits 9-0.

13.1.2.1.46 Register 53 (address = 35h)

Figure 165. Register 53

15	14	13	12	11	10	9	8
GAIN_CH15					0	OFFSET_CH15	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH15							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 73. Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH15	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 15 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH15	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 15 can be obtained with this 10-bit register. the offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 54, bits 9-0.

13.1.2.1.47 Register 54 (address = 36h)

Figure 166. Register 54

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH15	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH15							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 74. Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH15	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 15 can be obtained with this 10-bit register. the offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 53, bits 9-0.

13.1.2.1.48 Register 55 (address = 37h)

Figure 167. Register 55

15	14	13	12	11	10	9	8
GAIN_CH16					0	OFFSET_CH16	
R/W-0h					R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH16							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 75. Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH16	R/W	0h	When the DIG_GAIN_EN bit is set to 1, the digital gain value for channel 16 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, the digital gain gets set to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH16	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 16 can be obtained with this 10-bit register. the offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 56, bits 9-0.

13.1.2.1.49 Register 56 (address = 38h)

Figure 168. Register 56

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH16	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_CH16							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 76. Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH16	R/W	0h	When the DIG_OFFSET_EN bit is set to 1, the offset value for channel 16 can be obtained with this 10-bit register. the offset value is in twos complement format and its LSB corresponds to a 14-bit LSB. Write the same offset value in register 55, bits 9-0.

13.1.2.1.50 Register 57 (address = 39h)

Figure 169. Register 57

15	14	13	12	11	10	9	8
PAT_PRBS_ LVDS13	PAT_PRBS_ LVDS14	PAT_PRBS_ LVDS15	PAT_PRBS_ LVDS16	PAT_LVDS13[2:0]			PAT_ LVDS14[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAT_LVDS14[2:0]		0	HPF_CORNER_CH13-16[3:0]				DIG_HPF_EN_ CH13-16
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 77. Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS13	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 13 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS14	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 14 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS15	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 15 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS16	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the PRBS pattern on LVDS output 16 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS13[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 13 can be programmed with these bits; see Table 44 for bit descriptions.
8-6	PAT_LVDS14[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 14 can be programmed with these bits; see Table 44 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH13-16[3:0]	R/W	0h	When the DIG_HPF_EN_CH13-16 bit is set to 1, the digital HPF characteristic for the corresponding channels can be programmed by setting the value of *k* with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of *k* is defined by: $Y(n) = \frac{2^k}{2^k + 1}[x(n) - x(n-1) + y(n-1)]$ Note that the value of *k* can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH13-16	R/W	0h	0 = Digital HPF disabled for channels 13 to 16 (default) 1 = Enables digital HPF for channels 13 to 16

13.1.2.1.51 Register 59 (address = 3Bh)

Figure 170. Register 59

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PIN_PAT_LVDS15[2:0]			PAT_LVDS16[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 78. Register 59 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS15[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, the different pattern on LVDS output 15 can be programmed with these bits; see Table 44 for bit descriptions.
4-2	PAT_LVDS16[2:0]	R/W	0h	When the PAT_SELECT_IND bit is set to 1, then the different pattern on LVDS output 16 can be programmed with these bits; see Table 44 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.52 Register 60 (address = 3Ch)

Figure 171. Register 60

15	14	13	12	11	10	9	8
PDN_DIG_CH16	PDN_DIG_CH15	PDN_DIG_CH14	PDN_DIG_CH13	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDN_ANA_CH16	PDN_ANA_CH15	PDN_ANA_CH14	PDN_ANA_CH13	INVERT_CH16	INVERT_CH15	INVERT_CH14	INVERT_CH13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 79. Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH16	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 16
14	PDN_DIG_CH15	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 15
13	PDN_DIG_CH14	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 14
12	PDN_DIG_CH13	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 13
11	PDN_LVDS16	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 16
10	PDN_LVDS15	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 15
9	PDN_LVDS14	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 14
8	PDN_LVDS13	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 13
7	PDN_ANA_CH16	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 16
6	PDN_ANA_CH15	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 15
5	PDN_ANA_CH14	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 14
4	PDN_ANA_CH13	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 13
3	INVERT_CH16	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 16 (1)
2	INVERT_CH15	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 15 (1)
1	INVERT_CH14	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 14 (1)
0	INVERT_CH13	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 13 (1)

(1) Has no effect on test patterns.

13.1.2.1.53 Register 67 (address = 43h)

Figure 172. Register 67

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	LVDS_DCLK_DELAY_PROG[3:0]				0
R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 80. Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4-1	LVDS_DCLK_DELAY_PROG[3:0]	R/W	0h	The LVDS DCLK output delay is programmable with 110-ps steps. Delay values are in twos complement format. Increasing the positive delay increases setup time and reduces hold time, and vice-versa for the negative delay. 0000 = No delay 0001 = 110 ps 0010 = 220 ps … 1110 = –220 ps 1111 = –110 ps …
0	0	R/W	0h	Must write 0

13.1.3 VCA Register Map

This section discusses the VCA register map. A register map is available in Table 81.

DTGC_WR_EN must be set to 0 before programming the VCA register map.

Table 81. VCA Register Map

REGISTER ADDRESS		REGISTER DATA(1)															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
192	C0	0	0	0	0	0	0	0	0	0	0	0	1X_CLK_BUF_MODE	16X_CLK_BUF_MODE	CW_CLK_MODE		CW_TGC_SEL
193	C1	CW_MIX_PH_CH4				CW_MIX_PH_CH3				CW_MIX_PH_CH2				CW_MIX_PH_CH1			
194	C2	CW_MIX_PH_CH8				CW_MIX_PH_CH7				CW_MIX_PH_CH6				CW_MIX_PH_CH5			
195	C3	CW_MIX_PH_CH12				CW_MIX_PH_CH11				CW_MIX_PH_CH10				CW_MIX_PH_CH9			
196	C4	CW_MIX_PH_CH16				CW_MIX_PH_CH15				CW_MIX_PH_CH14				CW_MIX_PH_CH13			
197	C5	PDCH16	PDCH15	PDCH14	PDCH13	PDCH12	PDCH11	PDCH10	PDCH9	PDCH8	PDCH7	PDCH6	PDCH5	PDCH4	PDCH3	PDCH2	PDCH1
198	C6	0	0	0	0	0	0	0	0	0	0	0	0	PDWN_FILTER	PDWN_LNA	GBL_PDWN	FAST_PDWN
199	C7	0	0	0	0	LNA_HPF_PROG		LNA_HPF_DIS	LPF_PROG		0	0	0	0	0	0	0
200	C8	0	0	0	LOW_POW	0	0	0	0	0	0	0	0	0	0	0	0
202	CA	0	0	0	0	0	EN_CONS_CUR	0	0	0	0	0	0	0	0	0	0
206	CE	0	MEDIUM_POW	0	0	0	0	0	0	0	0	0	0	0	0	0	0
230	E6	0	0	0	0	0	0	0	0	0	0	0	TR_EXT_DIS	TR_DIS4	TR_DIS3	TR_DIS2	TR_DIS1

(1) The default value of all registers is 0.

13.1.3.1 Description of VCA Registers

13.1.3.1.1 Register 192 (address = C0h)

Figure 173. Register 192

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	1X_CLK_BUF_MODE	16X_CLK_BUF_MODE	CW_CLK_MODE		CW_TGC_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 82. Register 192 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4	1X_CLK_BUF_MODE	R/W	0h	0 = Accepts CMOS clocks 1 = Accepts differential clocks
3	16X_CLK_BUF_MODE	R/W	0h	0 = Accepts differential clocks 1 = Accepts CMOS clocks
2-1	CW_CLK_MODE	R/W	0h	Programs CW path clock mode 00 = 16X mode 01 = 8X mode 10 = 4X mode 11 = 1X mode
0	CW_TGC_SEL	R/W	0h	0 = TGC mode 1 = CW mode Note: In CW mode, the LNA gain changes to a fixed value of 18 dB and the input attenuator block and low-pass filter are disabled. Thus, TGC and CW mode cannot be used at the same time.

13.1.3.1.2 Register 193 (address = C1h)

Figure 174. Register 193

15	14	13	12	11	10	9	8
CW_MIX_PH_CH4				CW_MIX_PH_CH3			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CW_MIX_PH_CH2				CW_MIX_PH_CH1			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 83. Register 193 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH4	R/W	0h	These bits control the CW mixer phase for channel 4. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
11-8	CW_MIX_PH_CH3	R/W	0h	These bits control the CW mixer phase for channel 3. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
7-4	CW_MIX_PH_CH2	R/W	0h	These bits control the CW mixer phase for channel 2. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
3-0	CW_MIX_PH_CH1	R/W	0h	These bits control the CW mixer phase for channel 1. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.

13.1.3.1.3 Register 194 (address = C2h)

Figure 175. Register 194

15	14	13	12	11	10	9	8
CW_MIX_PH_CH8				CW_MIX_PH_CH7			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CW_MIX_PH_CH6				CW_MIX_PH_CH5			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 84. Register 194 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH8	R/W	0h	These bits control the CW mixer phase for channel 8. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
11-8	CW_MIX_PH_CH7	R/W	0h	These bits control the CW mixer phase for channel 7. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
7-4	CW_MIX_PH_CH6	R/W	0h	These bits control the CW mixer phase for channel 6. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
3-0	CW_MIX_PH_CH5	R/W	0h	These bits control the CW mixer phase for channel 5. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.

13.1.3.1.4 Register 195 (address = C3h)

Figure 176. Register 195

15	14	13	12	11	10	9	8
CW_MIX_PH_CH12				CW_MIX_PH_CH11			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CW_MIX_PH_CH10				CW_MIX_PH_CH9			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 85. Register 195 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH12	R/W	0h	These bits control the CW mixer phase for channel 12. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
11-8	CW_MIX_PH_CH11	R/W	0h	These bits control the CW mixer phase for channel 11. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
7-4	CW_MIX_PH_CH10	R/W	0h	These bits control the CW mixer phase for channel 10. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
3-0	CW_MIX_PH_CH9	R/W	0h	These bits control the CW mixer phase for channel 9. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.

13.1.3.1.5 Register 196 (address = C4h)

Figure 177. Register 196

15	14	13	12	11	10	9	8
CW_MIX_PH_CH16				CW_MIX_PH_CH15			
R/W-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CW_MIX_PH_CH14				CW_MIX_PH_CH13			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 86. Register 196 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH16	R/W	0h	These bits control the CW mixer phase for channel 16. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
11-8	CW_MIX_PH_CH15	R/W	0h	These bits control the CW mixer phase for channel 15. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
7-4	CW_MIX_PH_CH14	R/W	0h	These bits control the CW mixer phase for channel 14. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.
3-0	CW_MIX_PH_CH13	R/W	0h	These bits control the CW mixer phase for channel 13. Writing *N* to these bits sets the corresponding channel phase to N × 22.5° (N = 0 to 15); see Table 87 for further details.

Table 87. CW Mixer Phase Delay vs Register Settings

BIT SETTINGS	CW_MIX_PH_CHX, CW_MIX_PH_CHY PHASE SHIFT
0000	0
0001	22.5°
0010	45°
0011	67.5°
0100	90°
0101	112.5°
0110	135°
0111	157.5°
1000	180°
1001	202.5°
1010	225°
1011	247.5°
1100	270°
1101	292.5°
1110	315°
1111	337.5°

13.1.3.1.6 Register 197 (address = C5h)

Figure 178. Register 197

15	14	13	12	11	10	9	8
PDCH16	PDCH15	PDCH14	PDCH13	PDCH12	PDCH11	PDCH10	PDCH9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDCH8	PDCH7	PDCH6	PDCH5	PDCH4	PDCH3	PDCH2	PDCH1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 88. Register 197 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDCH16	R/W	0h	0 = Default 1 = Channel 16 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
14	PDCH 15	R/W	0h	0 = Default 1 = Channel 15 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
13	PDCH 14	R/W	0h	0 = Default 1 = Channel 14 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
12	PDCH 13	R/W	0h	0 = Default 1 = Channel 13 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
11	PDCH 12	R/W	0h	0 = Default 1 = Channel 12 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
10	PDCH 11	R/W	0h	0 = Default 1 = Channel 11 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.

Table 88. Register 197 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PDCH 10	R/W	0h	0 = Default 1 = Channel 10 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
8	PDCH 9	R/W	0h	0 = Default 1 = Channel 9 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
7	PDCH 8	R/W	0h	0 = Default 1 = Channel 8 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
6	PDCH 7	R/W	0h	0 = Default 1 = Channel 7 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
5	PDCH 6	R/W	0h	0 = Default 1 = Channel 6 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
4	PDCH 5	R/W	0h	0 = Default 1 = Channel 5 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
3	PDCH 4	R/W	0h	0 = Default 1 = Channel 4 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
2	PDCH 3	R/W	0h	0 = Default 1 = Channel 3 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
1	PDCH 2	R/W	0h	0 = Default 1 = Channel 2 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.
0	PDCH 1	R/W	0h	0 = Default 1 = Channel 1 is powered down. This bit powers down the channel of the VCA die only (LNA, LPF, CW mixer). This bit does not affect the ADC channel.

13.1.3.1.7 Register 198 (address = C6h)

Figure 179. Register 198

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	PDWN_FILTER	PDWN_LNA	GBL_PDWN	FAST_PDWN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 89. Register 198 Field Descriptions

Bit	Field	Type	Reset	Description
15-4	0	R/W	0h	Must write 0
3	PDWN_FILTER	R/W	0h	0 = Default 1 = The LPF in the VCA die is powered down
2	PDWN_LNA	R/W	0h	0 = Default 1 = The LNA in the VCA is powered down
1	GBL_PDWN	R/W	0h	0 = Normal operation 1 = The LNA, LPF, CW mixer, and TGC control engine are completely powered down (slow wake response) for the VCA die. Note that enabling this bit does not power-down the ADC. This bit only powers down the VCA die.
0	FAST_PDWN	R/W	0h	0 = Normal operation 1 = The LNA, LPF, and CW mixer are partially powered down (fast wake response) for the VCA die. Note that enabling this bit does not power-down the ADC. This bit only powers down the VCA die.

13.1.3.1.8 Register 199 (address = C7h)

Figure 180. Register 199

15	14	13	12	11	10	9	8
0	0	0	0	LNA_HPF_PROG		LNA_HPF_DIS	LPF_PROG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LPF_PROG	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 90. Register 199 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11-10	LNA_HPF_PROG	R/W	0h	These bits control the LNA HPF cutoff frequency. 00 = 75 kHz 01 = 150 kHz 10 = 300 kHz 11 = 600 kHz
9	LNA_HPF_DIS	R/W	0h	0 = LNA HPF enabled 1 = LNA HPF disabled
8-7	LPF_PROG	R/W	0h	These bits program the cutoff frequency of the antialiasing LPF. 00 = 15 MHz in low-noise and medium-power mode, 7.5 MHz in low-power mode 01 = 10 MHz in low-noise and medium-power mode, 5 MHz in low-power mode 10 = 25 MHz in low-noise and medium-power mode, 12.5 MHz in low-power mode 11 = 20 MHz in low-noise and medium-power mode, 10 MHz in low-power mode
6-0	0	R/W	0h	Must write 0

13.1.3.1.9 Register 200 (address = C8h)

Figure 181. Register 200

15	14	13	12	11	10	9	8
0	0	0	LOW_POW	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 91. Register 200 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	0	R/W	0h	Must write 0
12	LOW_POW	R/W	0h	0 = Default 1 = In TGC mode the VCA die is set to low-power mode. No effect in CW mode.
11-0	0	R/W	0h	Must write 0

13.1.3.1.10 Register 202 (address = CAh)

Figure 182. Register 202

15	14	13	12	11	10	9	8
0	0	0	0	0	EN_CONS_ CUR	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 92. Register 202 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	0	R/W	0h	Must write 0
10	EN_CONS_ CUR	R/W	0h	0 = Default 1 = In TGC mode, the LNA is programmed in constant-current TGC mode In CW mode, this bit does not do anything.
9-0	0	R/W	0h	Must write 0

13.1.3.1.11 Register 206 (address = CEh)

Figure 183. Register 206

15	14	13	12	11	10	9	8
0	MEDIUM_POW	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 93. Register 206 Field Descriptions

Bit	Field	Type	Reset	Description
15	0	R/W	0h	Must write 0
14	MEDIUM_POW	R/W	0h	0 = Default 1 = In TGC mode, the VCA die is set to medium-power mode. The LOW_POW bit must be set to 0 to enable this mode. This bit has no effect in CW mode.
13-0	0	R/W	0h	Must write 0

13.1.3.1.12 Register 230 (address = E6h)

Figure 184. Register 230

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	TR_EXT_DIS	TR_DIS4	TR_DIS3	TR_DIS2	TR_DIS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 94. Register 230 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4	TR_EXT_DIS(1)	R/W	0h	0 = The TR_EN<x> pins are used to disconnect the LNA HPF from the INP pins 1 = The TR_DIS[4:1] register bits are used to disconnect the LNA HPF from the INP pin
3	TR_DIS4(1)	R/W	0h	When the TR_EXT_DIS bit is set to 1: 0 = Disconnects the LNA HPF from the input of channels 13, 14, 15, and 16 1 = Enables the LNA HPF at the input of channels 13, 14, 15, and 16
2	TR_DIS3(1)	R/W	0h	When the TR_EXT_DIS bit is set to 1: 0 = Disconnects the LNA HPF from the input of channels 9, 10, 11, and 12 1 = Enables the LNA HPF at the input of channels 9, 11, 11, and 12
1	TR_DIS2(1)	R/W	0h	When the TR_EXT_DIS bit set to 1: 0 = Disconnects the LNA HPF from the input of channels 5, 6, 7, and 8 1 = Enables the LNA HPF at the input of channels 5, 6, 7, and 8
0	TR_DIS1(1)	R/W	0h	When the TR_EXT_DIS bit is set to 1: 0 = Disconnects the LNA HPF from the input of channels 1, 2, 3, and 4 1 = Enables the LNA HPF at the input of channels 1, 2, 3, and 4

(1) Note that when this bit is enabled, the LNA HPF remains powered up and is disconnected only from the input. This feature can be used for better overload recovery by disconnecting the LNA HPF during AFE overload conditions.

13.1.4 DTGC Register Map

This section discusses the DTGC register map. A register map is available in Table 23.

DTGC_WR_EN must be set to 1 before programming other bits of the global register map.

Table 95. DTGC Register Map

REGISTER ADDRESS		REGISTER DATA															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	MEM_WORD_0															
2-160	2-A0	MEM_WORD_1 to MEM_WORD_159															
161	A1	START_GAIN_0								STOP_GAIN_0							
162	A2	POS_STEP_0								NEG_STEP_0							
163	A3	START_INDEX_0								STOP_INDEX_0							
164	A4	START_GAIN_TIME_0															
165	A5	HOLD_GAIN_TIME_0															
166	A6	START_GAIN_1								STOP_GAIN_1							
167	A7	POS_STEP_1								NEG_STEP_1							
168	A8	START_INDEX_1								STOP_INDEX_1							
169	A9	START_GAIN_TIME_1															
170	AA	HOLD_GAIN_TIME_1															
171	AB	START_GAIN_2								STOP_GAIN_2							
172	AC	POS_STEP_2								NEG_STEP_2							
173	AD	START_INDEX_2								STOP_INDEX_2							
174	AE	START_GAIN_TIME_2															
175	AF	HOLD_GAIN_TIME_2															
176	B0	START_GAIN_3								STOP_GAIN_3							
177	B1	POS_STEP_3								NEG_STEP_3							
178	B2	START_INDEX_3								STOP_INDEX_3							
179	B3	START_GAIN_TIME_3															
180	B4	HOLD_GAIN_TIME_3															
181	B5	SLOPE_FAC[0]	ENABLE_INT_START	MEM_BANK_SEL		0	MANUAL_START	0	MANUAL_GAIN_DTGC								
182	B6	MODE_SEL		PROFILE_REG_SEL		PROFILE_EXT_DIS	INP_RES_SEL				FLIP_ATTEN	DIS_ATTEN	SLOPE_FAC[3:1]			0	0
183	B7	NEXT_CYCLE_WAIT_TIME															
185	B9	FIX_ATTEN_EN_0	ATTENUATION_0							FIX_ATTEN_EN_1	ATTENUATION_1						
186	BA	FIX_ATTEN_EN_2	ATTENUATION_2							FIX_ATTEN_EN_3	ATTENUATION_3						

13.1.4.1 Description of DTGC Register

13.1.4.1.1 DTGC Registers

DTGC_WR_EN must be set to 1 to write these registers.

13.1.4.1.1.1 Register 1 (address = 1h)

Figure 185. Register 1

15	14	13	12	11	10	9	8
MEM_WORD_0							
R/W-Undefined							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MEM_WORD_0							
R/W-Undefined							

LEGEND: R/W = Read/Write; -n = value after reset

Table 96. Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MEM_WORD_0	R/W	Undefined	The memory word register 0 stores the gain step information that is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details. A reset operation does not reset this register. After power-up, this register must be explicitly written to its desired content.

13.1.4.1.1.2 Registers 2-160 (address = 2h-A0h)

Figure 186. Registers 2-160

15	14	13	12	11	10	9	8
MEM_WORD_1 to MEM_WORD_159							
R/W-Undefined							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MEM_WORD_1 to MEM_WORD_159							
R/W-Undefined							

LEGEND: R/W = Read/Write; -n = value after reset

Table 97. Registers 2-160 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MEM_WORD_1 to MEM_WORD_159	R/W	Undefined	The memory word registers from 1 to 159 store the gain step information that is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details. A reset operation does not reset this register. After power-up, this register must be explicitly written to its desired content.

13.1.4.1.1.3 Register 161 (address = A1h)

Figure 187. Register 161

15	14	13	12	11	10	9	8
START_GAIN_0							
R/W-0h							
7	6	5	4	3	2	1	0
STOP_GAIN_0							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 98. Register 161 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_GAIN_0	R/W	0h	These bits determine the start gain value for profile 0 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	STOP_GAIN_0	R/W	9Fh	These bits determine the stop gain value for profile 0 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.4 Register 162 (address = A2h)

Figure 188. Register 162

15	14	13	12	11	10	9	8
POS_STEP_0							
R/W-0h							
7	6	5	4	3	2	1	0
NEG_STEP_0							
R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 99. Register 162 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	POS_STEP_0	R/W	0h	These bits determine the positive step value for profile 0 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	NEG_STEP_0	R/W	FFh	These bits determine the negative step value for profile 0 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.5 Register 163 (address = A3h)

Figure 189. Register 163

15	14	13	12	11	10	9	8
START_INDEX _0							
R/W-0h							
7	6	5	4	3	2	1	0
STOP_INDEX _0							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 100. Register 163 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_INDEX _0	R/W	0h	These bits determine the start index value for profile 0, which is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
7-0	STOP_INDEX _0	R/W	9Fh	These bits determine the stop index value for profile 0, which is used internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.6 Register 164 (address = A4h)

Figure 190. Register 164

15	14	13	12	11	10	9	8
START_GAIN_TIME_0							
R/W-0h							
7	6	5	4	3	2	1	0
START_GAIN_TIME_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 101. Register 164 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	START_GAIN_TIME_0	R/W	0h	These bits define the start gain time for profile 0 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.7 Register 165 (address = A5h)

Figure 191. Register 165

15	14	13	12	11	10	9	8
HOLD_GAIN_TIME_0							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOLD_GAIN_TIME_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 102. Register 165 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HOLD_GAIN_TIME_0	R/W	0h	These bits define the hold gain time for profile 0 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.8 Register 166 (address = A6h)

Figure 192. Register 166

15	14	13	12	11	10	9	8
START_GAIN_1							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STOP_GAIN_1							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 103. Register 166 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_GAIN_1	R/W	0h	These bits determine the start gain value for profile 1 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	STOP_GAIN_1	R/W	9Fh	These bits determine the stop gain value for profile 1 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.9 Register 167 (address = A7h)

Figure 193. Register 167

15	14	13	12	11	10	9	8
POS_STEP_1							
R/W-0h							
7	6	5	4	3	2	1	0
NEG_STEP_1							
R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 104. Register 167 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	POS_STEP_1	R/W	0h	These bits determine the positive step value for profile 1 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	NEG_STEP_1	R/W	FFh	These bits determine the negative step value for profile 1 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.10 Register 168 (address = A8h)

Figure 194. Register 168

15	14	13	12	11	10	9	8
START_INDEX _1							
R/W-0h							
7	6	5	4	3	2	1	0
STOP_INDEX _1							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 105. Register 168 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_INDEX _1	R/W	0h	These bits determine the start index value for profile 1 that is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
7-0	STOP_INDEX _1	R/W	9Fh	These bits determine the stop index value for profile 1 that is used internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.11 Register 169 (address = A9h)

Figure 195. Register 169

15	14	13	12	11	10	9	8
START_GAIN_TIME_1							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_GAIN_TIME_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 106. Register 169 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	START_GAIN_TIME_1	R/W	0h	These bits define the start gain time for profile 1 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.12 Register 170 (address = AAh)

Figure 196. Register 170

15	14	13	12	11	10	9	8
HOLD_GAIN_TIME_1							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HOLD_GAIN_TIME_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 107. Register 170 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HOLD_GAIN_TIME_1	R/W	0h	These bits define the hold gain time for profile 1 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.13 Register 171 (address = ABh)

Figure 197. Register 171

15	14	13	12	11	10	9	8
START_GAIN_2							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STOP_GAIN_2							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 108. Register 171 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_GAIN_2	R/W	0h	These bits determine the start gain value for profile 2 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	STOP_GAIN_2	R/W	9Fh	These bits determine the stop gain value for profile 2 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.14 Register 172 (address = ACh)

Figure 198. Register 172

15	14	13	12	11	10	9	8
POS_STEP_2							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEG_STEP_2							
R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 109. Register 172 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	POS_STEP_2	R/W	0h	These bits determine the positive step value for profile 2 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	NEG_STEP_2	R/W	FFh	These bits determine the negative step value for profile 2 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.15 Register 173 (address = ADh)

Figure 199. Register 173

15	14	13	12	11	10	9	8
START_INDEX _2							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STOP_INDEX _2							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 110. Register 173 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_INDEX _2	R/W	0h	These bits determine the start index value for profile 2 that is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
7-0	STOP_INDEX _2	R/W	9Fh	These bits determine the stop index value for profile 2 that is used internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.16 Register 174 (address = AEh)

Figure 200. Register 174

15	14	13	12	11	10	9	8
START_GAIN_TIME_2							
R/W-0h							
7	6	5	4	3	2	1	0
START_GAIN_TIME_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 111. Register 174 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	START_GAIN_TIME_2	R/W	0h	These bits define start gain time for profile 2 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.17 Register 175 (address = AFh)

Figure 201. Register 175

15	14	13	12	11	10	9	8
HOLD_GAIN_TIME_2							
R/W-0h							
7	6	5	4	3	2	1	0
HOLD_GAIN_TIME_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 112. Register 175 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HOLD_GAIN_TIME_2	R/W	0h	These bits define hold gain time for profile 2 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.18 Register 176 (address = B0h)

Figure 202. Register 176

15	14	13	12	11	10	9	8
START_GAIN_3							
R/W-0h							
7	6	5	4	3	2	1	0
STOP_GAIN_3							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 113. Register 176 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_GAIN_3	R/W	0h	These bits determine the start gain value for profile 3 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	STOP_GAIN_3	R/W	9Fh	These bits determine the stop gain value for profile 3 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.19 Register 177 (address = B1h)

Figure 203. Register 177

15	14	13	12	11	10	9	8
POS_STEP_3							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEG_STEP_3							
R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 114. Register 177 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	POS_STEP_3	R/W	0h	These bits determine the positive step value for profile 3 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.
7-0	NEG_STEP_3	R/W	FFh	These bits determine the negative step value for profile 3 that is used in different DTGC modes; see the *Digital TGC Modes* section for more details.

13.1.4.1.1.20 Register 178 (address = B2h)

Figure 204. Register 178

15	14	13	12	11	10	9	8
START_INDEX _3							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEG_STEP_0							
R/W-9Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 115. Register 178 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	START_INDEX _3	R/W	0h	These bits determine the start index value for profile 3 that is used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
7-0	STOP_INDEX _3	R/W	9Fh	These bits determine the stop index value for profile 3 that is used internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.21 Register 179 (address = B3h)

Figure 205. Register 179

15	14	13	12	11	10	9	8
START_GAIN_TIME_3							
R/W-0h							
7	6	5	4	3	2	1	0
START_GAIN_TIME_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 116. Register 179 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	START_GAIN_TIME_3	R/W	0h	These bits define the start gain time for profile 3 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.22 Register 180 (address = B4h)

Figure 206. Register 180

15	14	13	12	11	10	9	8
HOLD_GAIN_TIME_3							
R/W-0h							
7	6	5	4	3	2	1	0
HOLD_GAIN_TIME_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 117. Register 180 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HOLD_GAIN_TIME_3	R/W	0h	These bits define the hold gain time for profile 3 and are used in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.

13.1.4.1.1.23 Register 181 (address = B5h)

Figure 207. Register 181

15	14	13	12	11	10	9	8
SLOPE_FAC[0]	ENABLE_INT_START	MEM_BANK_SEL		0	MANUAL_START	0	MANUAL_GAIN_DTGC
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MANUAL_GAIN_DTGC							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 118. Register 181 Field Descriptions

Bit	Field	Type	Reset	Description
15	SLOPE_FAC[0]	R/W	0h	This bit is used to control the TGC gain curve slope in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
14	ENABLE_INT_START	R/W	0h	0 = External TGC start signal 1 = Periodic TGC start signal is generated by the device itself; see the *Digital TGC Test Modes* section for more details.
13-12	MEM_BANK_SEL	R/W	0h	These bits select the memory bank; see the *Internal Non-Uniform Mode* section for more details.
11, 9	0	R/W	0h	Must write 0
10	MANUAL_START	R/W	0h	0 = No operation 1 = The TGC start signal is generated internally for single-shot operation only; see the *Digital TGC Test Modes* section for more details.
8-0	MANUAL_GAIN_DTGC	R/W	0h	The value of the gain code is determined with this register in programmable fixed-gain mode; see the *Programmable Fixed Gain Mode* section for more details.

13.1.4.1.1.24 Register 182 (address = B6h)

Figure 208. Register 182

15	14	13	12	11	10	9	8
MODE_SEL		PROFILE_REG_SEL		PROFILE_EXT_DIS	INP_RES_SEL		
R/W-0h		R/W-0h		R/W-0h	R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INP_RES_SEL	FLIP_ATTEN	DIS_ATTEN	SLOPE_FAC[3:1]			0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 119. Register 182 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MODE_SEL	R/W	0h	These bits determine the DTGC mode. 00 = External non-uniform mode 01 = Up, down ramp mode 10 = Programmable fixed-gain mode 11 = Internal non-uniform mode
13-12	PROFILE_REG_SEL	R/W	0h	These bits determine which profile register to use when the PROFILE_EXT_DIS bit is 1. 00 = Profile 0 01 = Profile 1 10 = Profile 2 01 = Profile 3

Table 119. Register 182 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	PROFILE_EXT_DIS	R/W	0h	0 = Device pins TGC_PROF<2> and TGC_PROF<1> determine which profile to use 1 = The PROFILE_REG_SEL register bits determine which profile to use
10-7	INP_RES_SEL	R/W	0h	Depending upon source resistance, proper input attenuation resistance must be selected to obtain 8-dB attenuation. Table 120 lists the values to be written for different source resistances.
6	FLIP_ATTEN	R/W	0h	0 = In the TGC gain curve, the attenuation of the attenuator block varies first, followed by the LNA gain variation 1 = In the TGC gain curve, the LNA gain varies first, followed by the attenuation of the attenuator block
5	DIS_ATTEN	R/W	0h	0 = Attenuator is enabled 1 = Attenuator is disabled
4-2	SLOPE_FAC[3:1]	R/W	0h	These bits are used to control the TGC gain curve slope in internal non-uniform mode; see the *Internal Non-Uniform Mode* section for more details.
1-0	0	R/W	0h	Must write 0

Table 120. INP_RES_SEL Values

BIT SETTING	SOURCE RESISTANCE
0000	50 Ω
0001	115 Ω
0010	70 Ω
0011	270 Ω
0100	60 Ω
0101	160 Ω
0110	90 Ω
0111	800 Ω
1000	60 Ω
1001	130 Ω
1010	80 Ω
1011	400 Ω
1100	65 Ω
1101	200 Ω
1110	100 Ω
1111	Open

13.1.4.1.1.25 Register 183 (address = B7h)

Figure 209. Register 183

15	14	13	12	11	10	9	8
NEXT_CYCLE_WAIT_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
NEXT_CYCLE_WAIT_TIME							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 121. Register 183 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NEXT_CYCLE_WAIT_TIME	R/W	0h	When ENABLE_INT_START is set to 1, the periodicity of the internal start signal is controlled with this register; see the *Digital TGC Test Modes* section for more details.

13.1.4.1.1.26 Register 185 (address = B9h)

Figure 210. Register 185

15	14	13	12	11	10	9	8
FIX_ATTEN_EN_0	ATTENUATION_0						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
FIX_ATTEN_EN_1	ATTENUATION_1						
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 122. Register 185 Field Descriptions

Bit	Field	Type	Reset	Description
15	FIX_ATTEN_EN_0	R/W	0h	0 = Default 1 = Enable fixed attenuation mode for profile 0
14-8	ATTENUATION_0	R/W	0h	When the FIX_ATTEN_EN_0 bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_0 bits for profile 0. A value of *N* written in the ATTENUATION_0 register sets the attenuation level at –8 + N × 0.125 dB.
7	FIX_ATTEN_EN_1	R/W	0h	0 = Default 1 = Enable fixed attenuation mode for profile 1
6-0	ATTENUATION_1	R/W	0h	When the FIX_ATTEN_EN_1 bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_1 bits for profile 1. A value of *N* written in the ATTENUATION_1 register sets the attenuation level at –8 + N × 0.125 dB.

13.1.4.1.1.27 Register 186 (address = BAh)

Figure 211. Register 186

15	14	13	12	11	10	9	8
FIX_ATTEN_EN_2	ATTENUATION_2						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
FIX_ATTEN_EN_3	ATTENUATION_3						
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 123. Register 186 Field Descriptions

Bit	Field	Type	Reset	Description
15	FIX_ATTEN_EN_2	R/W	0h	0 = Default 1 = Enable fixed attenuation mode for profile 2
14-8	ATTENUATION_2	R/W	0h	When the FIX_ATTEN_EN_2 bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_2 bits for profile 2. A value of *N* written in the ATTENUATION_2 register sets the attenuation level at –8 + N × 0.125 dB.
7	FIX_ATTEN_EN_3	R/W	0h	0 = Default 1 = Enable fixed attenuation mode for profile 3
6-0	ATTENUATION_3	R/W	0h	When the FIX_ATTEN_EN_3 bit is set to 1, the attenuation level of the attenuator block is set by the ATTENUATION_3 bits for profile 3. A value of *N* written in the ATTENUATION_3 register sets the attenuation level at –8 + N × 0.125 dB.

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

AFE5818 Data Sheet, SBAS687

ADS8413 Data Sheet, SLAS490

ADS8472 Data Sheet, SLAS514

CDCE72010 Data Sheet, SCAS858

CDCM7005 Data Sheet, SCAS793

ISO7240 Data Sheet, SLLS868

LMK04803 Data Sheet, SNAS489

OPA1632 Data Sheet, SBOS286

OPA2211 Data Sheet, SBOS377

SN74AUP1T04 Data Sheet, SCES800

THS4130 Data Sheet, SLOS318

MicroStar BGA Packaging Reference Guide, SSYZ015

WEBENCH® Filter Designer

14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5816ZAV	ACTIVE	NFBGA	ZAV	289	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE5816	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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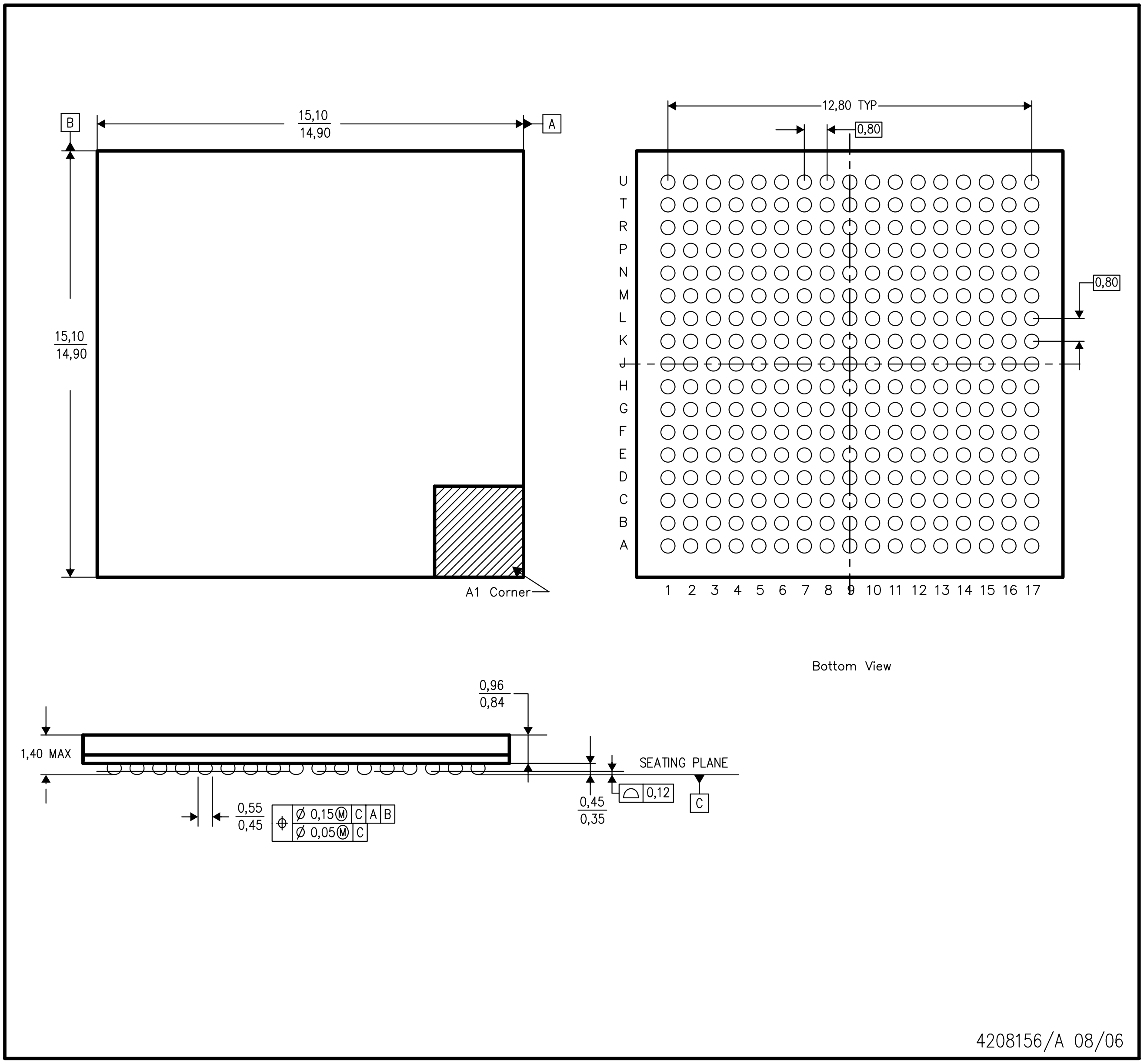
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZAV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

IMPORTANT NOTICE

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