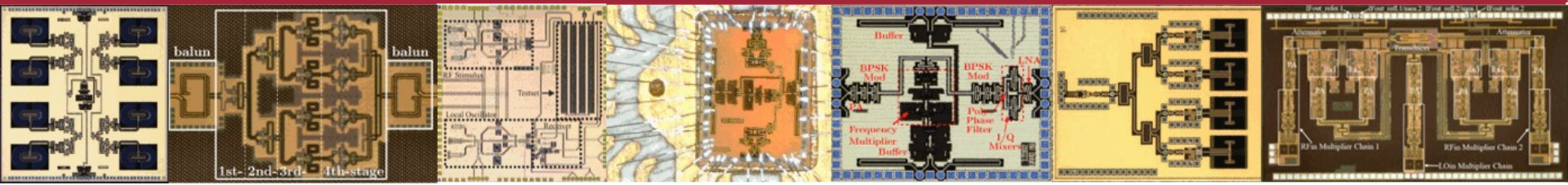
Tape-Out December 2023

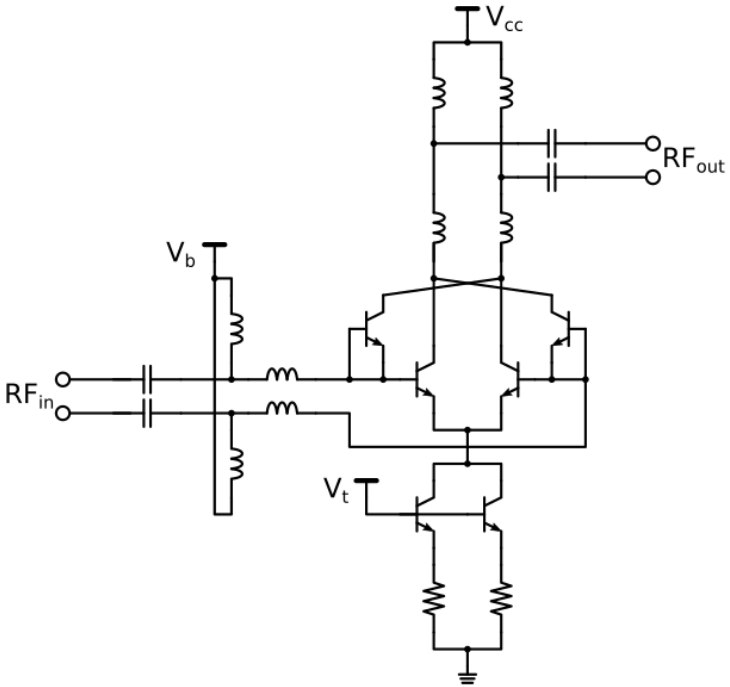
Open Source Design of a 24-GHz Low Noise Amplifier

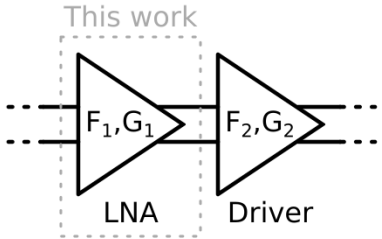


Martin Sander

Contents

Schematic of the LNA



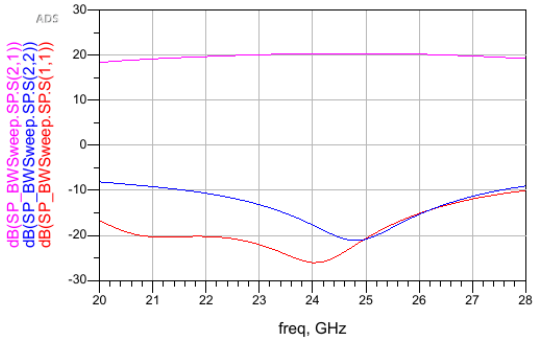


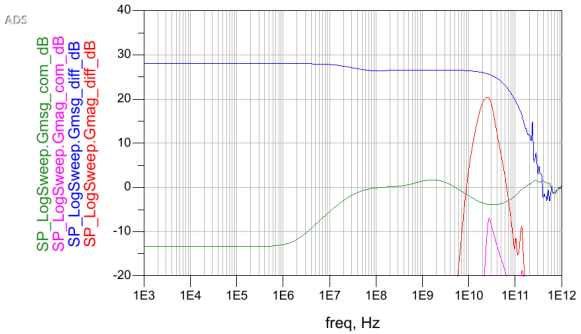
Design Goals:

- Low Noise Figure, best: 3 dB or below
- High Gain: 20 dB or more
- Fully Differential Design
- Common Mode Rejection: above 25 dB

Simulation Results including pads and ESD protection

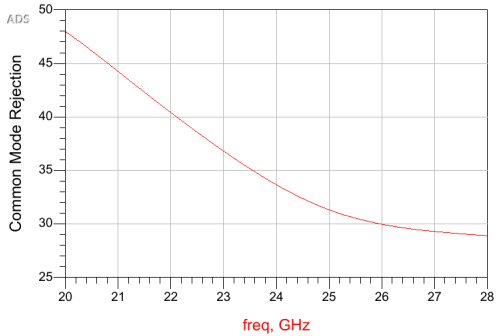
Differential input / output matching and gain

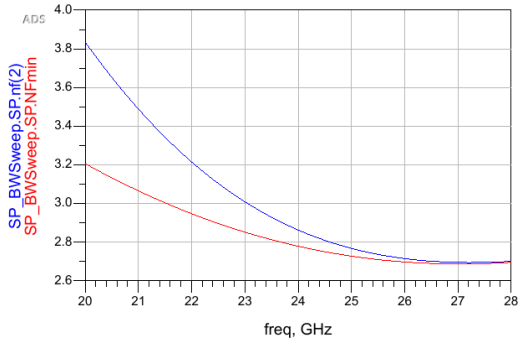




Max. Stable Gain and Max. Available Gain

Common mode rejection





NF_{min} and Realized Noise Figure

Chip Layout

- Total chip size: 780 x 680 µm
- LNA size: 380 x 300 µm
- GSGSG pads with ESD protection
- DC pads with ESD protection