/ALL/Xschem/OTA33.xyce/OTA33_test_01_xyce.sch

COMMANDS3
SIM=none

```
spice code

* schematic: OTA33_test_01_xyce
* dir:       /ALL/Xschem/OTA33.xyce
* test:      /ALL/Xschem/OTA33.xyce/OTA33_BIAS.sym

* mos_corner:
* mos_corner:



.option temp=27


.lib /home/ich/share/pdk/ihp-sg13g2/libs.tech/xyce/models/cornerRES.lib      res_typ
.lib /home/ich/share/pdk/ihp-sg13g2/libs.tech/xyce/models/cornerCAP.lib      cap_typ

.lib /home/ich/share/pdk/ihp-sg13g2/libs.tech/xyce/models/cornerMOShv.lib    mos_tt
.lib /home/ich/share/pdk/ihp-sg13g2/libs.tech/xyce/models/cornerMOSlv.lib    mos_tt
.lib /home/ich/share/pdk/ihp-sg13g2/libs.tech/xyce/models/cornerHBT.lib      hbt_typ

.param nw=1e-6
.param nl=1e-6
.param pw=2e-6
.param pl=1e-6
.param iset=3u

.op
.print dc format=raw v(*) i(*)
```

COMMANDS1
SIM=none

```
pdk_path = /home/ich/share/pdk/ihp-sg13g2

mosfet corners: tt ss ff sf fs
mcafet corners: tt

simulations: op dc dc_zoom ac tran

iset: 3u

ac 1e3..1e9Hz;

# pmos w/l = 2u/1u dont work for TCL
# nmos w/l = 1u/1u dont work for TCL
pmos w/l = 2e-6/1e-6
nmos w/l = 1e-6/1e-6


 #proc to ignore simulator=none evaluation for ngspice

.raw-file path and namebase: /ALL/Xschem/OTA33.xyce/simulation/OTA33_test_01_xyce
```

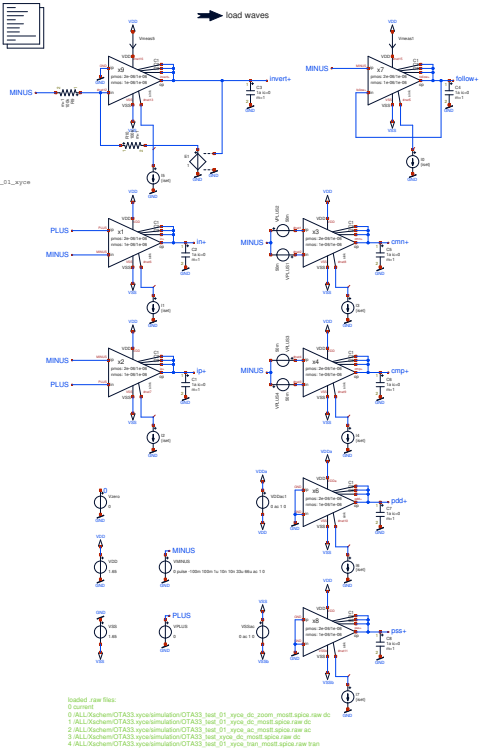
NGSPICE TCL
SIM=ngspice

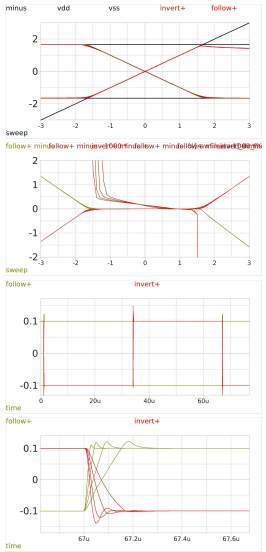
Xyce TCL
SIM=xyce

Xyce
SIM=xyce

xyce netlist simulate corners ALL

load waves





xschem annotate_op

SCHEM om 2024-11-29 17:35:06
/ALL/Xschem/OTA33.xyce/OTA33_test_01_xyce.sch