FMD_QNC_amps_filled

Release 0.1

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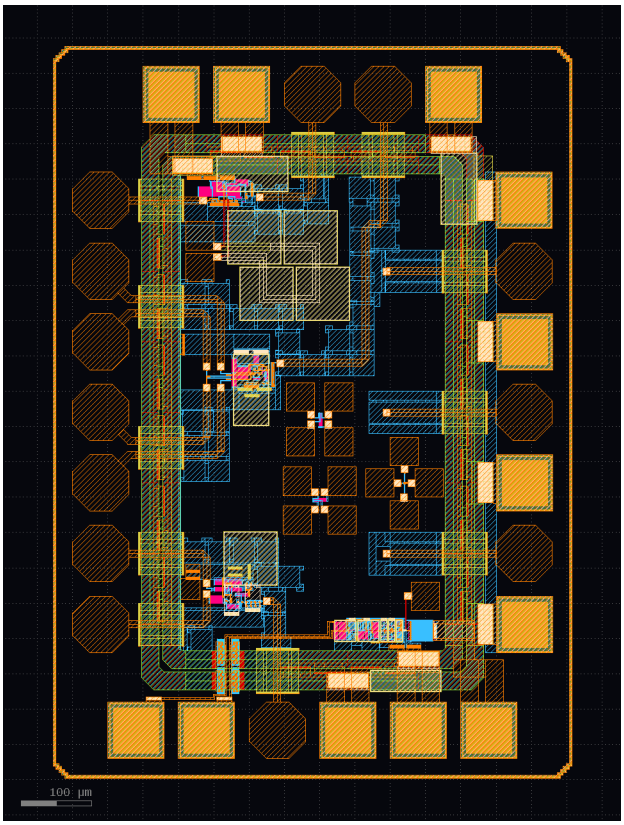
CONTENTS

Warning

this chip is designed without correct LVS. only parts are really verified…



CHAPTER

ONE

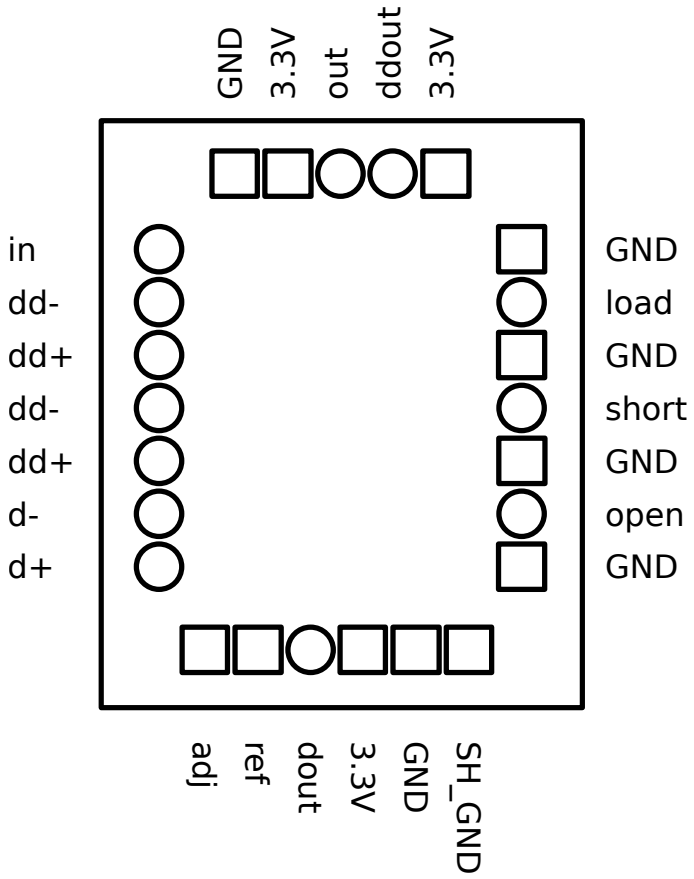
SPECIFICATIONS

there are 3 different amplifiers, a voltage-regulator and some experiments

1. **single ended lowpower amplifier**
    - 3.3V power supply
    - < 3.5mA current including powering of a laser-diode
    - > 30dB gain at 1GHz
    - 0..60°C
    - low-pass corner programmable via capacitor
2. **dual input differential lowpower amplifier**
    - 3.3V power supply
    - < 3.5mA current including powering of a laser-diode
    - > 10dB gain at 1GHz
    - 0..60°C
3. **differential lowpower amplifier**
    - 3.3V power supply
    - < 3.5mA current including powering of a laser-diode
    - 0dB gain at 1GHz
    - 0..60°C
4. **shunt-regulator 3.3V**
    - max. 50mA
    - delta tc = 0 @ 10..30°C
    - trimmable
    - possibility for lowpass filter
5. **test-structure for RPPD matching**
    - see differences in x and y build resistors, does it really matter?
    - see differences in middle and edge resistors, do we need dummy resistors?
6. **a sg13g2 transistor**
    - if nothing else is working, we get at least a transistor :)

7. **open, short & load**
    - to calibrate the pads and connections out, and measure the impedances of the amplifiers

1.1 pinout



1.2 signals

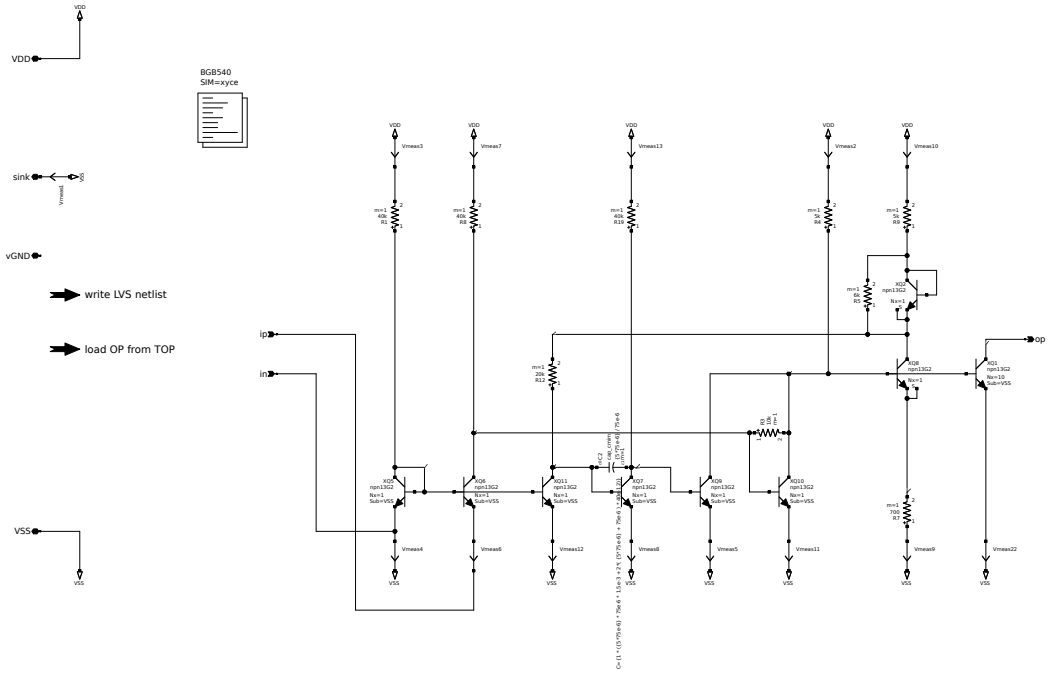
pin name	whats it
GND	supply and signal ground
SH_GND	shunt-anode, connect to GND, optional current measurement
3.3V	positive supply & shunt regulator cathode
ref	reference output & input. optional low-pass capacitor to GND
adj	adjust the band-gap-reference via resistor to 3.3V or GND
in	amplifier input
out	amplifier out
d-	differential amplifier inverting input
d+	differential amplifier non-inverting input
dout	differential amplifier laser diode output
dd-	double differential amplifier inverting input. connected together over two 50Omega
dd+	double differential amplifier non-inverting input. connected together over two 50Omega
ddout	double differential amplifier laser diode output

CHAPTER

TWO

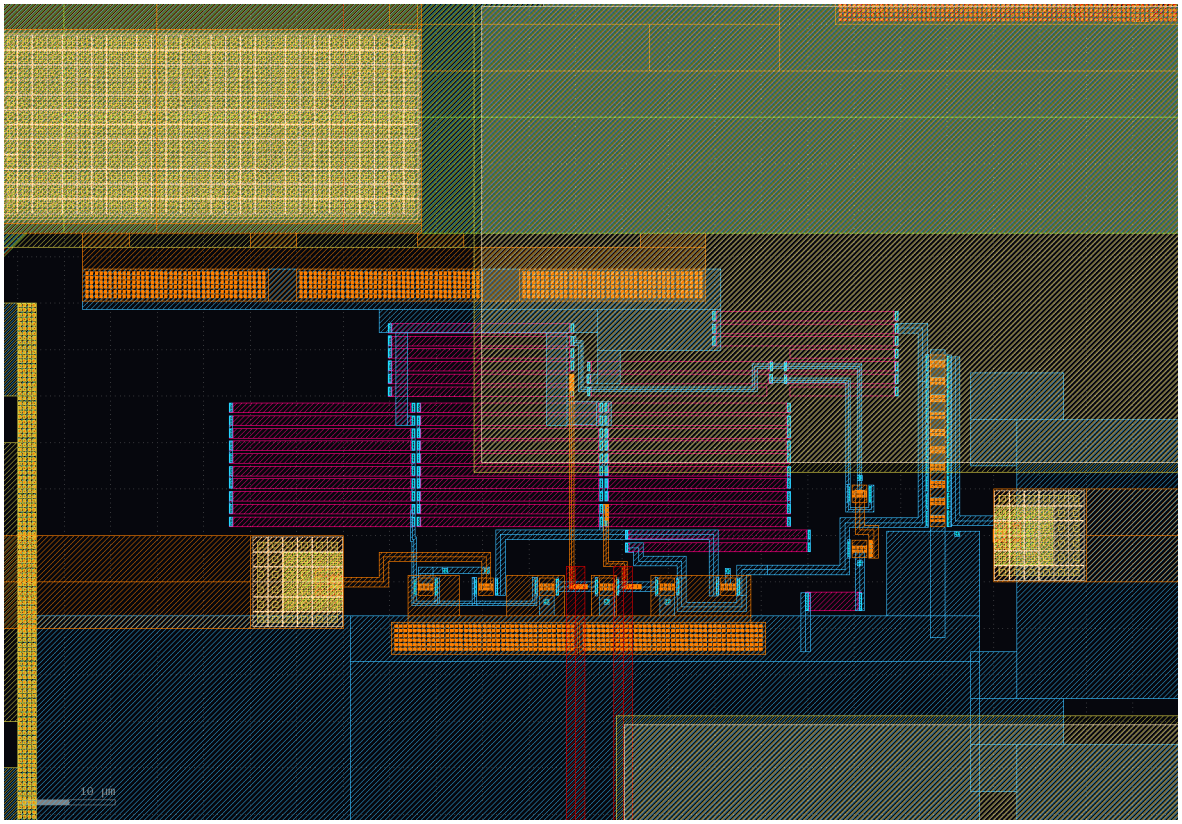
AMPLIFIER

2.1 schematic



this single input amplifier ist DC-coupled and GND referenced. it drives a laser diode over Q1. its bias current is measured via Q8 and regulated from a norton amplifier build from Q11, Q7 and Q9. the low-pass-corner is set by R12 and C2 (that is also available over test-pads inside the power-ring of the chip). the RF-path goes over a base-circuit Q6 to Q10 and Q1. R3 is used to set the gain. Q2's job is to improve the temperature dependence of the bias-current.

2.2 layout



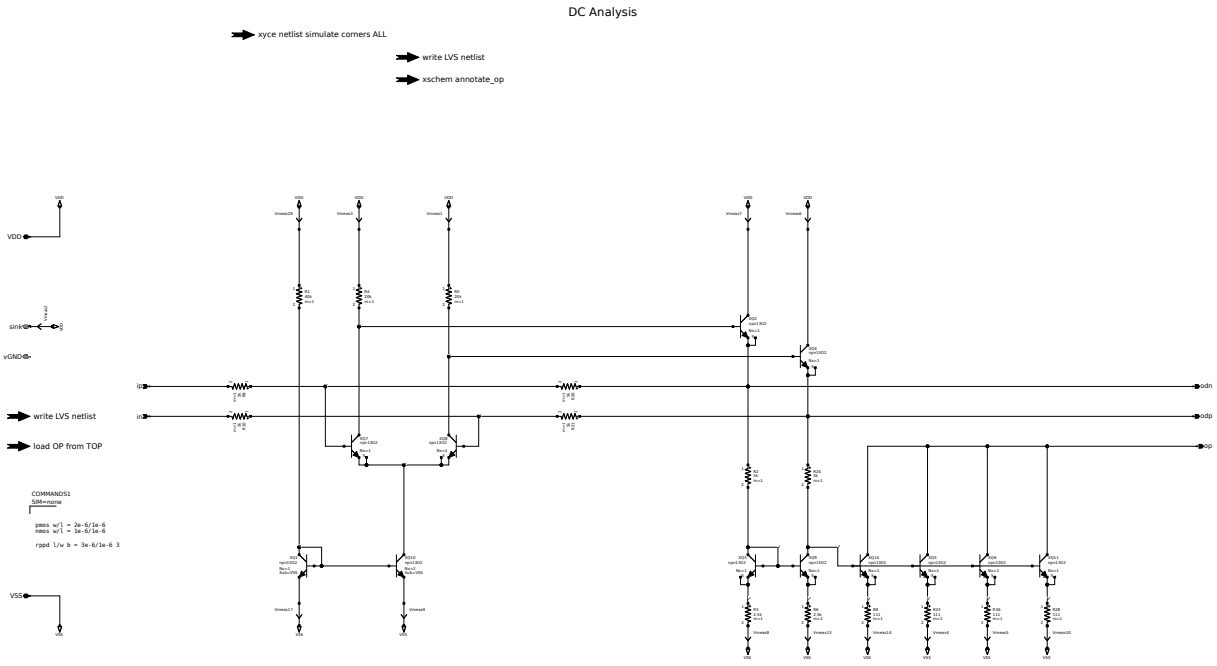
the RPPD resistors are layout that way, because i had problems using LVS with resistors and was hoping it works with the simples shape. but in the end, i didn't manage to make LVS work anyway.

CHAPTER

THREE

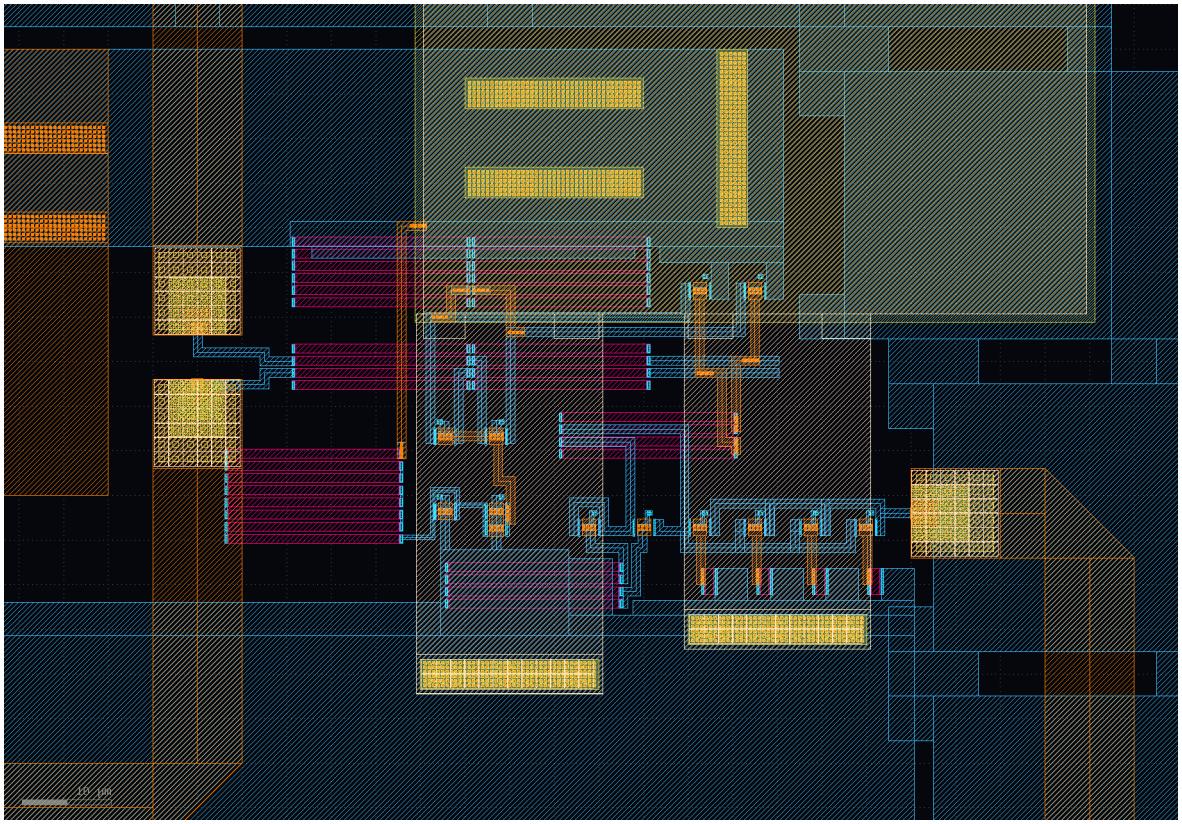
DIFFERENTIAL AMPLIFIER

3.1 schematic



a simple voltage feedback (R9, R10 to R20, R21) differential amplifier, without common-mode-regulator. the output is converted over a current differencing amplifier (Q5, Q9 and Q14, Q3, Q6, Q11) to a single-ended signal.

3.2 layout

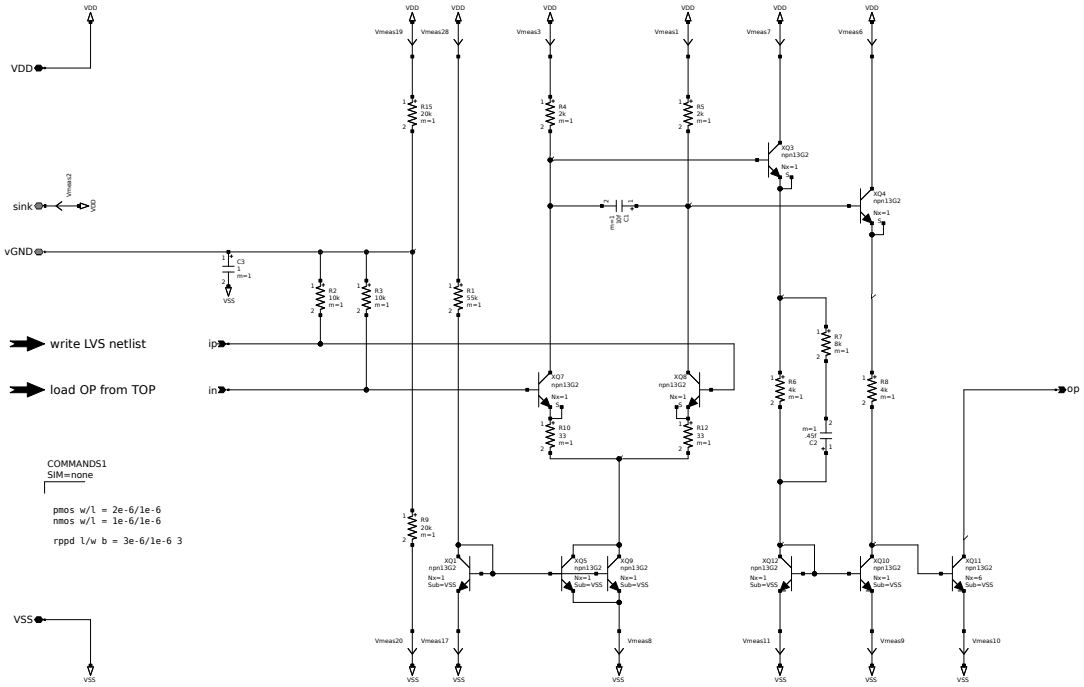


CHAPTER

FOUR

DUAL INPUT DIFFERENTIAL AMPLIFIER

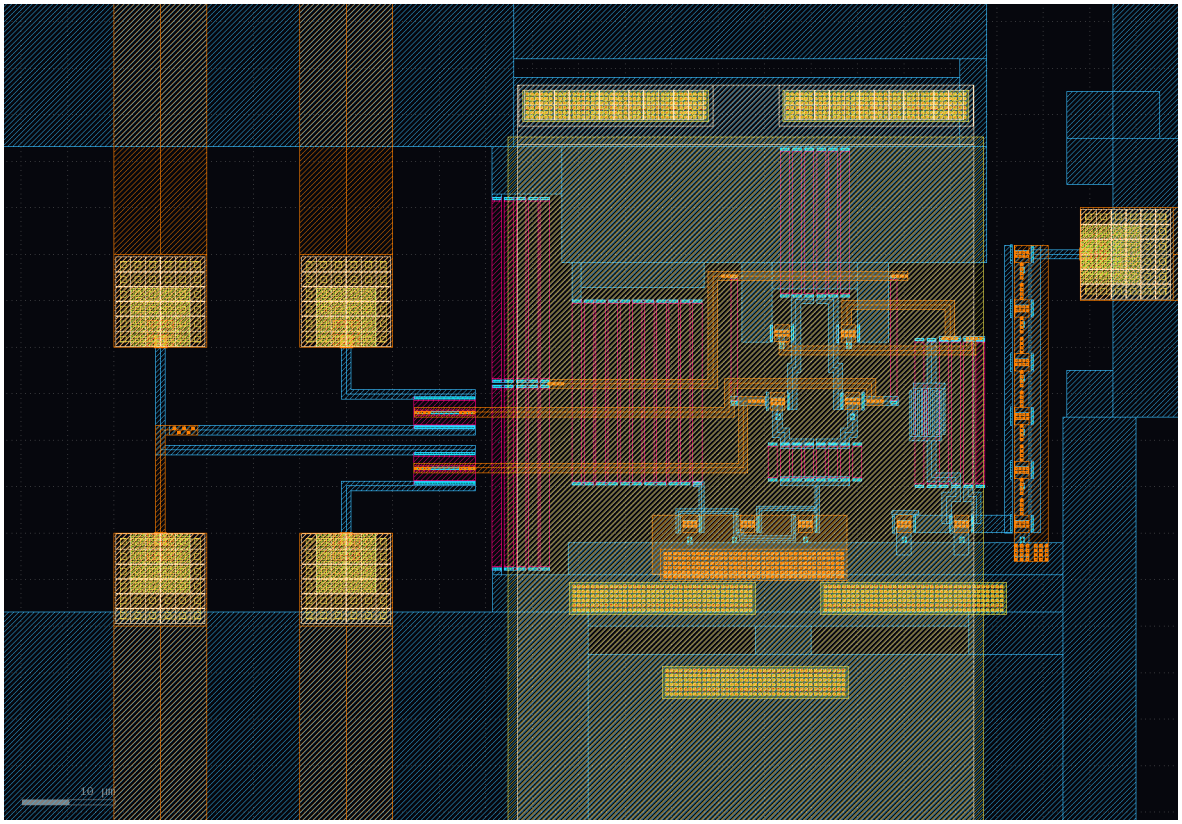
4.1 schematic



a simple current feedback (R10, R12) differential amplifier, without common-mode-regulator. the output is converted over a current differencing amplifier (Q12, Q10, Q11) to a single-ended signal.

the input ip is connected over two 50Omega resistors to both dd+ pads. the input in is connected over two 50Omega resistors to both dd- pads. its thought for compensation circuits that compensate capacitive coupled signals at the input.

4.2 layout



on the left side of the amplifier the for 50Omega resistors are connected to the input-microstriplines.

CHAPTER

FIVE

AMPLIFIER SIMULATIONS

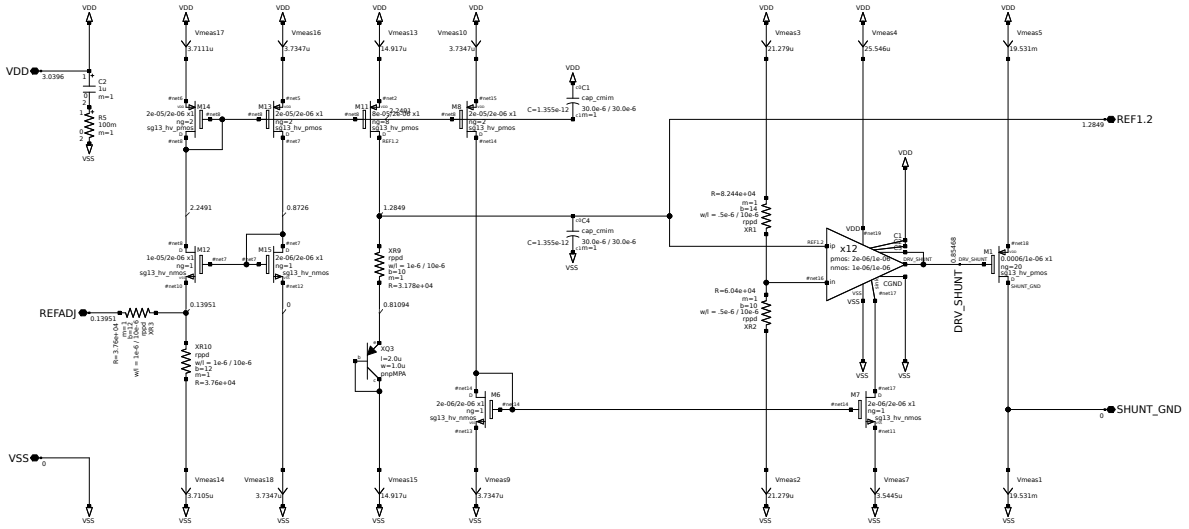
PDF with Xyce simulation

CHAPTER

SIX

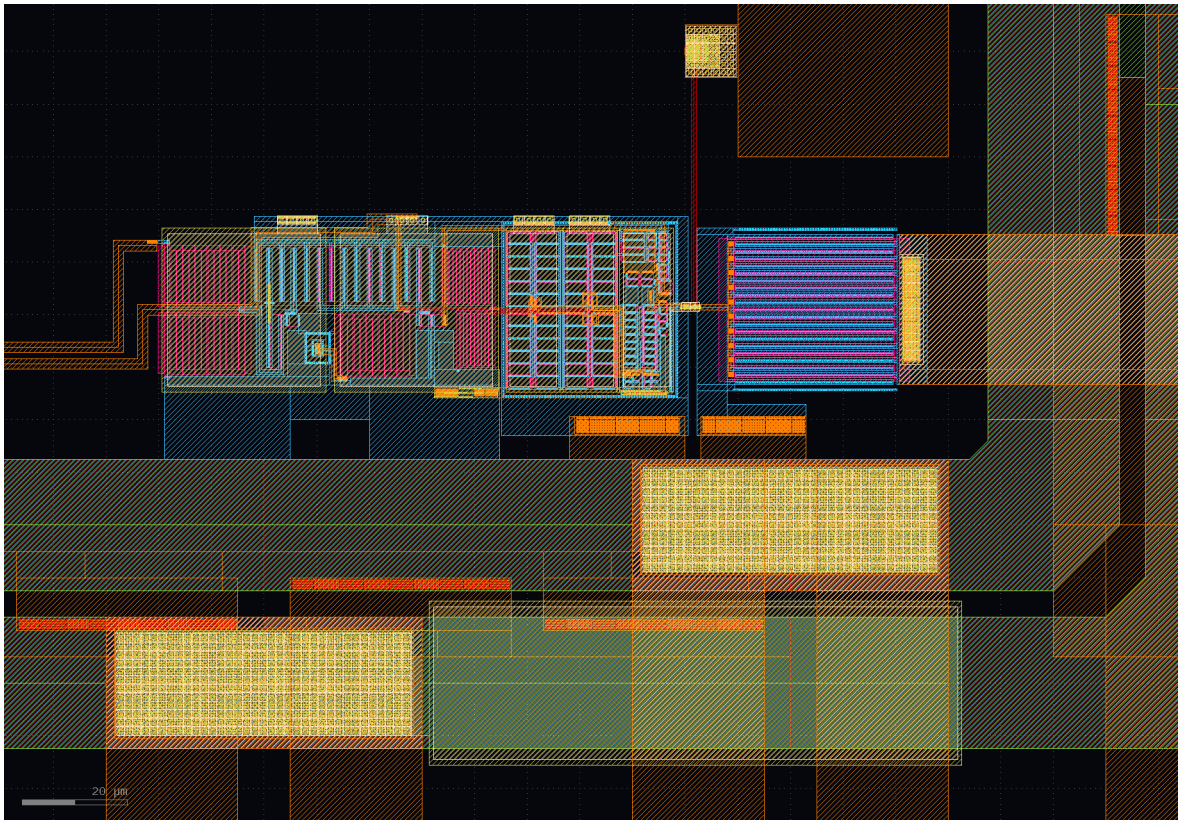
SHUNT REGULATOR 3.3V

6.1 schematic



this is a shunt-regulator for 3.3V and max. 50mA using a simple band-gap-reference. the reference uses MOSFET and BjT temperature coefficients, and needs only one BjT.

6.2 layout



6.3 options

there is the option to filter the reference output via a capacitor from the ref-pad to GND.

its also possible to adjust the temperature-turning-point via the adj-pad and the voltage via the ref pad.

6.4 simulation

PDF with Xyce simulation

CHAPTER

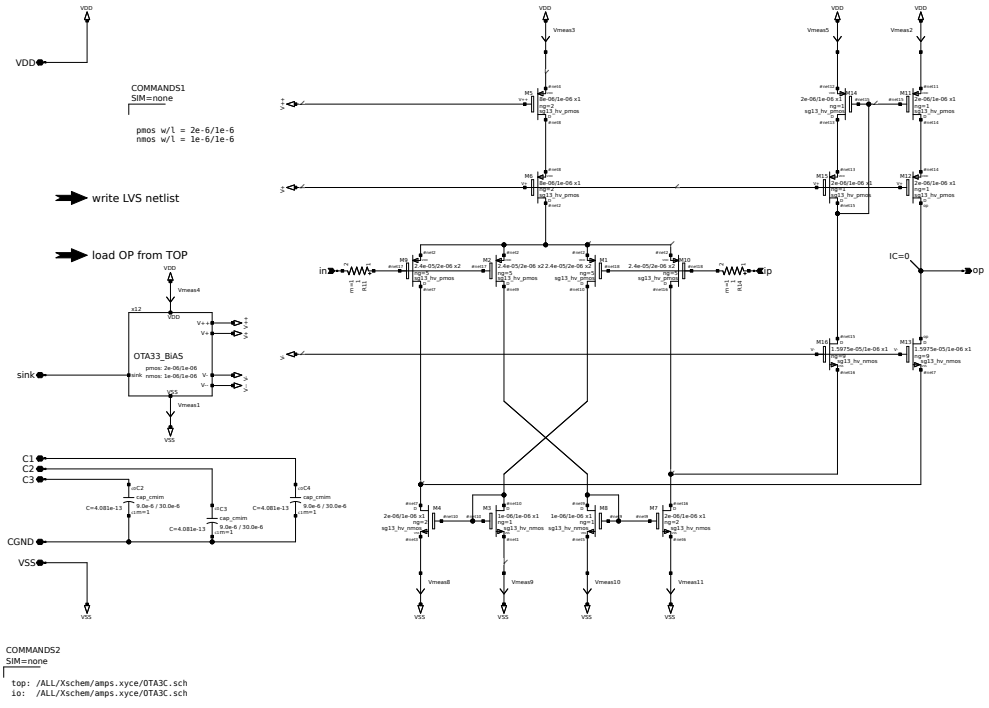
SEVEN

HIGH VOLTAGE OTA

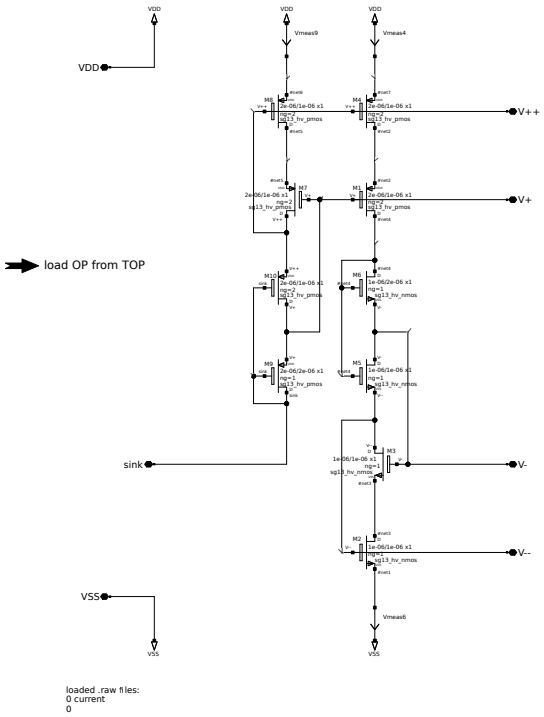
1.1. the OTA the circuit should be used with iHPs PNP-device pnpMPA, so it should be working from VSS. this called for an PMOS input. the design is a simplified version of `The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier`

because of the used CMOS-process the PMOS transistors could have an isolated bulk, without special effort. the simulations showed that the isolated versions had a bigger gain, but a smaller common-mode-range, and i preferred the later. the bias-current is programmable an so also the band-width. the bias-voltages should allow wide-swing output voltages. in the space the circuit uses are 3 MiM-capacitors placed. they are intended to use for frequency-compensation or as power-rail decoupling.

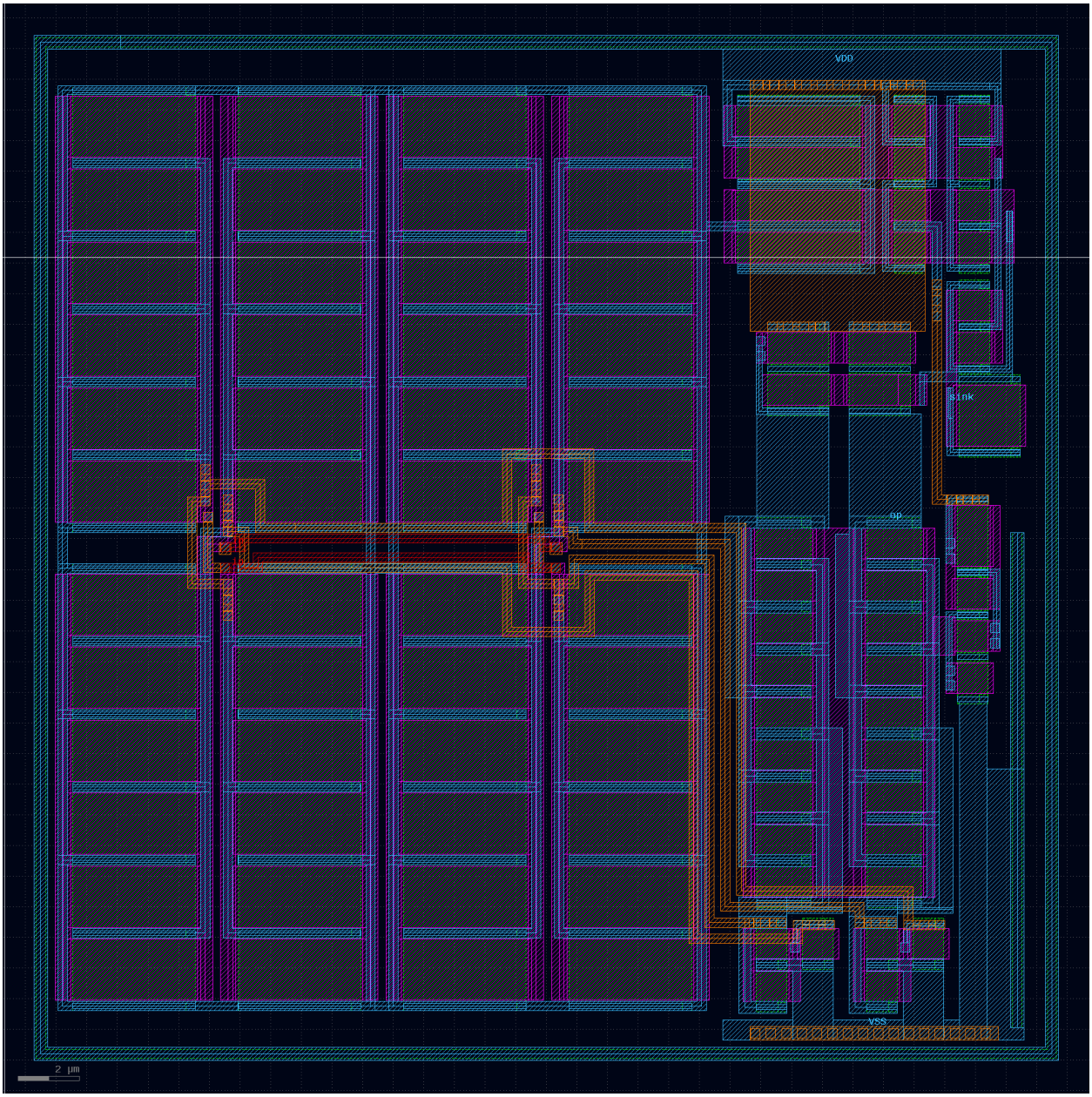
7.1 OTA



7.2 bias generator



7.3 layout



7.4 simulations

using different bias-currents of 1, 3 and 10µA a few simulations are printed into a PDF that allow to see the gain, common-mode-range, bandwidth and a slew-rate:

`PDF with Xyce simulations .ac .dc .trans`

the schematics of this simulations is `Xschem document`

7.5 ETHZ feedback

its a bit stupid to design OTAs that fit in a square, if there is no such space-requirement. the layout should be changed to minimize the conductor-length of the signals between the differential-stage and the current-mirrors.

CHAPTER

EIGHT

EXPERIMENTS

8.1 RPPD

there are 6 resistors available to measure: 3 in X and Y orientations and both versions as dummy and normal resistors

8.2 sg13g2

there is a fast BjT for measurements.

8.3 calibration kit

to measure the amplifier impedances and to see the effect of pads and wire-bonding, there are an open, short and load calkit.

CHAPTER

NINE

DESIGN DATA AND DESIGN PROCESS DESCRIPTION

9.1 iHP 130nm BiCMOS process sg13g2

the process is useable via iHPs openPDK:

source https://github.com/IHP-GmbH/IHP-Open-PDK

documentation https://ihp-open-pdk-docs.readthedocs.io/en/latest/index.html

open-source runs: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/fast-design-enablement/open-source-pdk

9.2 Xschem schematics:

folder	for
design_data/xschem/OTA	design and simulation of the OTA
design_data/xschem/amplifiers	simulations of the three amplifiers
design_data/xschem/shunt_regulator	simulations of the voltage regulators
design_data/xschem/symbol	symbols for Xschem schematics

9.3 KLayout .GDS:

file	for
design_data/FMD_QNC_amps_filled.gds	layout of the chip

CHAPTER

TEN

VALIDATION OF THE CIRCUITS

asap & subito…

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