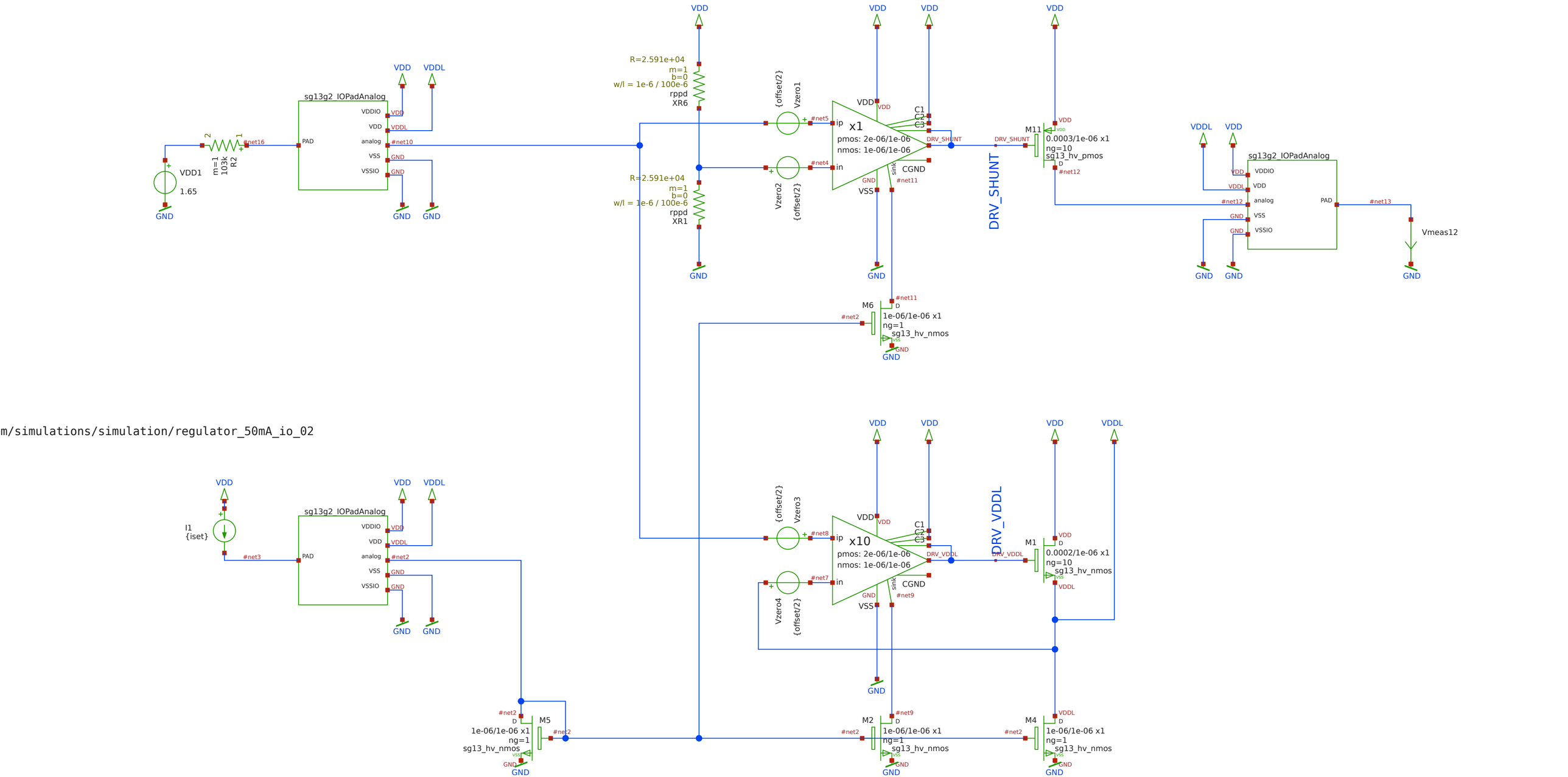
m/simulations/simulation/regulator_50mA_io_02
VDD
VDDL
GND
VDD1
1.65
R2
m=1
103k
sg13g2_IOPadAnalog
VDDIO
analog
VSS
VSSIO
PAD
#net16
#net10
R=2.591e+04
m=1
b=0
w/l = 1e-6 / 100e-6
rppd
XR6
XR1
Vzero1
Vzero2
Vzero3
Vzero4
{offset/2}
#net5
#net4
#net8
#net7
x1
x10
pmos: 2e-06/1e-06
nmos: 1e-06/1e-06
C1
C2
C3
CGND
sink
in
ip
DRV_SHUNT
DRV_VDDL
M11
M1
0.0003/1e-06 x1
ng=10
sg13_hv_pmos
0.0002/1e-06 x1
sg13_hv_nmos
#net12
#net13
Vmeas12
M6
1e-06/1e-06 x1
ng=1
#net11
#net2
I1
{iset}
#net3
M5
M2
M4
#net9