FMD_QNC_mmW_detector

Release 0.1

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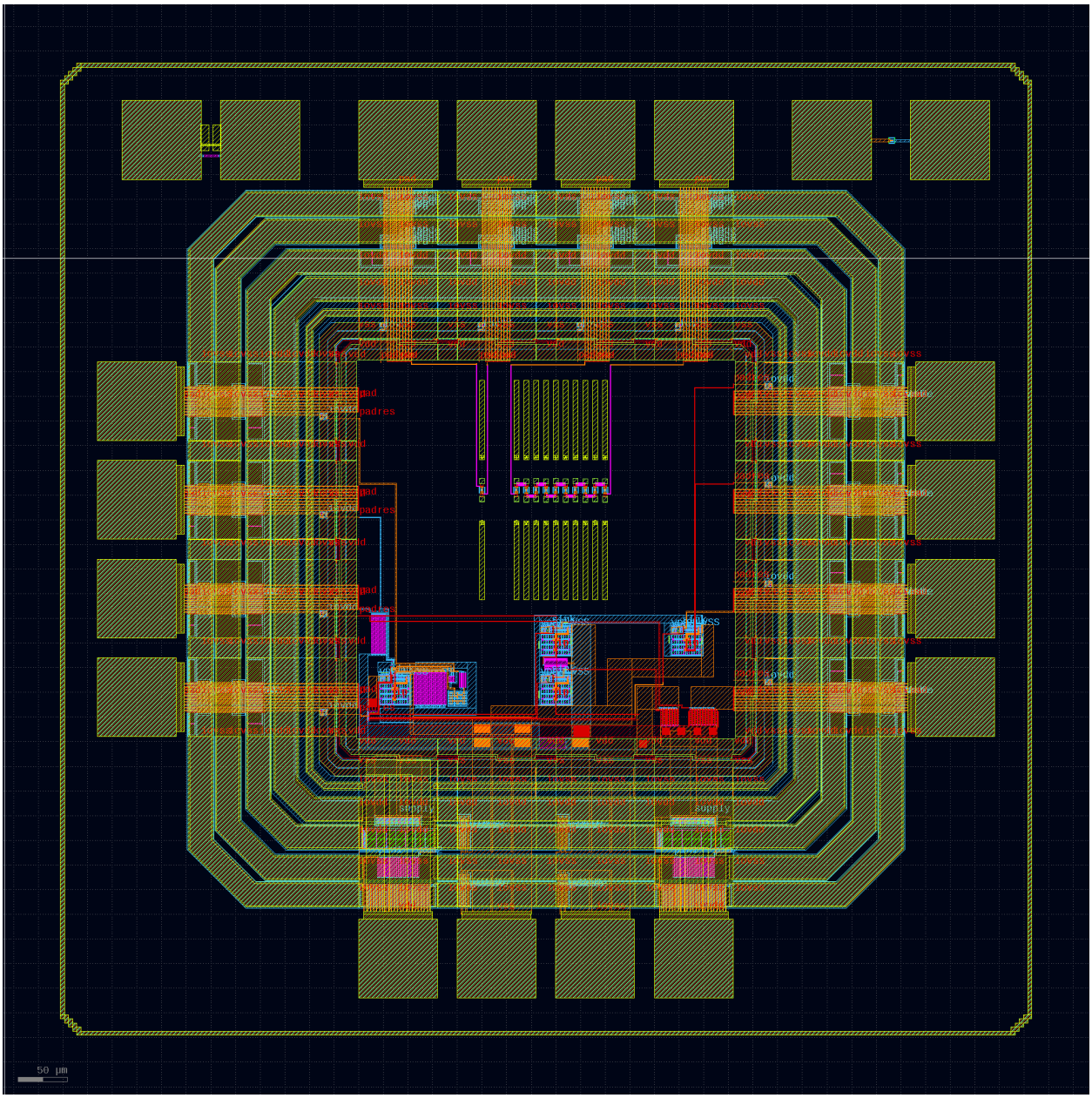
CONTENTS

> **Warning**
>
> this chip is mostly done using an unfinished PDK. LVS was done only for parts.



CHAPTER

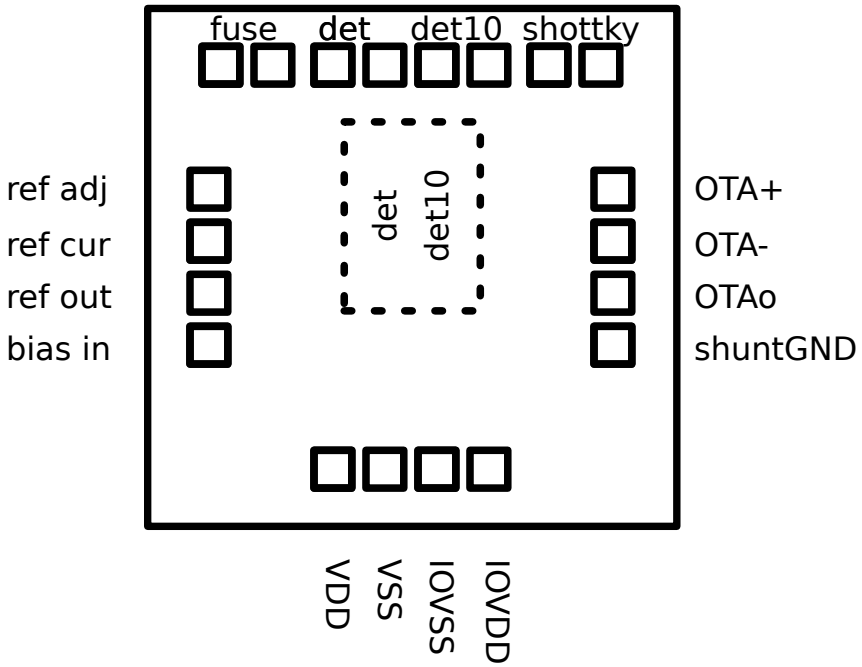
ONE

CMOS ONLY DESIGNS

this is a chip to test the following circuits:

1. **an 3.3V OTA**
    - an input common-mode-range from < VSS to VDD - 500mV
    - bias current programmable via resistor
    - gain about 70dB
    - offset in < 5mV
2. **a band gap design using this OTA.**
    - option to make an low-pass
    - option to adjust the delta temperature coefficient zero
3. **a shunt-regulator for 3.3V**
    - should heat until 50mA
    - option to disable and measure the shunt current
4. **a high dropout 1.8V regulator**
    - should be powered by the 3.3V
    - low output impedance
    - high power supply rejection
5. **two different mmW detector designs**
    - dipole/diode detector
    - a 1 diode design as reference of a
    - 10 serial connected diode design
6. iHPs standard IO-cells for analog signal, VSS, VDD and IOVSS, IOVDD
7. a schottky diode, for measurements
8. a fuse/resistor combination to test the possibility of fuse-trimming

1.1 pinout



1.2 signals

pin name	whats it
fuse	fuse experiment
det	dipole detector
det10	10x serial dipole detectors
schottky	test-diode
OTA+	non-inverting OTA input
OTA-	inverting OTA input
OTAo	OTA output
shuntGND	shunt-regulators VSS connection. can be used to measure the current
IOVDD	3.3V input and shunt-cathode if shuntGND is connected to IOVSS
IOVSS	0V - connect to VSS
VSS	0V - connect to IOVSS
VDD	1.8V regulator output
bias in	resistor from IOVDD sets the bias-currents of all OTAs
ref out	band-gap voltage - high impedance output and regulator ref input. low-pass possible.
ref cur	reference current source from IOVDD
ref adj	resistor to IOVDD or IOVSS to trim the zero of the temperature coefficient

CHAPTER

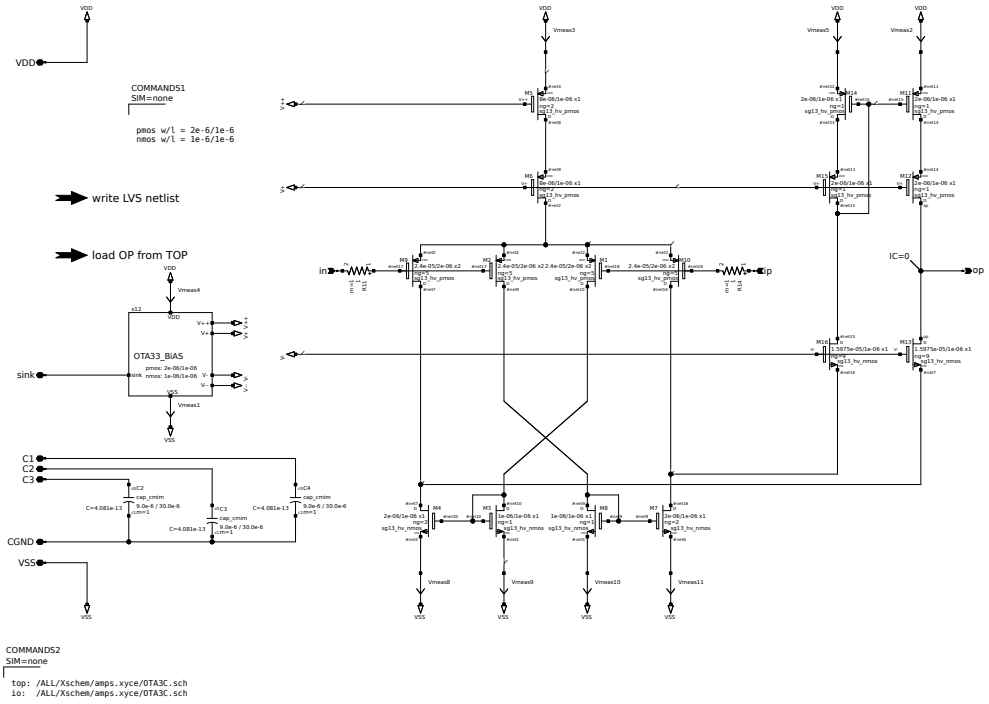
TWO

HIGH VOLTAGE OTA

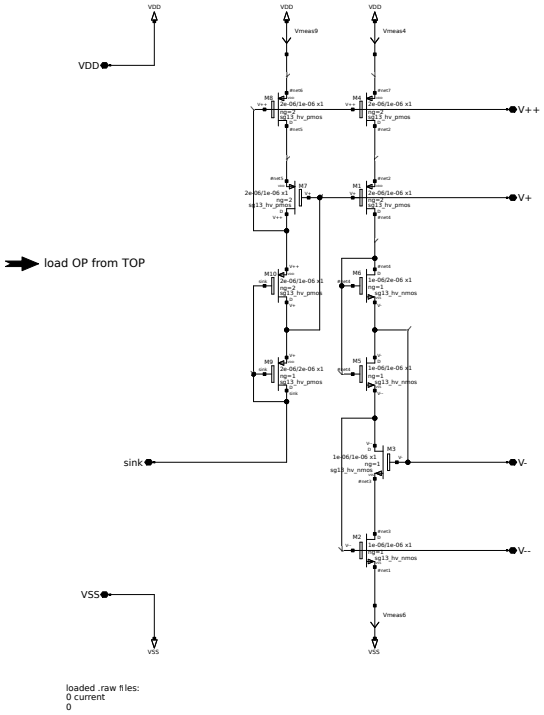
1.1. the OTA the circuit should be used with iHPs PNP-device pnpMPA, so it should be working from VSS. this called for an PMOS input. the design is a simplified version of `The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier`

because of the used CMOS-process the PMOS transistors could have an isolated bulk, without special effort. the simulations showed that the isolated versions had a bigger gain, but a smaller common-mode-range, and i preferred the later. the bias-current is programmable an so also the band-width. the bias-voltages should allow wide-swing output voltages. in the space the circuit uses are 3 MiM-capacitors placed. they are intended to use for frequency-compensation or as power-rail decoupling.

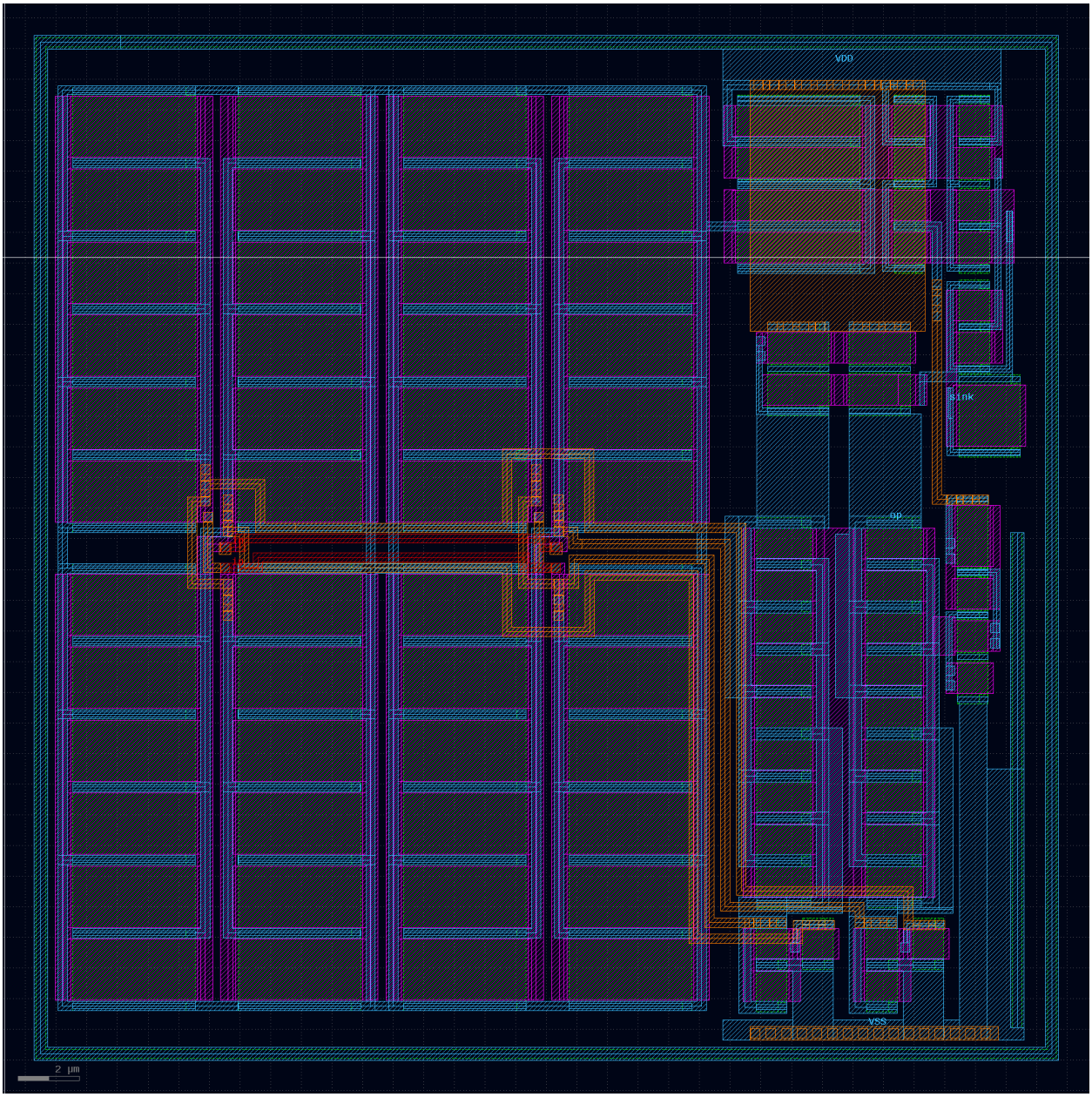
2.1 OTA



2.2 bias generator



2.3 layout



2.4 simulations

using different bias-currents of 1, 3 and 10µA a few simulations are printed into a PDF that allow to see the gain, common-mode-range, bandwidth and a slew-rate:

`PDF with Xyce simulations .ac .dc .trans`

the schematics of this simulations is `Xschem document`

2.5 ETHZ feedback

its a bit stupid to design OTAs that fit in a square, if there is no such space-requirement. the layout should be changed to minimize the conductor-length of the signals between the differential-stage and the current-mirrors.

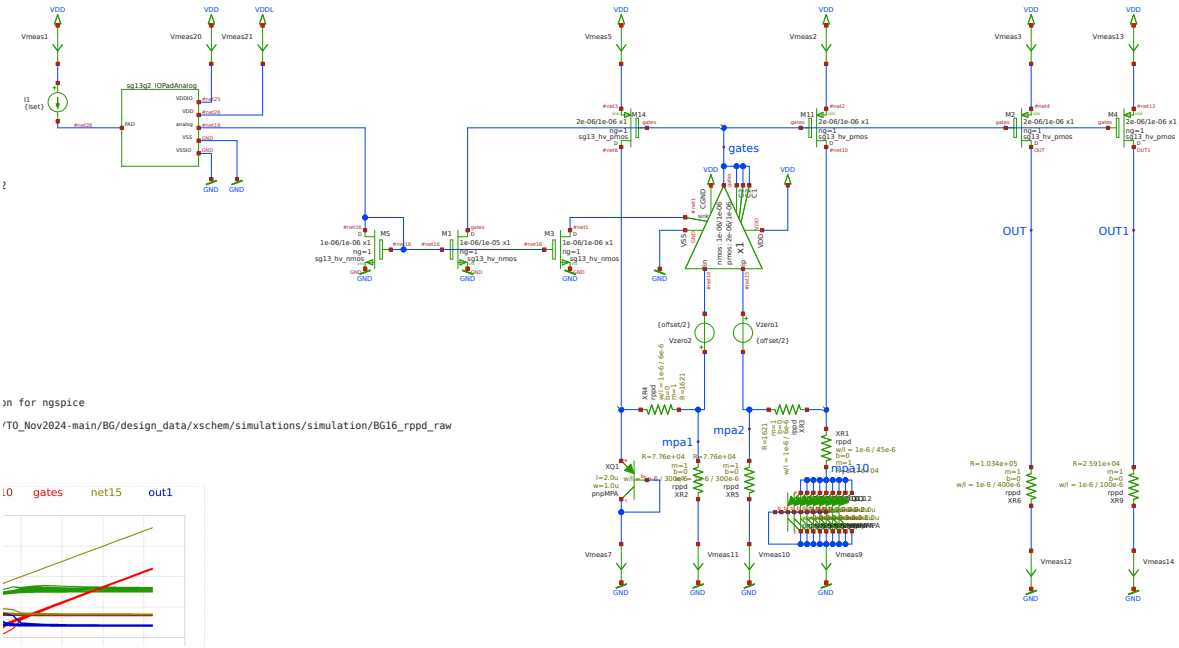
CHAPTER

THREE

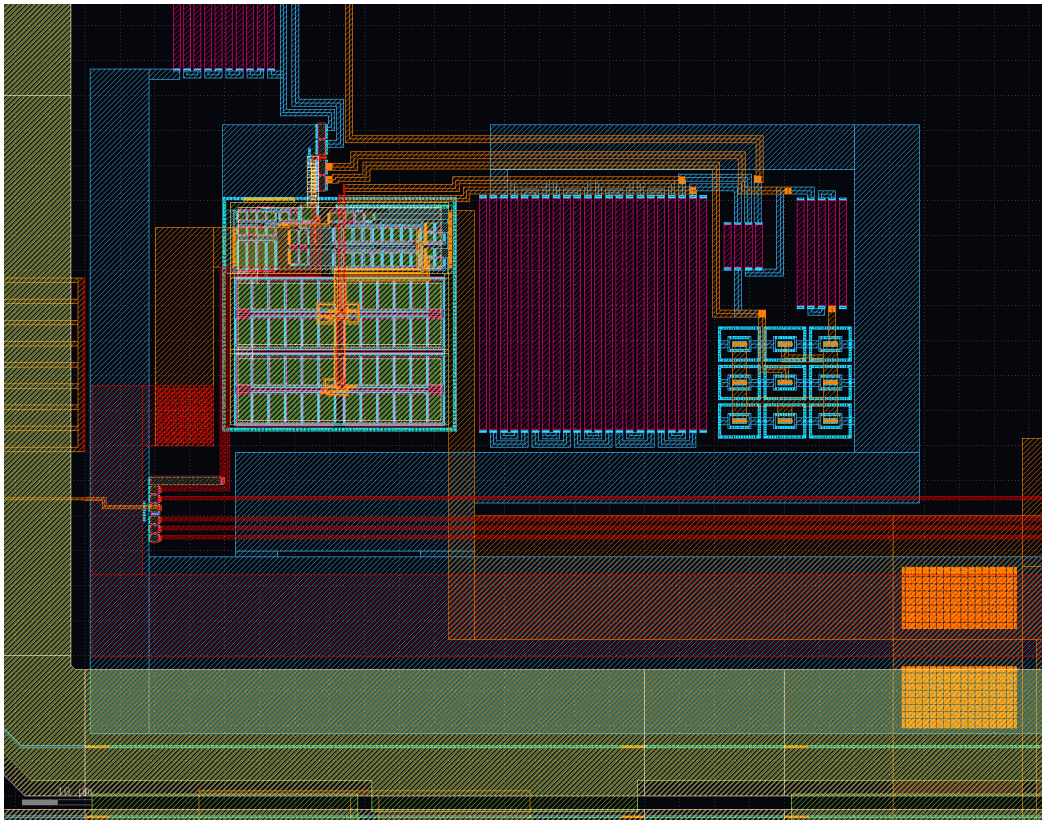
BAND GAP REFERENCE

the shunt-regulator has to limit the supply-voltage to 3.3V. it should be usable to 50mA.

3.1 schematic



3.2 layout



3.3 simulation

PDF with Xyce simulation

3.4 LVS

LVS wasn't working. and there are differences between layout and schematics

CHAPTER

FOUR

VOLTAGE-REGULATORS

4.1 shunt-regulator

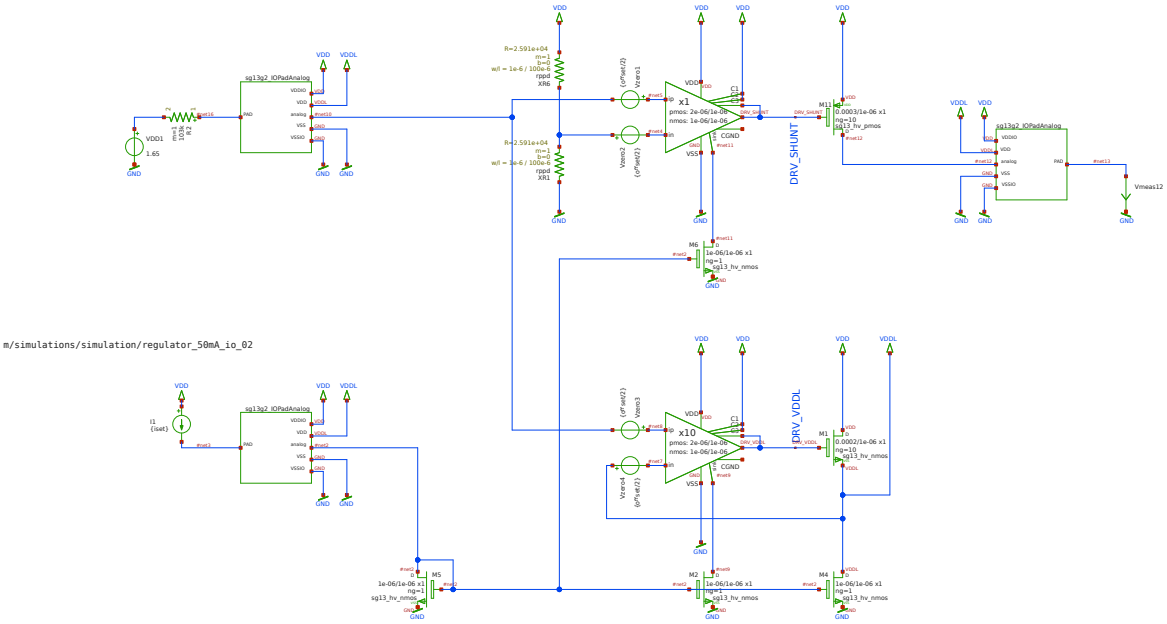
the shunt-regulator has to limit the supply-voltage to 3.3V. it should be usable to 50mA. the regulating current flows thru M11. and to allow this the pin SHUNT_GND needs to be connected to VSS. optional over an current-meter.

in the layout the left/top OTA is used in this circuit.

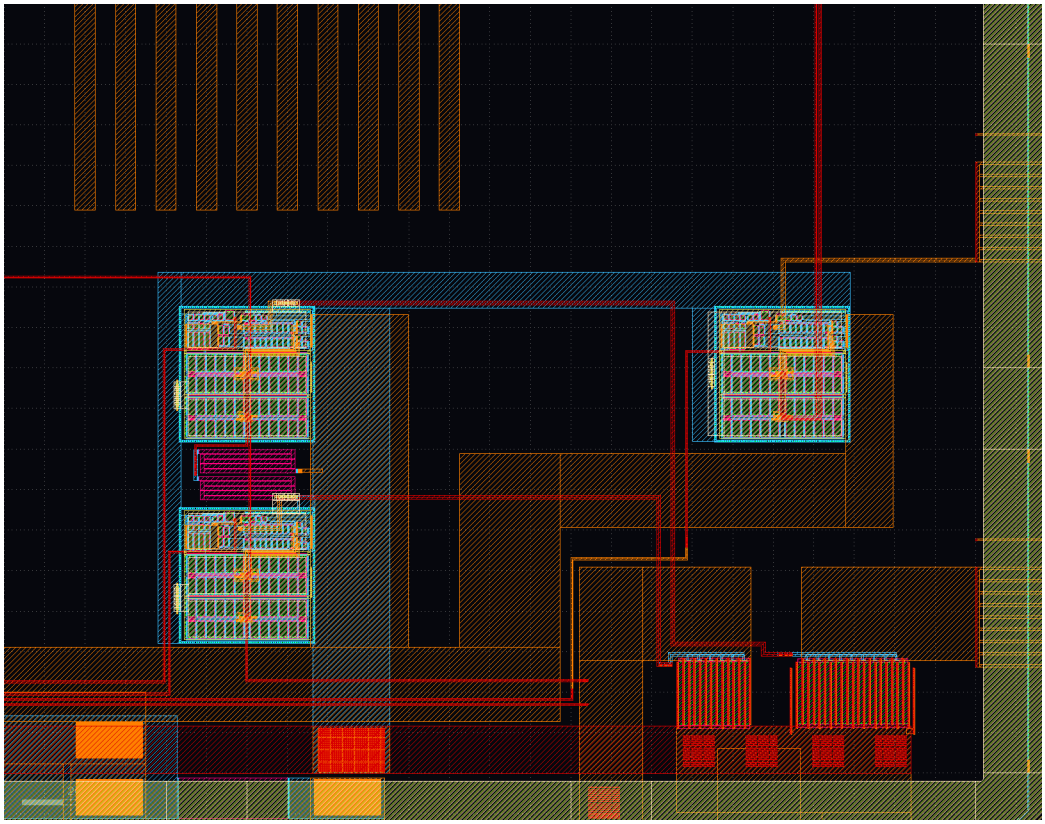
4.2 serial-regulator

the serial regulator should produce 1.8V for low-voltage MOSFETs. the OTA responsible for this regulator is left/bottom in the layout.

4.3 schematic



4.4 layout



4.5 simulations

PDF with Xyce simulation

4.6 LVS

LVS wasn't working

CHAPTER

FIVE

IHPS IO-CELLS

for ESD protection the analog-IO-cells where used. the cells support two voltages. a 3.3V IO and a 1.8V core-voltage.

my problem using the cells was, that the openPDK LVS scripts didn't could verify the .GDS with the provided .CDL. so that simply hope, they are correct used.

one problem i had, using this cells was the space they demand. i was trying to make a minimal chip of about 0.5x1mm. but the filler.py-script wasn't able to produce enough GatPoly-fill to pass the maximum-DRC script.

this IO infrastructure needs at least a 1x1mm chip (according my experience).

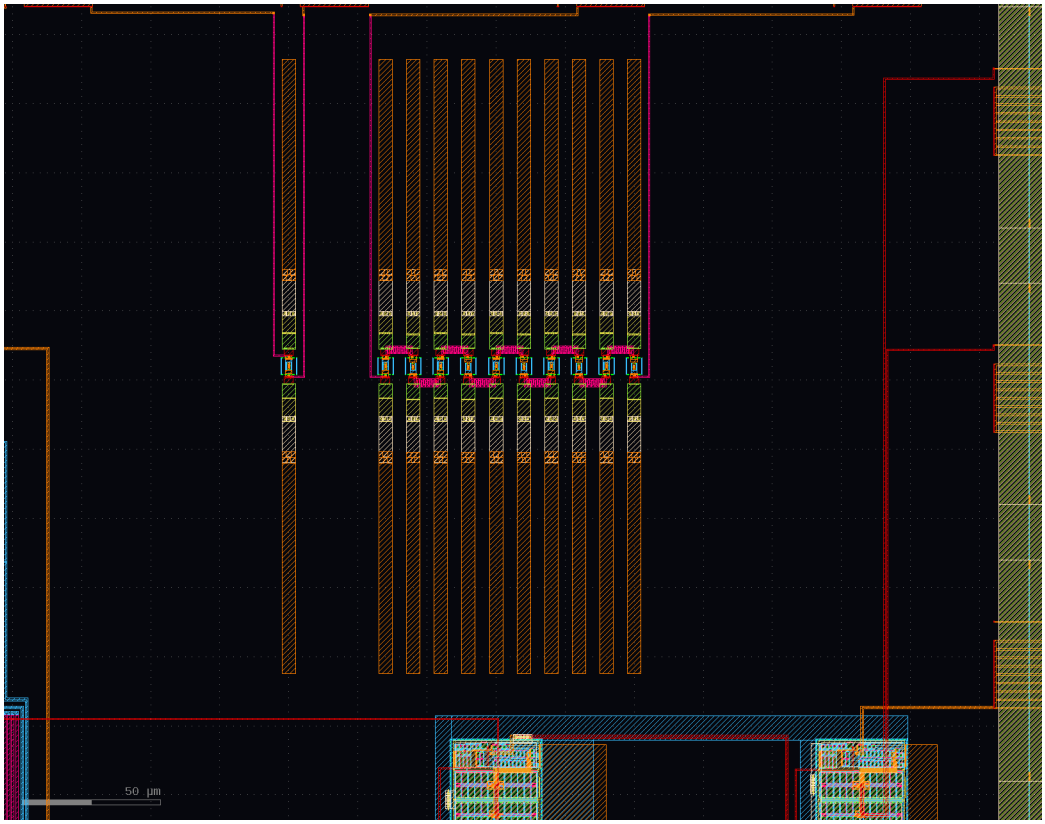
CHAPTER

SIX

MMW DIODE DETECTORS

there are two diode-detector designs to measure if serial circuits of detector diodes will increase the sensitivity of the sensor.

6.1 layout



CHAPTER

SEVEN

EXPERIMENTS

7.1 test schottky diode

to measure the schottky-diode used in the mmW-detectors, a device is connected to bond-pads outside the power-ring.

7.2 fuse

to test the possibility of using fuses to trim band-gap-references and the like a test-structure with a resistor, parallel to a fuse, is connected to two pads outside the power-ring.

CHAPTER

EIGHT

DESIGN DATA AND DESIGN PROCESS DESCRIPTION

8.1 iHP 130nm BiCMOS process sg13g2

the process is useable via iHPs openPDK:

source https://github.com/IHP-GmbH/IHP-Open-PDK

documentation https://ihp-open-pdk-docs.readthedocs.io/en/latest/index.html

open-source runs: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/fast-design-enablement/open-source-pdk

8.2 Xschem schematics:

folder	for
design_data/xschem/cdl	symbols for Xschem schematics
design_data/xschem/OTA	design and simulation of the OTA
design_data/xschem/simulations	simulations of the voltage regulators
design_data/xschem/symbol	symbols for Xschem schematics

8.3 KLayout .GDS:

file	for
design_data/gds/FMD_QNC_mmW_detector.gds.gz	layout of the chip

CHAPTER

NINE

VALIDATION SOMETIME IN THE FARFAR FUTURE

i cant wait…

Contents

CHAPTER

TEN

BACKGROUND

to make first steps using iHPs openPDK, Xschem and KLayout designing a OTA was obvious. this part is DRC and LVS clean, verified also using commercial tools.

but that's also the only clean part on this chip from my perspective. its highly likely that the IO cells are perfect, but i couldn't verify this my self. the opensource LVS didn't was ready, and i hadn't the time to verify any other part then the OTA via LVS.

CHAPTER

ELEVEN

THE SG13G2 PROCESS

there are two kinds of GateOxyde: thick for high-voltage like 3.3V circuits and standard for 1.2..1.8V circuits. there are three different SiGe BjTs, but all are NPNs. while the Si-parasitic transistors are only PNP.