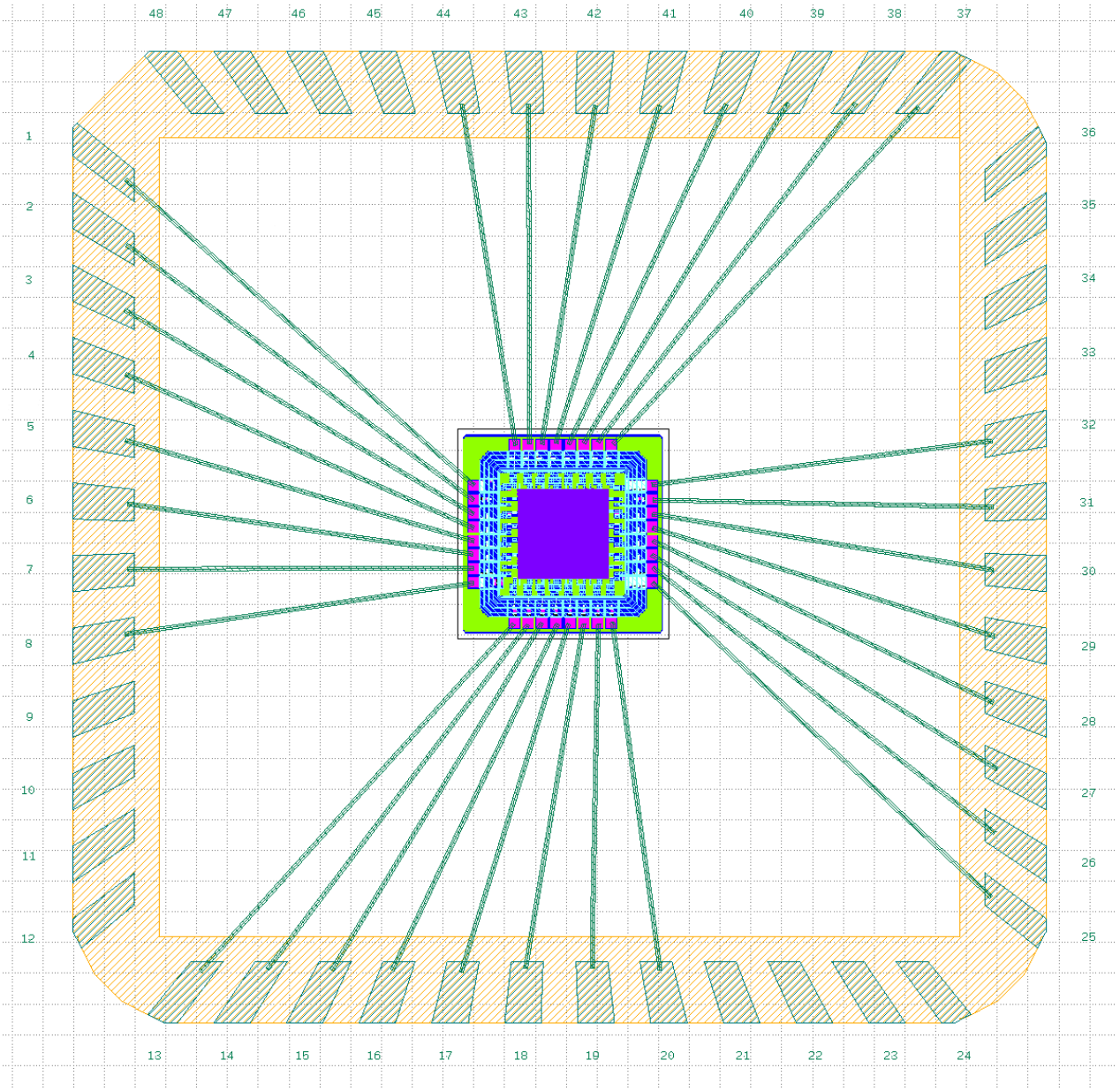
MARTIn Bonding Plan



LEFT SIDE

- 1: IOVDD
- 2: lfsr_out
- 3: shreg_in
- 4: aux_enable
- 5: wr_enable
- 6: rst
- 7: clk
- 8: VDD

BOTTOM SIDE

- 13: data_out[0]
- 14: data_out[1]
- 15: data_out[2]
- 16: data_out[3]
- 17: data_out[4]
- 18: data_out[5]
- 19: data_out[6]
- 20: data_out[7]

RIGHT SIDE

- 25: VSS
- 26: reg_addr[0]
- 27: reg_addr[1]
- 28: reg_addr[2]
- 29: out_select[0]
- 30: out_select[1]
- 31: shreg_out
- 32: IOVSS

TOP SIDE

- 37: data_in[0]
- 38: data_in[1]
- 39: data_in[2]
- 40: data_in[3]
- 41: data_in[4]
- 42: data_in[5]
- 43: data_in[6]
- 44: data_in[7]