**Indian Institute of Information Technology (IIIT) Chittoor, Sricity Questionnaire for BTP-Progress Evaluation**

**Wednesdays, 3:30 – 5pm**

**Spring 2016**

1. Describe what you have done in the last 3 weeks.

* Familiarization with Verilog HDL language.
* Familiarization with Xilinx Software
* Designing of digital circuits using structural modelling
* Design of ALU

2. How many times did you meet / talk with your faculty / guide?

* 1-2 times.

3. How many papers / articles / technical materials have you read in the last 3 weeks?

* Following the video lectures on Digital VLSI System Design by Prof. S. Srinivasan and Dr. S. Ramachandran (IIT Madras)
* Digital Logic and Design (Morris mano)
* Verilog Tutorial PDF’s
* Prototype design for a processor and microprocessor design papers

4. Provide a brief summary of your learning?

* I am able to successfully write the program for any digital circuits given and currently working on a prototype design for a 4-bit processor using verilog HDL in xilinx

5. What development / programming / practical activity did you do in the last 3 weeks?

Wrote program and simulated successfully for the following:-

* + - Simple logic gates
    - Adder (2-bit, 4-bit, user defined number of bits)
    - Multiplexer and demultiplexer
    - Encoder and decoder
    - Flip-Flop (using structural modelling)
    - Instruction Decoder(ongoing)
    - RAM
    - ALU

6. How close/far are you from the milestone set by your Guide?

* + There is no such milestone set by my Instructor

7. What specific challenges are you facing/you faced in the last 3 weeks?

* + Working with Xilinx
  + Instruction decoder architecture of a processor

8. Propose your plan for the next 3 weeks; as agreed with your supervisor. It would be verified in the next round (Q1).

Exploring the area of Digital VLSI design (RTL design) and trying to model a 4-bit processor.