Deep Learning – Final Project – Group 7

WaferMap Defect Pattern Recognition using improved DCN

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Abstract - WaferMap defect pattern recognition is a critical task in semiconductor manufacturing, essential for maintaining high yield and quality control. This paper presents a novel approach using an improved Deep Convolutional Network (DCN) to accurately identify and classify defect patterns on wafer maps. Utilizing the MixedWM38 dataset, which encompasses a diverse range of defect patterns, our method incorporates deeper network layers, optimized learning algorithms, and enhanced data augmentation strategies. Compared to the state-of-the-art WaferSegClassNet from Nag et al. (2022) [1], which achieves an accuracy of 98.2% with a training time of approximately 150 minutes over 50 epochs, our model attains a comparable validation accuracy of 98.16% in significantly less time—around 10 minutes over 22 epochs. Additionally, our approach outperforms previous DCN-based methods, such as the Deformable Convolutional Networks by Wang et al. (2020) [2], which reported an accuracy of 93.20%. While our model performs slightly below the latest SOTA in terms of accuracy, it excels in training efficiency and speed. These results highlight the effectiveness of our approach in enhancing defect detection processes, contributing to improved manufacturing efficiency and reduced costs. The source code can be obtained from github: ***https://github.com/IIRchen/Wafer_classification.git***

I. INTRODUCTION

WaferMap defect pattern recognition is a pivotal aspect of quality control in semiconductor manufacturing, where maintaining high yield and minimizing production costs are of utmost importance. The detection and classification of defect patterns on wafer maps help in identifying manufacturing issues and implementing corrective actions, thus ensuring the reliability and performance of semiconductor devices.

In recent years, machine learning and deep learning techniques have revolutionized defect pattern recognition, offering automated, accurate, and efficient solutions compared to traditional manual inspection methods. Among these techniques, Convolutional Neural Networks (CNNs) have gained prominence due to their ability to capture spatial hierarchies in image data. However, the complex and variable nature of defect patterns poses significant challenges, necessitating continuous advancements in model architectures and training methodologies. The state-of-the-art (SOTA) model, WaferSegClassNet, introduced by Nag et al. (2022), has set a high benchmark in this field, achieving an impressive accuracy of 98.2% on the MixedWM38 dataset. Despite its high accuracy, WaferSegClassNet requires substantial computational resources and training time, approximately 150 minutes over 50 epochs. Such requirements can be a bottleneck in a fast-paced manufacturing environment where rapid model training and deployment are crucial.

In this study, we propose an improved Deep Convolutional Network (DCN) designed to enhance training efficiency without significantly compromising accuracy. Our model achieves a validation accuracy of 98.16%, closely aligning with the SOTA performance, but with a drastically reduced training time of around 10 minutes over 22 epochs. This efficiency gain is achieved through deeper network layers, optimized learning algorithms, and advanced data augmentation strategies. Moreover, our model surpasses previous DCN-based methods, such as the Deformable Convolutional Networks by Wang et al. (2020), which reported an accuracy of 93.20%. This demonstrates the significant progress made in defect pattern recognition through our approach.

In addition to the primary model, we introduce several variations of our improved DCN. These variations explore different architectural configurations and training techniques to optimize performance further. One of these variations achieves the notable validation accuracy of 98.16%, exemplifying the robustness and adaptability of our approach. The following sections of this paper will delve into the details of our methodology, including the architectural innovations and training optimizations implemented. We will also present a comprehensive evaluation of our model's performance on the MixedWM38 dataset, highlighting its strengths and potential areas for improvement. Furthermore, we will discuss the different versions of our model, examining their performance metrics and identifying the optimal configurations for various scenarios. Finally, we will discuss the broader implications of our findings for semiconductor manufacturing and suggest possible directions for future research.

II. RELATED WORKS

In the evolving field of semiconductor manufacturing, defect pattern recognition and classification have become increasingly vital due to the growing complexity and integration density of semiconductor wafers. The traditional manual inspection methods are becoming cost-prohibitive and less feasible, sparking a shift towards automated solutions leveraging artificial intelligence (AI) and computer vision. This section reviews prominent contributions in the realm of AI-driven wafer defect analysis, focusing particularly on recent advancements in classification and segmentation techniques.

WaferSegClassNet: A Light-weight Network for Classification and Segmentation of Semiconductor Wafer Defects

A significant advancement is presented by Nag et al. in their development of the WaferSegClassNet (WSCN), a novel AI model designed to address the limitations of previous approaches that often suffered from low accuracy and the inefficiency of requiring multiple models for different tasks. The WSCN, detailed in their work, employs a lightweight encoder-decoder architecture that uniquely enables simultaneous classification and segmentation of both single and mixed-type defects on wafers. This network leverages a "shared encoder" strategy for both tasks, allowing it to be trained end-to-end efficiently. Notably, the model utilizes N-pair contrastive loss for pretraining the encoder, enhancing the latent space representation, followed by BCE-Dice loss for segmentation and categorical cross-entropy for classification. The efficacy of WSCN is demonstrated on the MixedWM38 dataset, where it achieves an impressive classification accuracy of 98.2% and a dice coefficient of 0.9999, marking it as a breakthrough in both performance and computational efficiency, with a model size of just 0.51MB and requiring significantly fewer computational resources (0.2M FLOPS) and training epochs (50 compared to 4,000 in prior works). This represents a substantial stride forward in developing scalable, effective solutions for wafer defect analysis. These developments underscore a pivotal shift towards more integrated and efficient models in semiconductor defect detection, highlighting the critical role of innovative AI techniques in enhancing the accuracy and operational efficiency of these systems. As the field progresses, the emphasis remains on refining these models to handle the increasing complexity and variety of wafer defects more effectively.

Deformable Convolutional Networks for Efficient Mixed-Type Wafer Defect Pattern Recognition

Wang et al. introduced an innovative approach to addressing mixed-type defect pattern recognition (DPR) in semiconductor wafers through their work on Deformable Convolutional Networks (DC-Net). The identification of mixed-type defects—where multiple defect characteristics such as type, position, angle, and number are intermingled—is notably more challenging than single-type defects due to the variability and complexity of the defect combinations. The DC-Net model devised by Wang et al. significantly advances the field by integrating a deformable convolutional unit specifically designed to adeptly sample and extract high-quality features from such complex defect configurations on wafer maps. This model includes a multi-label output layer enhanced with a one-hot encoding mechanism, which efficiently decomposes and categorizes the mixed features into distinct defect types. The empirical results from Wang et al.'s study illustrate that DC-Net not only surpasses traditional models but also improves upon other contemporary deep learning approaches in detecting and classifying mixed-type defects. Furthermore, the model provides valuable interpretive analysis, pinpointing defect areas with high precision even in the presence of noise, thereby offering substantial benefits for complex DPR tasks. This contribution is particularly relevant for enhancing root cause analysis and subsequently improving yield in wafer fabrication processes.

III. DATA

This study utilizes the MixedWM38 dataset (source: https://www.kaggle.com/datasets/co1d7era/mixedtype-wafer-defect-datasets), a comprehensive collection specifically designed for the research and development of defect detection models in semiconductor manufacturing. It consists of 38,015 images, with images of size 52 x 52 and class information as one hot encoded array in numpy format, categorized into 38 distinct defect patterns. These patterns are methodically divided into one normal class, eight single defect types, and 29 mixed defect types, offering a comprehensive overview of possible defect scenarios on semiconductor wafers.

The categorization of the dataset is particularly detailed (as Fig. 1 and Table 1), enhancing its utility for more nuanced analyses:

- Single Type: Represents the **normal + eight single defect** types individually.
- 2 Mixed-Type: Contains **13 combinations**, each featuring a blend of two different defect types.
- 3 Mixed-Type: Contains **12 combinations**, each merging three distinct defect types.
- 4 Mixed-Type: Contains **4 combinations**, each merging four different defect types.

Fig. 1: 38 defect patterns in MixedWM38 dataset

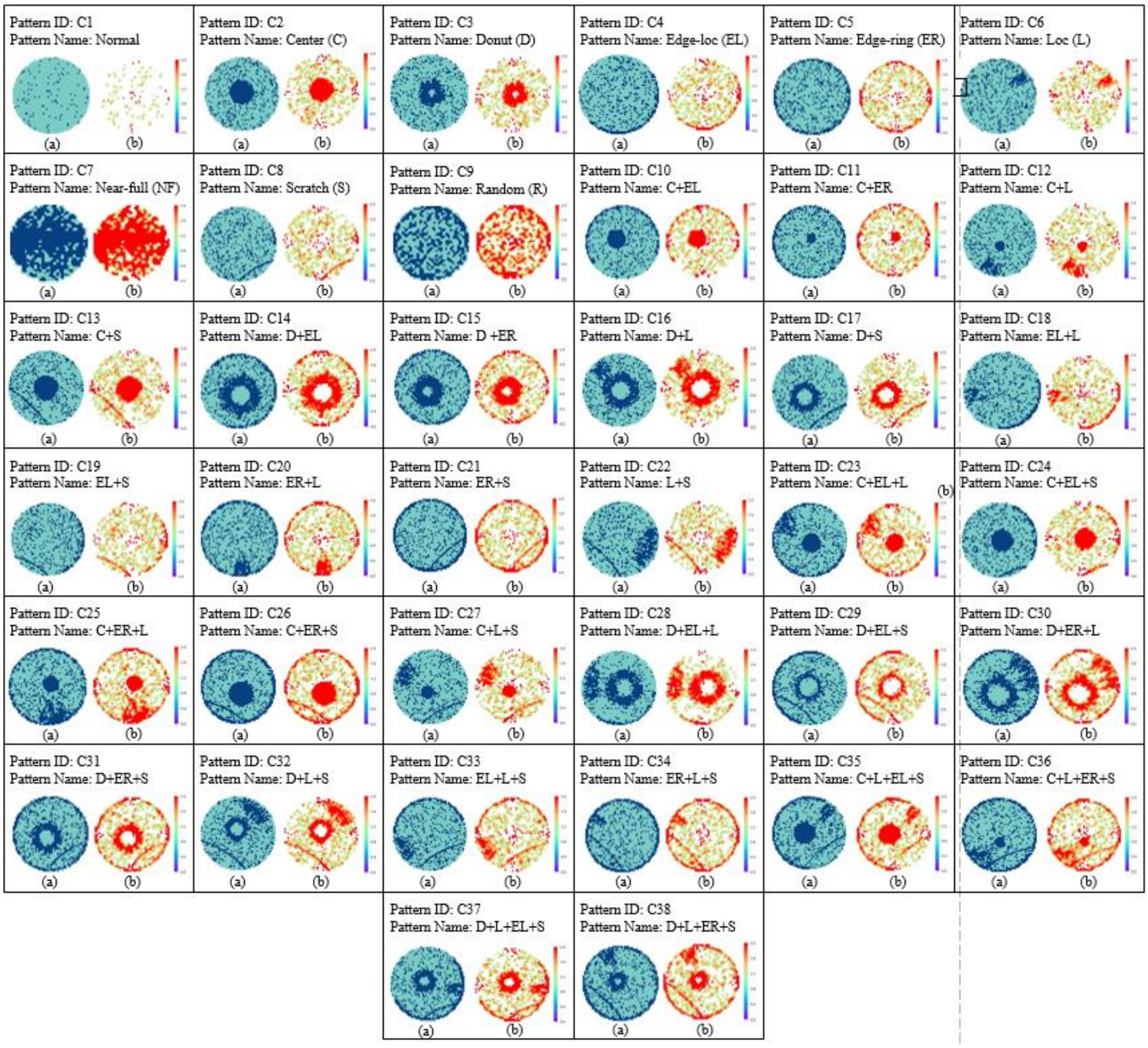


Table 1: 38 defect patterns in MixedWM38 dataset

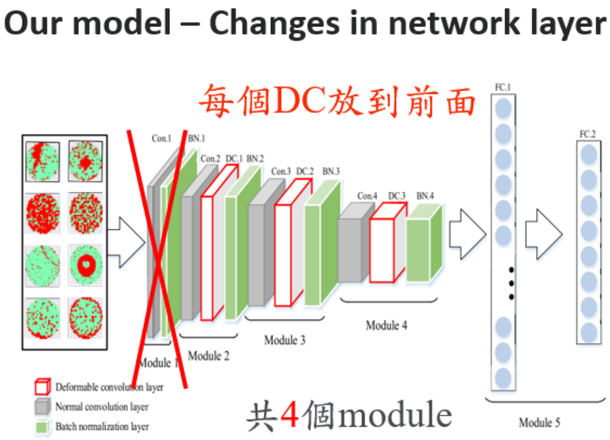
No.	Single Defect	No.	Two-mixed Defect	No.	Three-mixed Defect	No.	Four-mixed Defect
1	Normal	10	C + EL	23	C + EL + L	35	C + L + EL +S
2	Center (C)	11	C + ER	24	C +EL + S	36	C + L + ER +S
3	Donut (D)	12	C + L	25	C + ER +L	37	D + L + EL +S
4	edgeLoc (EL)	13	C + S	26	C + ER + S	38	D + L + ER +S
5	edgeRing (ER)	14	D + EL	27	C + L + S		
6	Loc (L)	15	D + L	28	D + EL +L		
7	Nearful (NF)	16	ER + L	29	D + EL + S		
8	Scratch (S)	17	EL + S	30	D + L + S		
9	Random (R)	18	ER + S	31	D + ER + L		
		19	L + S	32	D +ER + S		
		20	D + ER	33	EL + L + S		
		21	D + S	34	ER + L + S		
		22	EL + L				

In our study, we utilize the MixedWM38 dataset as the foundational data for training and evaluating our enhanced Deep Convolutional Network (DCN). This dataset is processed in two primary ways to optimize the performance and robustness of our model: using original data and applying various filtering methods. They enable a comprehensive evaluation of the DCN's performance under varying input conditions, showcasing its effectiveness in diverse operational scenarios. The processed data ensures that our model not only learns to identify and classify a wide range of defect types accurately but also becomes resilient to potential variations and imperfections in real-world manufacturing processes.

IV. METHODOLOGY

In our study, we significantly revised the Deformable Convolutional Network (DCN) architecture originally proposed by Wang et al. in 2020 [2], leading to the development of model V1, which also utilized the upgraded version of DCNv2. This enhanced model targets increased efficiency in detecting mixed-type wafer defect patterns. Key architectural modifications included the removal of the first module, reducing the network from five to four modules, thereby streamlining the model to decrease computational demand without compromising its learning capabilities. We also changed the offset layer at the start of the convolution sequence (previously after the convolution), which dynamically adjusts the receptive field to better capture the spatial variability in defects (Fig. 2).

Fig 2: Changes in network layer



Using this concept as our **V1 model**, we extended our research to develop six additional versions of the model, resulting in a comprehensive suite of seven versions. Each version was crafted to test various modifications and enhancements aimed at optimizing performance and applicability in real-world settings. Below, I'll outline the methodology and specific characteristics of each version, as summarized in Table 2, to give a clearer picture of our iterative development and testing approach.

Table 2: Model Version and Contents

Model Version	Model Contents	Activation Function	Epochs
V1	Modify the model from Wang et al. 2020	relu	10
V2	Modify Abnormal Values + V1	gelu	30
V3	Denoise images + V2	gelu	30
V4	Data augmentation (vertical & horizontal flip) + V2	gelu	30
V5	V1 + V3 (no data augmentation)	gelu	30
V6	V1 + V3 (data augmentation)	gelu	30
V7	3 channels (original + CCA + Filter)	gelu	30

Version 2: Addressing Data Anomalies in MixedWM38

In developing Version 2, we identified anomalies within the MixedWM38 dataset; specifically, it contained unexpected values of 3, despite being expected to only include values of 0, 1, or 2. Version 2 was therefore designed with a focus on resolving this issue to ensure data consistency and reliability in our model training process.

Version 3: Advanced Denoising Techniques for Preprocessing

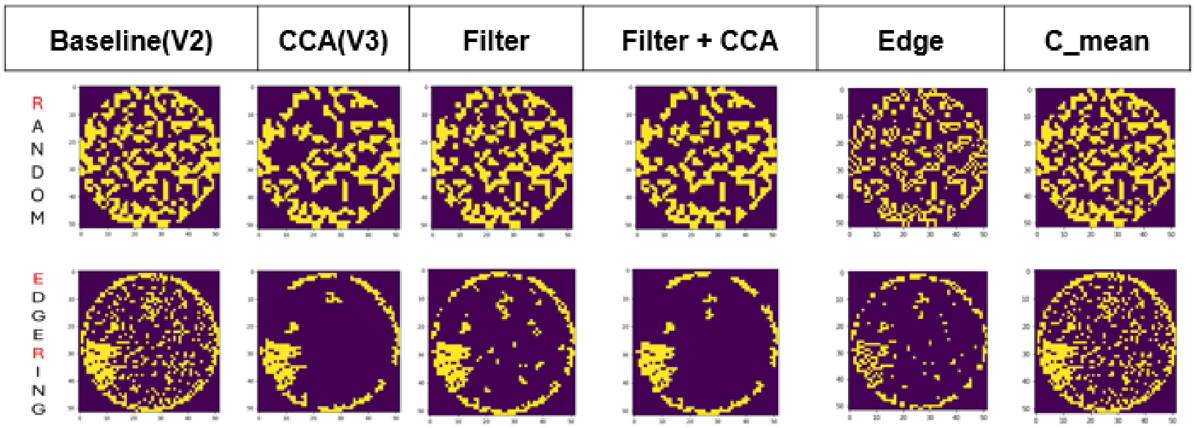
In the development of Version 3, we focused on enhancing the preprocessing stage of our model by implementing various denoising methods. These techniques were specifically chosen to improve image quality and clarity, which are critical for accurate defect detection in wafer maps. The denoising methods tested in Version 3 included:

- **Connected Component Analysis (CCA):** This method was applied with a threshold greater than 10 to isolate and analyse connected regions in the images, helping to reduce noise by focusing on significant components.
- **Matrix Filtering:** We utilized a 3x3 matrix filter with a threshold greater than 3. This approach helped in smoothing the image while preserving essential features necessary for accurate defect recognition.

- **Combined Filtering:** This method integrated the 3x3 matrix filter with a threshold greater than 3 and CCA with a threshold greater than 5. The combination aimed to leverage the strengths of both techniques to achieve a more refined denoising effect.
- **Edge Filtering using Laplace:** The Laplacian filter was employed to enhance the edges within the images. This edge enhancement is crucial for detecting the boundaries and extents of defects accurately.
- **C_mean Filtering:** We implemented C_mean filtering with a threshold greater than 0.5. This technique is effective in reducing noise by replacing each pixel value with the mean of the neighboring pixel values, depending on the defined threshold.

These denoising strategies were systematically evaluated to determine their effectiveness in improving the quality of the input images for our model. By preprocessing the images with these advanced denoising methods, Version 3 aims to enhance the model's ability to detect and classify defects more accurately and reliably. Fig. 3 shows an example of results from above mentioned denoising methods.

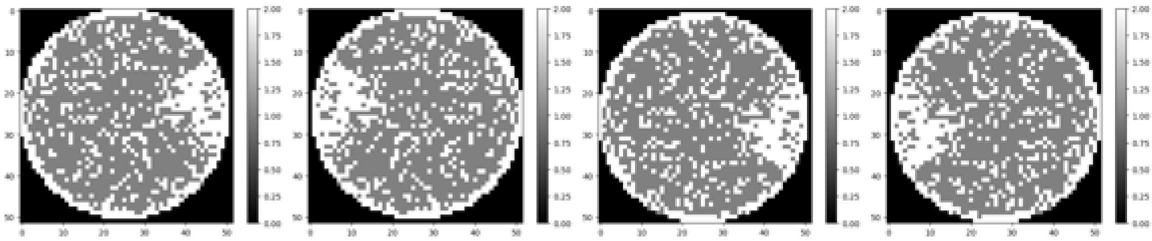
Fig 3: Advanced Denoising Techniques for Preprocessing



Version 4: Data Augmentation for Enhanced Model Robustness

In Version 4 of our model development, we implemented data augmentation techniques to enhance the robustness and generalizability of our model. Specifically, we applied vertical and horizontal flips to the original images in the MixedWM38 dataset (Fig. 4). By augmenting the data in these ways, Version 4 aims to train a model that is more adaptable and capable of accurately identifying defects across various orientations and configurations. This is particularly valuable in semiconductor manufacturing, where defects can appear in any orientation due to the diverse nature of the production processes.

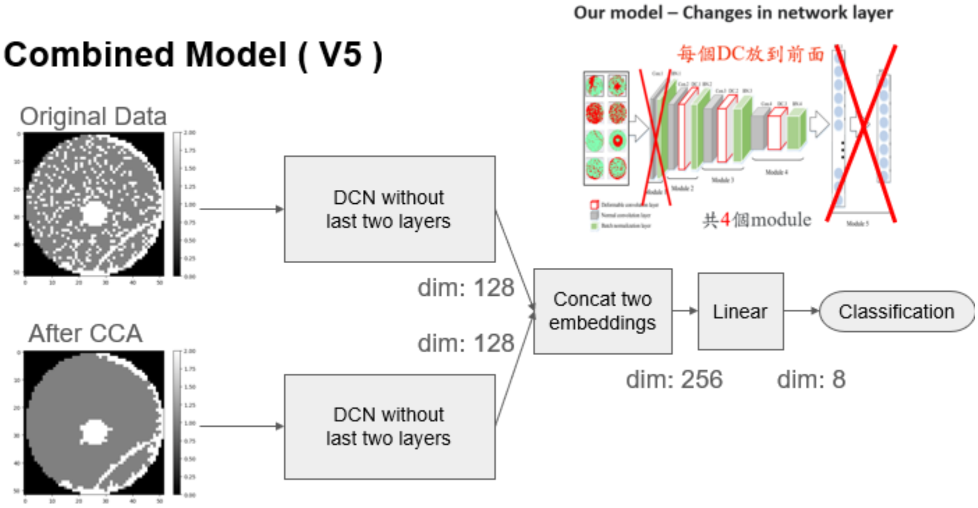
Fig 4: Data Augmentation for Enhanced Model Robustness



Version 5: Combined Model Utilizing CCA and Dual DCN Streams

Version 5 of our model development represents a significant innovation through the integration of a dual-stream Deformable Convolutional Network (DCN) architecture, enhanced with pre-processed inputs using Connected Component Analysis (CCA). The model architecture includes two parallel DCN streams, each processing different versions of the data: the original wafer map images and the CCA-processed images (Fig. 5). Both streams utilize a DCN architecture but with the last two layers removed to adapt the network for feature extraction rather than full end-to-end classification. This combined model approach in Version 5 is designed to capitalize on the strengths of both raw and pre-processed data, providing a more comprehensive understanding of the defect patterns. By merging features from both the original and CCA-processed streams, the model aims to achieve higher accuracy and reliability in defect detection, particularly in environments with complex defect configurations.

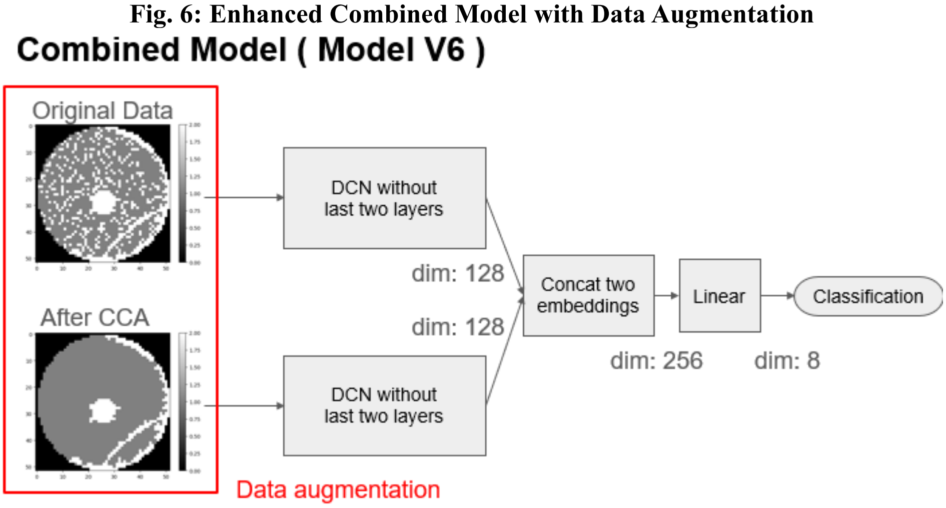
Fig 5: Combined Model Utilizing CCA and Dual DCN Streams



Version 6: Enhanced Combined Model with Data Augmentation

Version 6 builds upon the dual-stream architecture introduced in Version 5, enhancing its capability with the integration of data augmentation techniques (Fig. 6). This version aims to further improve the robustness and generalization of the model by introducing variations in the training data, which help the model adapt to diverse defect presentations in semiconductor wafer maps. With the addition of data augmentation, Version 6 not only capitalizes on the combined strengths of processing both raw and enhanced images but also trains the network to be resilient to variations in defect appearance. This approach is particularly beneficial in semiconductor manufacturing, where defects can vary widely in appearance due to differences in production conditions.

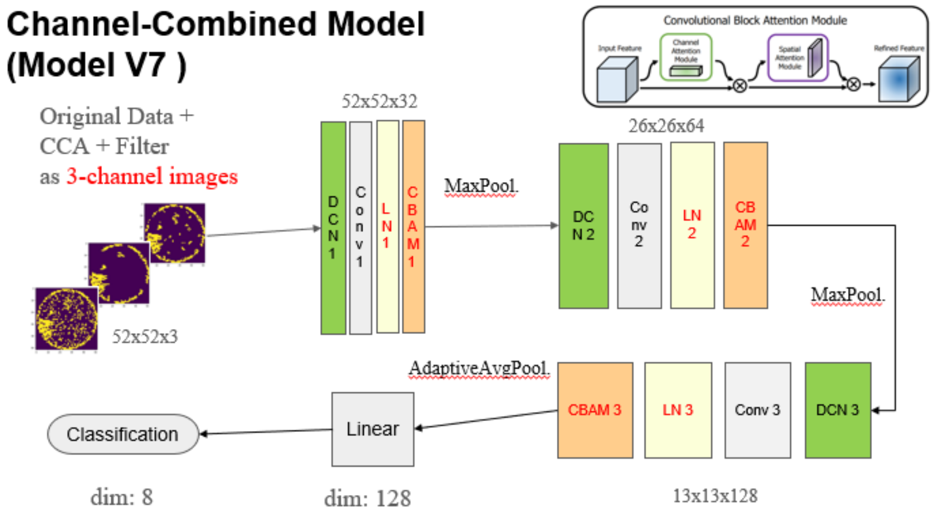
Fig. 6: Enhanced Combined Model with Data Augmentation



Version 7: Channel-Combined Model with Enhanced Feature Integration

In this version, the model processes a composite image comprising three distinct channels, each derived from the original wafer map data but treated differently to enhance feature detection: one channel presents the raw data, another applies Connected Component Analysis (CCA), and the third channel incorporates additional filtering methods. This diversified input approach is engineered to capture a wider range of data features, significantly enhancing the model's ability to detect various defect characteristics. Furthermore, techniques like Layer Normalization (LN) and Convolutional Block Attention Modules (CBAM) are strategically placed at the end of each module (Fig. 7). These attention mechanisms are critical for highlighting the most pertinent features within the input data, refining the process of feature extraction and bolstering the accuracy of the classification results. Version 7's channel-combined strategy leverages multiple data representations to maximize the extraction and utilization of informative features from the wafer images. By integrating advanced attention mechanisms and a multi-layered convolutional approach, this version aims to achieve superior accuracy in defect detection, addressing complex and subtle defect patterns that might be missed by less sophisticated models.

Fig. 7: Channel-Combined Model with Enhanced Feature Integration



V. EXPERIMENTAL RESULTS

In this section, we will detail the experimental outcomes beginning with the validation accuracies for Version 1 throughout Version 7 of our model (Table 3). This will be followed by an analysis of the results from the various denoising methods employed (Table 4). Lastly, we will discuss the accuracy, precision, and recall metrics, providing a class-wise breakdown of the performance results (Table 5) with #PARAMS and FLOPS (Table 6) from SOTA model compared with our V5, V6 and V7 of our model.

Table 3: Validation Accuracy Across Different Model Versions

Model Version	V1	V2	V3	V4	V5	V6	V7
Validation Accuracy	96.60	97.78	94.00	97.92	97.65	**98.17**	98.15

The experimental results from our series of model iterations demonstrate a progressive refinement in semiconductor defect detection capabilities. Starting with a strong baseline in Version 1, we saw peak performance in Version 6, which achieved a validation accuracy of 98.17% due to its dual-stream architecture and sophisticated data augmentation techniques. Version 7 closely followed, showing the benefit of integrating multi-channel inputs with advanced attention mechanisms.

Table 4: Various Denoising Techniques and Their Corresponding Accuracies

Techniques	Original Data	CCA	Filter	Filter + CCA	Edge Filtering	C_mean filtering
Validation Accuracy	**97.78**	94.00	96.66	95.34	95.55	95.17

Table 4 presents the validation accuracies for various denoising techniques applied within our model development process. Using the original data, the model achieved a validation accuracy of 97.78%. Techniques such as Connected Component Analysis (CCA) and simple filtering resulted in accuracies of 94.00% and 96.66% respectively. Combining filtering with CCA slightly decreased the accuracy to 95.34%. More complex methods like edge filtering and C-mean filtering showed accuracies of 95.55% and 95.17% respectively. This data suggests that while some denoising techniques, like simple filtering, significantly enhance model performance, more complex methods might not always lead to higher accuracy, indicating a trade-off between the sophistication of the method and its practical utility in enhancing model performance.

In our study, we conducted a comparative analysis of the classification performance between our model versions (V5, V6, and V7) and the state-of-the-art WaferSegClassNet (WSCN). This comparison was detailed through a class-wise breakdown, providing a granular view of how each model version performs across different defect types specified in the dataset. This approach allowed us to assess the strengths and weaknesses of our models in relation to the leading benchmark model in the field, offering insights into specific areas where our models excel or may require further improvement. The class-wise performance metrics, such as precision, recall, and overall accuracy, were key in determining the relative effectiveness of our models compared to WSCN, highlighting the impact of various architectural and processing enhancements we implemented in the later versions. This was shown in below Table 5.

Table 5: Class-wise Accuracy Results

Class	Accuracy				Precision				Recall			
	WSCN	V5	V6	V7	WSCN	V5	V6	V7	WSCN	V5	V6	V7
1	100	100	100	100	100	98	99	99	100	100	100	100
2	100	100	100	99.10	99	99	99	98	100	100	100	99
3	100	99.45	100	100	96	98	97	97	100	99	100	100
4	97	96.52	99.5	97.98	98	99	99	99	98	97	99	98
5	99	99.11	98.5	98.79	97	97	98	98	99	99	98	99
6	99	98.96	99	97.93	99	100	98	99	99	99	99	98
7	100	85.71	100	100	92	100	100	100	100	89	100	100
8	99	98.26	99.5	97.13	97	97	99	98	100	98	99	97
9	98	100	99.42	98.25	100	98	100	100	98	100	99	96
10	98	98.08	98.5	97.66	98	97	98	99	99	98	98	98
11	100	100	99.5	100	99	98	99	98	100	100	99	100
12	99	98.94	99	97.88	99	97	97	97	100	99	99	98
13	99	100	99	98.51	98	97	98	99	100	100	99	99
14	94	97.52	99.5	97.21	100	99	98	99	95	98	99	97
15	99	99.5	97.5	100	98	99	97	97	99	100	97	100
16	95	98.85	99	96.55	100	97	98	98	95	99	99	97
17	100	98.63	98	100	96	98	98	98	100	99	98	100
18	99	98.93	98.5	98.97	99	96	97	96	100	99	98	99
19	97	96.74	99.5	98.97	99	99	100	98	98	97	99	99
20	96	96.61	98	99.53	99	98	98	99	96	96	98	100
21	100	99	100	99.56	98	97	99	99	100	99	100	100
22	97	97.98	97	96.86	99	98	98	95	97	98	97	97
23	97	93.88	95	97.51	97	98	96	98	97	94	95	98
24	99	98.56	99	99.48	99	99	99	99	99	99	99	99
25	97	97.45	96.98	98.48	98	96	97	97	98	97	96	98
26	100	99.52	99.5	100	99	97	98	98	100	100	99	100
27	97	95.50	96	97.01	99	99	99	97	97	95	96	97
28	97	99.09	99	98.54	95	98	99	97	97	99	99	99
29	96	98.99	94.5	97.60	97	98	96	98	97	99	94	98
30	100	100	97.5	99.48	94	100	98	100	100	100	97	99
31	98	99.07	98	98.44	98	97	96	97	99	99	98	98
32	97	97	97	96.19	98	98	98	99	97	97	97	96
33	96	96.46	95.5	94.37	100	99	99	99	96	96	95	94
34	97	97.19	97	98.99	97	98	99	98	98	97	97	99
35	94	93.75	96	95.05	100	97	98	98	95	94	96	95
36	97	95.67	98	96.79	98	98	98	99	98	96	98	97
37	95	93.58	94.5	95.81	99	99	100	99	95	94	94	96
38	95	97.12	99	97.95	99	98	99	99	95	97	99	98
AVG (1 Defect)	99.00	97.55	99.54	98.64	97.25	98.44	98.78	99.33	99.33	97.89	99.33	98.44
AVG (2 Defect)	97.92	98.52	98.69	98.61	98.62	97.69	98.07	97.53	98.38	98.61	98.46	98.69
AVG (3 Defect)	97.58	97.73	97.08	97.41	97.58	98.08	97.83	97.25	97.92	97.67	96.83	97.25
AVG (4 Defect)	95.25	95.03	96.88	94.39	99.00	98.00	98.75	98.25	95.75	95.25	96.75	94.00
AVG (All Defect)	98.20	97.65	98.17	98.15	98.08	98.03	98.24	98.21	98.18	97.79	97.97	98.21

In the table, blue-highlighted numbers indicate classes where our models outperformed the benchmark, while a blue background signifies the highest accuracy achieved in that class by any model, which may include multiple top performers. The comparative analysis between our models (V5, V6, V7) and the state-of-the-art WaferSegClassNet (WSCN) reveals detailed insights into class-wise performance, highlighting areas where our models either matched or surpassed the benchmark. Notably, our models demonstrated superior accuracy in several classes. For instance, in classes 2, 7, 10, and 26, our model V6 achieved the highest accuracies of 100%, 100%, 99.42%, and 100% respectively, showcasing its robustness in identifying specific defect types. Additionally, in class 30, model V7 excelled with a leading accuracy of 99.48%. These results underscore the effectiveness of the architectural and processing enhancements incorporated into models V6 and V7, particularly in their ability to outperform WSCN in detecting and classifying complex defect patterns across various classes, confirming the success of our targeted improvements in these areas.

Table 6: Model Comparison

Model	Validation Accuracy	Params	FLOPS
WSCN	98.20	90.00K	0.2M
Model V5	97.65	437.78K	1.817G
Model V6	98.17	437.77K	14.536G
Model V7	98.15	543.91K	2.740G

The comparative overview of our models (V5, V6, V7) against the state-of-the-art WaferSegClassNet (WSCN) underscores key differences in terms of validation accuracy, model complexity, and computational cost. While the WSCN leads slightly in accuracy at 98.20% and is notably more efficient with only 90,000 parameters and 0.2M FLOPS, our models, though slightly less accurate, demonstrate competitive performance with deeper complexity. Model V6 achieves a near-comparable accuracy of 98.17% but with significantly higher computational demand at 14.536G FLOPS. Model V7, with 543.91K parameters, also maintains a high accuracy of 98.15% at a computational cost of 2.740G FLOPS. Model V5, despite its lower accuracy of 97.65%, still requires a considerable 1.817G FLOPS. This analysis highlights the trade-offs between accuracy, model size, and computational efficiency, suggesting areas for optimization in future iterations.

VI. CONCLUSION

In this project, we undertook substantial modifications to the original Deformable Convolutional Network (DCN) model to address the challenges of wafer map defect pattern classification. Our series of enhanced models, though not surpassing the state-of-the-art (SOTA) model in overall accuracy, demonstrated superior performance in 21 out of 38 classes. This success highlights the specific strengths of our adaptations in handling complex defect types more effectively than the benchmark model. Moving forward, to further enhance the utility and interpretability of our models, we plan to explore the realm of explainable AI. Specifically, we aim to incorporate Class Activation Map (CAM) based models, which could provide clearer insights into the decision-making processes of our networks, thereby improving the transparency and trustworthiness of the predictions in practical applications.

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