Pipelined IITB-RISC

Simulation

Since windows development environment was not available (quartus not available) **GHDL** an open source alternative to **modelsim altera** was used to test and run simulations.

How to use GHDL?

1. First Install GHDL from this page: https://github.com/ghdl/ghdl/releases
2. Now after installation test: `ghdl --version`
3. Once GHDL installed the project directory can be opened and the following code should be run: `sh ./compile.sh`

   > `compile.sh` is a script provided in the project directory to compile all of the VHDL entities.

4. After VHDL code compiles with no error.
5. Use following command to run simulation `ghdl -r testbench --wave=waveform.ghw`
6. Now use gtkwave: http://gtkwave.sourceforge.net/ to open the waveform file

   > Waveform files contain data / signal plot of all the internal signals and ports for each entity instance.

How to program the Pipelined-IITB-RISC?

- Open `memory.vhdl` file in the project directory, the vector of signals from line 16, `RAM` contains the data memory and 16 bit data can be assigned via the following port mapping `<index> => <16bit data>`
- The instruction memory is the vector of signals from line 60, `RAM` contains the instructions and 16 bit instructions can be assigned here using the following port

mapping `<index> => <16bit instruction>`.

> for example for `lw r0, r0, 1` to be the first instruction, `0 =>
> "0111000000000001"`

How to use GTKWave?

Reference Video: https://drive.google.com/file/d/1atz7Ppbnt99kECCTt-CgmDzd1Un9AelK/view?usp=sharing