EE309 Microprocessors Project - Pipelined RISC Design - IITB-RISC

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The problem statement can be found in `Pipeline Problem Statement.pdf`.

The microprocessor has 6 stages of pipelining. The stages are **Instruction Fetch (IF)**, **Instruction Decode (ID)**, **Register Read (RR)**, **Execution (EX)**, **Instruction Fetch (IF)**, **Memory Management/Memory Access (MM)**, **Write Back (WB)**. The datapath consists of entities of all the above six stages and 5 pipeline registers connecting the stages, the datapath also uses two 16 bit ALUs.
The project folder also has attached the hardware descriptions of the various components in VHDL. The toplevel entity contains the Datapath and the FSM. *GHDL* and *GTKWave* were used to test and debug some of the instructions, namely ADD, LHI, LW

Screenshots of the wave viewer(GTKWave) are placed in the `waveforms` folder. The instructions listed in `waves.txt` were run by placing them in memory and the waveforms were captured.

Instructions to run the code, set up GHDL, GTKWave are provided in `User Instructions - Readme.pdf`