EE 791: ASSIGNMENT-3

Submitted by: Group-6
Surjeet Sarangi (213070033), Parimey Dnyaneshwar Patil (213070043), Rajat Sankhla (213079008), Subhasree Mondal (213079009)

1.

Grid-connected Photovoltaic (PV) Systems - Control of real and reactive power from VSC to the grid in αβ0 frame.

The values of filter inductance and capacitance: L = 1.5mH and C = 100μF such that the THD obtained was 0.19% (<5% obtained)

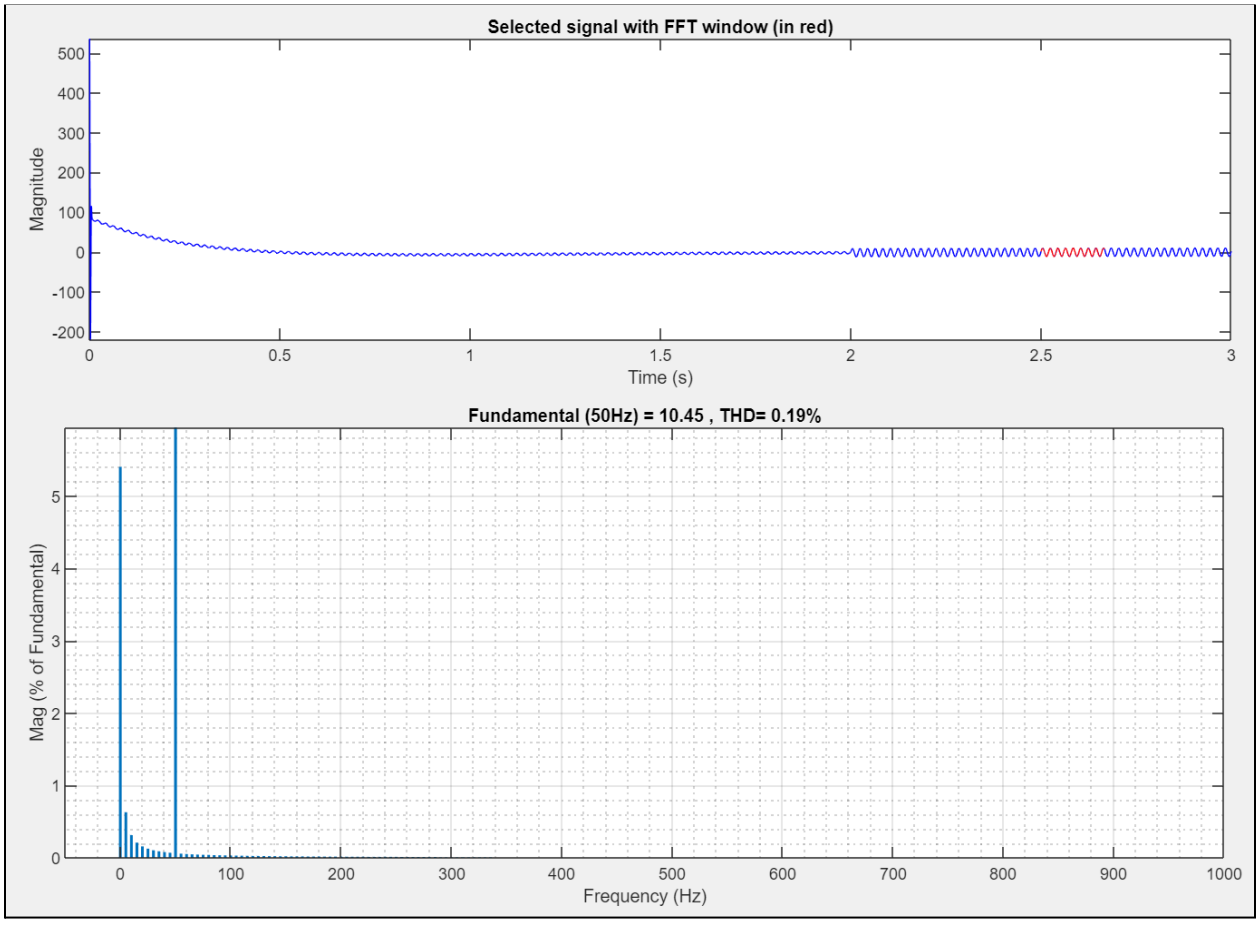


Figure 1: FFT analysis of phase-a current to the grid to compute THD

Design of compensator for the real and reactive power control:

The compensators, for the power control by controlling the current into the grid, each for α-axis and β-axis controlled, were designed for a step change of power from zero to maximum power. For that, the real and reactive power references were set accordingly.

Since the current in the αβ frame of reference is sinusoidal, in order to track sinusoidal reference, a PR controller is implemented.

Given:

$V_{s(peak)} = 230 \times \sqrt{2}\ V = 325.27\ V$

Switching frequency = 10 kHz

$R = 5m\Omega$

With $L = 1.5mH$ and $C = 100\mu F$

Plant transfer function, $G(s) = \dfrac{1}{R + sL}$

$$\Rightarrow G(s) = \frac{1/L}{s + R/L}$$

$$\Rightarrow G(s) = \frac{666.67}{s + 3.33}$$

Bandwidth required $= \omega_b \approx 9\omega_0$

$= 900\pi$ rad/s

where $\omega_0 = 2\pi f_0 = 2\pi \times 50$ rad/s $= 100\pi$ rad/s

Due to the pole at $s = -3.33$, it introduces 90° phase delay for frequency > 3.33 rad/s

∴ To improve loop gain, we cancel the pole by a compensator zero at $s = -3.33$ rad/s

Also, to satisfy zero steady state error requirement, a pair of complex conjugate poles were introduced at $s = \pm j100\pi$

∴ Open loop transfer function:

~~$K(s) = G(s) \times H(s)$~~

$$K(s) = \frac{s + 3.33}{s^2 + (100\pi)^2} \times H(s)$$

In order to get relatively large phase margin, the loop gain at ω_c must be supplemented with lead compensation:

$$F_{lead}(s) = \frac{s + p_1/\alpha}{s + p_1}$$

Maximum phase of filter:

$$\delta_m = \sin^{-1}\left(\frac{\alpha - 1}{\alpha + 1}\right)$$

occurs at frequency $\omega_m = \frac{p_1}{\sqrt{\alpha}}$ rad/s

Let $\omega_m = \omega_{gc} = 600\pi$ rad/s

Choosing $\delta_m = 45^\circ$ in order to get maximum positive loop gain, which gives $\alpha = 5.83$ and $p_1 = 600\pi\sqrt{5.83} = 455.29$

$$\therefore \frac{p_1}{\alpha} = 780.67$$

$\therefore$ Modified compensator;

$$K(s) = \left(\frac{s + 3.33}{s^2 + (180\pi)^2}\right)\left(\frac{s + 780.67}{s + 4551.29}\right) H(s)$$

$H(s) = K_1$ such that $|K(j\omega)G(j\omega)| = 1$ (at $\omega = \omega_c$)

$$\therefore K_1 = \frac{(600\pi)^2 + (100\pi)^2}{\sqrt{(600\pi)^2 + (100\pi)^2}} \times \frac{\sqrt{(600\pi)^2 + (455.29)^2}}{\sqrt{(600\pi)^2 + (780.67)^2}} \times \frac{\sqrt{(600\pi)^2 + (3.33)^2}}{666.67}$$

$$= 13225.86 \approx 13226$$

A lag filter is introduced in the compensator to ensure that the loop gain exhibits large gain magnitude at low frequencies. (by 32dB)

$$F_{lag}(s) = \frac{s+2}{s+0.05}$$

∴ Compensator transfer function: (PR controller)

$$K(s) = 13226\left(\frac{s+3.33}{s^2+(100\pi)^2}\right)\left(\frac{s+780.67}{s+4571.29}\right)\left(\frac{s+2}{s+0.05}\right)$$

The DC bus voltage was found to be 1000 V (V_{dc})

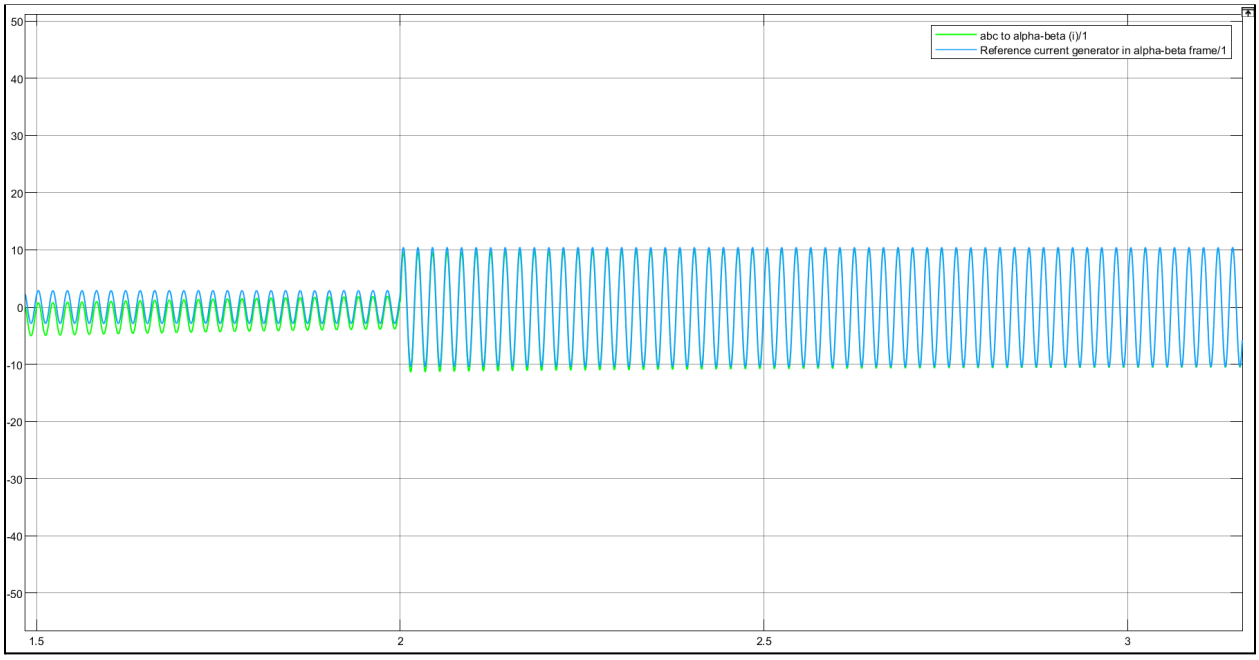


Figure 2: Snapshot of actual i_α current (Green waveform) and generated reference current i_α (blue waveform)

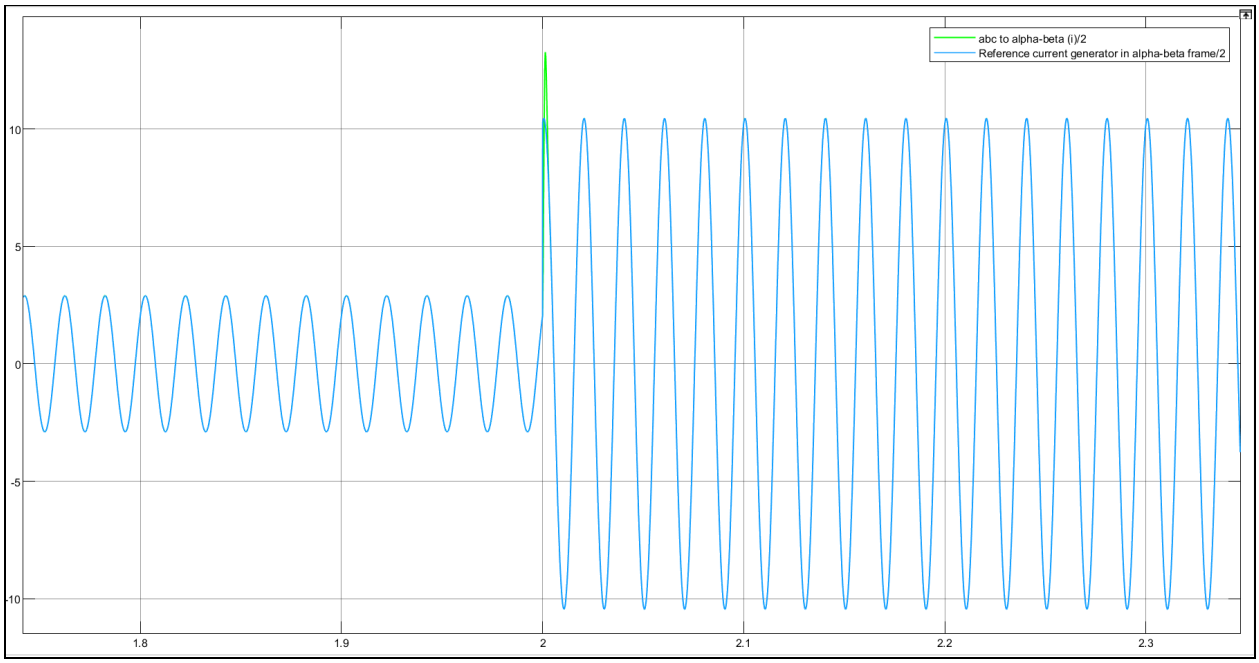


Figure 3: Snapshot of actual i_β current (Green waveform) and generated reference current i_β (blue waveform)

As can be seen from figure 2 and 3, actual currents in αβ frame are perfectly tracking reference currents in αβ frame even when the power references are changed. And during the change in reference value, we can see a sharp spike in actual current.

(a) Real power increased from 1kW to 5kW at t=2s keeping reactive power constant.

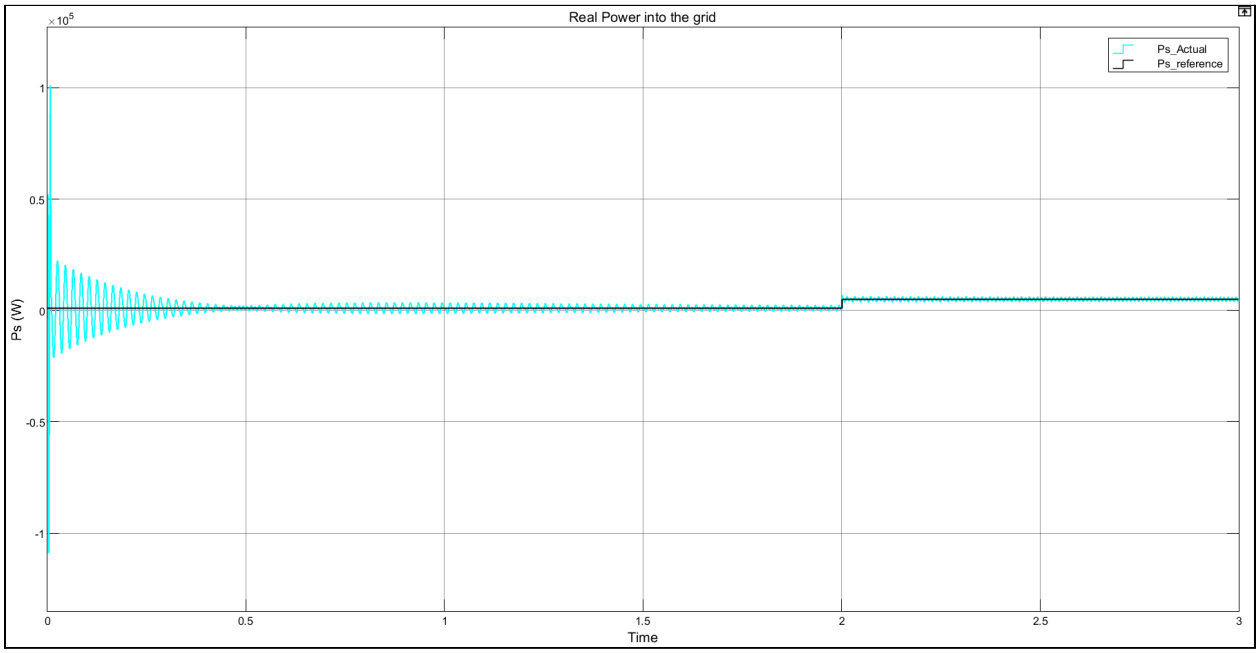


Figure 4: Real and reactive power control: real power changed at t=2s

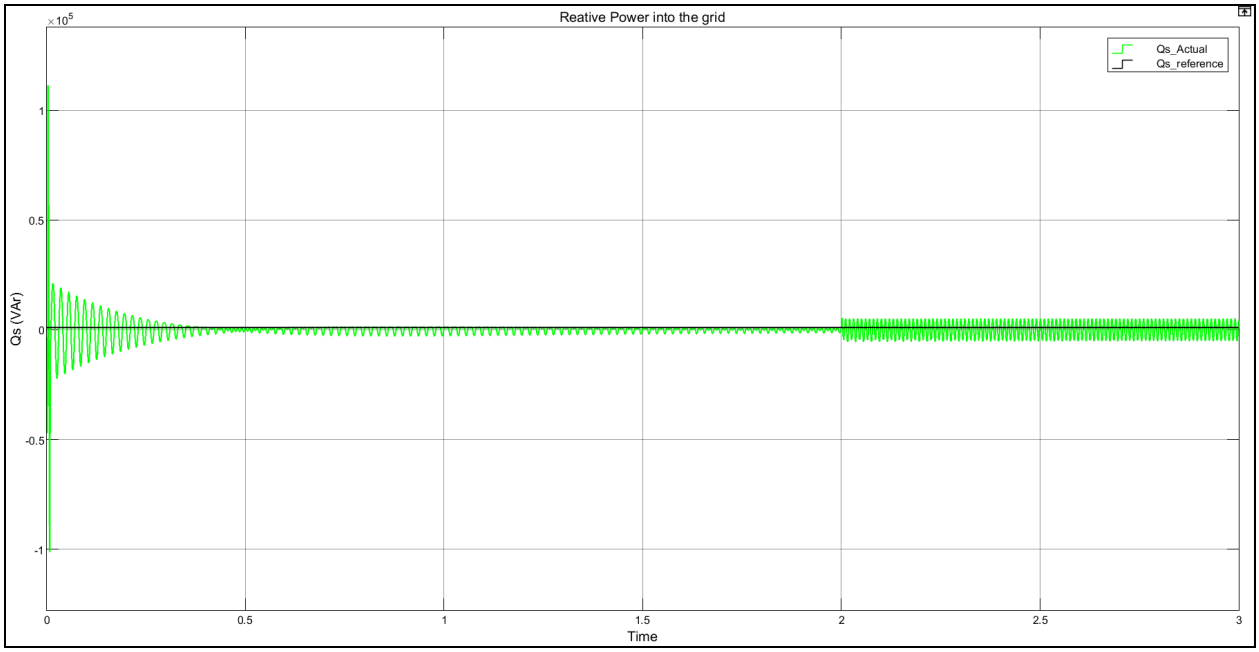


Figure 5: Real and reactive power control: reactive power unchanged at t=2s

(b) Reactive power changed from 1kVAr to 3kVAr at t=5s while real power remain unchanged.

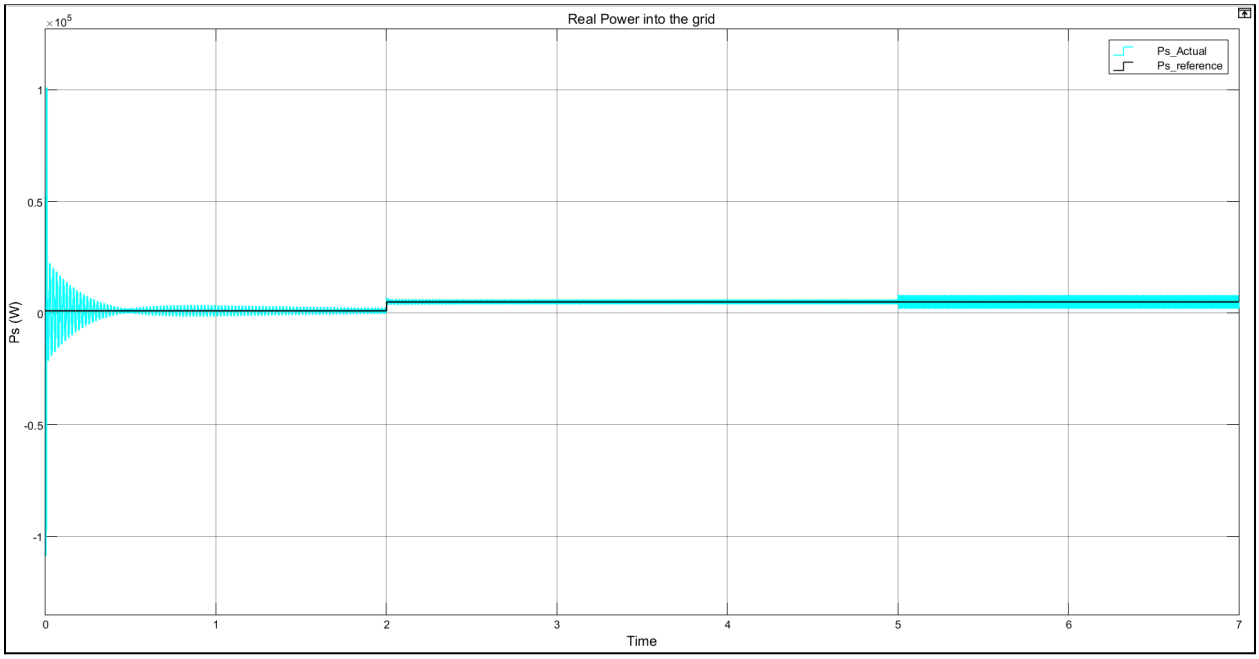


Figure 6: Real and reactive power control: real power changed at t=2s and remained unchanged at t=5s.

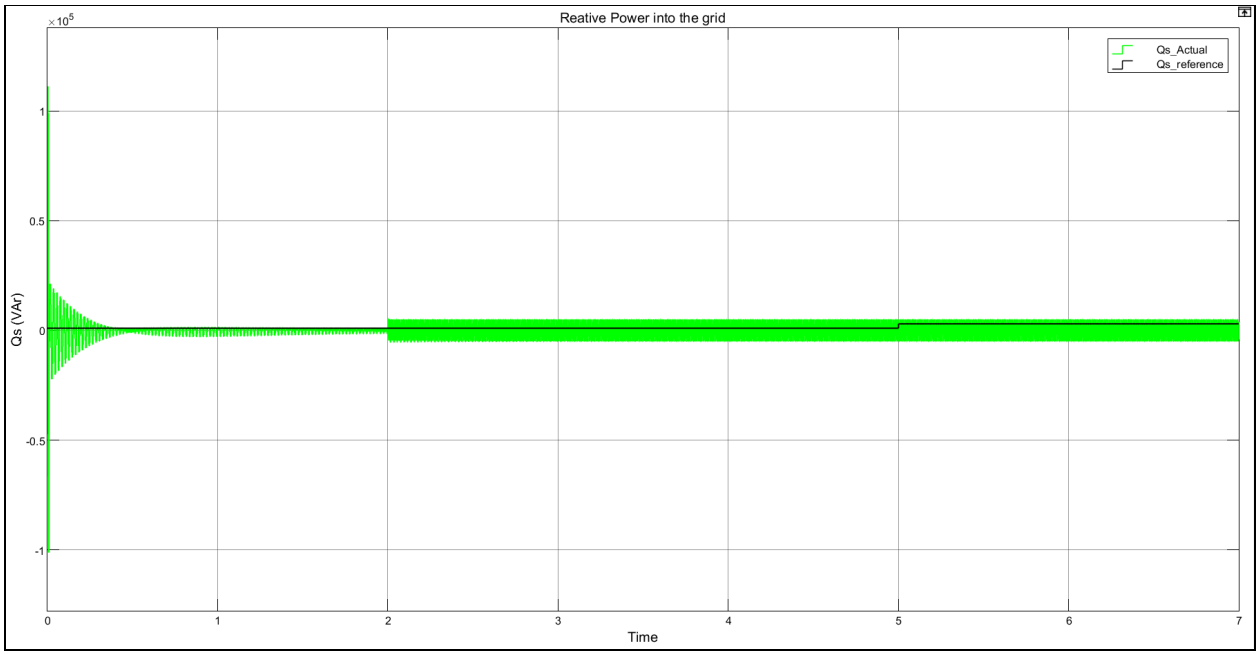


Figure 7: Real and reactive power control: reactive power unchanged at t=2s and changed at t=5s.

(c) Both the real and reactive power increased by 30% of its previous values at t=8s

Real power changed from 5kW to 6.5kW and reactive power changed from 3kVAr to 3.9kVAr at t=8s.

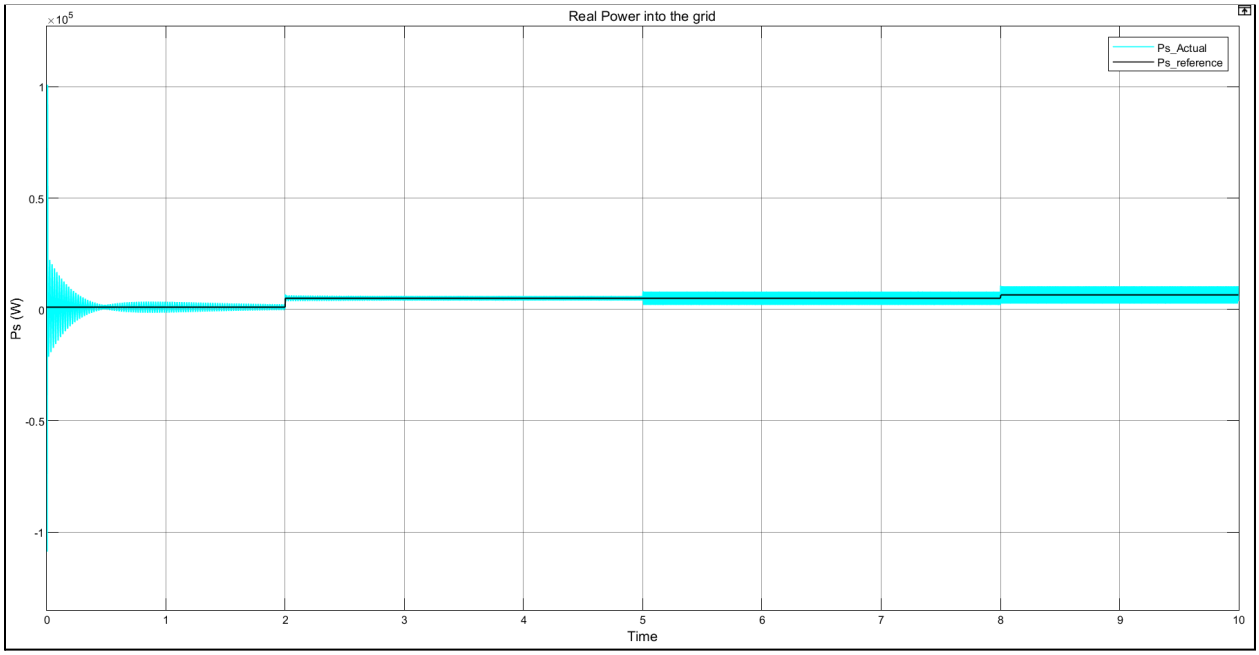


Figure 8: Real and reactive power control: Real power increased by 30% of its previous value at t=5s.

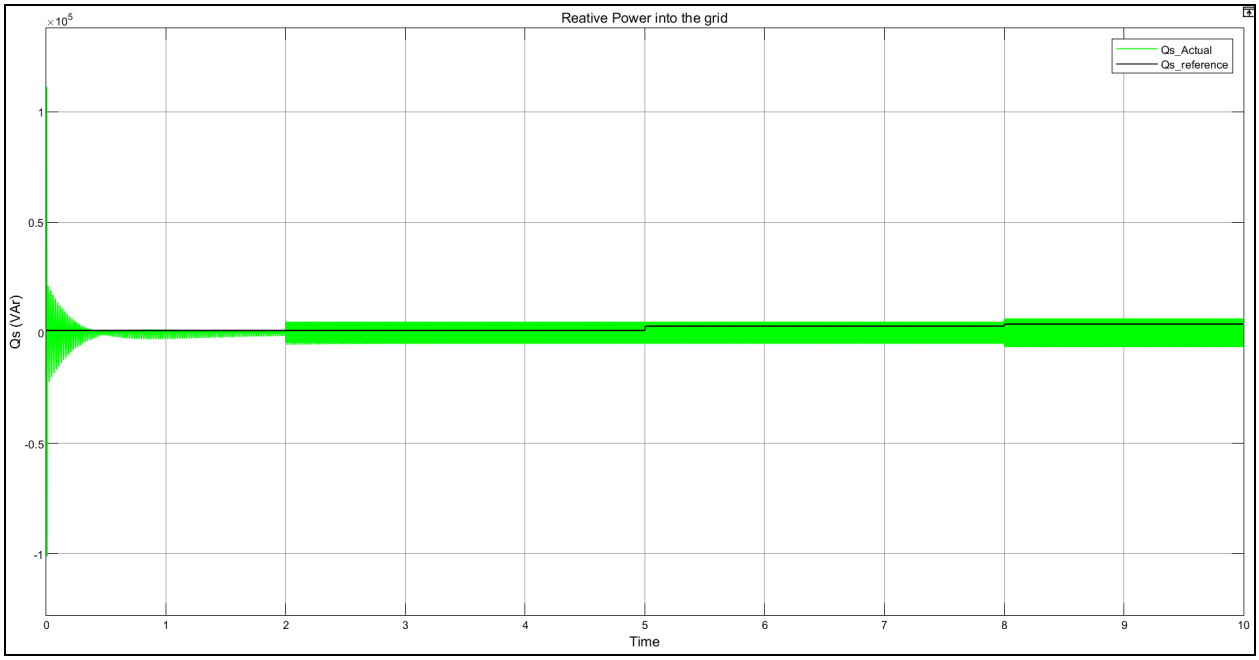


Figure 9: Real and reactive power control: Reactive power increased by 30% of its previous value at t=5s.

With a PR controller in αβ frame, we are able to achieve real and reactive power control with certain oscillations.

2.

Grid-connected Photovoltaic (PV) Systems - Control of real and reactive power from VSC to the grid in dq frame.

Compensator design for q and d axis current controller

Lets design a q and d axis controller to track id and iq such that they have a first order response. In order to do that as per the rule of thumb we chose bandwidth(1/Ti) as 10 times the switching frequency in (rad/sec).

q axis and d-axis compensators design

$$\frac{1}{T_i} \qquad 10 \times (2\pi \times f_s) = \omega_b = \frac{2\pi}{T_i}$$

$$f_s = 10 \times 10^3$$

$$\star \quad \boxed{\frac{1}{T_i} = 10^5}$$

By Taking care of THD considerations, lets choose $L = 25\,mH$;

For the response of id to track as a first order response:

$$\frac{id(s)}{id_{ref}(s)} = \frac{1}{1+sT_i}$$

$$\boxed{K_p = \frac{L}{T_i} = 25 \times 10^{-3} \times 10^5 = 250}$$

$$\boxed{K_I = \frac{R}{T_i} = 5 \times 10^{-3} \times 10^5 = 500}$$

→ We can keep a value of $K_p = 250$; and K_I any greater than 500. so i keep $K_I = 1000$.

$$\boxed{K_p = 250}; \quad \boxed{K_I = 1000}.$$

Compensator design for PLL

→ Synchronous frame PLL must be able to force $V_q = 0$ at steadystate, for that, we tune a PI (PLL).

With, $K_p = 10$ → faster response
$K_I = 5000$ → zero steady state error

→ It was found that these values gave e.g. $V_{sq} = 0$ @ steady state with nearly 0 steady state error.

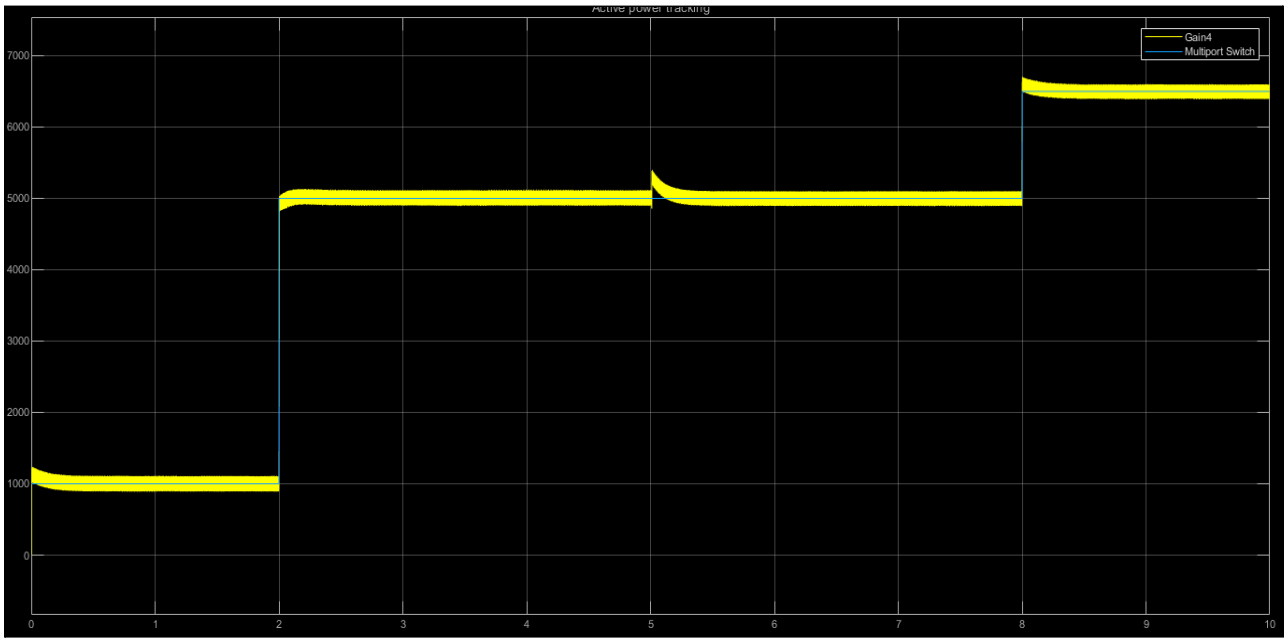


Figure 10: Real power control: Real power changed from 1kW to 5kW at t=2s, remained unchanged till t=8s and increased by 30% of 5kW (=6.5kW) at t=8s.

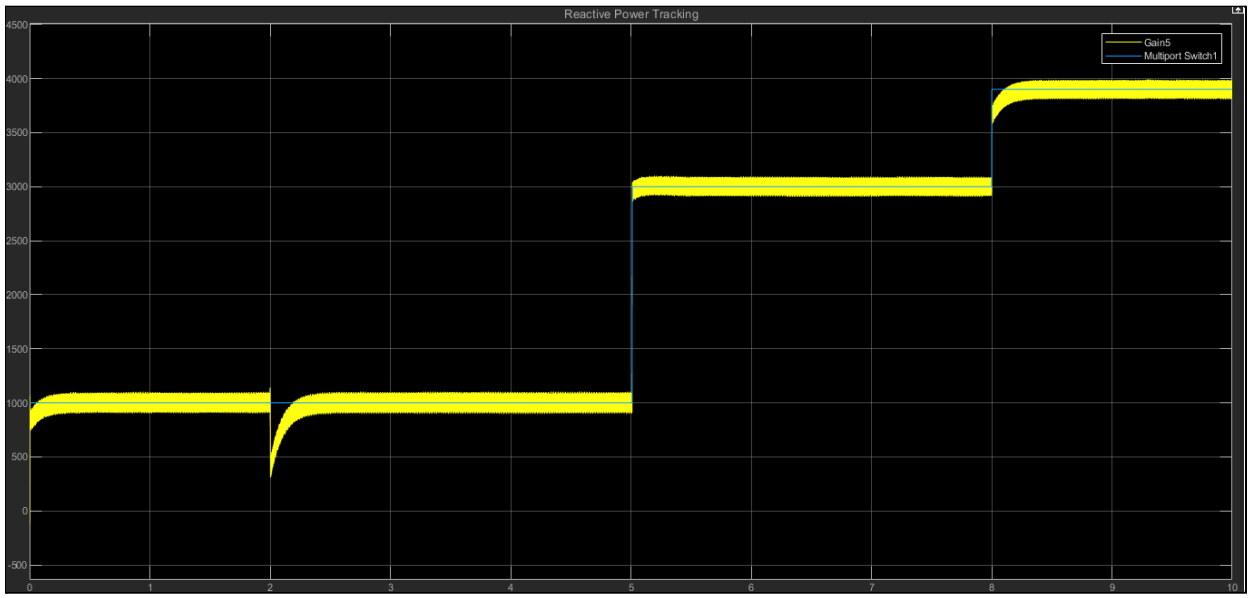


Figure 11: Reactive power control: Reactive power kept at 1kVAr till t=5s, changed to 3kVAr t=8s and increased by 30% of 3kVAr (=3.9kVAr) at t=8s.

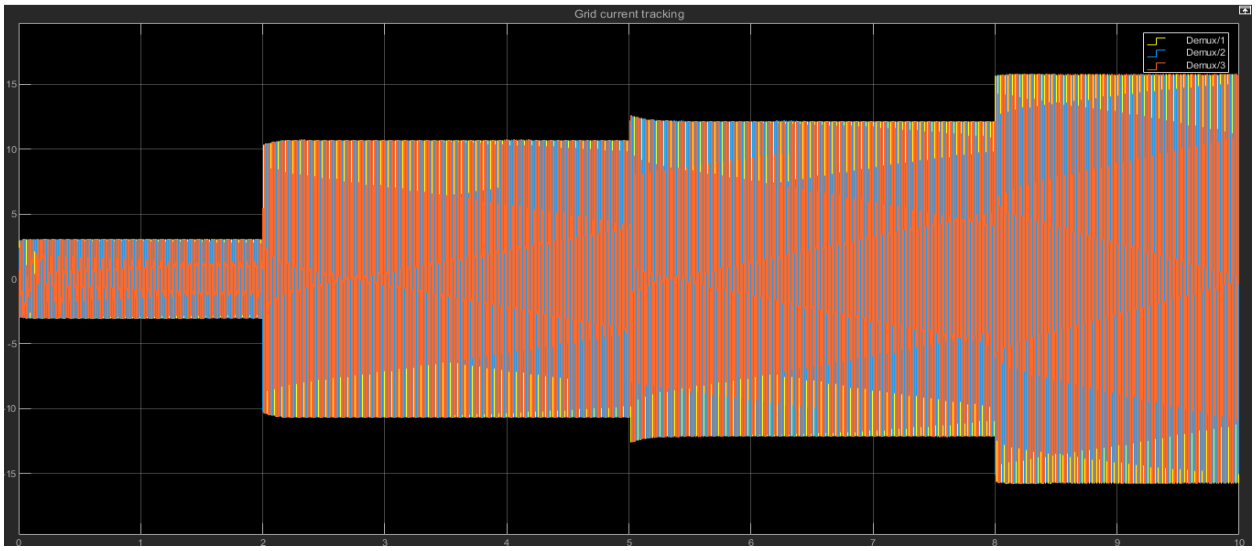


Figure 12: Grid current (i_{sa}, i_{sb}, i_{sc})

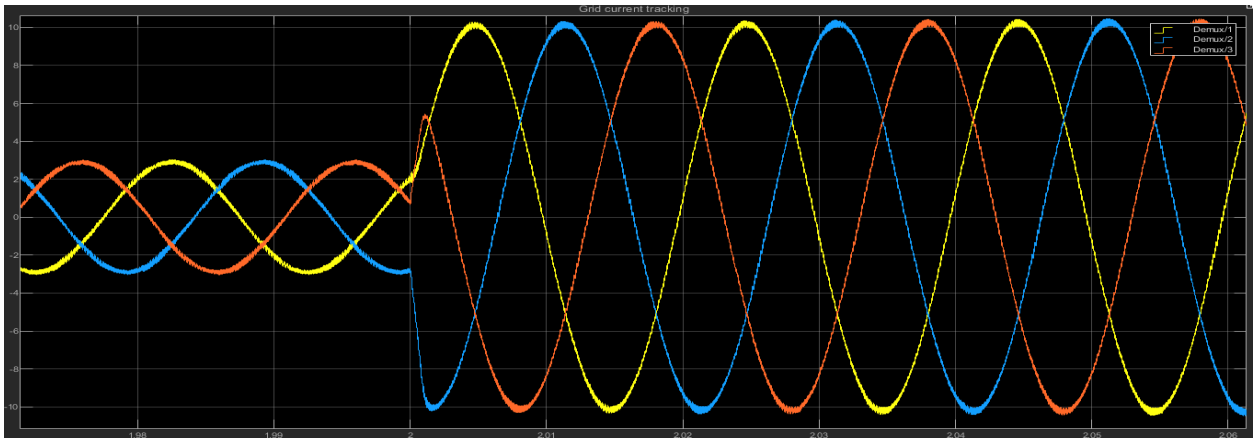


Figure 13: Current injected by inverter into the grid changes due to the change in reference for Active power from 1kw to 5kw at 2 sec.

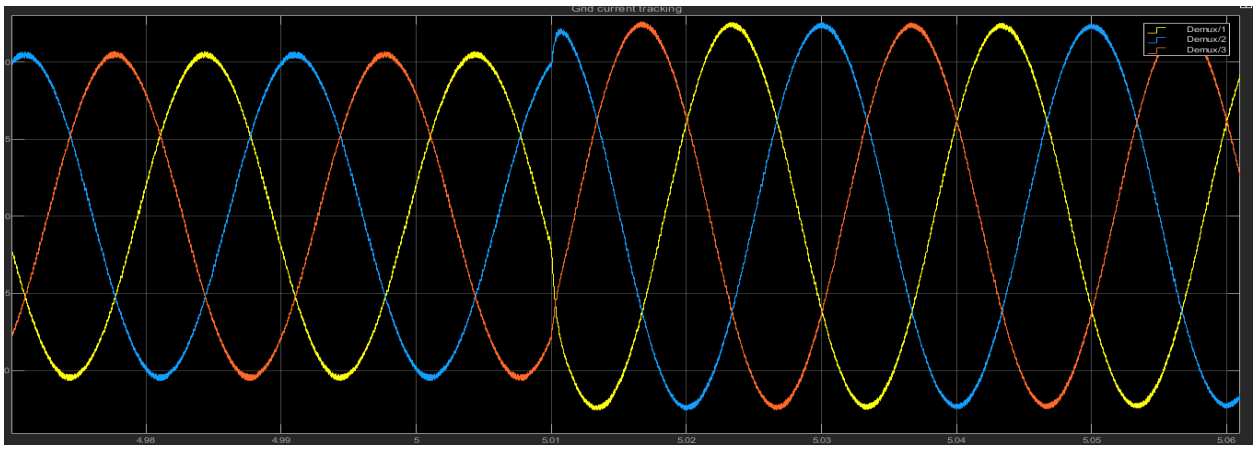


Figure 14: Current injected by inverter into the grid changes due to the change in reactive power reference from 1kvar to 3kvar at 5 sec.

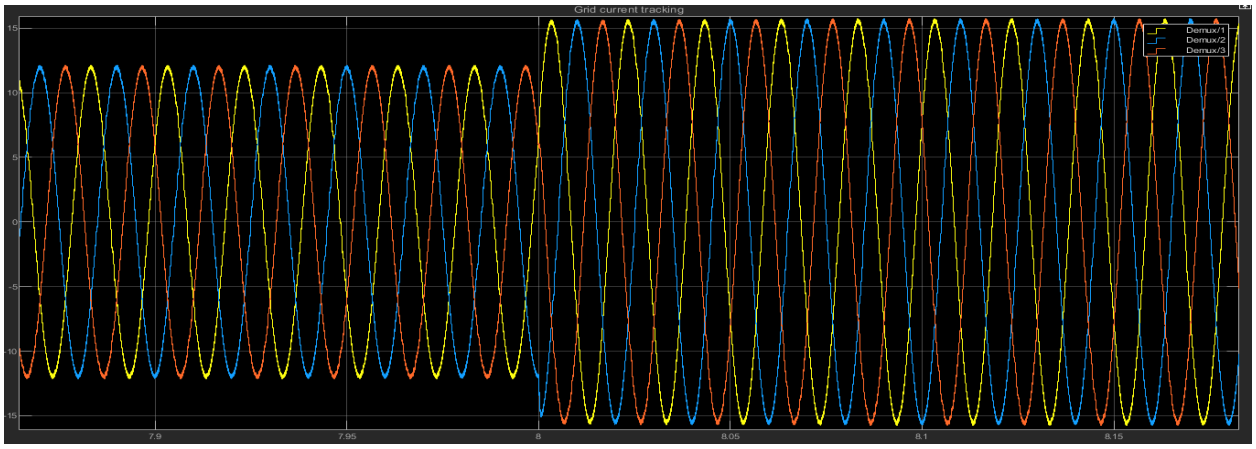


Figure 15: Current injected by inverter into the grid changes due to the change in active and reactive power reference to 1.3 times the earlier values at 8 sec.

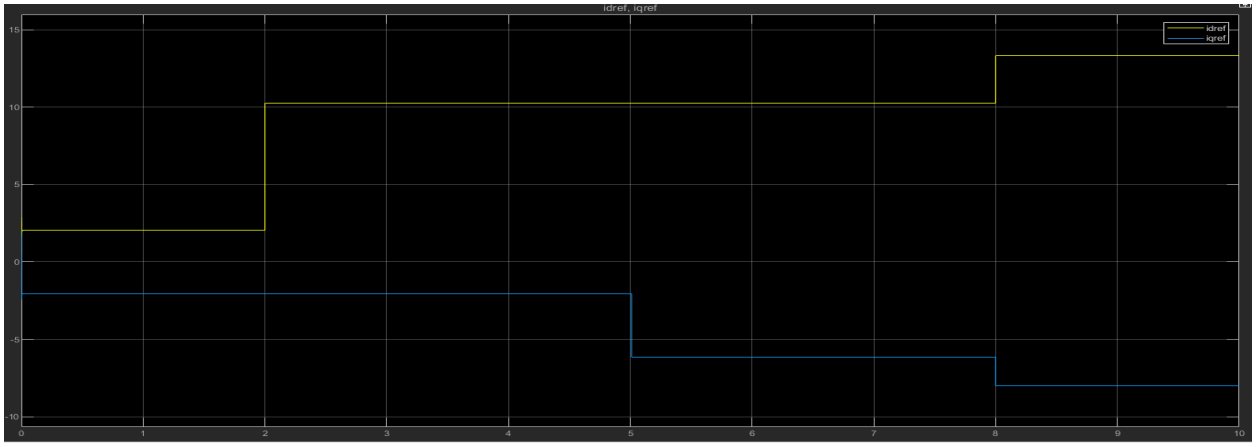
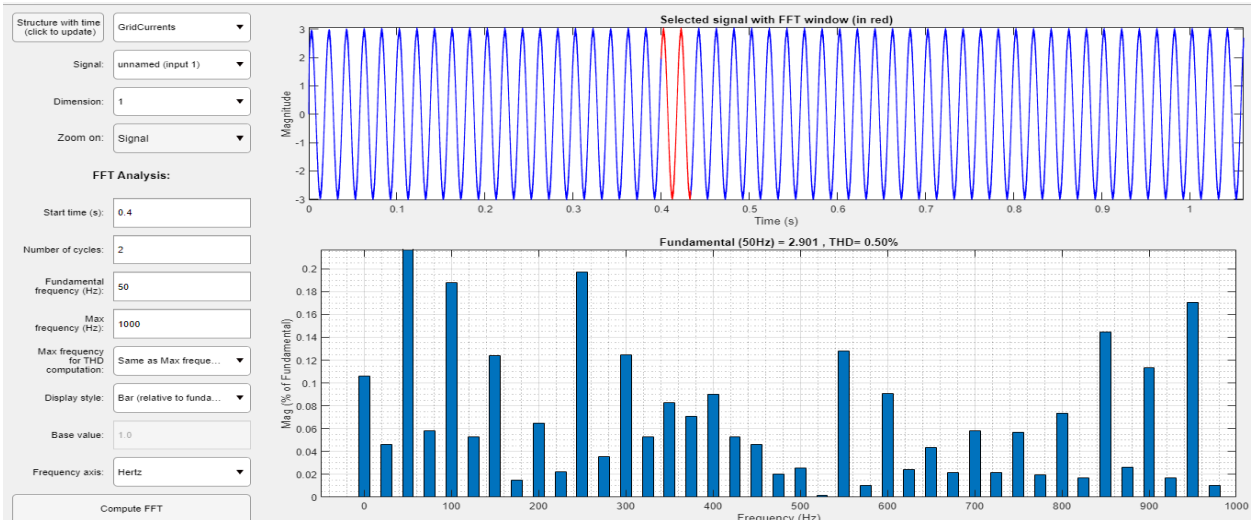


Figure 16: Reference currents generated from the Active and reactive power references.



As per the given grid norms the THD of current must be less than 5 percent and we are getting 0.5 percent.

Calculation of DC Bus voltage.

$$V_{td} = \left(\frac{2L}{3V_{sd}}\right)\frac{dP_s}{dt} + \left(\frac{2L\omega_0}{3V_{sd}}\right)Q_s + V_{sd},$$

$$V_{tq} = -\left(\frac{2L}{3V_{sd}}\right)\frac{dQ_s}{dt} + \left(\frac{2L\omega_0}{3V_{sd}}\right)P_s.$$

$$\widehat{V}_t = \sqrt{V_{td}^2 + V_{tq}^2}.$$

$$V_{DC} \geq 2\widehat{V}_t, \quad \text{PWM},$$

$$V_{DC} \geq 1.74\widehat{V}_t, \quad \text{PWM with third-harmonic injection.}$$

By this calculation i found out DC bus voltage as 1000V
With 1000 Volts our system is able to deliver the highest amount of reactive power and active power that were mentioned in the problem,

3.

The Phase Locked Loop (PLL) is a closed-loop system which locks the frequency and phase angle of a signal and generates another signal with the same frequency and phase angle using a feedback loop. It is one of the most important components of grid connected systems, as it should work in harmony with the grid. The PLL provides continuous information about the grid phase angle and grid frequency of signal of interest, which is generally the fundamental grid voltage, which is essential for the control of the inverter output voltage, using PI controller in dq0 frame.

The PLL consists of the following basic components:

(1) Phase Detector (PD): It generates a signal which is the error between input signal to it and the signal generated by an internal oscillator. Depending on the type of PD, the AC components appear along with the DC-signal phase angle difference.
(2) Loop Filter: It attenuates the AC components of the PD output signal.
(3) Voltage Controlled Oscillator (VCO): It generates an AC signal based on the input it receives from the output of the loop filter.

There are different techniques which are used to implement each of these blocks which constitutes complete PLL. The PLL can be implemented in analog or digital or combination of both. But analog-based PLL has disadvantages as it is sensitive to process variations, and also being inaccurate. However, digital PLL doesn't have such disadvantages and are reliable, stable, fast and precise, and have easy adjustments and so on. In digital PLL, all the basic components are implemented digitally.

Digital PLL works in the digital domain, in a processor. To implement PLL digitally:

(1) Phase Detector - It should be able to produce the phase difference between input reference signal to it and output signal from VCO. In order to get the phase difference of these two signals, we need to multiply both the signals. An assumption is made that the phase difference is so small, that the relationship is linear, although in reality, it is non-linear as the sine function gets associated with the phase difference.
So PD is essentially a multiplier, having a gain of k_{pd}.

(2) Low Pass Filter - The job of this block is to filter out or attenuate the high frequency components which results in the multiplication of two signals in PD. This is best implemented using a PI controller. And for this to be achieved, the PI controller is regulated accordingly.

(3) VCO - It consists of a gain followed by a linear integrator. The input to it is in the form of voltage signal from the output of the PI controller. It generates ω corresponding to the

voltage signal input and on integrating ω (using an integrator), it generates the corresponding phase angle Θ, which is the output of the PLL. And it is implemented without the use of any analog oscillators like colpitts oscillators, and the operation is performed in the digital domain.

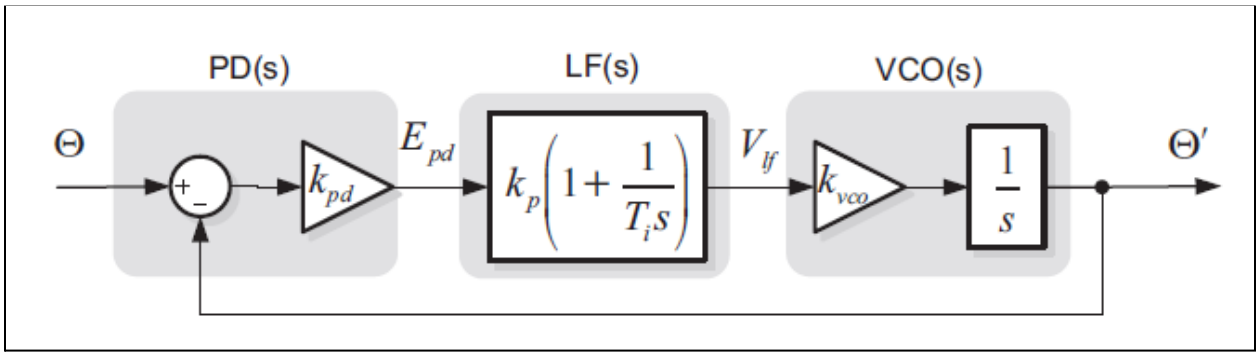


Figure 17: Basic block diagram of digital (closed-loop) PLL.[1]

The reasons we need to go for quadrature signal based PLL are:

(1) The assumption which we have taken for making the dynamic behavior of PLL appear to be linear, which is, the frequency of the signal to be phase-locked (phase difference assumed to be very small) and is much higher than the bandwidth of the PLL, makes the analysis and formulas describing it much simpler but results in low reliability of the analysis and formulations made because of the assumptions taken, which is valid only theoretically as in real, PLL is a nonlinear system.

(2) In grid-connected systems, the grid frequency is very close to the cutoff frequency of the PLL. When the PLL is locked, the high frequency oscillations in the phase-angle error are only twice the input frequency, which appears to be very close. With this, the assumption of cancellation of high frequency components is not accepted.

Because of these reasons, we need a PD different from a simple multiplier PD, in order to cancel out high oscillations which occur at twice the grid frequency. That's why we go for a PD based on in-quadrature signals.

Design of compensator for quadrature signal based PLL:

For the compensator design, we are considering the case where the three-phase grid voltages are unbalanced, distorted due to the presence of harmonics. In such cases, we require a compensator H(s). If the grid voltages were balanced and free from harmonic distortion, instead of H(s), we would require only a PI controller.

V_{sabc} represents here an unbalanced voltage with fundamental component, a negative fundamental component and a fifth harmonic component.

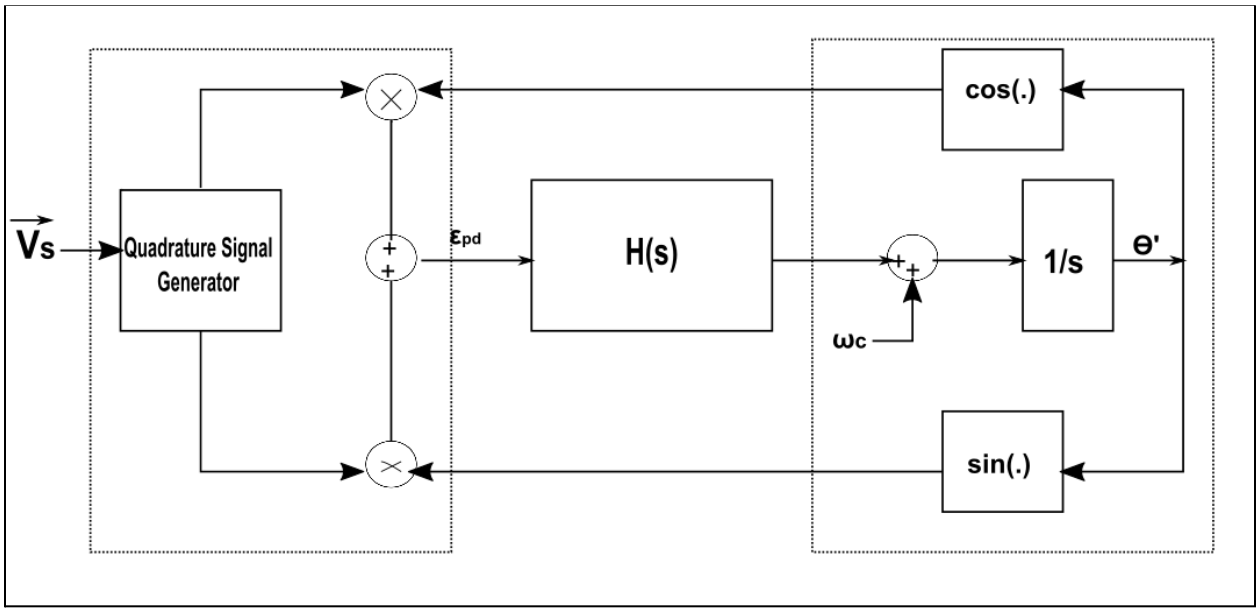


Figure 16: Basic block diagram of quadrature signal based PLL.[1]

$$V_{sa}(t) = \hat{V}_s \cos(\omega_0 t + \theta_0) + k_1 \hat{V}_s \cos(\omega_0 t + \theta_0) + k_5 \hat{V}_s \cos(5\omega_0 t + \phi_5)$$

$$V_{sb}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) + k_1 \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) + k_5 \hat{V}_s \cos\left(5\omega_0 t + \phi_5 - \frac{4\pi}{3}\right)$$

$$V_{sc}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) + k_1 \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) + k_5 \hat{V}_s \cos\left(5\omega_0 t + \theta_0 - \frac{2\pi}{3}\right)$$

Where k_1 and k_5 are the amplitudes of the negative-sequence (fundamental) and fifth-order harmonic components, respectively, relative to the amplitude of the positive sequence (fundamental) component.

The space-phasor corresponding to V_{sabc}:

$$\vec{V_s} = \hat{V}_s e^{j(\omega_0 t + \theta_0)} + k_1 \hat{V}_s e^{-j(\omega_0 t + \theta_0)} + k_5 \hat{V}_s e^{-j(5\omega_0 t + \phi_5)}$$

Then the space-phasor is converted to α-β frame using Quadrature-Signal generator.

$$\vec{V_\alpha} = \hat{V}_s \cos(\omega_0 t + \theta_0) + k_1 \hat{V}_s \cos(\omega_0 t + \theta_0) + k_5 \hat{V}_s \cos(5\omega_0 t + \phi_5)$$

$$\vec{V_\beta} = \hat{V}_s \sin(\omega_0 t + \theta_0) - k_1 \hat{V}_s \sin(\omega_0 t + \theta_0) + k_5 \hat{V}_s \sin(5\omega_0 t + \phi_5)$$

Based on the block diagram:

$$\varepsilon_{pd} = \vec{V}_\alpha \cos(\omega' t + \phi') + \vec{V}_\beta \sin(\omega' t + \phi')$$

(where, $\theta' = \omega' t + \phi'$ is the phase angle output from V_{co})

$$\Rightarrow \varepsilon_{pd} = \hat{V}_s \cos(\omega_0 t + \theta_0) \cos(\omega' t + \phi') + k_1 \hat{V}_s \cos(\omega_0 t + \theta_0) \cos(\omega' t + \phi') + k_5 \hat{V}_s \cos(5\omega_0 t + \phi_5) \cos(\omega' t + \phi')$$

$$+ \hat{V}_s \sin(\omega_0 t + \theta_0) \sin(\omega' t + \phi') + k \hat{V}_s \sin(\omega_0 t + \theta_0) \sin(\omega' t + \phi') - k_5 \hat{V}_s \sin(5\omega_0 t + \theta_0) \sin(\omega' t + \phi')$$

$$\Rightarrow \varepsilon_{pd} = \frac{\hat{V}_s}{2} \cos\left((\omega_0 t + \theta_0) - (\omega' t + \phi')\right) + \frac{k_1}{2} \hat{V}_s \cos\left((\omega_0 t + \theta_0) + (\omega' t + \phi')\right) + \frac{k_5}{2} \hat{V}_s \cos\left((5\omega_0 t + \phi_5) + (\omega' t + \phi')\right)$$

When the PLL is well synchronized, $\omega_0 = \omega'$

$$\therefore \varepsilon_{pd} = \frac{\hat{V}_s}{2} \cos(\theta_0 - \phi') + \frac{k_1}{2} \hat{V}_s \cos(2\omega_0 t + (\theta_0 - \phi')) + \frac{k_5}{2} \hat{V}_s \left(6\omega_0 t + (\theta_0 - \phi')\right)$$

Here, θ_o - ϕ' is the phase difference, which is a constant.

Unlike in the case of balanced grid voltages where we get only the first term, getting the benefit of quadrature signal based PLL by not getting any AC component, here, due to the unbalanced grid voltages, we are getting the last two AC components in the error signal ε_{pd}, with frequencies $2\omega_o$ and $6\omega_o$, the $2\omega_o$ component being the main concern.

Based on that, the compensator H(s) is designed with the cut-off frequency as double the grid frequency ($2\omega_o$). The steps involved in the design of compensator H(s) are as follows[2]:

(1) We need to attenuate the $2\omega_o$ and $6\omega_o$ frequency components present in the error signal ε_{pd}. For that, H(s) needs to have low-pass characteristics with the cut-off frequency set to $2\omega_o$, and for that, we need to introduce a pair of complex-conjugate zeros at $s = \pm j2\omega_o$.
(2) We want ϕ' to track θ_o (reference/grid phase angle) with zero steady state error. For that, we need to introduce a pole in H(s) at s=0.
(3) To ensure that the open loop gain magnitude of H(s) continues to drop with the slope of -40dB/decade for $\omega > 2\omega_o$, two equal real poles at $s = -2\omega_o$ need to be included in H(s).
(4) Based on the transfer function of H(s) obtained till now, frequency response of open loop gain of H(s) is plotted and checked, and based on the desired phase margin and gain margin of the compensator system, lead/lag compensators are included with H(s) to improve the steady-state performance of the system.
(5) The gain of H(s) is calculated by making the magnitude of the open loop gain obtained till now equal to 1.
(6) An additional lag compensator is included in H(s), which doesn't affect the rest of the transfer function, to ensure the open loop gain exhibits large magnitudes at low frequencies.

References:
[1] Remus Teodorescu, Marco Liserre and Pedro Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*.
[2] Amirnaser Yazdani, Reza Iravani, *Voltage-Sourced Converters in Power Systems - Modeling, Control, and Applications*.