

74F374

Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 74F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

Features

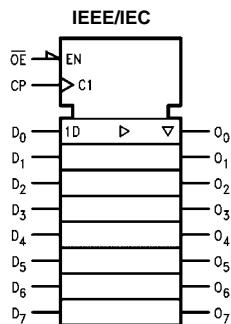
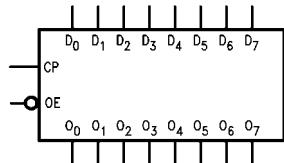
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Ordering Code:

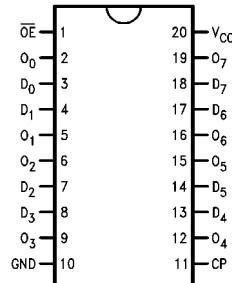
Order Number	Package Number	Package Description
74F374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F374MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
D ₀ -D ₇	Data Inputs	1.0/1.0	20 µA/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/-0.6 mA
OE	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 µA/-0.6 mA
O ₀ -O ₇	3-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

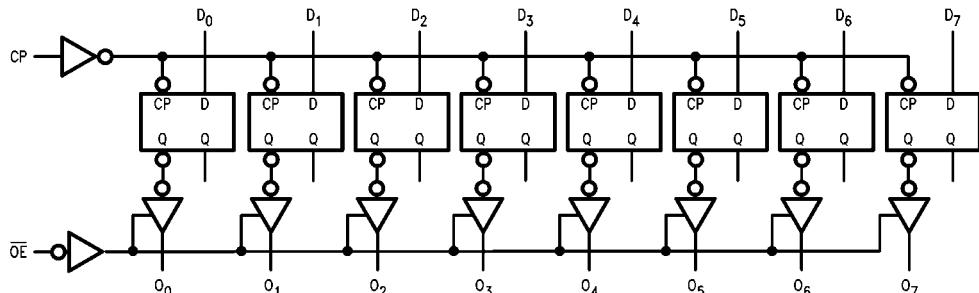
The 74F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output O _n
D _n	CP	\overline{OE}		
H	✓	L	H	H
L	✓	L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
✓ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V_{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

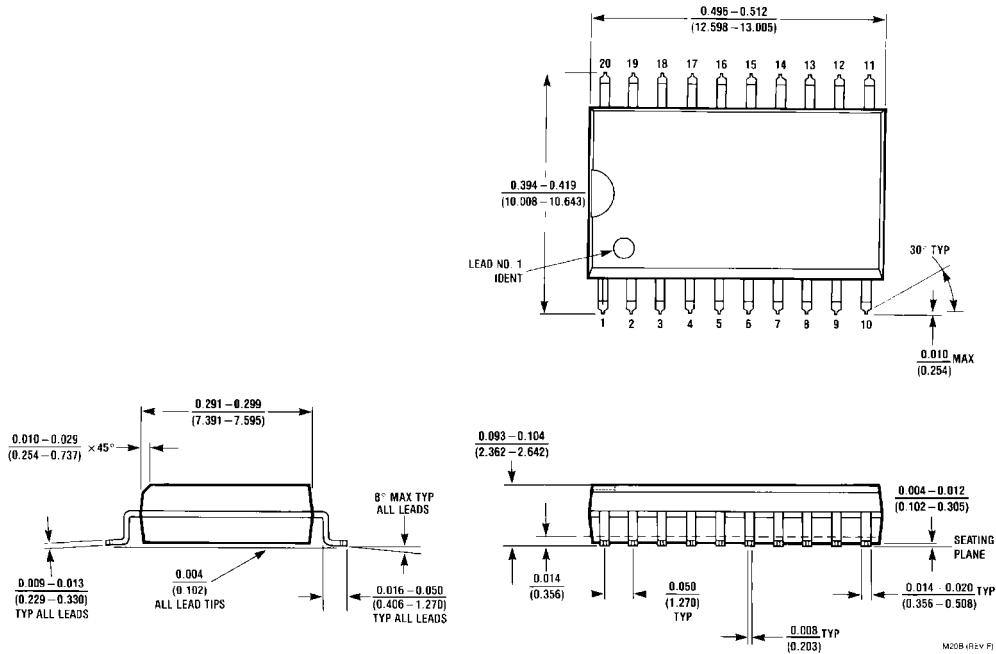
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage 10% V_{CC}	2.5					$I_{OH} = -1 \text{ mA}$
	10% V_{CC}	2.4					$I_{OH} = -3 \text{ mA}$
	5% V_{CC}	2.7					$I_{OH} = -1 \text{ mA}$
	5% V_{CC}	2.7					$I_{OH} = -3 \text{ mA}$
V_{OL}	Output LOW Voltage 10% V_{CC}			0.5	V	Min	$I_{OL} = 24 \text{ mA}$
I_{IH}	Input HIGH Current			5.0	μA	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	$V_{IN} = 7.0V$
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9 \text{ }\mu\text{A}$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μA	0.0	$V_{OD} = 150 \text{ mV}$ All Other Pins Grounded
I_{IL}	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OZH}	Output Leakage Current			50	μA	Max	$V_{OUT} = 2.7V$
I_{OZL}	Output Leakage Current			-50	μA	Max	$V_{OUT} = 0.5V$
I_{OS}	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0V$
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	$V_{OUT} = 5.25V$
I_{CCZ}	Power Supply Current		55	86	mA	Max	$V_O = \text{HIGH Z}$

AC Electrical Characteristics

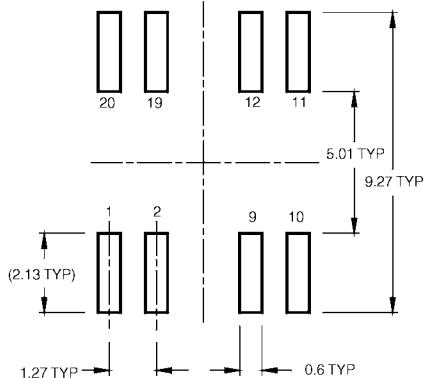
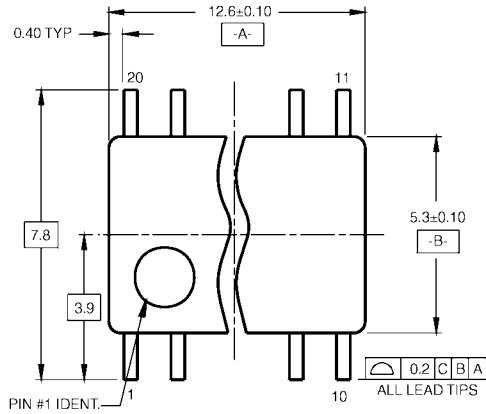
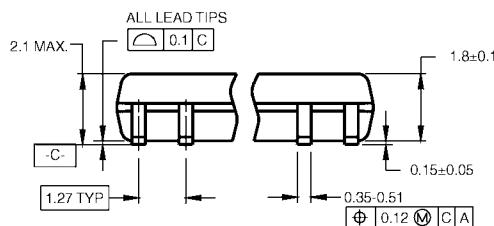
Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = -55^\circ C \text{ to } +125^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = 0^\circ C \text{ to } +70^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{MAX}	Maximum Clock Frequency	100	140		60		70				MHz
t_{PLH}	Propagation Delay CP to O_n	4.0	6.5	8.5	4.0	10.5	4.0	10.0			ns
t_{PHL}		4.0	6.5	8.5	4.0	11.0	4.0	10.0			
t_{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5			
t_{PZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5			
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0			
t_{PLZ}		1.5	4.3	5.5	1.5	7.5	1.5	6.5			

AC Operating Requirements

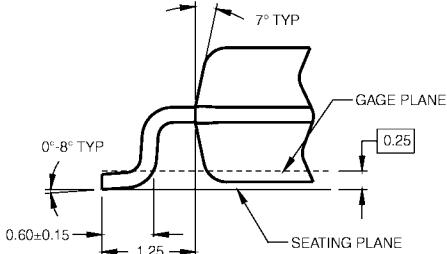
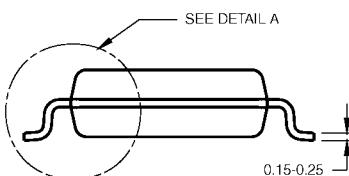
Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$			$T_A = -55^\circ C \text{ to } +125^\circ C$ $V_{CC} = +5.0V$			$T_A = 0^\circ C \text{ to } +70^\circ C$ $V_{CC} = +5.0V$			Units	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	2.0		2.5		2.0						
$t_S(L)$	D_n to CP	2.0		2.0		2.0						
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0						
$t_H(L)$	D_n to CP	2.0		2.5		2.0						
$t_W(H)$	CP Pulse Width	7.0		7.0		7.0						
$t_W(L)$	HIGH or LOW	6.0		6.0		6.0						ns

Physical Dimensions inches (millimeters) unless otherwise noted

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS



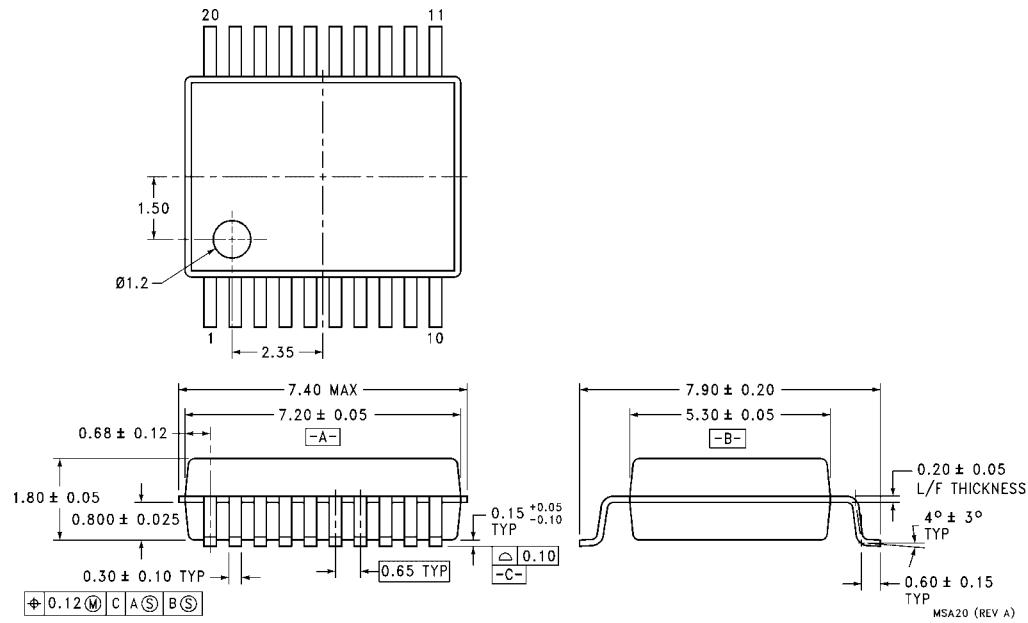
NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

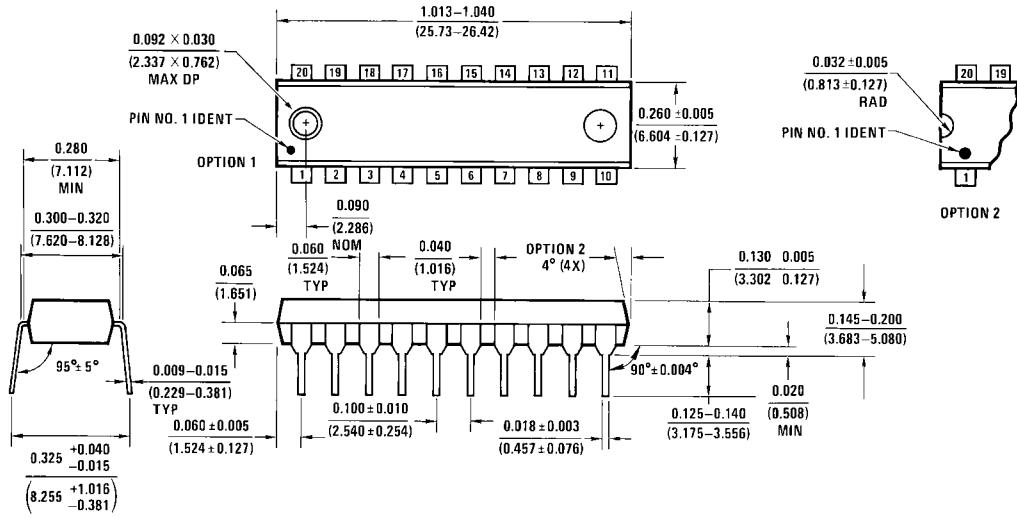
DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

74F374 Octal D-Type Flip-Flop with 3-STATE Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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