Questions on *mfs*

1. Is *mfs* a state-of-the-art method for logic synthesis with EXDCs?
2. Is *mfs* only designed for FPGAs? Does it also work for ASICs?

Questions on my research with *mfs*

The idea is to generate approximate circuits by approximating its EXDCs with logic simulation. I start from the *mfs* method in the paper *Scalable Don't-Care-Based Logic Optimization and Resynthesis*. The **only** change is the structure of miter in Figure 1 (the Figure 4.2.1 in the *mfs* paper).

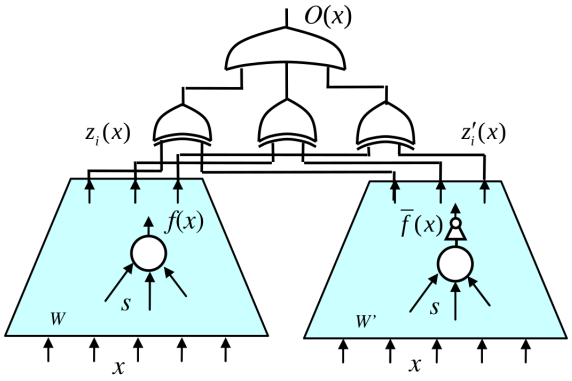

Figure 1: Original miter for care set computation

Instead of constructing such a miter in Figure 1 to represent the care set, I simulate the circuit for N rounds and generate a set of patterns for window inputs $\mathbf{x}$. Those patterns are treated as the **approximate care set** and used to synthesize the approximate circuit.

For example, the window inputs are A, B and C, and three rounds simulation patterns for ABC are 010, 111, 101. Then I use $O(x) = \overline{A}B\overline{C} + ABC + A\overline{B}C$ to represent the approximate care set.

1. Is the modification on *mfs* reasonable to generate approximate designs?
2. I have an interesting observation on *c880* with my idea:

   (a) In most cases, for some values of N within a continuous interval, the final approximate circuit does not change. For example, I increase N from 192 to 256, the results are same.

   (b) But the error rate of the approximate circuit might change dramatically due to the addition of one simulation frame. For example, when N change from 256 to 257 (the first 256 inputs patterns for simulation are same), the error rate of the final circuit changes greatly (from 0.2% to 5%).

   Is the observation caused by the property of *mfs*?