Weekly Report

April 9, 2019

1 Targets

1.1 Urgent

- Change PI don't care set: simplify CNF by logic synthesis or special input pattern.
- Change PI care set: use different random seed.
- Change window don't care set.

1.2 Important

- Randomly selecting a node, compute its care set, change its care set, synthesize the local circuit, evaluate its area and error rate, accept it with a certain probability.
- How DC affects BDD. Change simplification method (mfs→bdd).
- Induce DC with PLA files
- Use model counting to compute error rate, i.e., how many assignments satisfying a SAT problem.
- Use approximate confidence interval / hypothesis testing of Bernoulli experiments to evaluate the accuracy of error rate.
- Trade off the accuracy of batch error estimation for speed (even directly use Su's equation to update Boolean difference), perhaps use hypothesis testing to evaluate the accuracy.
- Combine the simulation of circuits with the simulation of Monte Carlo Tree Search. In other words, in one loop of Monte Carlo Tree Search, merge logic simulation and playout (only simulate circuit once and playout once).
- Represent circuit with AIG because of more potential LAC candidates. For each round, select one or more input wires and replace them with constant 0 or 1. Consider how to combine Wu's method (choose a subset of input wires and substitute).
- Accelerate Approximate Logic Synthesis Ordered by Monte Carlo Tree Search: reuse the result of batch error estimation in playout.
- Use UCB1's bound to guide the simulation time. Find relationship of different bounds.

1.3 Worth Trying

- Enhance default policy with greedy approach or field domain knowledge.
- In expansion process of MCTS, expand more than one layers.
- Tune parameters in MCTS.

- Perform greedy flow on leaves of the final Monte Carlo Search Tree.
- Combine beam search and MCTS.
- Influence of network representation on synthesis. Why does mfs use local AIG function to represent the circuit, is it more fittable to LUT mapping?

1.4 Potential Topics

- Relationship between power simulation and logic simulation.
- Combine Binarized Neural Network with approximate computing.
- Relationship between Boolean network and Bayesian Network.
- Approximate TMR.

2 Progress

2.1 Issues of Last Meeting

How to synthesize using external don't-cares (EXDCs)

Alan said that it was possible to use EXDCs in ABC but it was rather complicated. He recommended me to refer to the SIS script "full_simplify" to handle EXDCs.

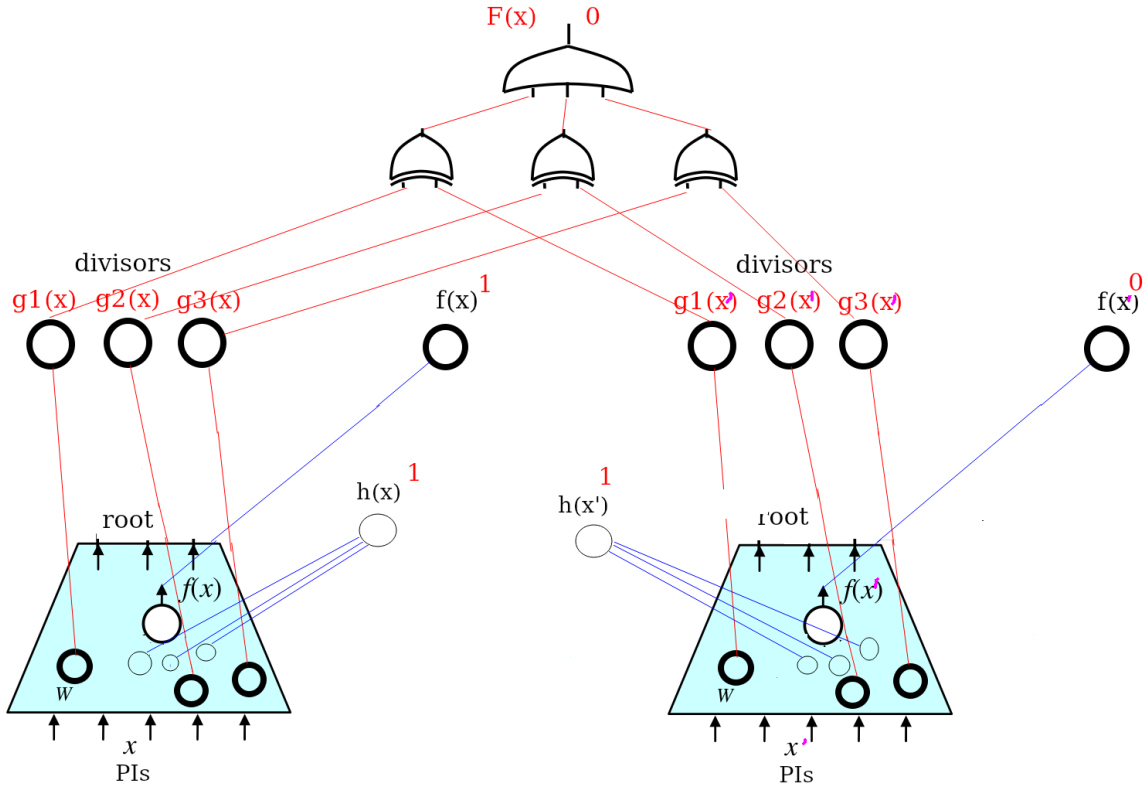
2.2 Issues of This Week

Fixed the bug of logic simulation on AIG network

Since it is too detailed and not very relevant to the project, I do not expand here.

Set the approximate care set on windows in a circuit

For a node f, I extract its window W. The "roots" of the window are the nodes 2 levels away from f in f's transitive fanouts. The inputs of the window are the nodes l levels away from f in all the "roots" transitive fanins. However, the divisors are also the nodes in the transitive fanins of all the "roots".
The logic simulation process generates M assignments for the inputs of the window W. Assuming that those M assigments are the approximate care set of the window. Let h be the corresponding expression of the M assignments. For example, if there are 3 assignments for a 3-input window, 010, 100, 111, then $h = \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$.
The SAT solver is built like the following figure:



For $M = 10240$, I test the result under different l on c880. Wu+Su's method can generate an area of 504 under 0.05 error rate.

l	final area	error rate
1	539	0.110156
2	530	0.14248
3	517	0.150195
4	509	0.152246
5	508	0.170996

However, for a fixed l, the result does not change with M. For example, when $l = 3$,

M	final area	error rate
64	517	0.150195
1024	517	0.150195
10240	517	0.150195