Weekly Report

April 13, 2019

1 Targets

1.1 Urgent

- ~~Change PI don't care set: simplify CNF by logic synthesis or special input pattern.~~
- ~~Change PI care set: use different random seed.~~
- ~~Change window care set.~~
- Change window don't care set.

1.2 Important

- Randomly selecting a node, compute its care set, change its care set, synthesize the local circuit, evaluate its area and error rate, accept it with a certain probability.
- How DC affects BDD. Change simplification method (mfs→bdd).
- Introduce DC with PLA files
- Use model counting to compute error rate, i.e., how many assignments satisfying a SAT problem.
- Use approximate confidence interval / hypothesis testing of Bernoulli experiments to evaluate the accuracy of error rate.
- Trade off the accuracy of batch error estimation for speed (even directly use Su's equation to update Boolean difference), perhaps use hypothesis testing to evaluate the accuracy.
- Combine the simulation of circuits with the simulation of Monte Carlo Tree Search. In other words, in one loop of Monte Carlo Tree Search, merge logic simulation and playout (only simulate circuit once and playout once).
- Represent circuit with AIG because of more potential LAC candidates. For each round, select one or more input wires and replace them with constant 0 or 1. Consider how to combine Wu's method (choose a subset of input wires and substitute).
- Accelerate Approximate Logic Synthesis Ordered by Monte Carlo Tree Search: reuse the result of batch error estimation in playout.
- Use UCB1's bound to guide the simulation time. Find relationship of different bounds.

1.3 Worth Trying

- Enhance default policy with greedy approach or field domain knowledge.
- In expansion process of MCTS, expand more than one layers.
- Tune parameters in MCTS.
- Perform greedy flow on leaves of the final Monte Carlo Search Tree.
- Combine beam search and MCTS.
- Influence of network representation on synthesis. Why does mfs use local AIG function to represent the circuit, is it more fittable to LUT mapping?

1.4 Potential Topics

- Relationship between power simulation and logic simulation.
- Combine Binarized Neural Network with approximate computing.
- Relationship between Boolean network and Bayesian Network.
- Approximate TMR.

2 Progress

2.1 Issues of Last Meeting

Why area does not change with M for a fixed l

Recall the definition of k and l: l is a relevant level. For a node V, we extract its local circuit $\mathbb{W}$ by limiting the level of transitive fanins/fanouts as k and l.

The issue is: For a fixed l, area of the generated approximate circuit did not change with the simulation number M.

I made a stupid mistake. In my wrong code, M is set as a constant value 64.

The relationship between DCs on local inputs and primary inputs

Need to be discussed.

2.2 Issues of This Week

Result of changing window care set

Let $k = 2$, $l = 1$. Set approximate care set on local inputs according to simulation values. The result is in Table 1.

Table 1: Area and error versus simulation number

	Approximate windows care set			reference (Su TCAD)	
circuit	#simulation	area	error	area	error upper bound
c880	64	477	0.743945000	504	0.05
	128	404	0.839746000		
	192	537	0.480078000		
	256	519	0.470801000		
	257	545	0.002343750	554	0.003
	320	545	0.002343750		
	384	550	0.002148440		
	448	559	0.000292969	569	0.001
	512	546	0.003515620		
	576	559	0.000292969		
	640	559	0.000292969		
	704	573	0.002148440		
	768	577	0.000292969		
	832	581	0.000195313		
	896	576	0.000097656		
	960	559	0.000292969		
	1024	580	0.00195312		
	10240	591	0	599.00	0
c1908	1	717	0	284	0.05
	16	624	0.702344		
	31	697	0.0775391		
	32	706	0.00478516	619	0.005
	48	706	0.00478516		
	64	710	0		

Problems in Table 1

- Error rate changes dramatically near some values of simulation number, such as 256→ 257 for c880, 31→32 for c1908.
- Error rate dose not monotonous to simulation number.

The drawback of mfs method (only find one feasible re-substitution function) might be responsible for those.

Other problems

The number of local circuit inputs is not balanced, and it may result in large error rate for those local circuit with many inputs.