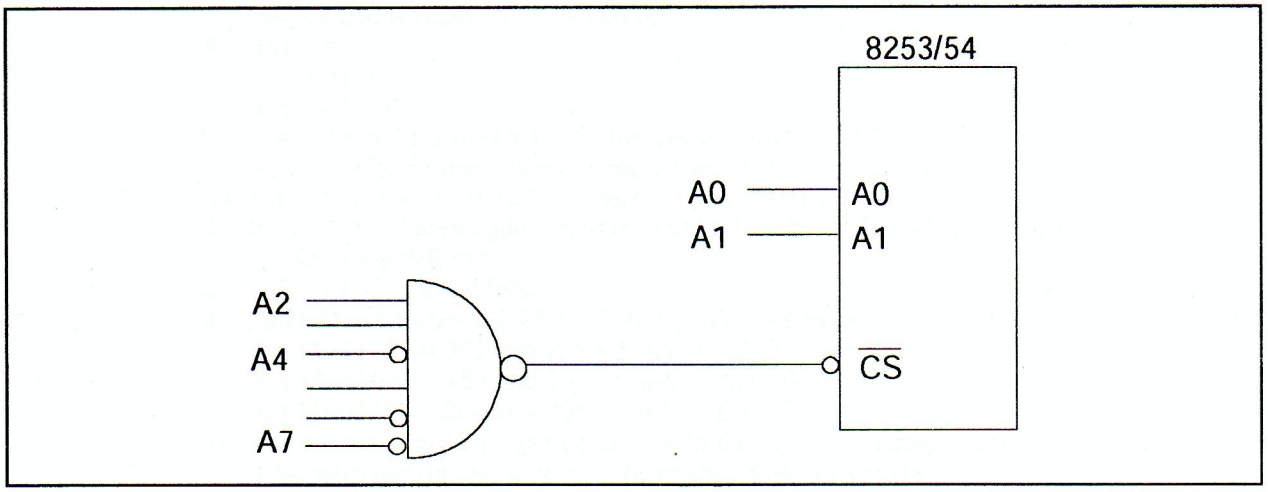
SOLUTIONS FOR CHAPTER 13 (5)

SECTION 13.1 (5.1): 8253/54 TIMER DESCRIPTION AND INITIALIZATION

1. true
2. input, square wave
3. The base port address is 2CH. The port addresses are 2CH: counter 0;2DH: counter 1; 2EH:counter 2; and 2FH: control register. The design is as follows:



4. 23H, 97H, 51H, and 59H since counter 0 must have A0 = 0 and A1 = 0
5. In binary mode, the highest value is 65,536 and programmed as 0000. In BCD mode, it is 10,000 and programmed as 0000.
6. true
7. 76H
8.

```
MOV     AL,76H      ;countr1,mode 3,binary,lo byte,and hi byte
OUT     2FH,AL
MOV     AX,1333     ;divisor=1.6M/1200=1333
OUT     2DH,AL      ;the low byte first
MOV     AL,AH
OUT     2DH,AL      ;then the high byte
```

9.

```
MOV     AL,76H      ;countr1,mode 3,binary,lo byte,and hi byte
OUT     2FH,AL
MOV     AX,6400     ;divisor=1.6M/250=6400
OUT     2DH,AL      ;the low byte first
MOV     AL,AH
OUT     2DH,AL      ;then the high byte
```

10. In the binary option, the maximum divisor is 65,536; therefore, we have 1.6 MHz /65536 = 24 Hz. For the BCD, option we have 160 Hz since 1.6 MHz /10000 =160 Hz.

SECTION 13.2 (5.2): IBM PC 8253/54 CONNECTIONS, PROGRAMMING

11. CLK0, CLK1, and CLK2 are connected to a fixed frequency of 1.19 MHz.
12. The source of the square wave is the 8284's PCK which is 2.38 MHz. After it is divided by 2 using a simple D-FF, 1.19 MHz is fed to all CLKs inputs.
13. 40H - 43H. No, they cannot be changed. If a given clone does not use these port addresses, it is not compatible with the IBM PC.

14. Counter0 is used by IRQ0 to cause the interrupt 18.2 times per second. Counter1 is used for the DRAM memory refreshing circuitry. Counter2 is connected to the PC speaker.
15. true
16. GATE0 and GATE1 are connected to V_{CC} permanently. GATE2 is controlled by D0 of port address 61H.
17. This is due to the fact that such a time delay is not fixed and can vary depending on the speed of the 80x86 processor in different PCs, plus the fact that the clock count of a given instruction varies among the 80x86 family.
18.

```
                                    clock count
        SUB   CX,CX
AGAIN:  NOP                         3
        NOP                         3
        NOP                         3
        LOOP  AGAIN                 17
                                    26T
```

T = 1/8 MHz = 125 ns
(17 + 3 + 3 + 3) × 65,535 × 125 ns = 212.9887 ms

19. true
20.

```
        MOV     BL,20           ;20 X 0.5SEC=10SEC
AGAIN:  MOV     CX,33144        ;0.5SEC DELAY
        CALL    WAITF
        DEC     BL
        JNZ     AGAIN
```

;for the WAITF subroutine see the text.

SECTION 13.3 (5.3): GENERATING MUSIC ON THE IBM PC

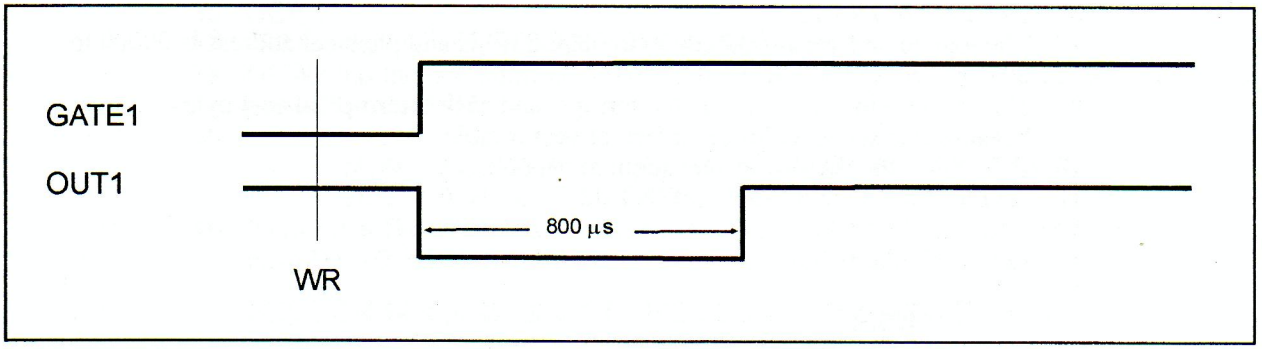
21. A3 frequency is 220 Hz; therefore, 5423 is the divisor since 1.1931 MHz/5423 = 220 Hz. By the same token, we have a divisor of 1522 for G5 and 604 for B6.
22.

```
PAGE   60,132
;THIS PROGRAM USES THE BUILT-IN TIMER CLOCK #2 TO PLAY A SONG
;OVER THE INTERNAL SPEAKER
;*********************************************************
;
MYSTAK          SEGMENT
        DB              32 DUP(?)
MYSTAK          ENDS
;*********************************************************
;
MYDATA  SEGMENT
FREQS   DW      330,1,294,1,262,1,294,1,330,1,330,1
        DW      330,2,294,1,294,1,294,2,330,1,392,1
        DW      392,2,330,1,294,1,262,1,294,1,330,1
        DW      330,1,330,1,330,1,294,1,294,1,330,1
        DW      294,1,262,4
MYDATA  ENDS
;*********************************************************
;
MYCODE  SEGMENT
MAIN    PROC    FAR
        ASSUME  CS:MYCODE,DS:MYDATA,SS:MYSTAK
        MOV     AX,MYDATA
        MOV     DS,AX
        MOV     AL,0B6H         ;program timer clock 2
        OUT     43H,AL
        LEA     DI,FREQS        ;pointer to notes & counts
```

```
HERE:       MOV   AX,34DEH      ;1.193182 MHz = 001234DEH
            MOV   DX,0012H      ;clock freq is loaded in numerator
            MOV   BX,[DI]       ;denominator
            CMP   BX,0000H      ;check for end of song
            JE    THU           ;if end of song, back to DOS
            DIV   BX            ;calculate divide #
            OUT   42H,AL
            MOV   AL,AH         ;high byte divider
            OUT   42H,AL
            IN    AL,61H        ;save speaker status
            MOV   AH,AL
            OR    AL,03         ;turn speaker on
            OUT   61H,AL
            INC   DI
            INC   DI
            MOV   BX,[DI]       ;set note delay
            CALL  DELAY         ;note delay
            INC   DI
            INC   DI
            MOV   AL,AH         ;restore speaker status
            OUT   61H,AL        ;and turn speaker off
            CALL  DELAY2
            JMP   HERE          ;get next note
THU:        MOV   AH,4CH        ;end of song return to DOS
            INT   21H
MAIN        ENDP                ;end main procedure
;*****************************************************
DELAY       PROC
            PUSH  AX            ;save AX
AGAIN1:     MOV   CX,16578      ;16578 * 15.08us = 250ms
AGAIN:      IN    AL,61H        ;run 15.08 us delay
            AND   AL,10H
            CMP   AL,AH
            JE    AGAIN
            MOV   AH,AL
            LOOP  AGAIN         ;end of 250 ms
            DEC   BL            ;decrement note count
            JNZ   AGAIN1        ;more time if note is longer
            POP   AX            ;restore AX
            RET
DELAY       ENDP
;*****************************************************
DELAY2      PROC
            MOV   CX,1328       ;1328 * 15.08 us = 20 ms
REPEAT:     IN    AL,61H
            AND   AL,10H
            CMP   AL,AH
            JE    REPEAT
            MOV   AH,AL
            LOOP  REPEAT        ;end of 20ms
            RET
DELAY2      ENDP
;*****************************************************
MYCODE      ENDS
            END   MAIN
```

SECTION 13.4 (5.4): SHAPE OF 8253/54 OUTPUTS

23. square wave shape
24. Duty cycle is 50% since the divisor is an even number. The pulse width (duration) is 32,768 × 838 ns =27.45 ms for high and low parts.
25. mode 2 rate generator
26. The period is 18 × 838 ns = 15.09 microsec. The high part of the pulse is 17 × 838 ns = 14.2 microsec and the low part is 838 ns. That makes the duty cycle = 14.2 μs/15.09 μs × 100 =94%.
27. mode 3 square wave
28. (a) For a divisor of 1200 the duty cycle is 50% since it is an even number. The low and high parts of the pulse are 600 × 838 ns = 502.8 μs each.
    (b) By the same token the pulse period for the divisor of 1825 is 1825 × 838 ns = 1.529 msec. Now since the divisor is odd we have 913 × 838 ns =765 μs for the high part and 912 × 838 ns = 764.2 μs for the low part. The duty cycle is approximately 50.02% (913/1825 × 100 =50.027%).
29. 1/1.5 MHz = 666 ns and 1200 × 666 ns = 800 μs; see the following diagram



30. 1/1.8 MHz = 555 ns; 1450 × 555 ns = 805 μs; see the following diagram