The x86 PC

assembly language, design, and interfacing

fifth edition

Prentice Hall

Dec Hex Bin
25 19 00011001

ORG ; TWENTY-FIVE

SYSTEM DESIGN
ISSUES AND
FAILURE ANALYSIS

The x86 PC

assembly language, design, and interfacing

fifth edition

MUHAMMAD ALI MAZIDI
JANICE GILLISPIE MAZIDI
DANNY CAUSEY

OBJECTIVES

this chapter enables the student to:

- Contrast and compare MOS and bipolar transistors.
- Evaluate logic families according to speed, power dissipation, noise immunity, input/output interface compatibility, and cost.
- Trace the evolution of Intel x86 microprocessors in terms of IC technology.
- Define IC fan-out and describe why connecting an output to too many inputs can cause false logic.

OBJECTIVES (*cont*)

this chapter enables the student to:

- Describe capacitance derating and its effect on system design and the use of buffers to decrease its effect.
- Discuss power in system design, including static and dynamic currents, power dissipation, and sleep mode for peripherals.
- Define ground bounce and VCC bounce and describe methods that designers use to avoid the false signal generation that they may cause.

OBJECTIVES (*cont*)

this chapter enables the student to:

- Define crosstalk and describe ways to avoid crosstalk in system design.
- Define transmission line ringing and discuss ways to reduce its effect.
- Define measures of system reliability: FIT and MTBF

25.1: OVERVIEW OF IC TECHNOLOGY

- Invention of the transistor & advent of integrated circuit (IC) technology is believed by many to be the start of the second industrial revolution.
  - The transistor was invented in 1947 by three scientists at Bell Laboratory.
  - In the 1950s, transistors replaced vacuum tubes in many electronics systems, including computers.
- Prior to invention of the integrated circuit, use of transistors, with other discrete components like capacitors & resistors, was common.
  - In 1959 the first integrated circuit was successfully fabricated & tested at Texas Instruments, by Jack Kilby

25.1: OVERVIEW OF IC TECHNOLOGY

- By the late 60s & early 70s, use of silicon-based ICs was widespread in mainframes and minicomputers.
  - Transistors and ICs were based on P-type materials.
    - By the mid-1970s, NPN and NMOS transistors had replaced the slower PNP and PMOS transistors.
  - Since the early 1980s, CMOS (complementary MOS) has become the dominant method of IC design.

25.1: OVERVIEW OF IC TECHNOLOGY
MOS vs.bipolar transistors

- There are two type of transistors: bipolar and MOS (metal-oxide semiconductor), both have three leads.
  - In bipolar transistors, the three leads are referred to as the *emitter*, *base*, *and collector*.
    - The carrier flows from the emitter to the collector, and the base is used as a flow controller.
  - In MOS transistors they are *source*, *gate*, *and drain*.
    - The carrier flows from the source to the drain, and the gate is used as a flow controller.

25.1: OVERVIEW OF IC TECHNOLOGY
MOS vs.bipolar transistors

- In NPN-type bipolar transistors, the electron carrier leaving the emitter must overcome two voltage barriers before it reaches the collector.
  - One is the N-P junction of the emitter-base.
  - The other is the P-N junction of the base-collector.

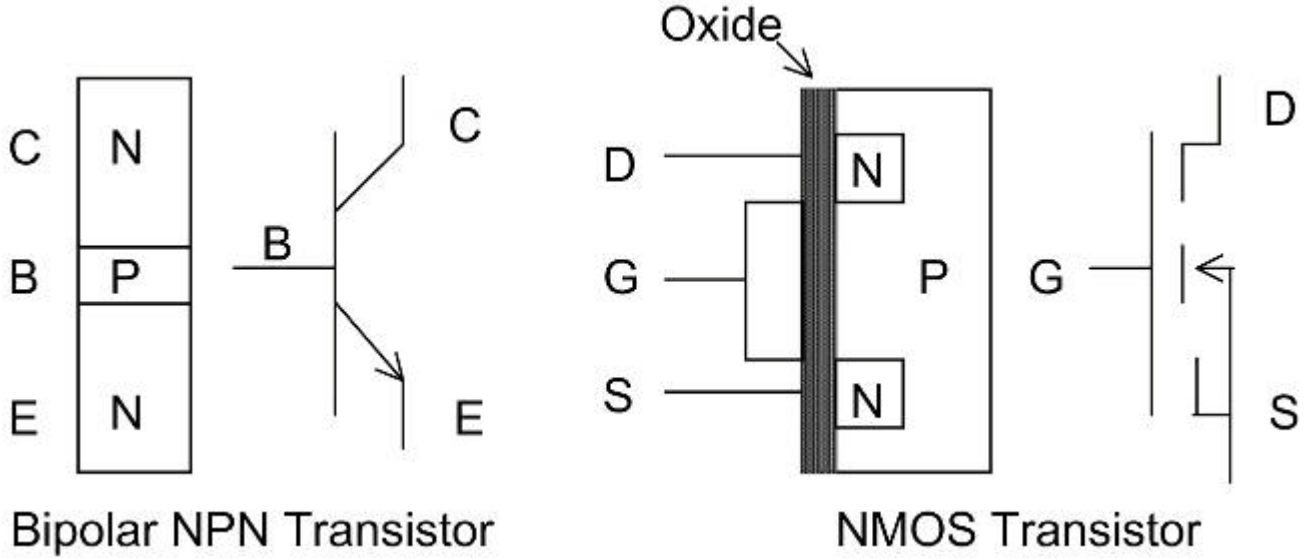


Fig. 25-1
Bipolar vs.
MOS Transistors

25.1: OVERVIEW OF IC TECHNOLOGY
MOS vs.bipolar transistors

- The voltage barrier of the reversed biased base-collector is the most difficult one for the electrons to overcome, and causes the most power dissipation.
  - This led to the unipolar type transistor called MOS.
    - Electrons reach the drain without any voltage barrier.
- Absence of voltage barrier is one reason why MOS dissipates much less power than bipolar transistors.
  - Allowing millions of transistors on a single IC chip.
    - Without the MOS transistor, the desktop personal computer would not have been possible, at least not so soon
  - MOS transistors are slower than bipolar transistors.
    - Due partly to the gate capacitance of the MOS transistor

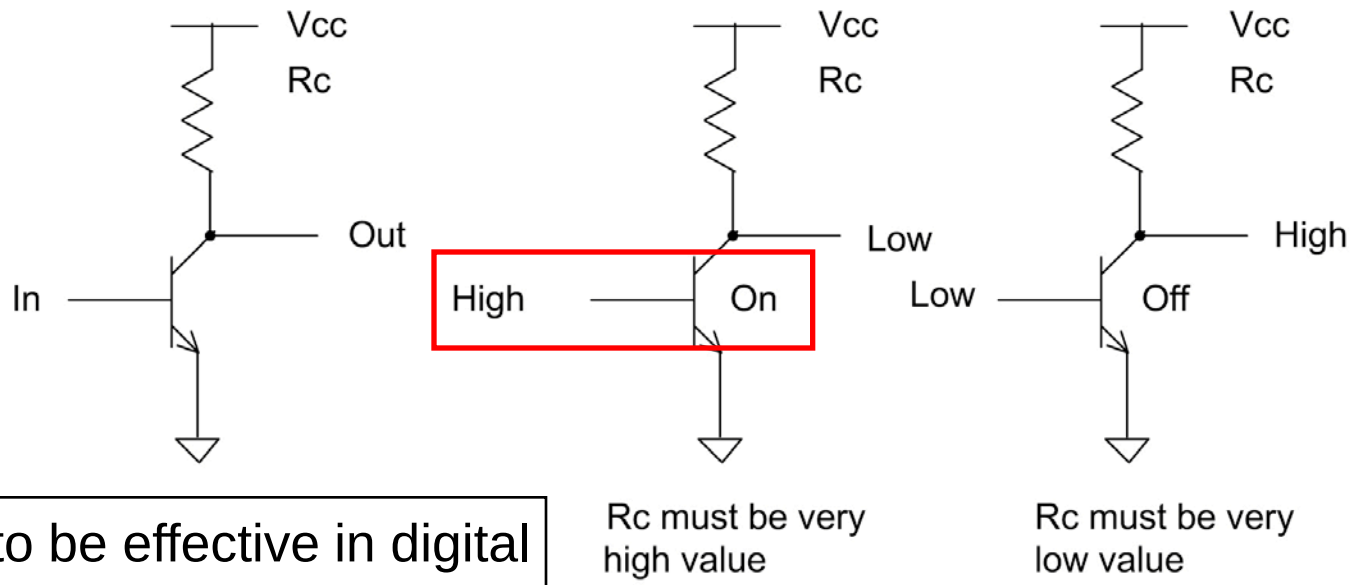
25.1: OVERVIEW OF IC TECHNOLOGY
overview of logic families

- Logic families are judged according to…
  - Speed; Power dissipation; Noise immunity.
  - Input/output interface compatibility; Cost.
- Desirable qualities are high speed, low power dissipation, and high noise immunity
- In interfacing logic families, the more inputs that can be driven by a single output, the better.
  - High-driving-capability outputs are desired.
- Cost of a given logic family is high during the early years of its introduction.
  - Prices decline as production and use rise.

25.1: OVERVIEW OF IC TECHNOLOGY
the case of inverters

- In a one-transistor inverter, while the transistor plays the role of a switch, **R** is the pull-up resistor.

Fig. 25-2
One-Transistor Inverter with Pull-up Resistor



Rc must be very high value

Rc must be very low value

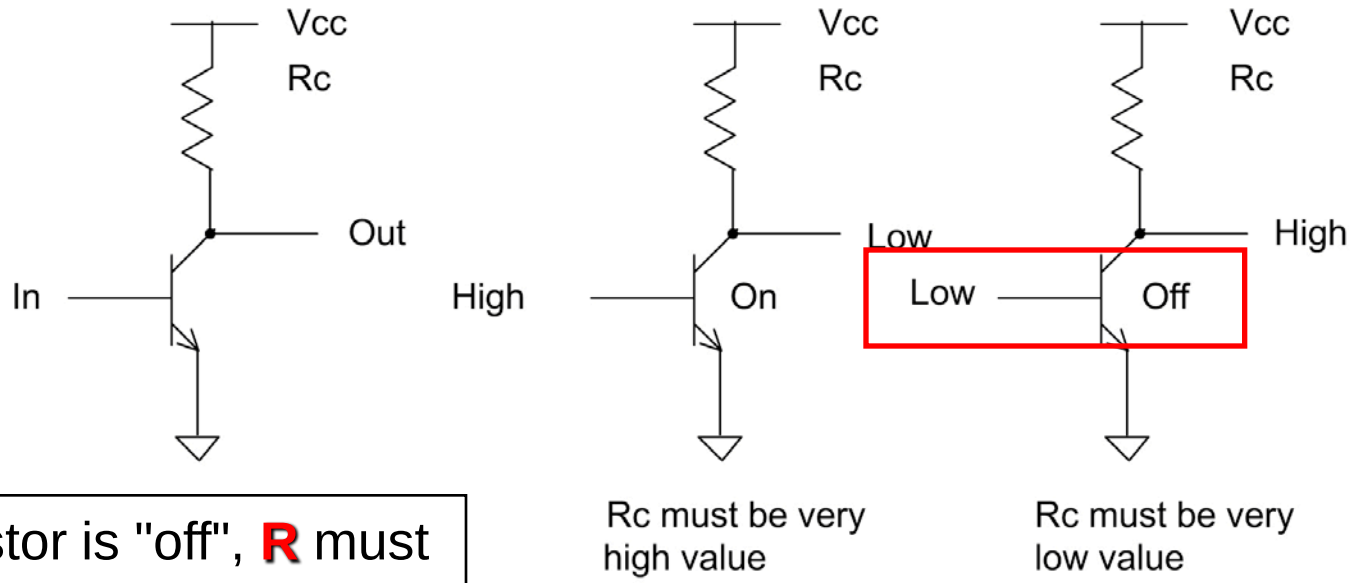
For this inverter to be effective in digital circuits, the **R** value must be *high* when the transistor is "on" to limit the current flow from $\mathbf{V_{CC}}$ to ground in order to have low power dissipation.

P = VI, where V = 5 V

25.1: OVERVIEW OF IC TECHNOLOGY
the case of inverters

- In a one-transistor inverter, while the transistor plays the role of a switch, **R** is the pull-up resistor.

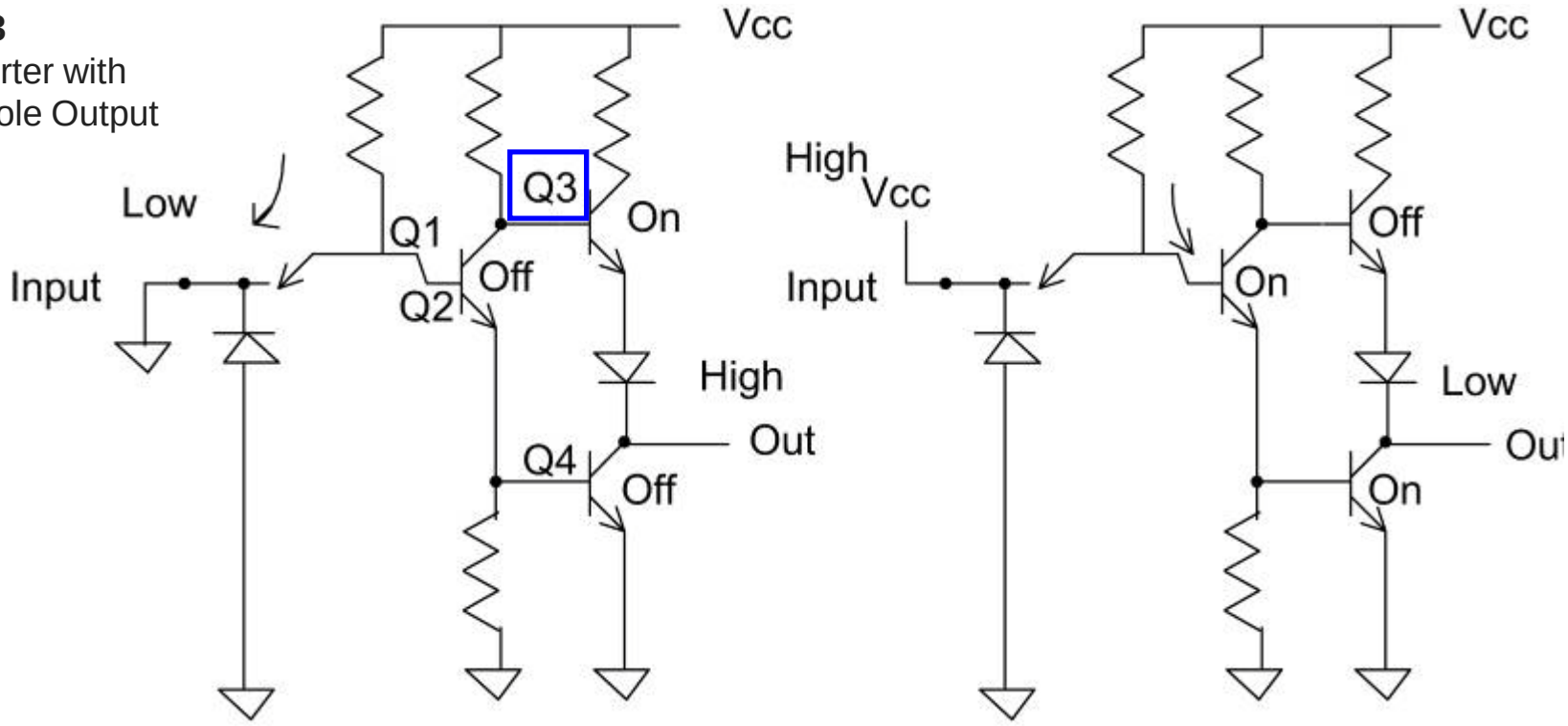
Fig. 25-2
One-Transistor Inverter with Pull-up Resistor



When the transistor is "off", **R** must be a small value to limit the voltage drop across **R**, making sure that V_{OUT} is close to V_{CC}. This is a contradictory demand on **R**.

25.1: OVERVIEW OF IC TECHNOLOGY
the case of inverters

Fig. 25-3
TTL Inverter with
Totem-Pole Output



Logic gate designers use active components (transistors) instead of passive components (resistors) to implement pull-up resistor **R**.

A TTL inverter with totem pole output is shown. **Q3** plays the role of a pull-up resistor.

25.1: OVERVIEW OF IC TECHNOLOGY
CMOS inverter

- In CMOS-based logic gates, PMOS and NMOS are used to construct a CMOS (complementary MOS) inverter.

In CMOS inverters, when the PMOS transistor is *off*, it provides a very high impedance path, making leakage current almost zero (about 10 nA).

When PMOS is *on*, it provides a low resistance on the path of $\mathbf{V_{DD}}$ to load.

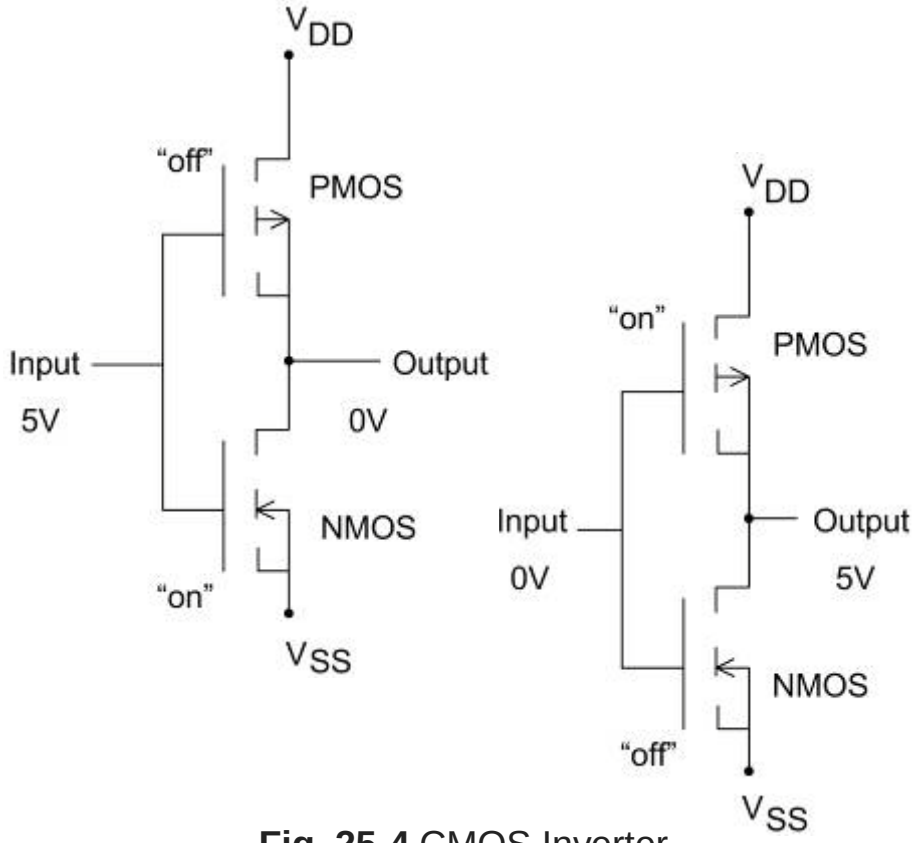


Fig. 25-4 CMOS Inverter

25.1: OVERVIEW OF IC TECHNOLOGY
i/o characteristics of logic families

- In 1968 the first logic family made of bipolar transistors was marketed, commonly referred to as the standard TTL (transistor-transistor logic) family.
- The first MOS-based logic family, the CD4000/74C series, was marketed in 1970.
- Addition of the Schottky diode to the base-collector of early 70s bipolar transistors led to the S family.
  - The Schottky diode shortens propagation delay of the TTL family by preventing the collector from going into what is called deep saturation.

25.1: OVERVIEW OF IC TECHNOLOGY
history of logic families

In the mid-1970s, 5V V_{cc} became standard.

Table 25-1: Characteristics of Some Logic Families

Characteristic	STD TTL	LSTTL	ALSTTL	HCMOS
V_{CC}	5 V	5 V	5 V	5 V
V_{IH}	2.0 V	2.0 V	2.0 V	3.15 V
V_{IL}	0.8 V	0.8 V	0.8 V	1.1 V
V_{OH}	2.4 V	2.7 V	2.7 V	3.7 V
V_{OL}	0.4 V	0.5 V	0.4 V	0.4 V
I_{IL}	−1.6 mA	−0.36 mA	−0.2 mA	−1 μA
I_{IH}	40 μA	20 μA	20 μA	1 μA
I_{OL}	16 mA	8 mA	4 mA	4 mA
I_{OH}	−400 μA	−400 μA	−400 μA	4 mA
Propagation delay	10 ns	9.5 ns	4 ns	9 ns
Static power dissipation (f = 0)	10 mW	2 mW	1 mW	0.0025 nW
Dynamic power dissipation at f = 100 kHz	10 mW	2 mW	1 mW	0.17 mW

25.1: OVERVIEW OF IC TECHNOLOGY
history of logic families

- In the late 1970s, advances allowed combining the speed & drive of the S family with the lower power of LS to form a new logic family called FAST
  - Fairchild Advanced Schottky TTL.
- In 1985, AC/ACT (Advanced CMOS Technology), a higher speed version of HCMOS, was introduced.
  - With the introduction of FCT (Fast CMOS Technology) in 1986, the speed gap between CMOS & TTL closed.
  - FCT is the CMOS version of FAST, has the low power consumption of CMOS but speed comparable with TTL.

25.1: OVERVIEW OF IC TECHNOLOGY
history of logic families

Table 25-2: Logic Family Overview

Product	Year Introduced	Speed (ns)	Static Supply Current (mA)	High/Low Family Drive (mA)
Std TTL	1968	40	30	−2/32
CD4K/74C	1970	70	0.3	−0.48/6.4
LS/S	1971	18	54	−15/24
HC/HCT	1977	25	0.08	−6/−6
FAST	1978	6.5	90	−15/64
AS	1980	6.2	90	−15/64
ALS	1980	10	27	−15/64
AC/ACT	1985	10	0.08	−24/24
FCT	1986	6.5	1.5	−15/64

25.1: OVERVIEW OF IC TECHNOLOGY
recent advances in logic families

- As speed of high-performance processors reached 25 MHz, it shortened CPU cycle time, leaving less time for the *path delay*.
  - Manufacturers have responded to this need by providing logic families with high speed, low noise, and high drive.

25.1: OVERVIEW OF IC TECHNOLOGY
recent advances in logic families

- ACQ/ACTQ are the second-generation advanced CMOS (ACMOS) with much lower noise.
  - ACQ has the CMOS input level.
  - ACQT is equipped with TTL-level input.
- FCTx and FCTx-T are second-generation FCT with much higher speed.
  - The x refers to various speed grades, such as A, B & C
    - Where A means low speed and C means high speed.
- FASTr is an ideal choice, as it is faster, has higher driving capability (IOL, IOH), and produces much lower noise than FAST.

25.1: OVERVIEW OF IC TECHNOLOGY
recent advances in logic families

- In recent years, a 3.3V $\mathbf{V_{cc}}$ with higher speed and lower power consumption has become standard.
- Combining high-speed bipolar TTL & low power consumption CMOS has led to BICMOS.
  - Although expensive due to extra steps required in fabrication, in some cases there is no other choice.

25.1: OVERVIEW OF IC TECHNOLOGY
recent advances in logic families

Table 25-3: Advanced Logic General Characteristics

Family	Year	Number Suppliers	Tech Base	I/O Level	Speed (ns)	Static Current	I_{OH}/I_{OL}
ACQ	1989	2	CMOS	CMOS/CMOS	6.0	80 μA	−24/24 mA
ACTQ	1989	2	CMOS	TTL/CMOS	7.5	80 μA	−24/24 mA
FCTx	1987	3	CMOS	TTL/CMOS	4.1–4.8	1.5 mA	−15/64 mA
FCTxT	1990	2	CMOS	TTL/TTL	4.1–4.8	1.5 mA	−15/64 mA
FASTr	1990	1	Bipolar	TTL/TTL	3.9	50 mA	−15/64 mA
BCT	1987	2	BICMOS	TTL/TTL	5.5	10 mA	−15/64 mA

Table 25-4: Importance of Speed

System Clock Speed (MHz)	Clock Period (ns)	Predominant Logic for Path
2–10	100–500	HC, LS
10–30	33–100	ALS, AS, FAST, FACT
30–66	15–33	FASTr, BCT, FCTA

25.1: OVERVIEW OF IC TECHNOLOGY
evolution of IC technology in Intel x86

- Early Intel processors (4004 & 8008) used PMOS.
  - 8080, 8085, 8088, 8086, & 80286 all used NMOS when first introduced.

Table 25-5: Intel Microprocessor Evolution

Microprocessor	Year	IC Tech	Line Thickness (μm)	Power Supply (V)	Number of Transistors
8086	1978	NMOS	3.0	5	29,000
80286	1982	NMOS	1.5	5	134,000
80386	1985	CMOS	1.5	5	275,000
80486	1989	CMOS	1.0	5	1.2 million
Pentium I	1993	BICMOS	0.8	5	3.1 million
Pentium II	1997	BICMOS	0.25	3.3	7.5 million
Pentium III	1999	BICMOS	0.18	3.3	9.5 million
Pentium IV	2000	BICMOS	0.18	3.3	42 million

25.1: OVERVIEW OF IC TECHNOLOGY
evolution of IC technology in Intel x86

- Currently, CMOS is the universal technology in the design of microprocessors.
  - Only BICMOS could allow designers to put over 3 million transistors on a single chip, make it work at 1 GHz, and consume around 10 watts of power.
- There has been a steady decline in the transistor's dimensions from the 1980s to the 2000s.
  - The thickness of the lines inside the IC, has come from a few microns to a fraction of a micron.

25.1: OVERVIEW OF IC TECHNOLOGY
evolution of IC technology in Intel x86

- Early microprocessors used power supplies with negative (–) and positive (+) voltages.
  - The +5 V power supply has become standard.
    - To reduce power consumption, 3.3V $\mathbf{V_{cc}}$ is being embraced.
- Lowering $\mathbf{V_{cc}}$ to 3.3 V has two major advantages:
  - (1) Lowers power consumption, resulting in prolonged battery life in laptops or hand-held PDA devices
  - (2) Allows a further reduction of line size (design rule) to submicron dimensions, resulting in more transistors in a given die size.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES

- There are several issues to be considered in designing a microprocessor-based system:
  - IC fan-out.
  - Capacitance derating.
  - Ground bounce.
  - VCC bounce.
  - Crosstalk.
  - Transmission lines.
  - Power dissipation.
  - Chip failure analysis.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

- *How many inputs can an output signal drive?*
  - Must be addressed for both logic "0" & logic "1" outputs.
- Fan-out for *low* and fan-out for high are as follows:

$$\text{fan-out (of low)} = \frac{I_{OL}}{I_{IL}} \qquad \text{fan-out (of high)} = \frac{I_{OH}}{I_{IH}}$$

Of the above two values the lower number is used to ensure the proper noise margin.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

Sinking & sourcing of current when ICs are connected.

As the number of inputs connected to output increases, I_{OL} rises, which causes V_{OL} to rise.

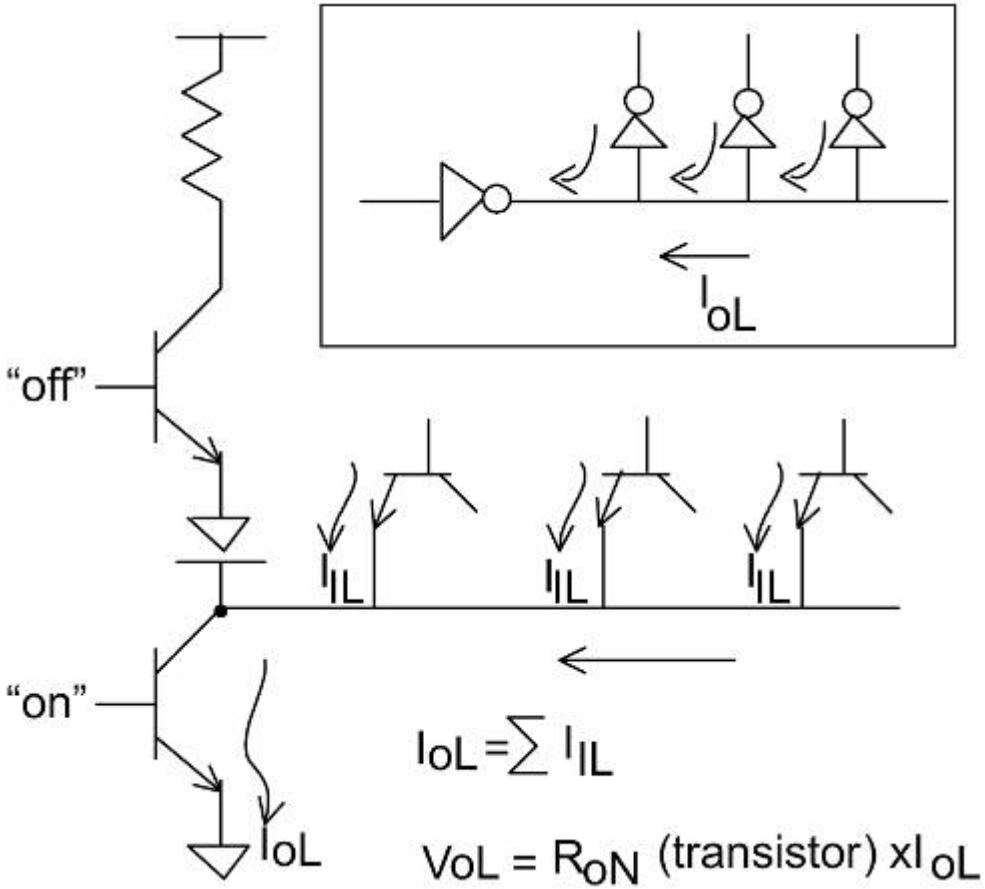


Fig. 25-5a Current Seeking and Sourcing in TTL

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

Sinking & sourcing of current when ICs are connected.

If this continues, the rise of V_{OL} makes the noise margin smaller, and this results in the occurrence of false logic due to the slightest noise.

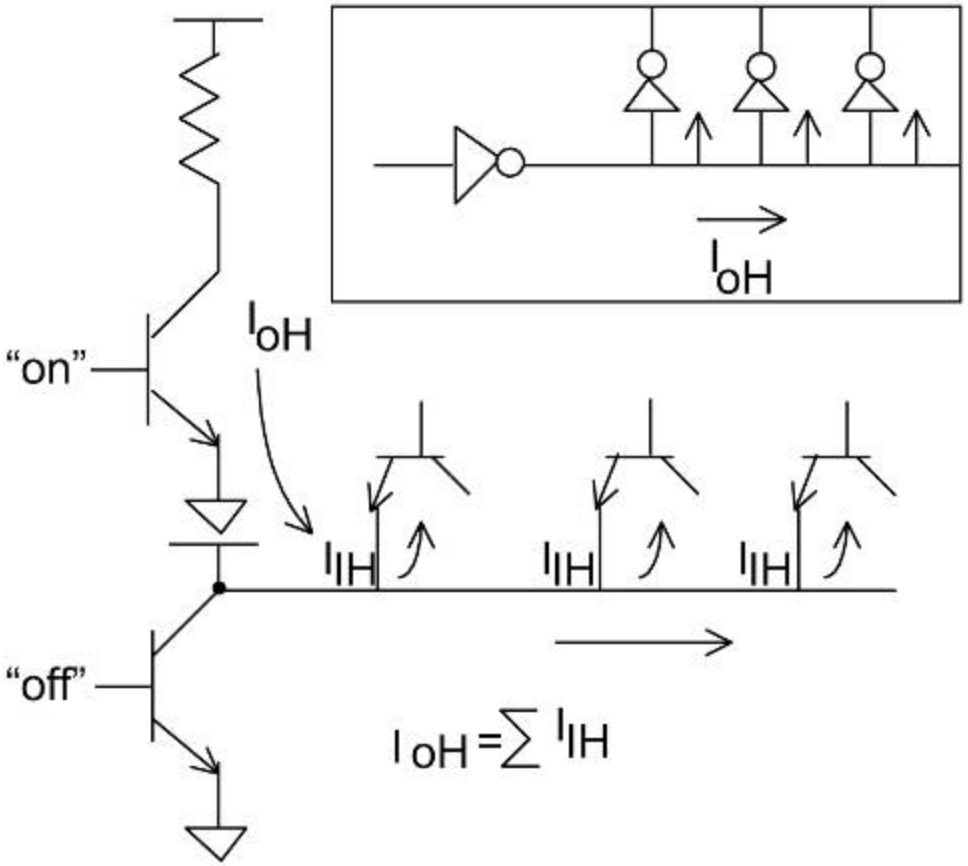


Fig. 25-5b Current Seeking and Sourcing in TTL

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

In designing the system, very often an output is connected to various kinds of inputs.

Example 25-1

Find how many unit loads (UL) can be driven by the output of the LS logic family.

Solution:

The unit load is defined as $I_{IL} = 1.6$ mA and $I_{IH} = 40$ A. Table 25-1 shows $I_{OH} = 400$ A and $I_{OL} = 8$ mA for the LS family. Therefore, we have

$$\text{fan-out (low)} = I_{OL}/I_{IL} = 8 \text{ mA} / 1.6 \text{ mA} = 5$$

$$\text{fan-out (high)} = I_{OH}/I_{IH} = 400 \text{ µA} / 40 \text{ µA} = 10$$

This means that the fan-out is 5. In other words, the LS output must not be connected to more than 5 inputs with unit load characteristics.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

In designing the system, very often an output is connected to various kinds of inputs.

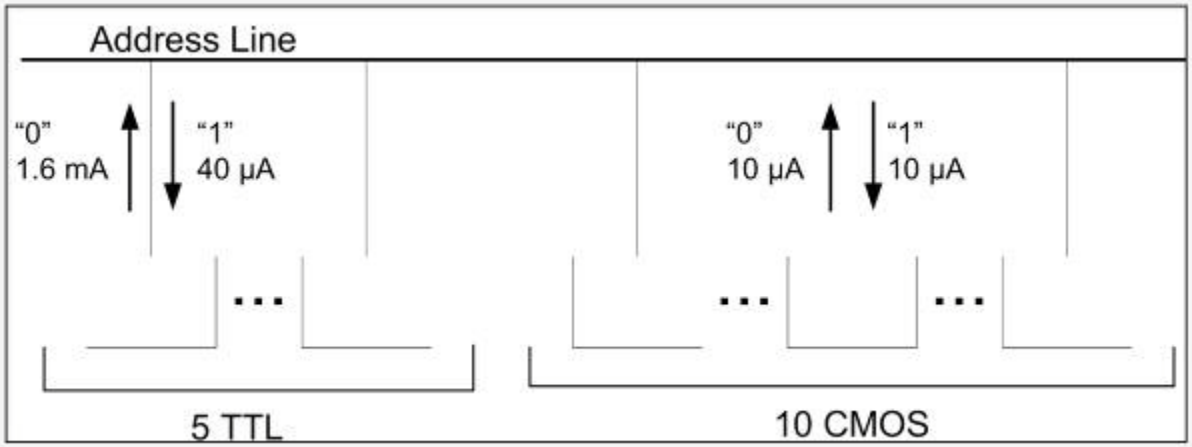
Example 25-2 An address pin needs to drive 5 standard TTL loads in addition to 10 CMOS inputs of DRAM chips. Calculate the minimum current to drive these inputs for both logic "0" and "1".

Solution:

The standard load for TTL is $I_{IH} = 40$ A and $I_{IL} = 1.6$ mA, and for CMOS, $I_{IL} = I_{IH} = 10$ A.

minimum current for "0" = total of all $I_{IL} = 5 \times 1.6$ mA $+ 10 \times 10$ A $= 8.1$ mA

minimum current for "1" = total of all $I_{IH} = 5 \times 40$ A $+ 10 \times 10$ A $= 300$ A



25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
IC fan-out

Total I_{IL} & I_{IH} requirement of all the loads on a given output must be less than the driver's maximum I_{oL} & I_{OH}

Example 25-3

Assume that the microprocessor address pin in Example 25-2 has specifications I_{OH} = 400 A and I_{OL} = 2 mA. Do the input and output current needs match?

Solution:

For a high output state, there is no problem since $I_{OH} > I_{IH}$. However, the number of inputs exceeds the limit for I_{OL} since an I_{IL} of 8.1 mA is much larger than maximum I_{OL} allowed by the processor.

When receiver current requirements exceed driver capability, a buffer must be used.

74xx245 is used for bidirectional and 74xx244 for unidirectional signals.

Table 25-6: Electrical Specifications for Buffers

Note: VOL = 0.4 V and VOH = 2.4 V are assumed.

Buffer	IOH (mA)	IOL (mA)	IIH (µA)	IIL (mA)
74LS244	3	12	20	0.2
74LS254	3	12	20	0.2

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
capacitance derating

- A pin of an IC has an input capacitance of 5 to 7 pF.
  - A single output driving many inputs sees a large capacitance load, since the inputs are in parallel.
    - And therefore added together.

Consider these equations:

$$Q = CV$$

$$\frac{Q}{T} = \frac{CV}{T}$$

$$F = \frac{1}{T}$$

$$I = CVF$$

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
capacitance derating

$$I = CVF$$

I is the driving capability of the output pin.
C is $\mathbf{C_{IN}}$, as seen by the output.
V is the voltage.

- As the number of $\mathbf{C_{IN}}$ loads goes up, there must be a corresponding increase in **IO**, the driving capability of the output.
  - Outputs with high values of $\mathbf{I_{OL}}$ & $\mathbf{I_{OH}}$ are desirable.
- If ***I*** = constant, as ***C*** goes up, ***F*** must come down, resulting in lower speed.
  - The most widely accepted solution is the use of a large number of drivers to reduce the load capacitance seen by a given output.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
capacitance derating

- Assume a single address bus line driving 16 banks of 32-bit-wide memory.
  - Each bank has 4 chips of 64K x 8 organization, which results in 16 x 4 = 64 memory chips, or 16 x 64K x 32 = 32M bytes of SRAM.
  - Depending on how many 244s are used to drive the memory addresses, the delay due to the address path varies substantially.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
two 244 drivers

- This option uses two 244 drivers, one for A0–A7 and one for A8–A15.
  - An output of the 244 drives 16 banks of memory, each with 4 inputs.
  - Assuming each memory input has 5 pF capacitance:
    - A total of 4 x16 x 5 = 320 pF capacitance load seen by the 244.
- Since the 244 output can handle no more than 50 pF, the delay due to extra capacitance must be added to the address path delay.
  - For each 50 to 100 pF of capacitance, an extra 3 ns delay is added to the address path delay.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
two 244 drivers

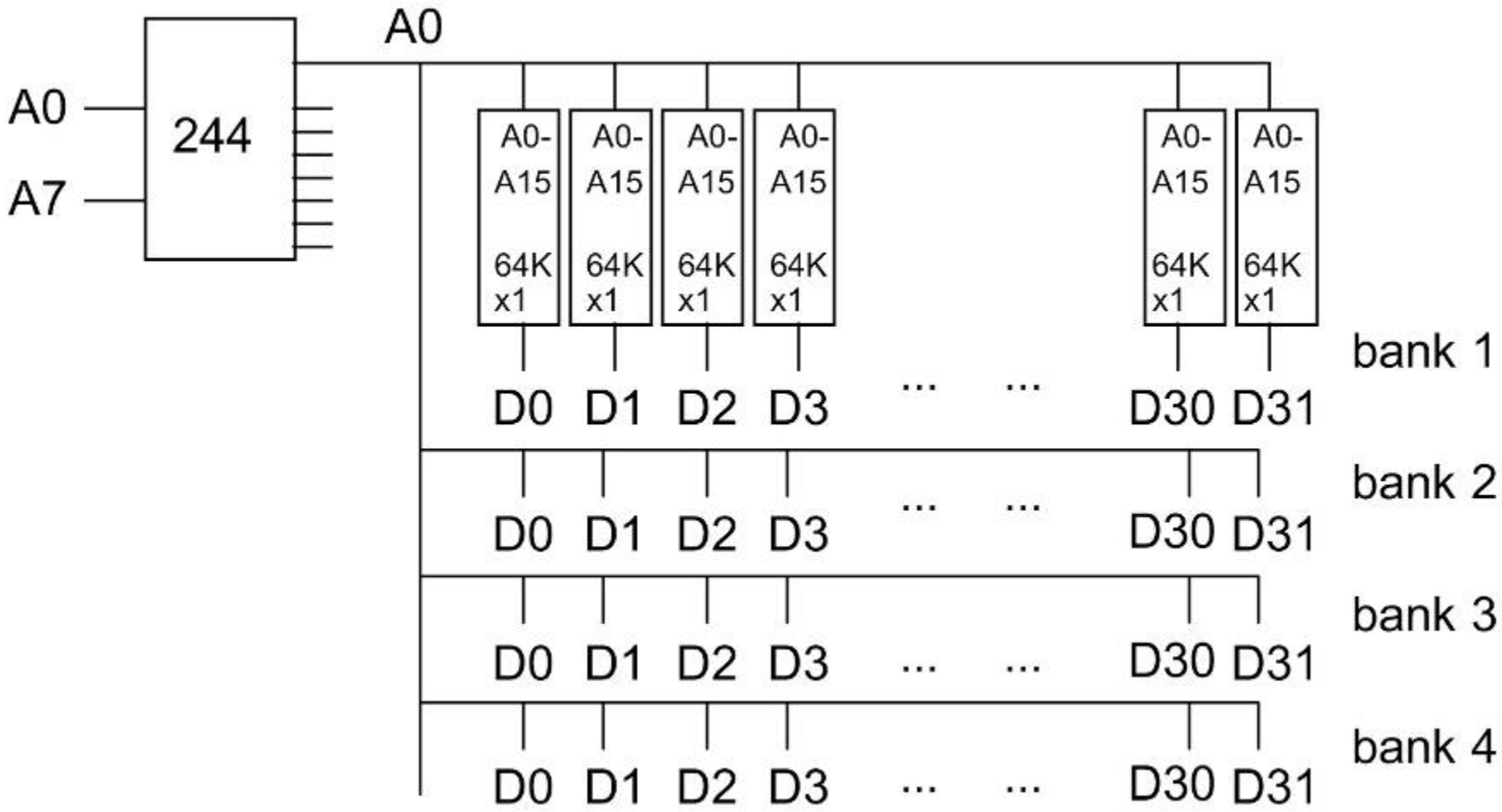


Fig. 25-6 Case 1:Two 244 Address Drivers (the second 244 for A8 –A15 is not shown)

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
two 244 drivers

Example 25-4

Calculate the following for Figure 25-6, assuming a memory access time of 25 ns and a propagation delay of 10 ns for the 244.
(a) delay due to capacitance derating on the address path
(b) the total address path delay for case 1

Solution:

(a) Of the 320 pF capacitance seen by the 244, only 50 pF is taken care of; the rest, which is 270 (320 – 50 = 270), causes a delay. Since there are 3 ns for each extra 100 pF, we have the following delay due to capacitance derating, (270/100) × 3 ns = 8.1 ns.
(b) Address path delay = 244 buffer propagation delay + capacitance derating delay + memory access time = 10 ns + 8.1 ns + 25 ns = 43.1 ns.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES doubling the number of 244 buffers

- Doubling the number of 244 buffers will reduce the address path delay.
  - A single 244 drives only 8 banks, or a total of 32 inputs, since there are 4 inputs in each bank.
    - A 244 output will see a capacitance load of 32 x 5 = 160 pF.

Example 25-5

Calculate (a) delay due to capacitance derating on the address path, and (b) total address path delay for case 2. Assume a memory access time of 25 ns and a propagation delay of 10 ns for the 244.

Solution:

(a) Of the 160 pF capacitance seen by the 244, only 50 pF is taken care of; the rest, which is 110 pF, causes a delay. Since there are 3 ns for each extra 100 pF, we have (110/100) × 3 ns = 3.1 ns delay due to capacitance derating.
(b) The address path delay = 244 buffer propagation delay + capacitance derating delay + memory access time = 10 ns + 3.1 ns + 25 ns = 28.1 ns.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES doubling again

- Doubling the number of 244 buffers *again*, so a 244 output drives four banks, each with 4 inputs.
  - Resulting in a total capacitance load of 4 x 4 x 5 = 80 pF.
    - The 244 handles only 50 pF, leaving 30 pF, causing a delay.

For high-speed system design a higher cost due to extra parts & higher power consumption must be accepted.

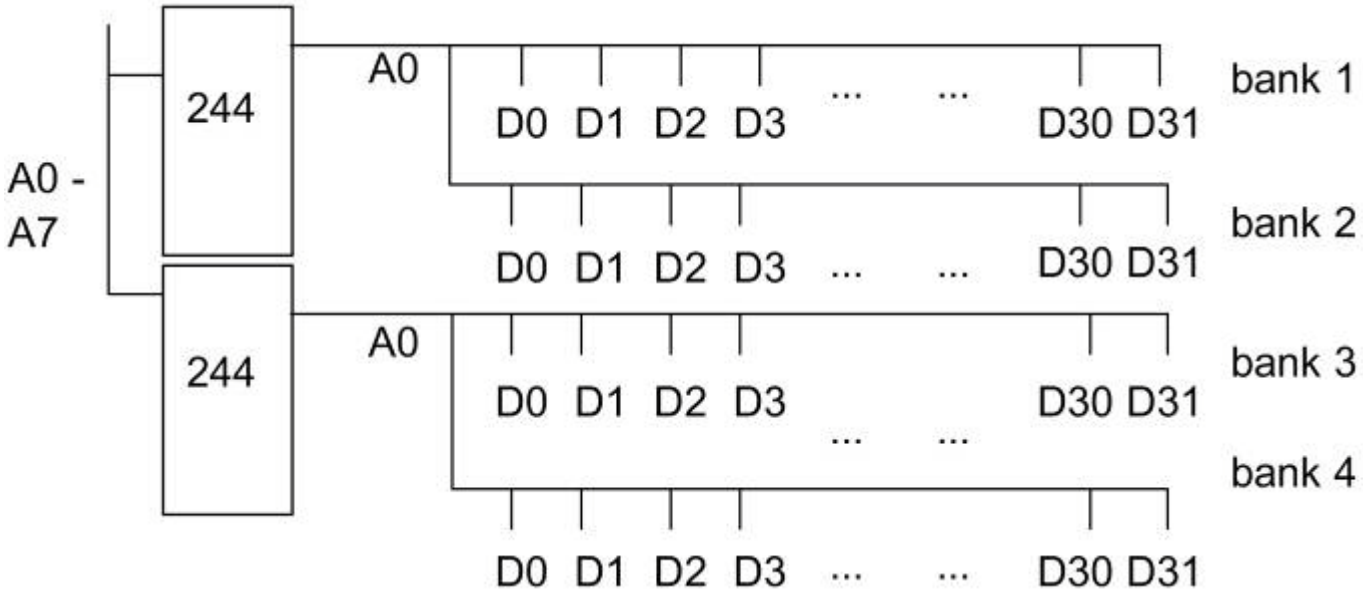


Fig. 25-7
Case 2:Four 244 Address Drivers (the two 244s for A8 –A15 are not shown)

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
power dissipation considerations

- Although power dissipation is a function of the total current consumption of all components of a system, impact of $\mathbf{V_{CC}}$ is much more pronounced.
- Equation (26-4) showed that ***I*** = ***CFV***.
  - Substituting this in equation ***P*** = ***VI*** yields the following:

$$F = VI = CFV^2$$

While power dissipation goes up *linearly* with frequency, impact of power supply voltage is *squared*.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
power dissipation considerations

- Although power dissipation is a function of the total current consumption of all components of a system, impact of V_{CC} is much more pronounced.

Example 25-6

Prove that a 3.3 V system consumes 56% less power than a system with a 5 V power supply.

Solution:

Since $P = VI$, by substituting $I = V/R$, we have $P = V^2/R$. Assuming that $R = 1$, we have $P (3.3)^2 = 10.89$ W and $P = (5)^2 = 25$ W. This results in using 14.11 W less ($25 - 10.89 = 14.11$), which means a 56% power saving ($14.11 \text{ W}/25 \text{ W} \times 100 = 56\%$).

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
dynamic and static currents

- There are two major types of currents flowing through an IC: dynamic and static.
  - A dynamic current is a function of the frequency under which the component is working, seen in Equation (25-4).
    - As frequency goes up, dynamic current & power dissipation go up.
  - Static current, also called **dc**, is the current consumption of the component when it is inactive (not selected).

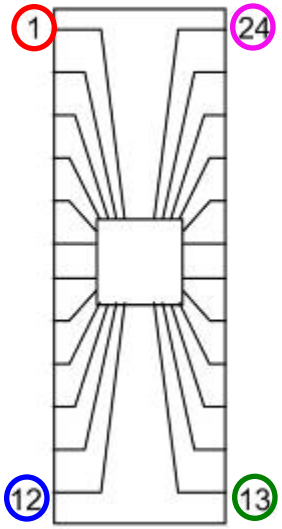
25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
power-down option

- Today processors have what is called system management mode (SMM), which reduces energy consumption by turning off peripherals or the entire system when not in use.
  - Effects on the 3.3 V power supply translate into a power savings of up to 56% over systems with a 5 V power supply.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
ground bounce

- There is a certain capacitance, resistance, and inductance associated with each pin of the IC.
  - The size of these elements varies depending on many factors such as length, area, etc.

Pin	Self-inductance	Capacitance
1	15.10 nH	1.86 pF
2	12.20 nH	1.70 pF
3	9.54 nH	1.29 pF
4	7.44 nH	0.95 pF
5	5.31 nH	0.61 pF
6	3.73 nH	0.43 pF
7	3.41 nH	0.43 pF
8	4.66 nH	0.61 pF
9	6.95 nH	0.95 pF
10	8.96 nH	1.29 pF
11	11.70 nH	1.70 pF
12	14.50 nH	1.86 pF



Pin	Self-inductance	Capacitance
13	14.50 nH	1.86 pF
14	11.70 nH	1.70 pF
15	8.96 nH	1.29 pF
16	6.95 nH	0.95 pF
17	4.66 nH	0.61 pF
18	3.41 nH	0.43 pF
19	3.73 nH	0.43 pF
20	5.31 nH	0.61 pF
21	7.44 nH	0.95 pF
22	9.54 nH	1.29 pF
23	12.20 nH	1.70 pF
24	15.10 nH	1.86 pF

Fig. 25-9 Inductance and Capacitance of 24-pin DIP

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
ground bounce

- Capacitance has three components:
  - Resistance; Inductance; Self-inductance
- The inductance of the IC pins, commonly referred to as *self-inductance,* causes the most problems in high-frequency system design.
  - It can result in *ground bounce*, when a massive amount of current flows through the ground pin when multiple outputs change from *high* to *low* all at the same time.

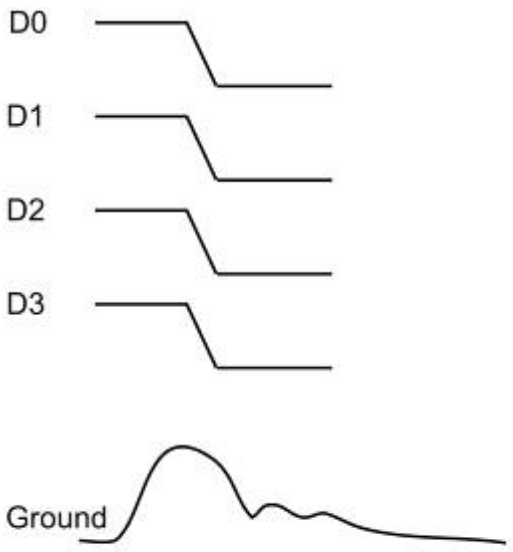
25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
ground bounce

The voltage relation to the induction of the ground lead is as follows:

$$V = L \frac{d_i}{d_t}$$

As system frequency increases, rate of dynamic current, **di/dt**, is also increased, with an increase in the inductance voltage **L** (**di/dt**) of the ground pin.

The *low state* (ground) has a small noise margin, so any extra voltage due to inductance voltage can cause a false signal.



Ground bounce occurs when data switches from all 1s to all 0s

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
filtering the transient currents using decoupling

- To reduce ground bounce:
  - Locate the $\mathbf{V_{cc}}$ & ground pins in the middle of the chip
  - Use logics with a minimum number of outputs.
  - Use as many pins as possible for the $\mathbf{V_{cc}}$ & ground.

Self-inductance of a wire with length ***l*** and a cross section of ***B*** x ***C*** is:

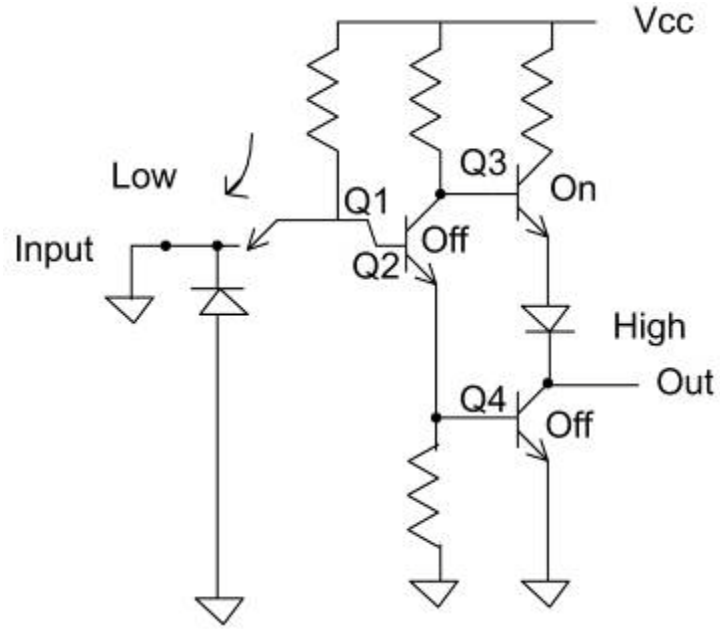
$$L = 0.002 \ln\left(\frac{2l}{B+C} + \frac{l}{2}\right)$$

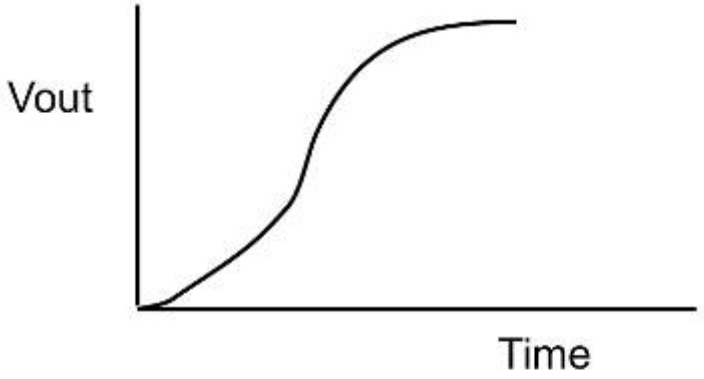
Wire length, ***l***, contributes more to self-inductance than does the cross section.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
filtering the transient currents using decoupling

- In the TTL family, the change of the output from *low* to *high* can cause what is called *transient current*.

In totem-pole output, when output is *low*, **Q4** is on & saturated, **Q3** is off.





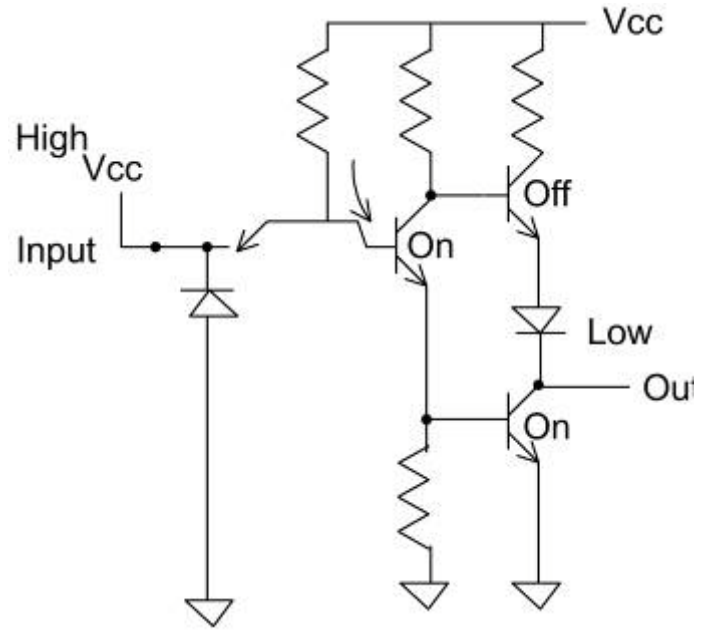
There is a time that both transistors are on & drawing currents from the $\mathbf{V_{CC}}$.

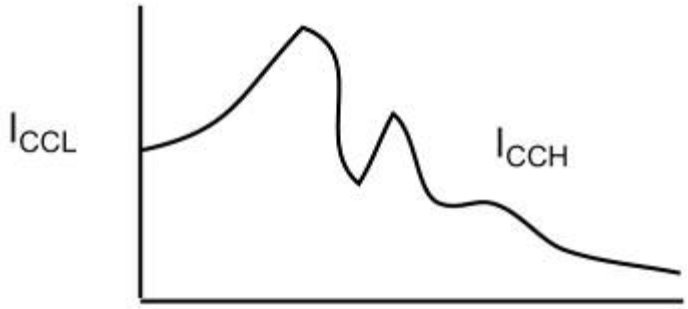
The amount depends on the $\mathbf{R_{ON}}$ values of the transistors.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
filtering the transient currents using decoupling

- In the TTL family, the change of the output from *low* to *high* can cause what is called *transient current*.

In changing output from low to high state, **Q3** becomes *on,* and **Q4** *off*.





The net effect is a large spike in the output current.

A 0.01 F or 0.1 F ceramic disk capacitor placed between $\mathbf{V_{CC}}$ & ground for each TTL IC will filter the transient current.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
bulk decoupling capacitor

- As many IC chips change state at the same time, combined currents drawn from the board's $\mathbf{V_{CC}}$ power supply can be massive.
  - Causing fluctuation of $\mathbf{V_{CC}}$ on the board where all the ICs are mounted.
    - A relatively large tantalum capacitor is placed between the $\mathbf{V_{CC}}$ and ground lines will eliminate this.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
crosstalk

Crosstalk is due to *mutual inductance*, caused by two electric lines running parallel to each other.

(electromagnetic interference or EMI)

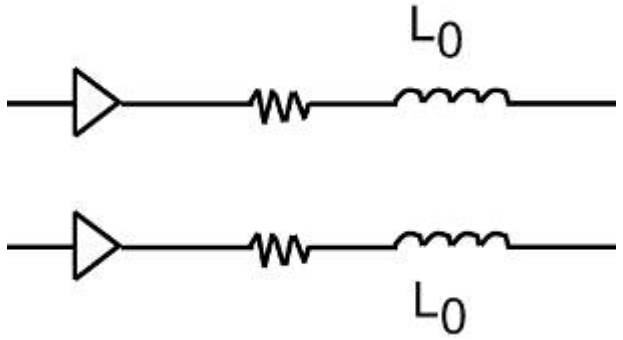


Fig. 25-11 Crosstalk (EMI)

$$M = 0.002\, l \ln\frac{2l}{d} - \ln\left(\frac{2l}{B+C} + \frac{l}{2}\right)$$

The effect of crosstalk can be reduced by increasing the distance between parallel or adjacent lines. (or circuit boards traces).

…where ***l*** is the length of two conductors running in parallel, & ***d*** is the distance between them.

The medium material placed in between affects ***K***.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
transmission line ringing

Ringing

The square wave in digital circuits is made of a single fundamental pulse & many harmonics of various amplitudes

When the signal travels on the line, not all harmonics respond the same way to the capacitance, inductance & resistance of the line.

This causes *ringing*, and depends on the thickness and the length of the line driver, among other factors.

In high-frequency systems, wire traces on the printed circuit board (PCB) behave like transmission lines, causing ringing.

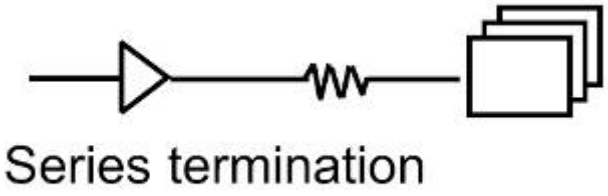
The severity of this ringing depends on the speed and the logic family used.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES transmission line ringing

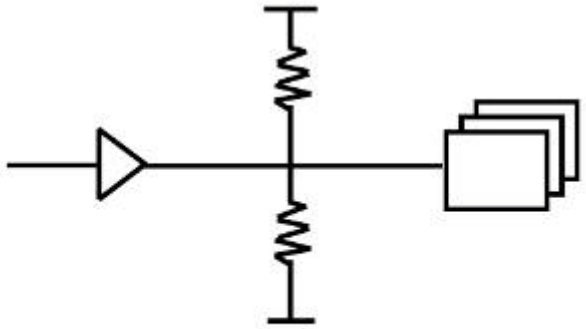
- Three major methods of line driver termination:
  - Parallel; Serial; Thevenin.
    - Parallel and Thevenin methods when there is a need to match impedance of the line with load impedance.

Table 25-8: Line Length Beyond Which Traces Behave Like Transmission Lines

Logic Family	Line Length (in.)
LS	25
S, AS	11
F, ACT	8
AS, ECL	6
FCT, FCTA	5



Series termination



Parallel termination

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
FIT and failure analysis

- Chip manufacturers provide a parameter called FIT (*failure in time*) to measure reliability of a single chip.
  - The FIT of a single chip is the number of expected failures in a billion (10^9) hours of operation.
- Manufacturers use burn-in to eliminate early failures before the product is shipped to the customer.
  - Commonly referred to as infant mortality, since the failure rate starts high and eventually levels off to a constant level.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
FIT and failure analysis

- Although early failures can be eliminated using burn-in, failure rate can never be reduced to zero.
  - Due to wearout and other factors such as soft error.

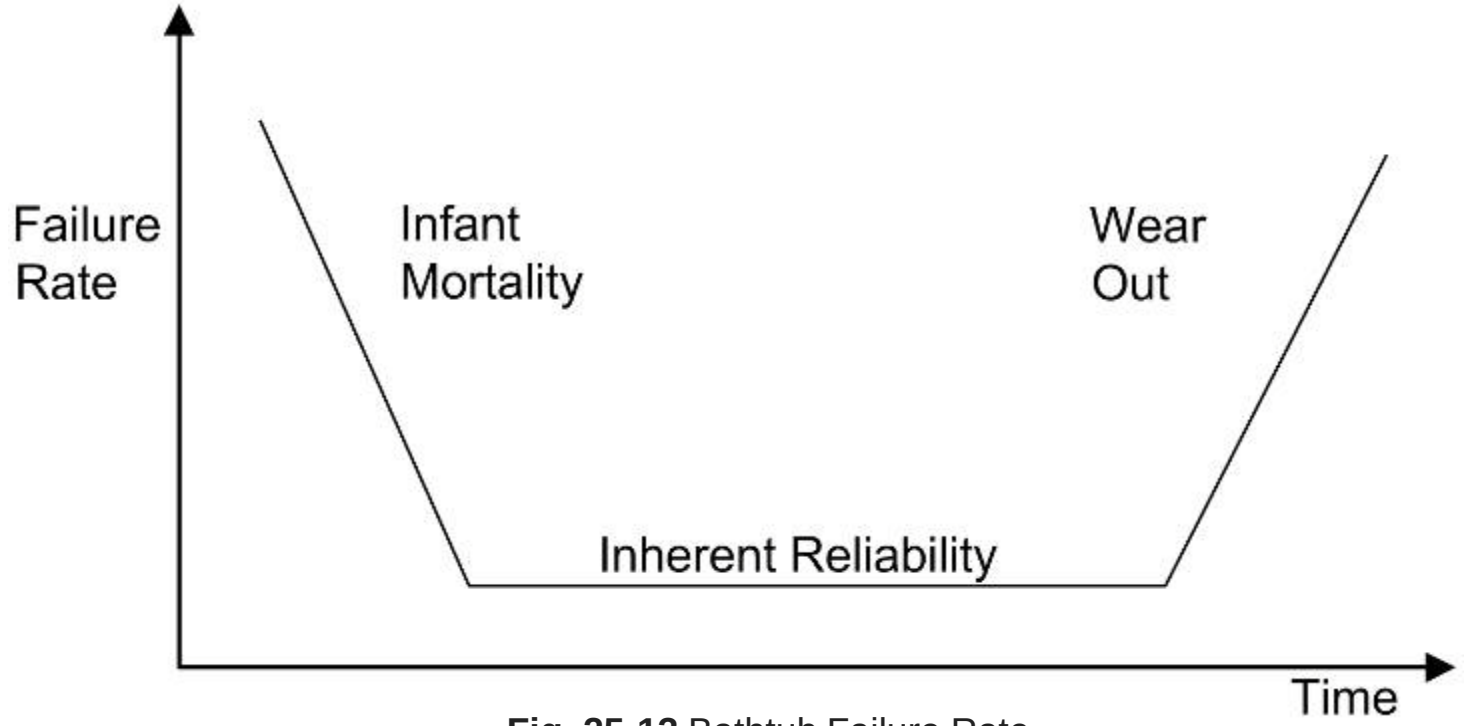


Fig. 25-13 Bathtub Failure Rate

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
soft error and hard error

- In memory there are two kinds of errors that can cause a bit to change: soft error and hard error.
- If the cell bit gets stuck permanently in a "*high*" or "*low*" state, this is referred to as a *hard error*.
  - Due to cell deterioration caused by wear-out.
    - There no remedy except to replace the defective chip.
- A *soft error* alters the cell bit from 1 to 0 or from 0 to 1, even though the cell is perfectly fine.
  - Caused by alpha particle radiation and power surges.
  - As density of RAM chips increases & RAM cell size goes down, probability of a soft error for a given cell goes up.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
mean time between failures (MTBF) for system

- System reliability of system depends on two factors, used to calculate the *mean time between failures*, or MTBF:
  - The FIT (failures in time) value of a single part.
  - The number of parts in the system.
- A prediction of average time before the first failure occurs, MTBF for a single chip is calculated, using the FIT, as follows:

$$\text{MTBF} = \frac{1{,}000{,}000{,}000 \text{ hours}}{\text{FIT}}$$

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
mean time between failures (MTBF) for system

- For the MTBF rate for the system, divide the single-chip MTBF by the number of chips in the system.

$$\text{MTBF of system} = \frac{\text{MTBF of one chip}}{\text{number of chips in system}}$$

See Technical Notes TN-00-14
and TN-00-18 on *www.micron.com*

http://download.micron.com/pdf/technotes/TN0014.pdf

http://download.micron.com/pdf/technotes/TN0018.pdf

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
mean time between failures (MTBF) for system

Example 25-7

Assuming that the FIT for a single chip is 252, calculate the MTBF for:
(a) a single chip
(b) a system with 512 chips

Solution:
(a) The MTBF for a single chip is as follows: MTBF for 1 chip = 1,000,000,000 hr / 252 = 3,968,254 hr = 453 years
(b) The MTBF for 512 chips is = 453 years / 512 chips = 0.884 year = 323 days

"Testing RAM for Embedded Systems"
by Jack Ganssle, is available from:
http://www.ganssle.com/testingram.pdf

Example 25-8

Calculate the system MTBF for the system in Example 25-7 if FIT = 745.

Solution:
MTBF for a single chip = 10^9 / 745 hrs. = 153 years. For the system it is 153 years / 512 = 109 days.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
ECL and gallium arsenide (GaAs) chips

- Use of secondary cache & EDC in systems 66 MHz higher is adding to the data and address path delay.
  - This forces designers to resort to ECL & GaAs chips.
- GaAs chips are used in high-speed x86 and RISC-based computers, especially GaAs EDC and cache controller chips.
- The mass of electrons in GaAs is lighter than in silicon, due to its quantum mechanics structure.
  - The electrons have a much higher speed, meaning GaAs chips achieve much higher speed than silicon.
    - Power dissipation is comparable to the silicon-based MOS transistor.

25.2: IC INTERFACING/SYSTEM DESIGN ISSUES
ECL and gallium arsenide (GaAs) chips

- GaAs has the following disadvantages:
  - Unlike silicon, of which there is a plentiful supply, GaAs is a rare commodity, and therefore more expensive.
  - GaAs is a compound of two elements, Ga and As, and therefore unstable at high temperatures.
  - It is very brittle, making large wafers impossible.
    - At this time no more than 100,000 transistors on a single chip.
  - GaAs yields are much lower than for silicon, making the cost per chip much more expensive than for silicon chips.
- The CRAY III supercomputer was based on GaAs, with buses at speeds of multiple GHz.
  - Eventually abandoned due to these issues.

Dec Hex Bin
25 19 00011001

ENDS ; TWENTY-FIVE

The x86 PC

assembly language, design, and interfacing

fifth edition

MUHAMMAD ALI MAZIDI
JANICE GILLISPIE MAZIDI
DANNY CAUSEY

The x86 PC
assembly language, design, and interfacing
fifth edition

Prentice Hall