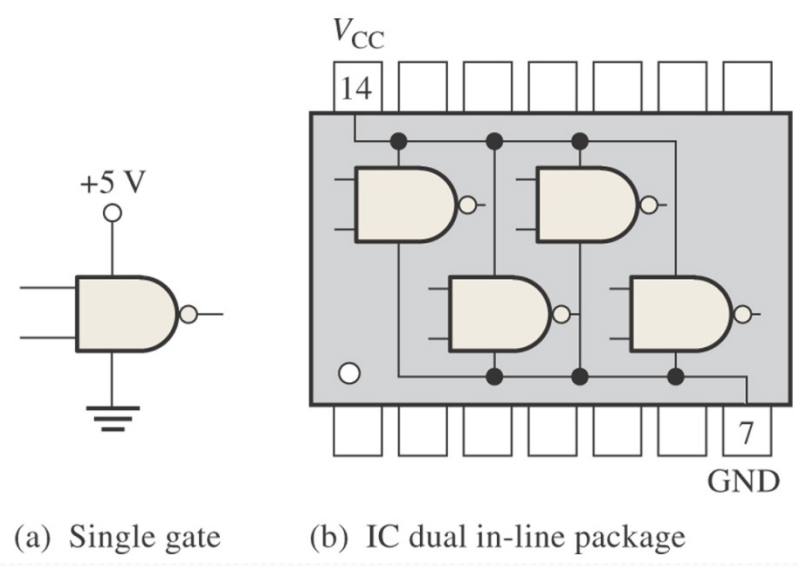
# Chapter 12 Integrated Circuit Technologies

# OUTLINE

- Basic Operational Characteristics and Parameters
- CMOS Circuits
- TTL Circuits
- Practical Considerations in the Use of TTL
- Comparison of CMOS and TTL Performance

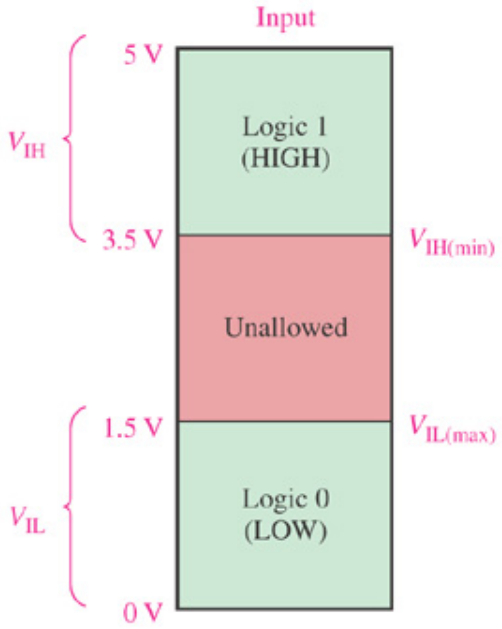
# 12.1 Basic Operational Characteristics and Parameters

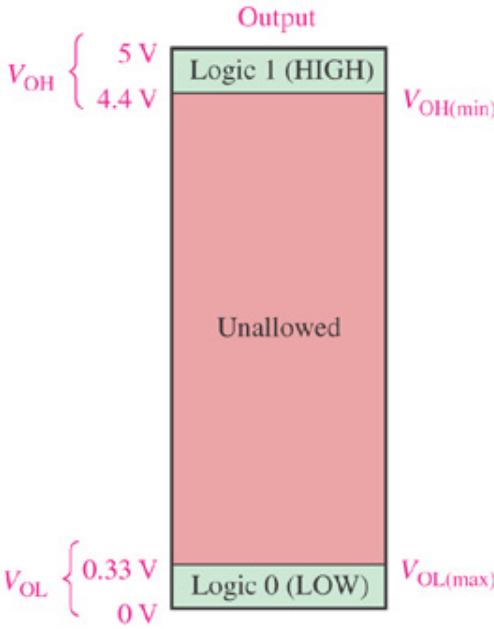
- DC Supply Voltage
  - TTL: +5V
  - CMOS
    - +5V
    - +3.3V
    - +2.5V
    - +1.2V



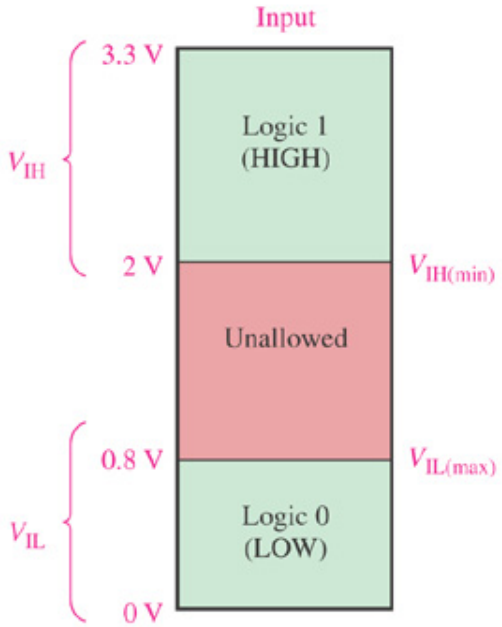

(a) Single gate (b) IC dual in-line package

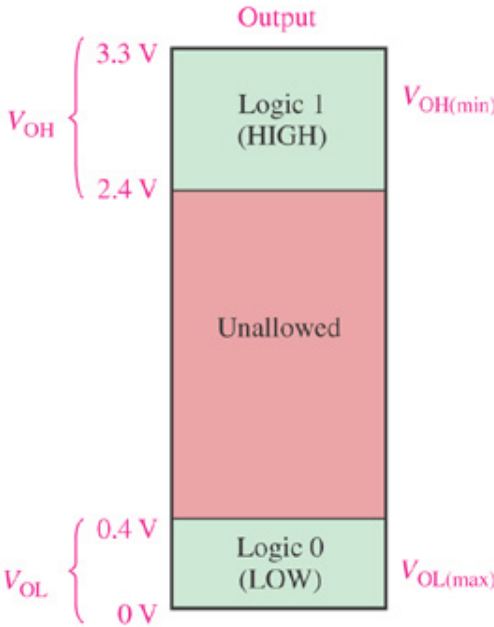
- CMOS Logic Levels
  - $V_{IL}$,$V_{IH}$
  - $V_{OL}$,$V_{OH}$



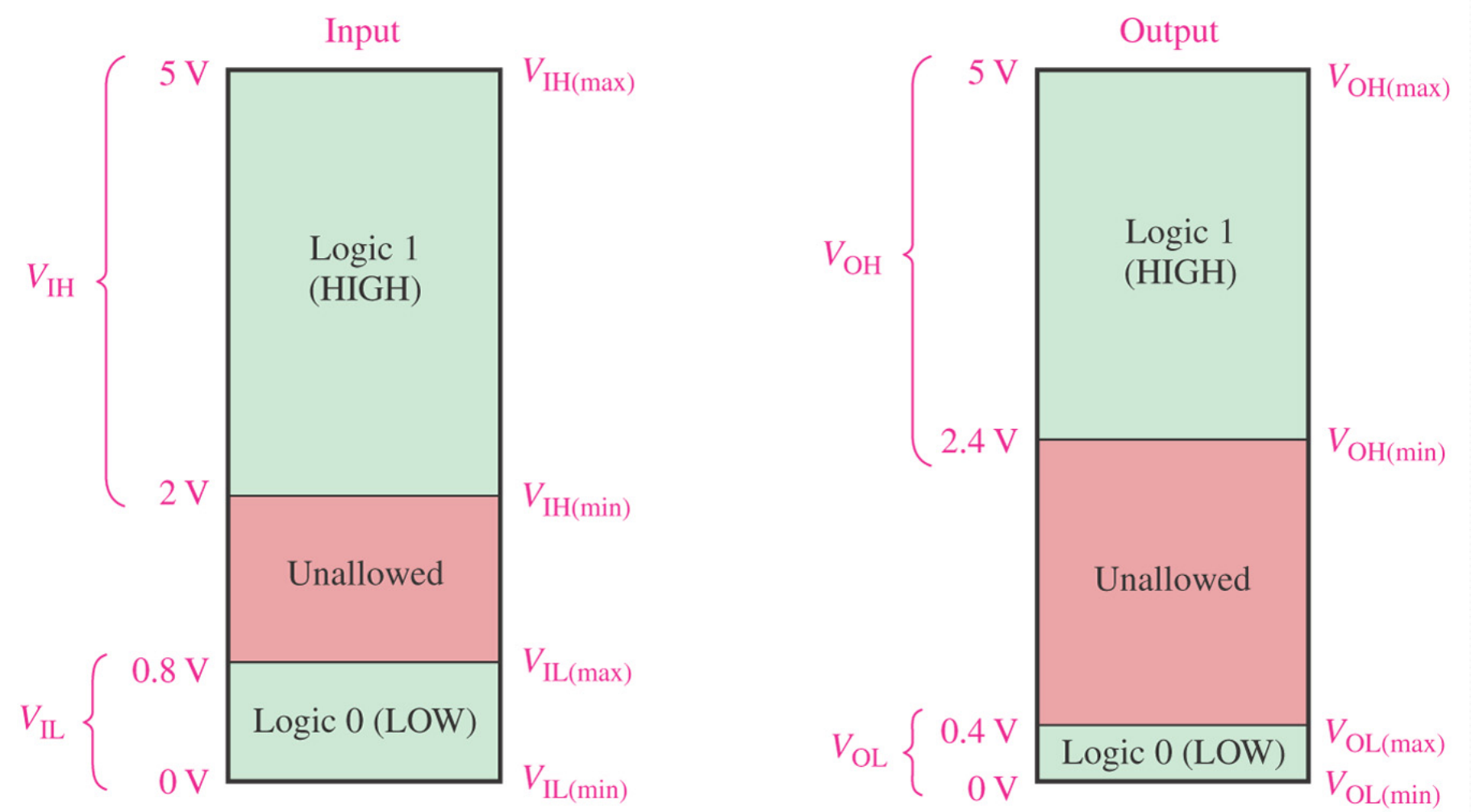

(a) +5 V CMOS



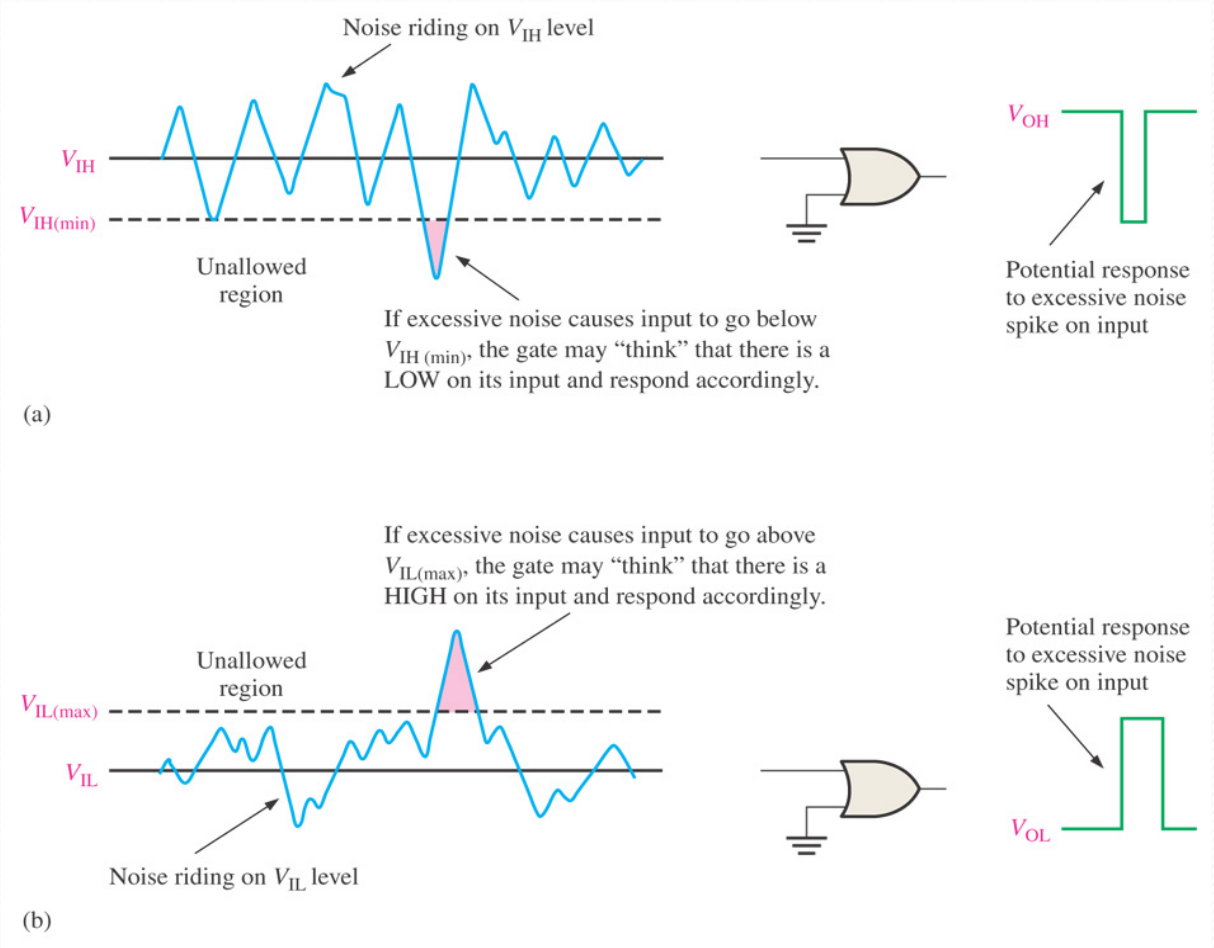




(b) +3.3 V CMOS

# TTL Logic Levels



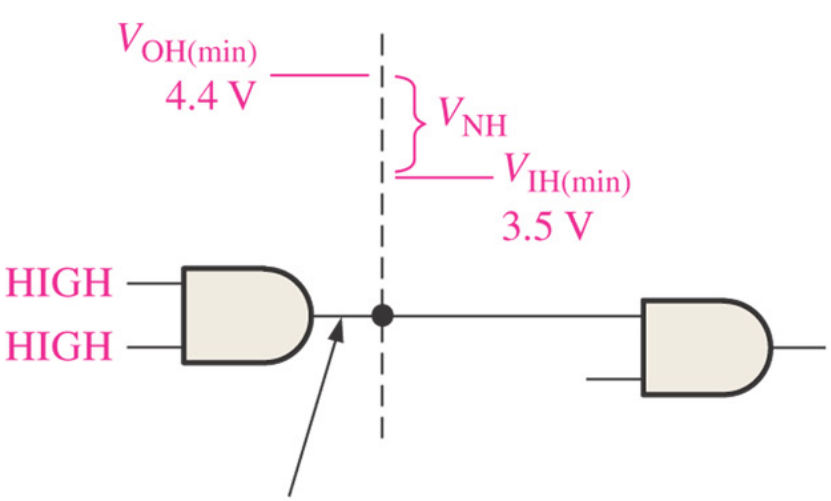
- Noise Immunity
  - Noise induced in electrical circuits can present a threat to the proper operation of circuits.
  - In order not to be adversely affected by noise, a logic circuit must have a certain amount of noise immunity.



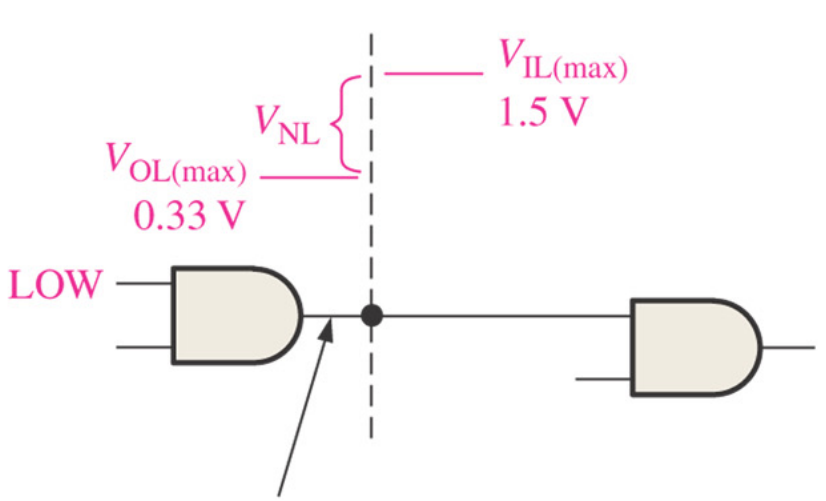
# Noise Margin

$$V_{NH} = V_{OH(\min)} - V_{IH(\min)}$$

$$V_{NL} = V_{IL(\max)} - V_{OL(\max)}$$



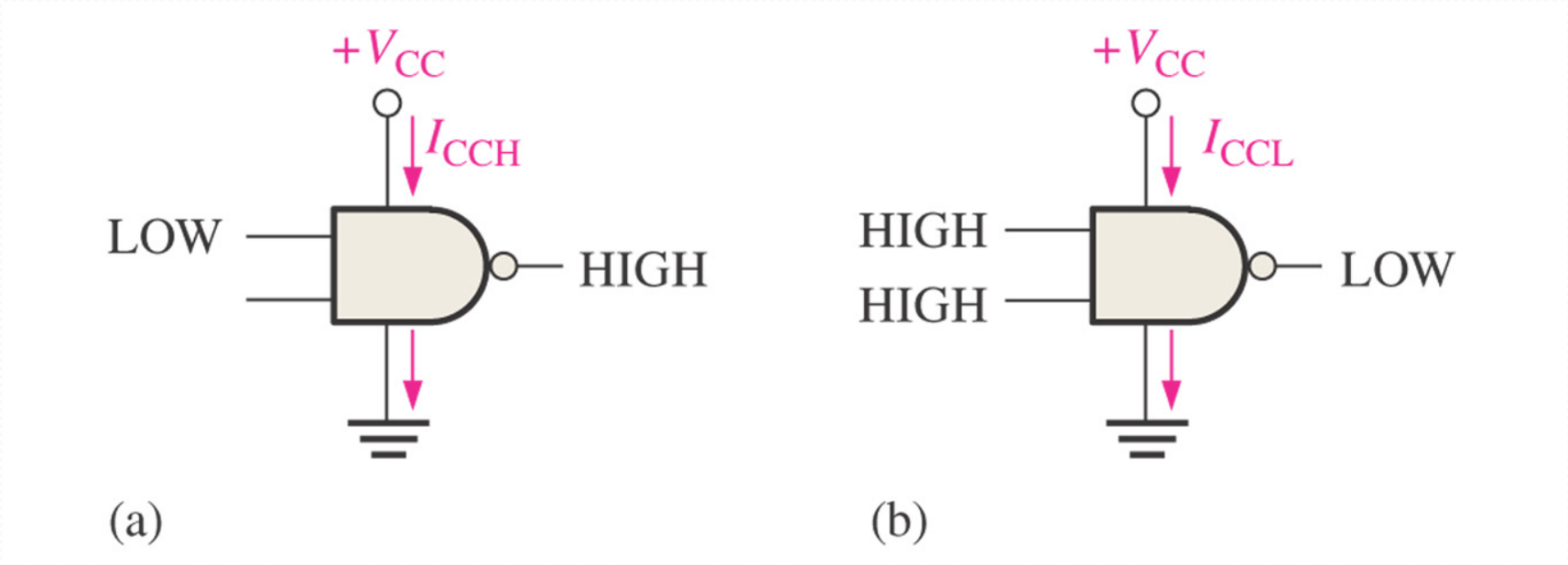

(a) HIGH-level noise margin



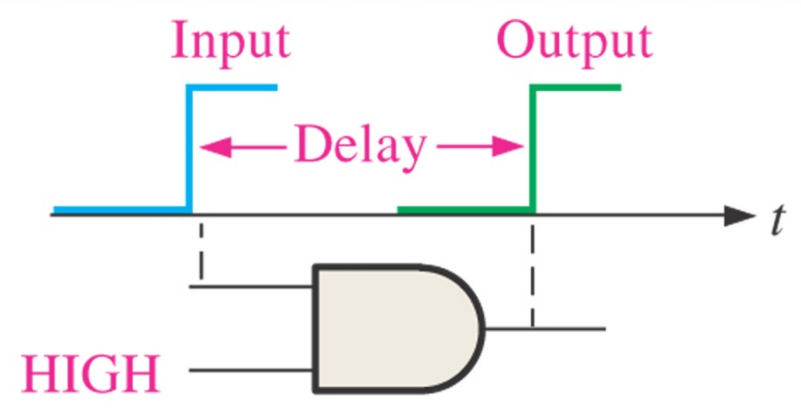

(b) LOW-level noise margin

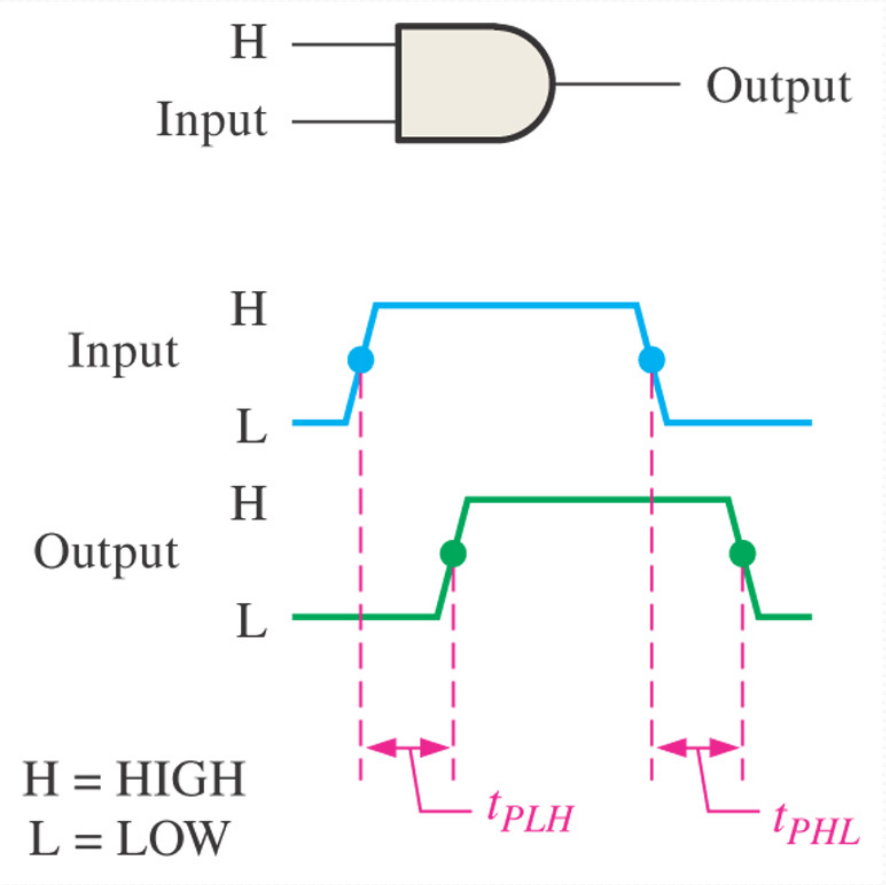
- Power Dissipation
  - TTL circuits: power dissipation is constant over its range of operating frequencies.
  - CMOS: power dissipation is frequency dependent

$$P_D = V_{CC} I_{CC}$$



- Propagation Delay Time



- Speed-Power Product
  - A basis for the comparison of logic circuits when both propagation delay time and power dissipation are important considerations in the selection of the type of logic to be used in a certain application.

- Loading and Fan-Out

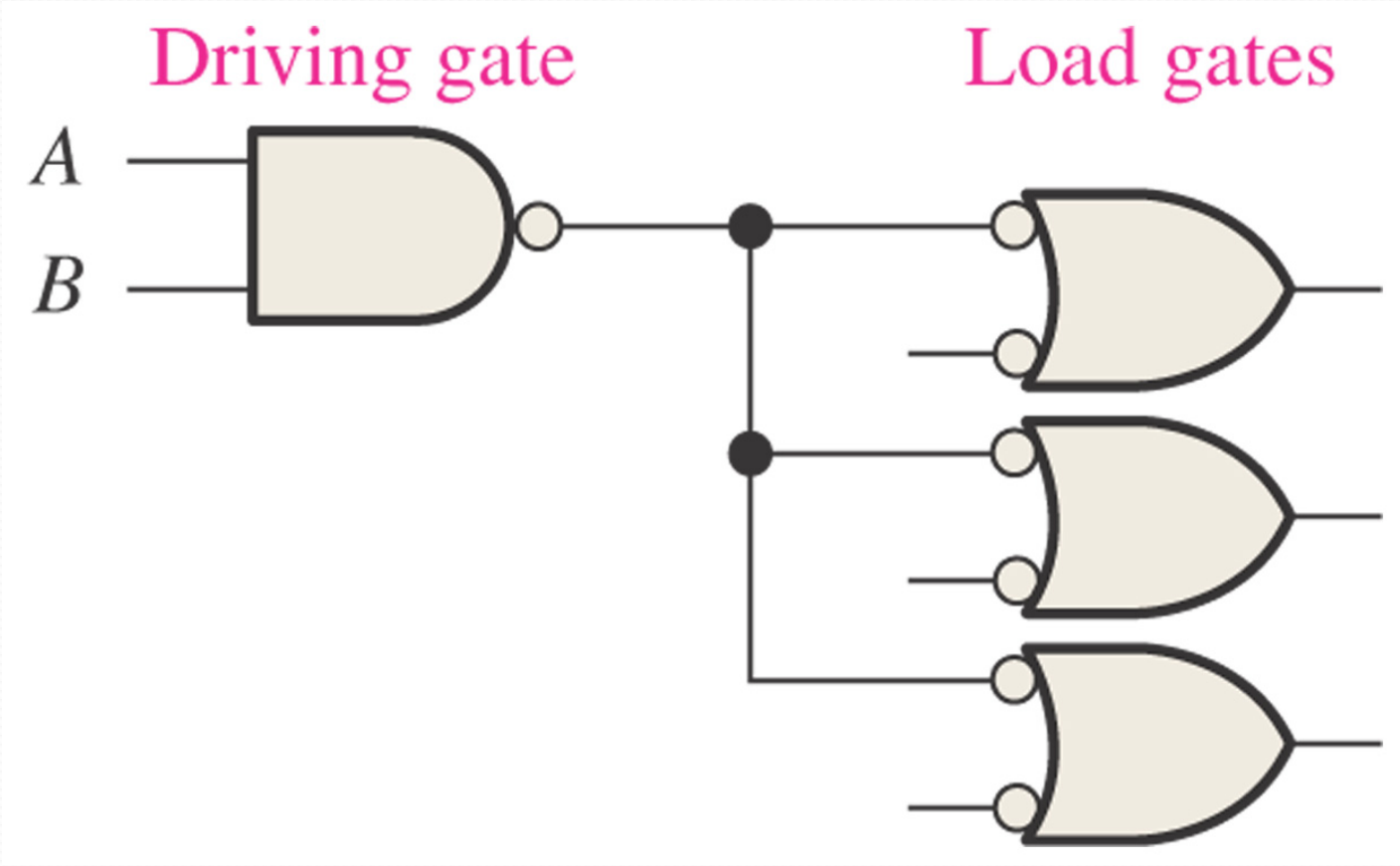


**Figure 14–11** Capacitive loading of a CMOS gate.

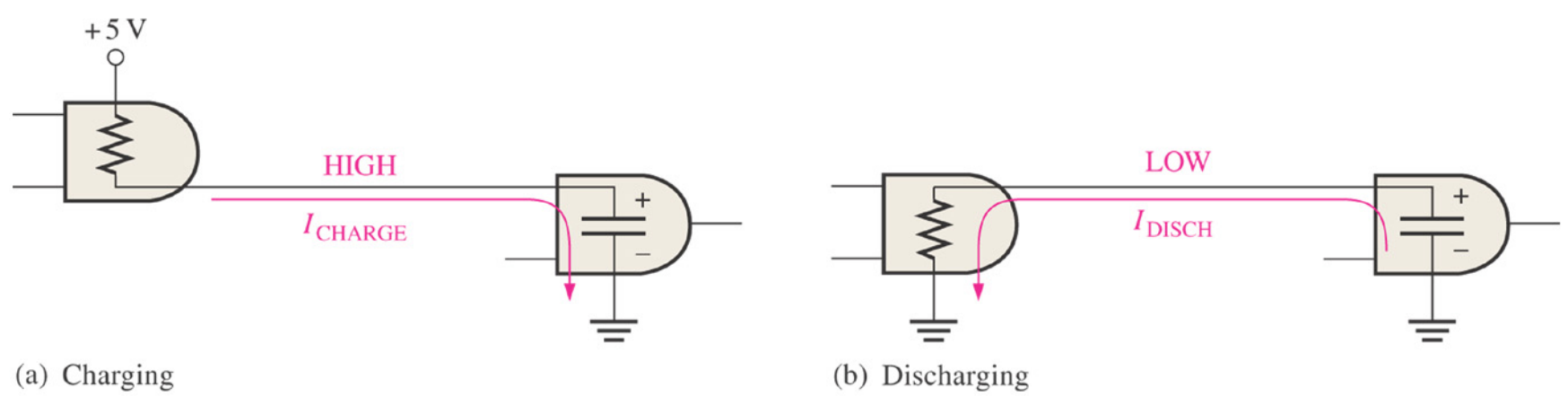


**Figure 14–12** Basic illustration of current sourcing and current sinking in logic gates.

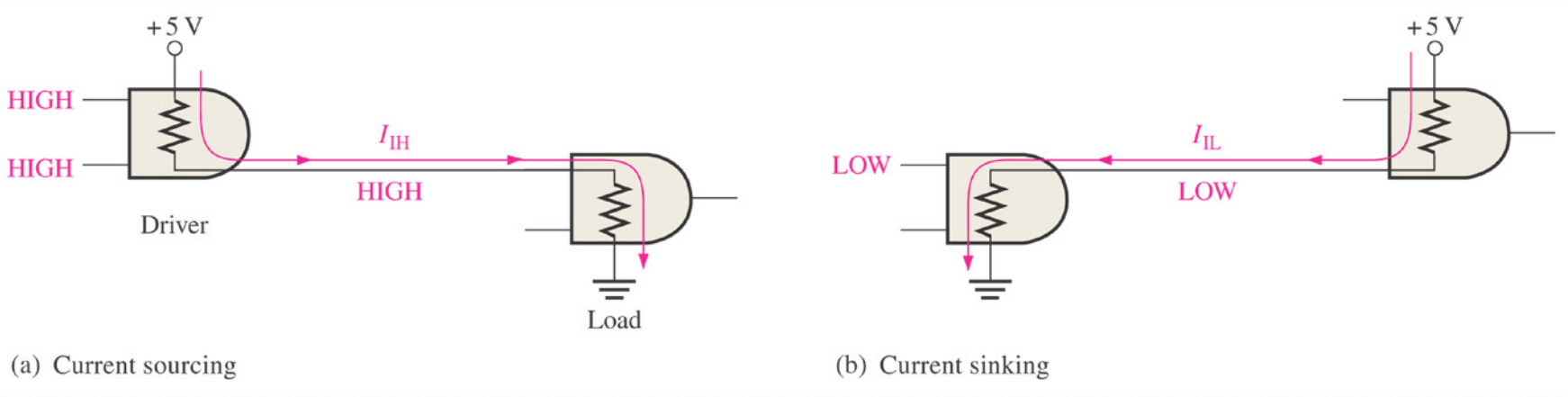


**Figure 14–13** HIGH-state TTL loading.

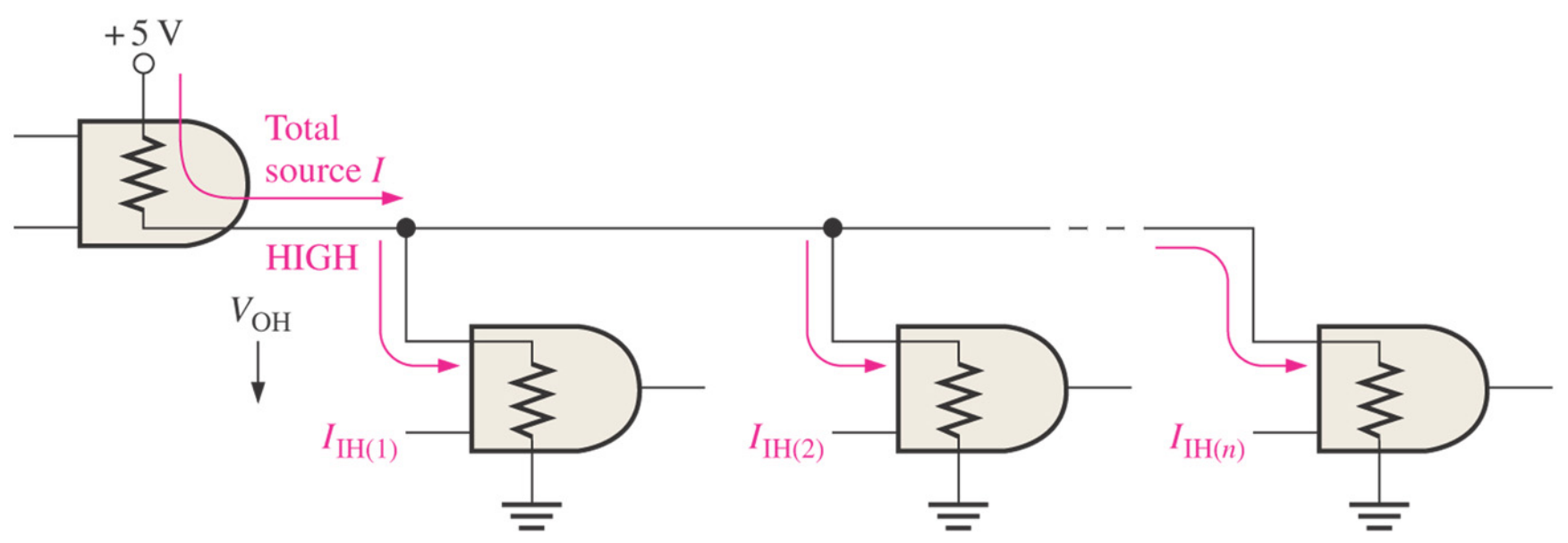
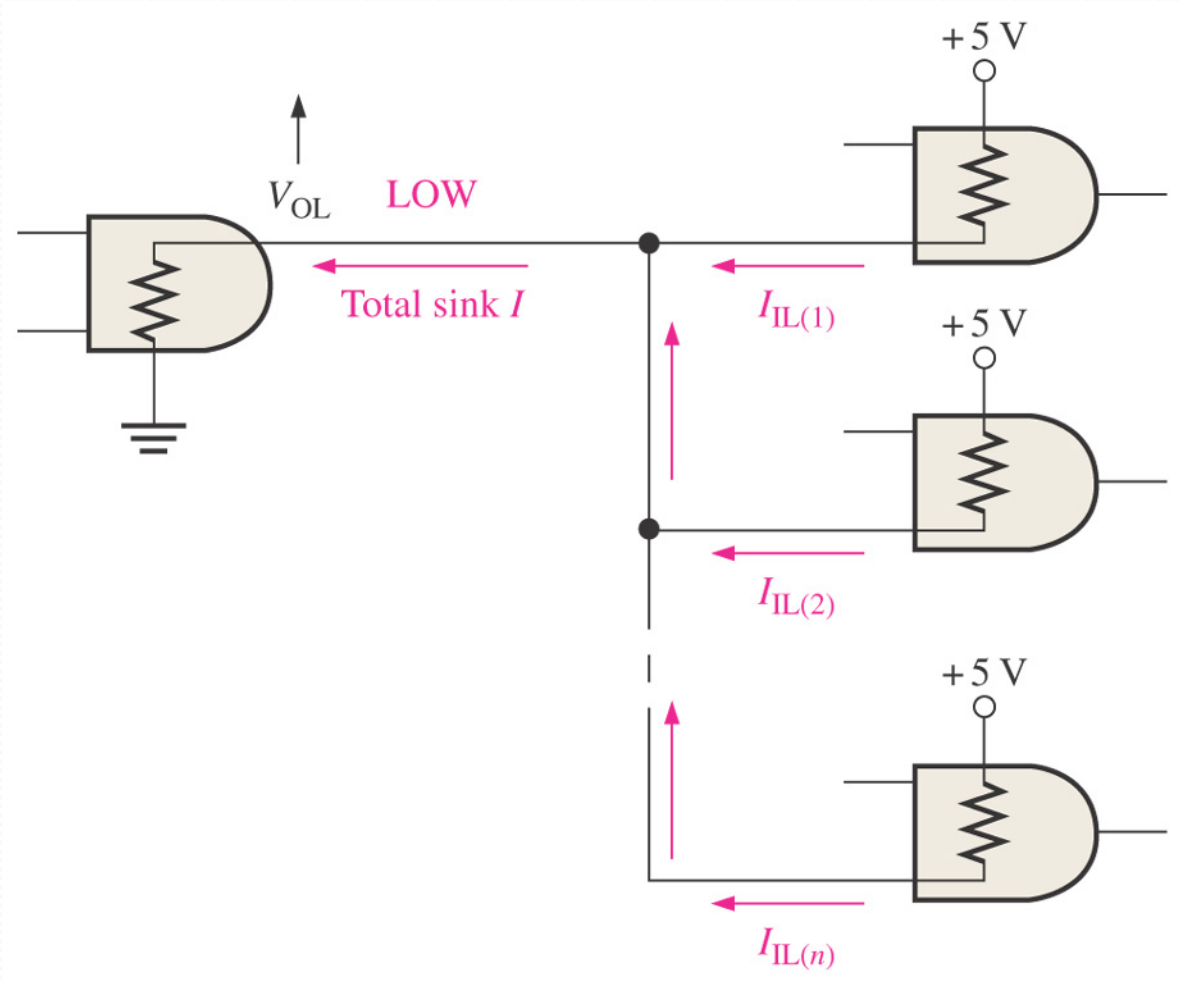


**Figure 14–14** LOW-stage TTL loading.

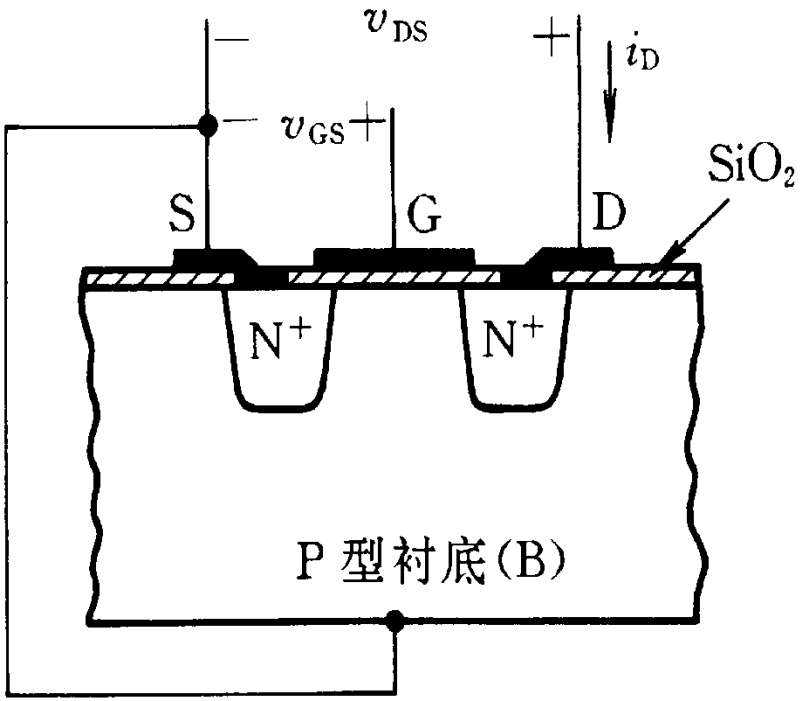


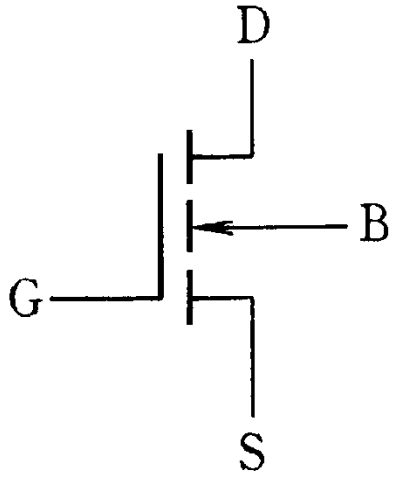
# 12.2 CMOS Circuits

- CMOS: Complementary Metal-Oxide Semiconductor
- Complementary: an n-channel MOSFET and a p-channel MOSFET are used

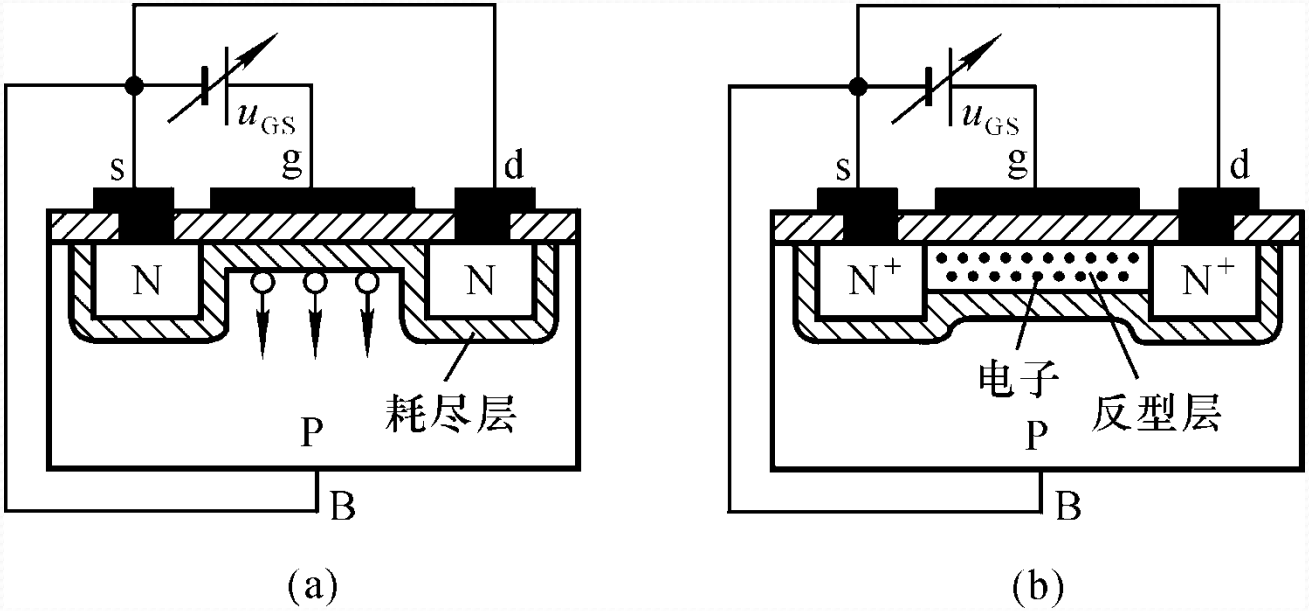
# The MOSFET

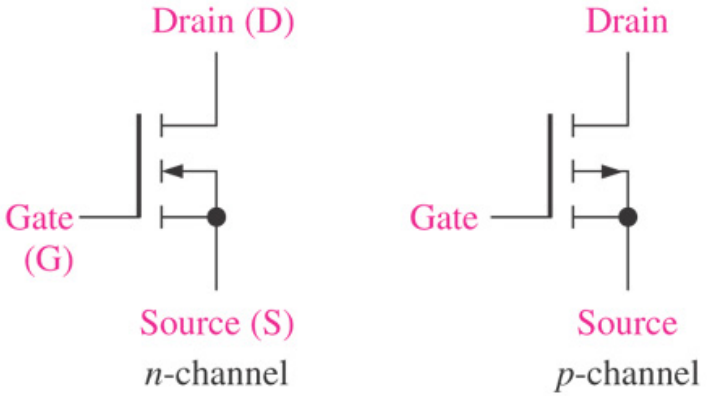
- Two types
  - P-channel
  - N-channel
- Three terminals
  - Gate, drain and source



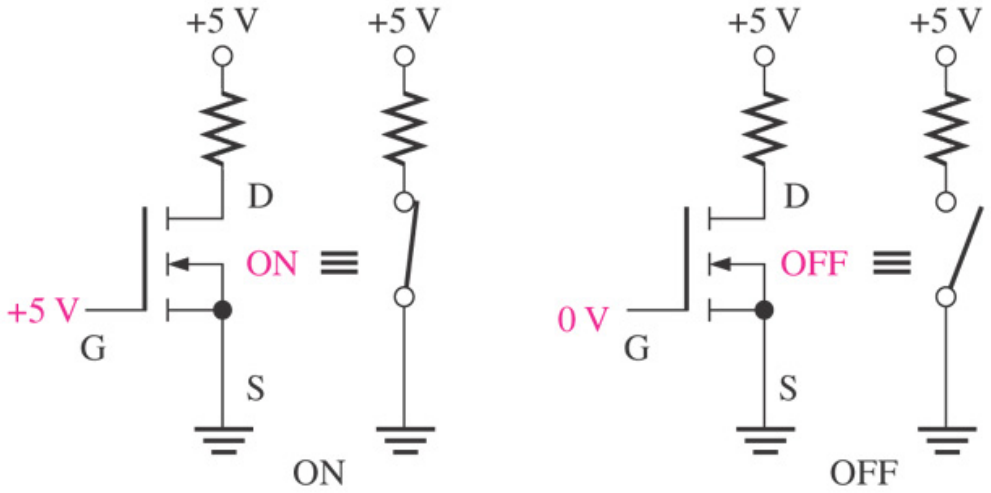




The Structure and Symbol of N-channel MOSFET

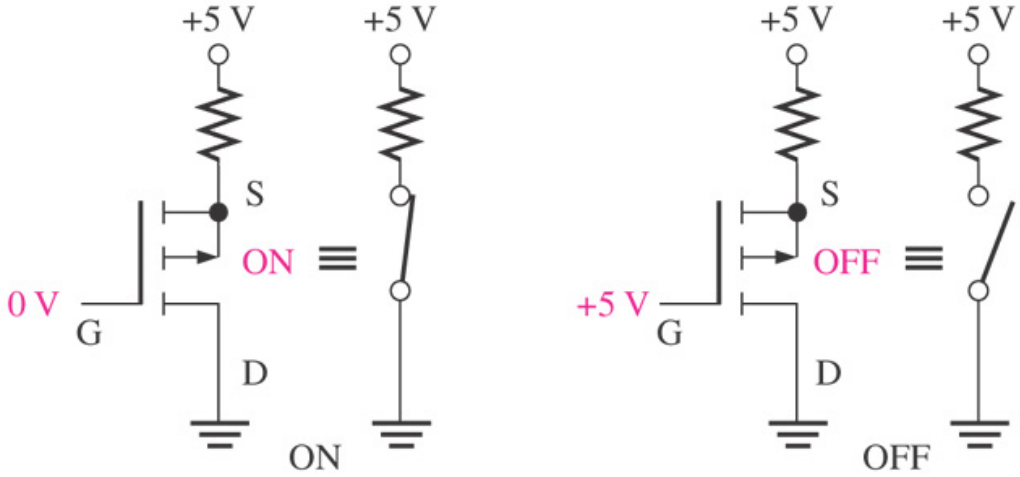

$u_{GS}$
s
g
d
N
N
P
耗尽层
B
(a)
$u_{GS}$
s
g
d
$N^+$
$N^+$
电子
反型层
P
B
(b)




(a) MOSFET symbols



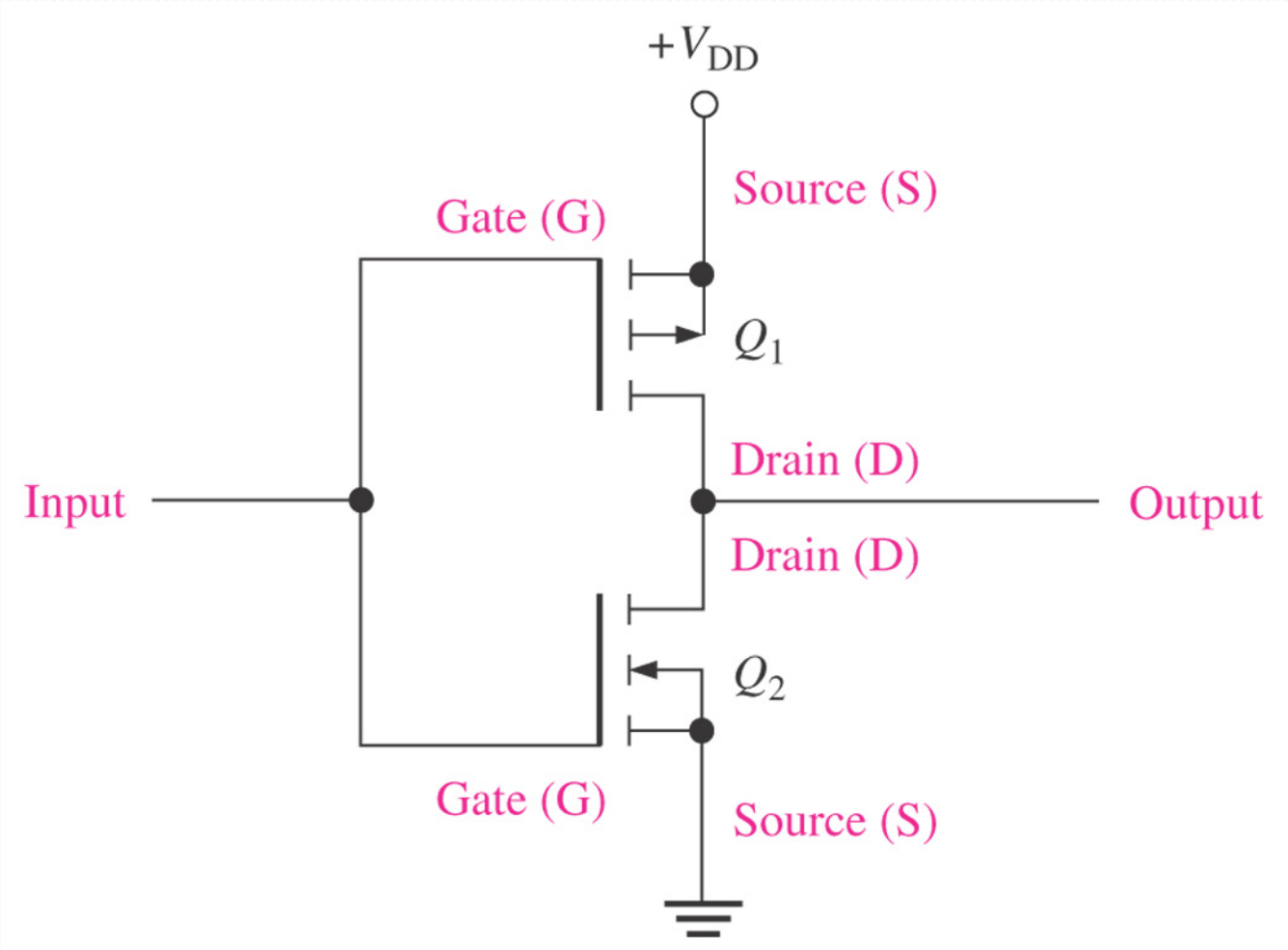

(b) *n*-channel switch



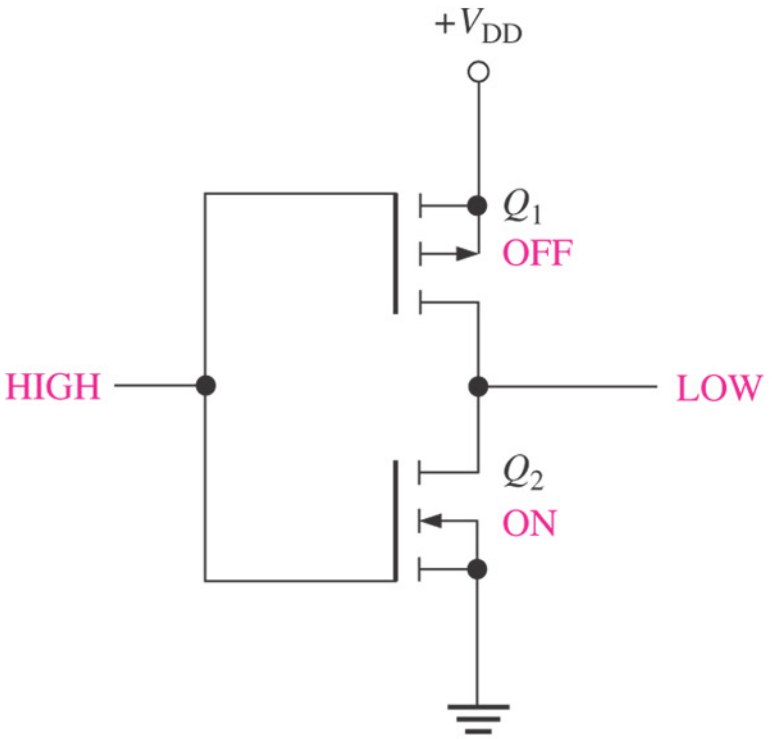

(c) *p*-channel switch

**Figure 14–16** Simplified MOSFET symbol.

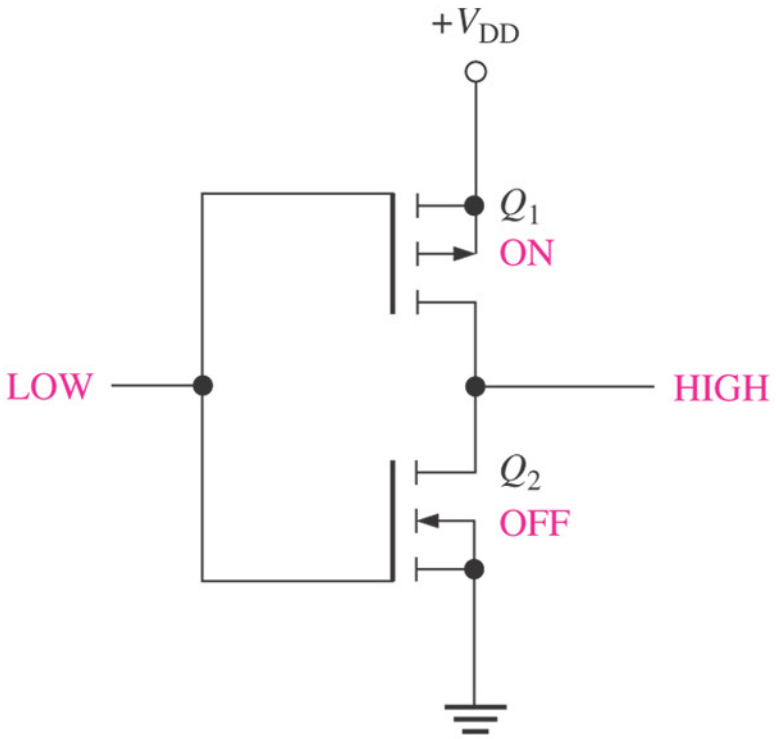
A CMOS inverter circuit.



# Operation of a CMOS inverter.

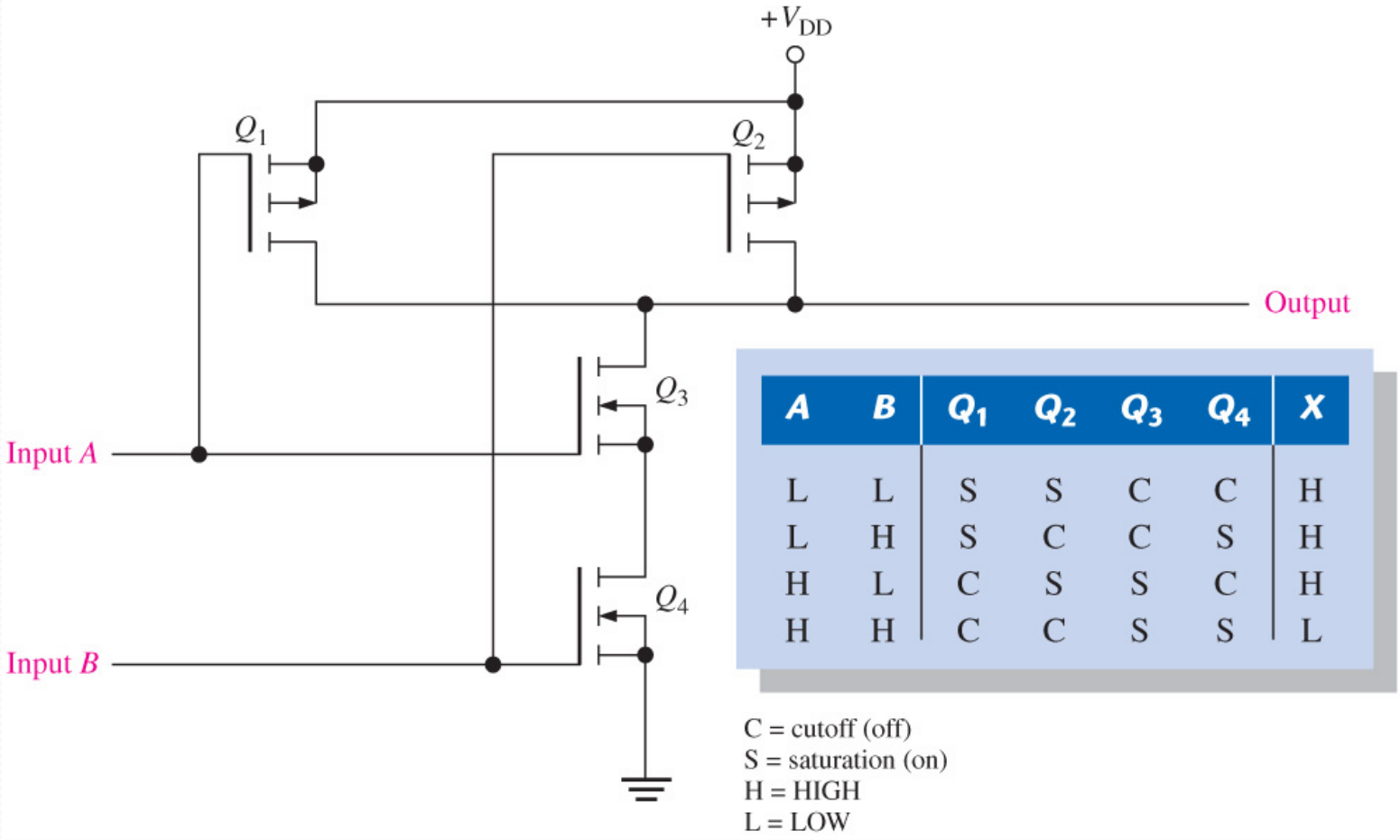



(a) HIGH input, LOW output




(b) LOW input, HIGH output

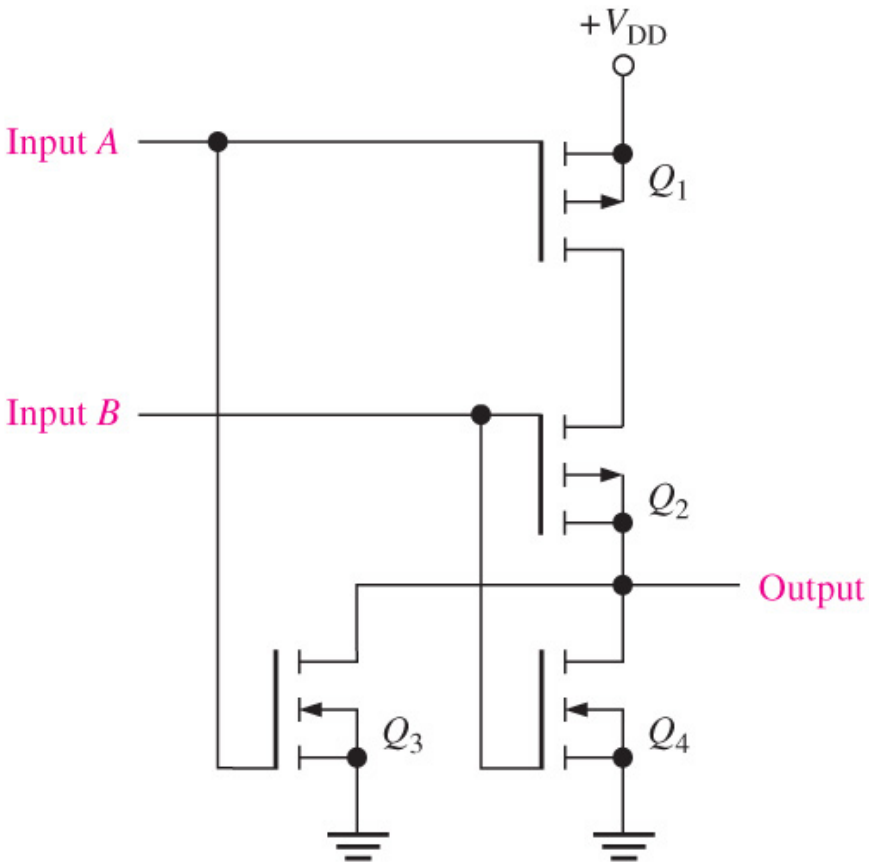
# A CMOS NAND gate circuit.




| A | B | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | X |
|---|---|---|---|---|---|---|
| L | L | S | S | C | C | H |
| L | H | S | C | C | S | H |
| H | L | C | S | S | C | H |
| H | H | C | C | S | S | L |

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

# A CMOS NOR gate circuit.

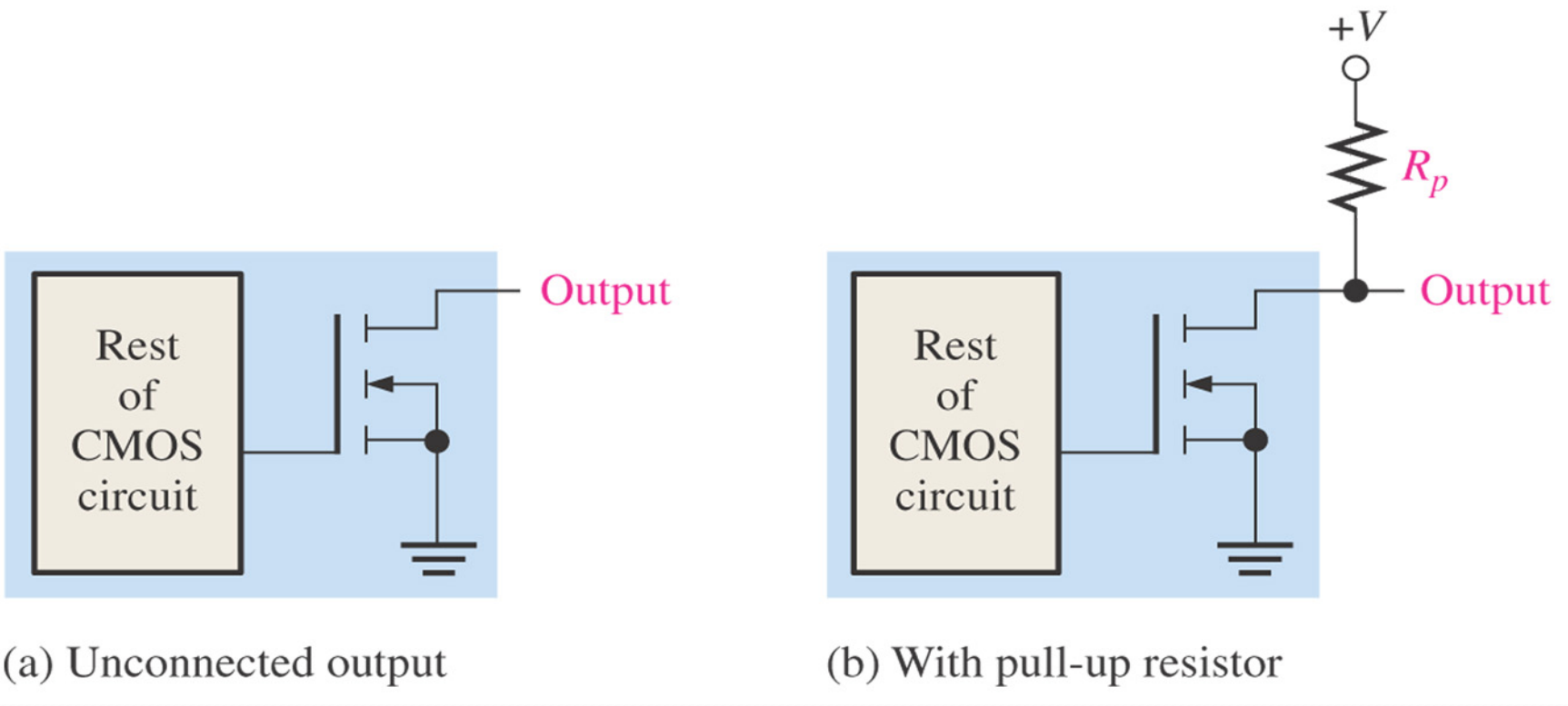



| $A$ | $B$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $X$ |
|---|---|---|---|---|---|---|
| L | L | S | S | C | C | H |
| L | H | S | C | C | S | L |
| H | L | C | S | S | C | L |
| H | H | C | C | S | S | L |

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

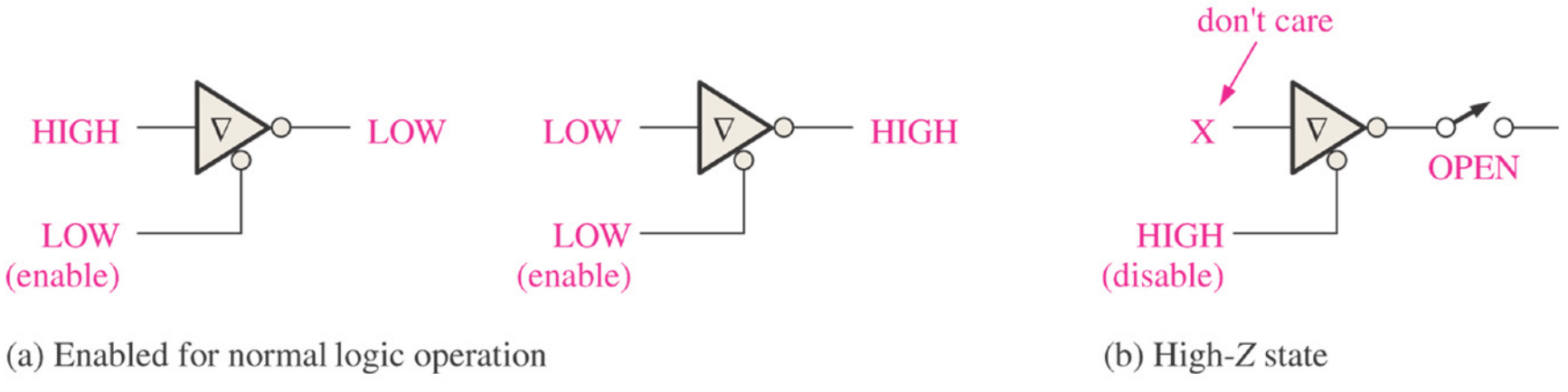
# Open-drain CMOS gates

- The drain terminal of the output transistor is unconnected and *must be connected externally to* $V_{DD}$ *through a load.*



# The three states of a tristate circuit.

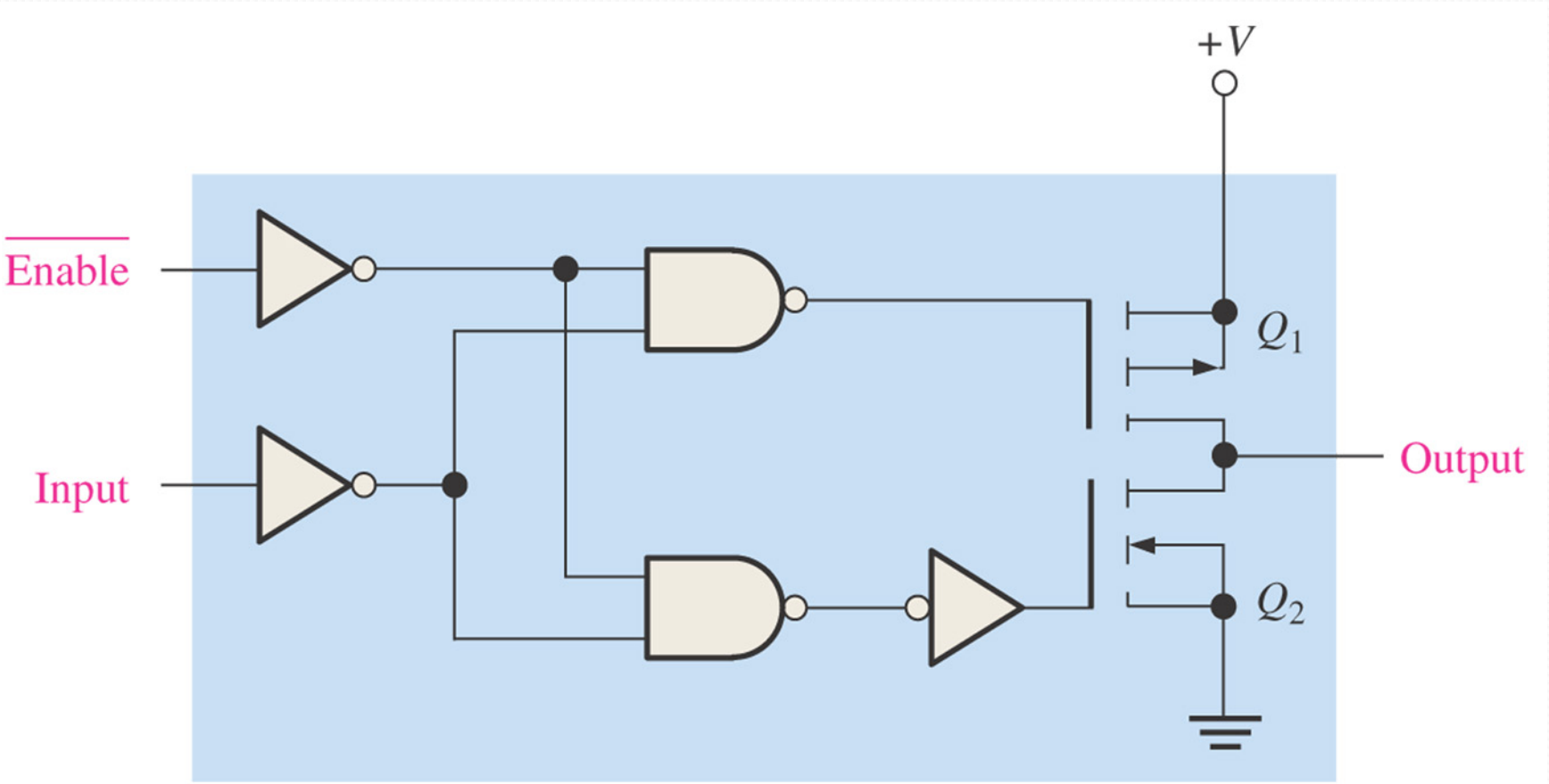
- HIGH, LOW and high-Z




(a) Enabled for normal logic operation

(b) High-*Z* state

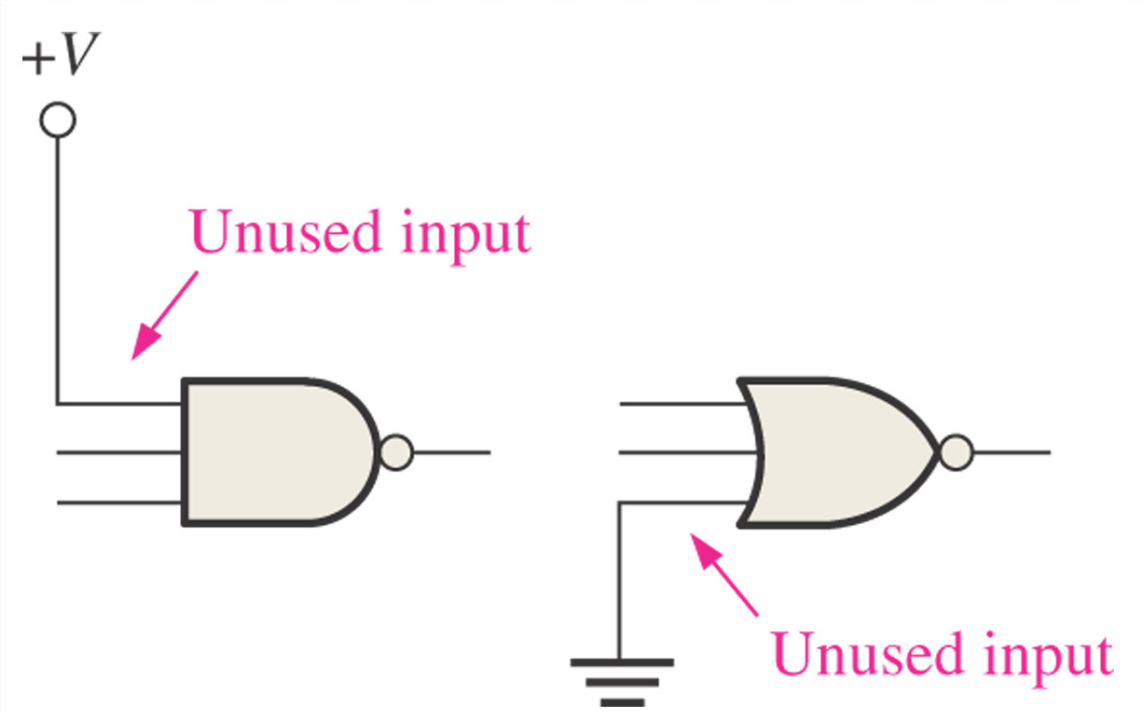
**Figure 14–23** A tristate CMOS inverter.



# Precautions for handling CMOS

- When CMOS devices are removed from the foam, the pins should not be touched.
- Do not place CMOS devices in polystyrene foam or plastic trays.
- All tool, test equipment, and metal workbenches should be earth-grounded.
- Do not insert CMOS devices into sockets or PC boards with the power on.
- All unused inputs should be connected to the supply voltage or ground.
- After assembly on PC boards, protection should be made.

**Figure 14–24** Handling unused CMOS inputs.

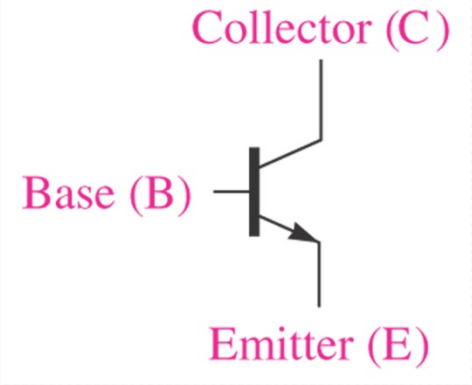


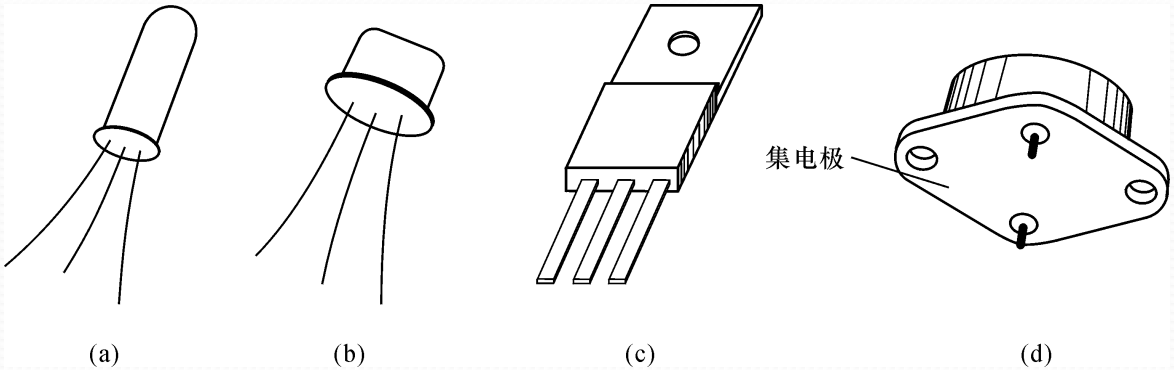
# 12.3 TTL Circuits

- TTL: Transistor-transistor logic
- With totem-pole output

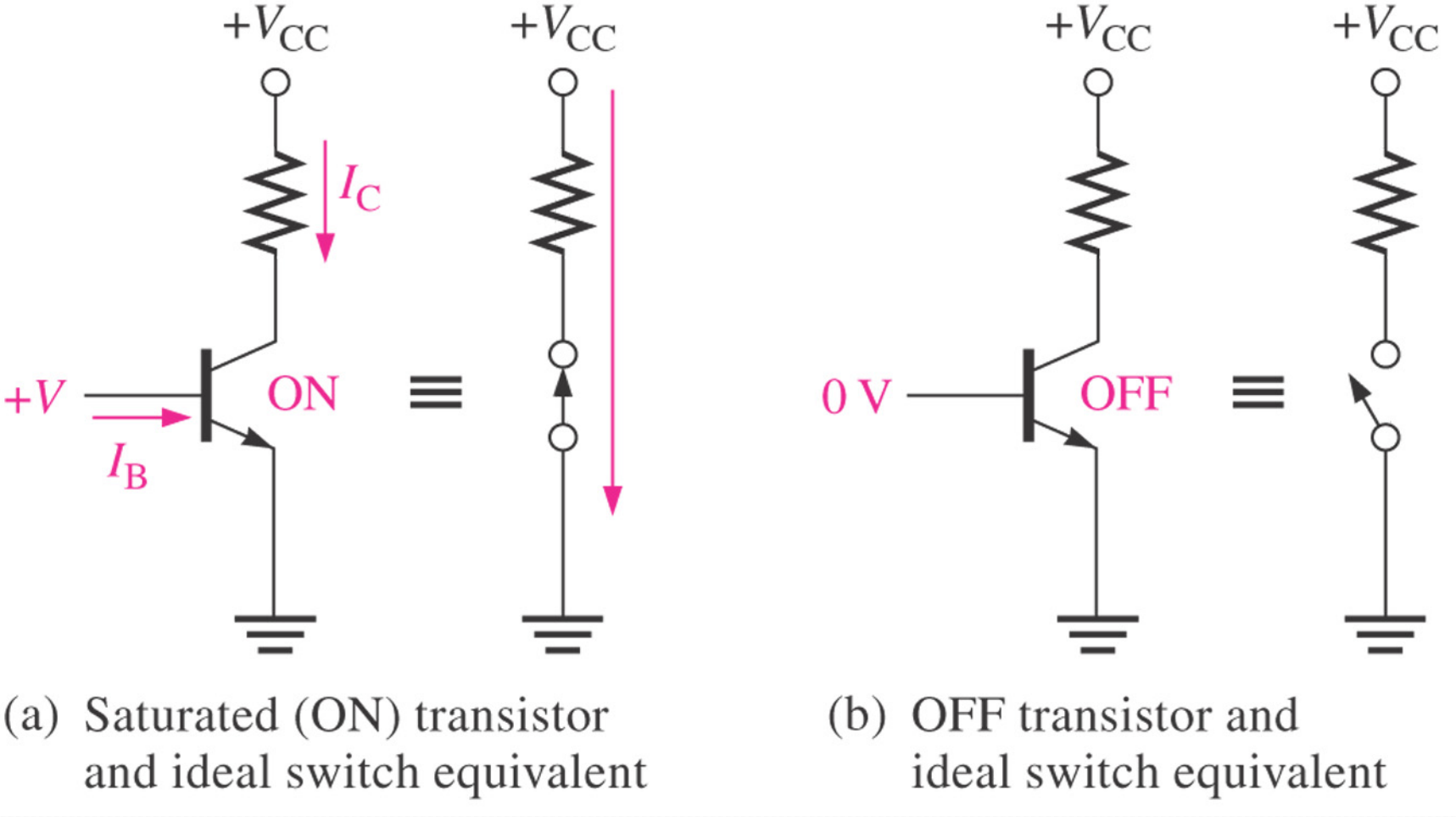
# The Bipolar Junction Transistor

- Three terminals
  - Base, emitter, and collector



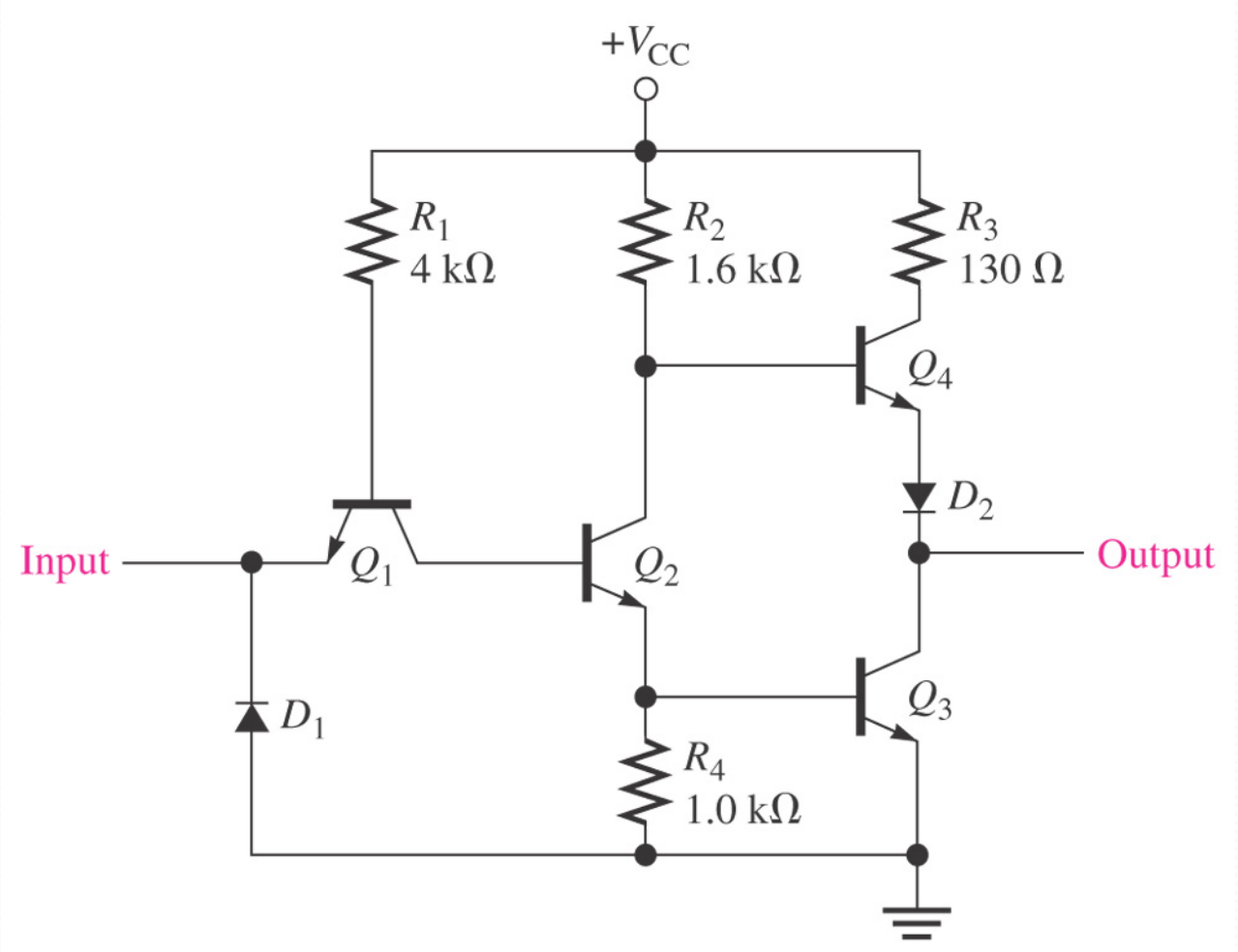
# The ideal switching action of the BJT



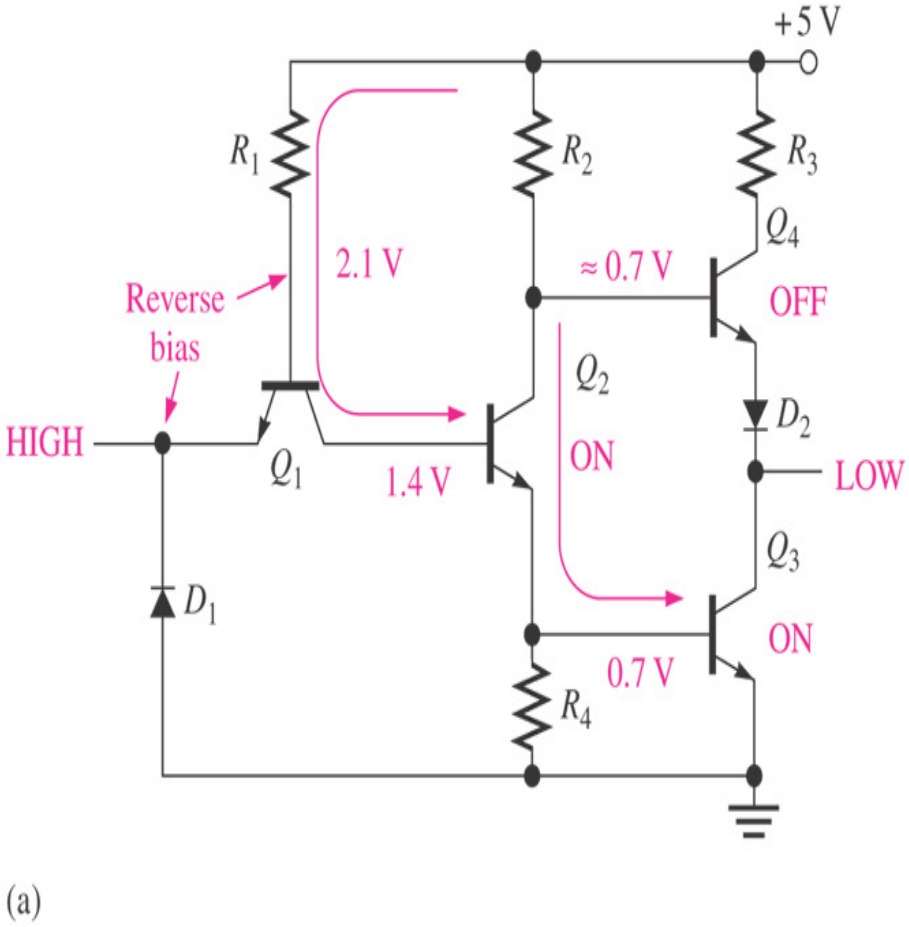

(a) Saturated (ON) transistor and ideal switch equivalent

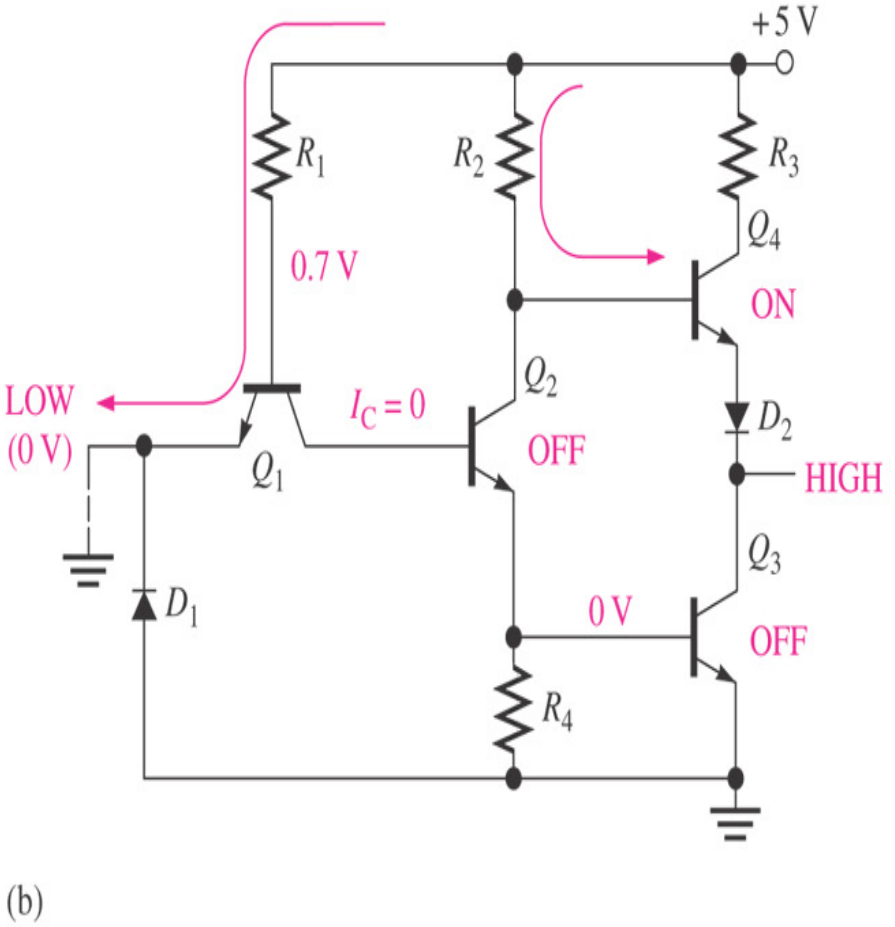
(b) OFF transistor and ideal switch equivalent

# A standard TTL inverter circuit.

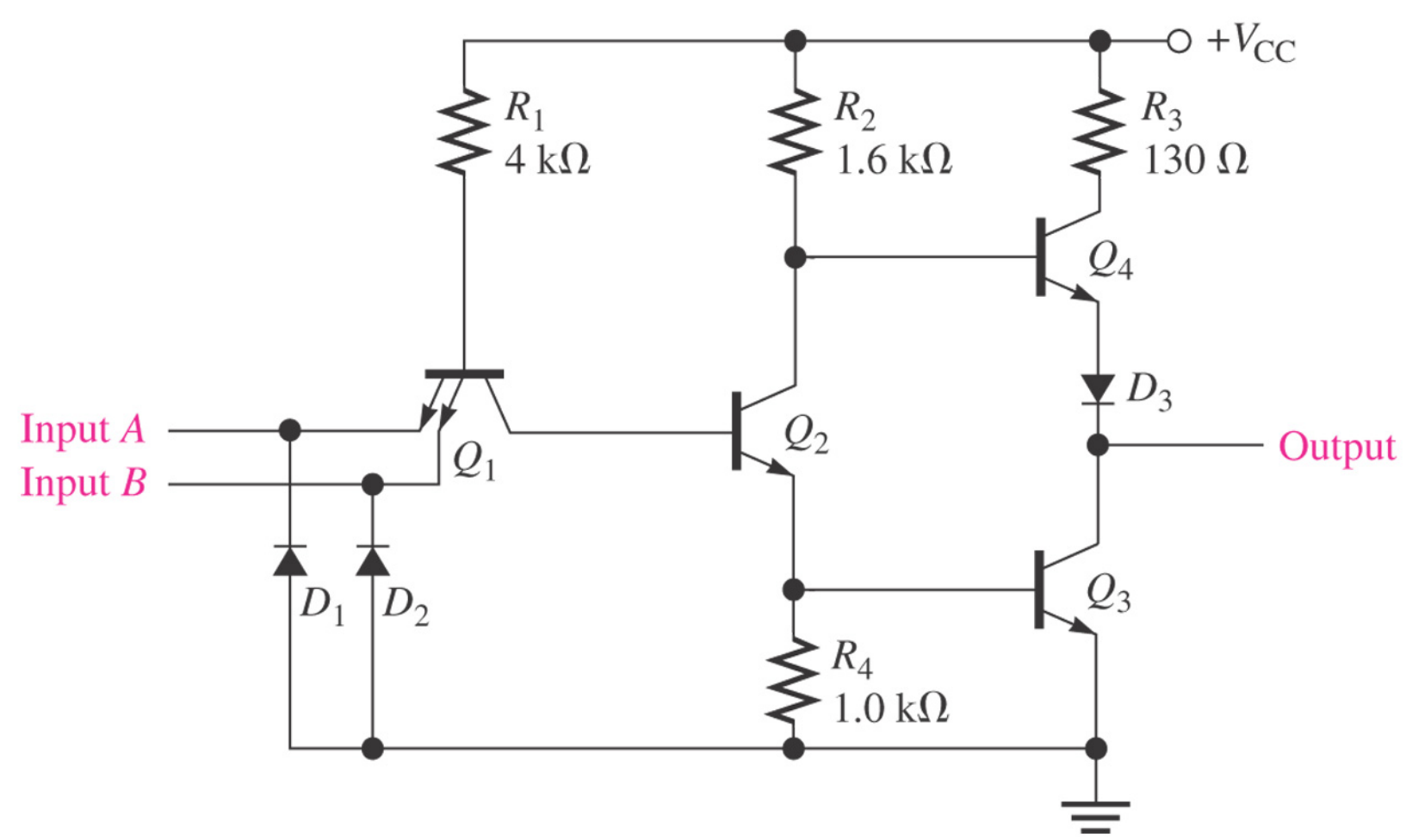


# Operation of a TTL inverter

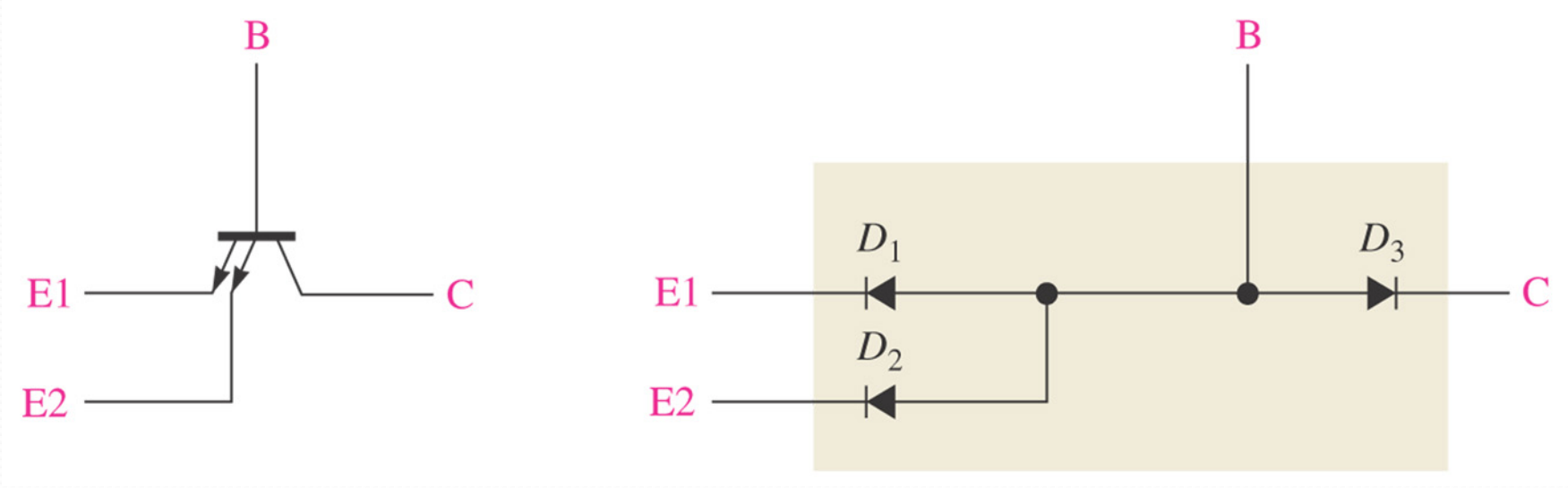


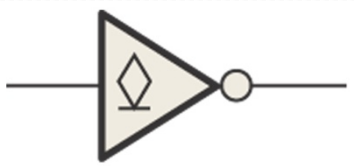
# A TTL NAND gate circuit.

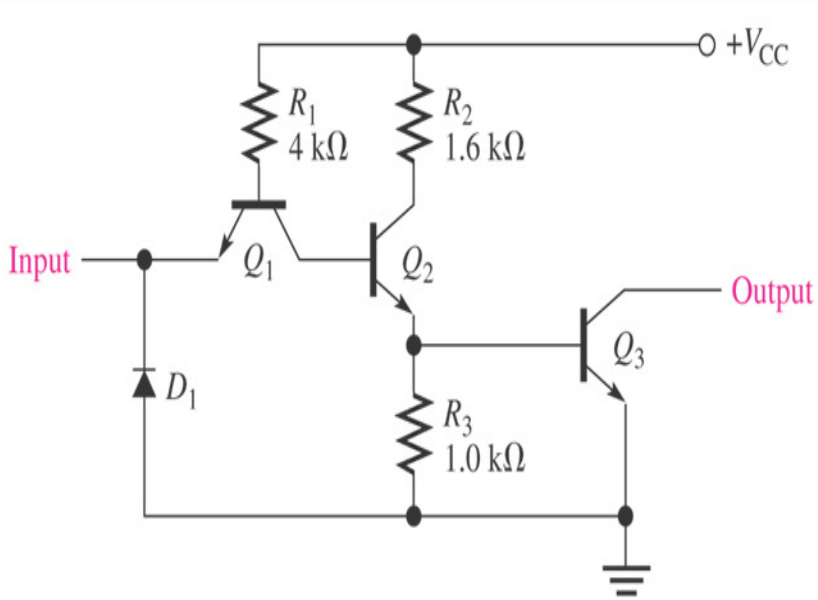


# Diode equivalent of a TTL multiple-emitter transistor.

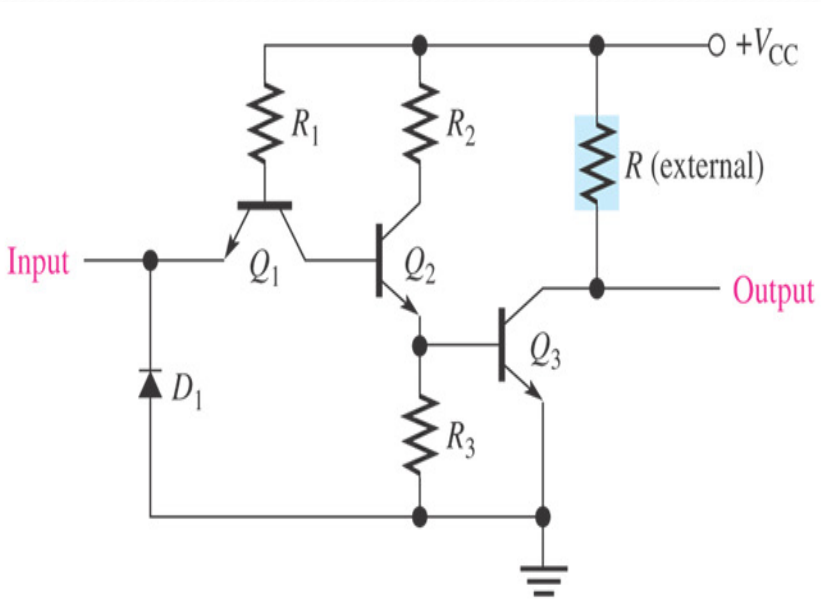


# TTL inverter with open-collector output (Open-Collector Gates)



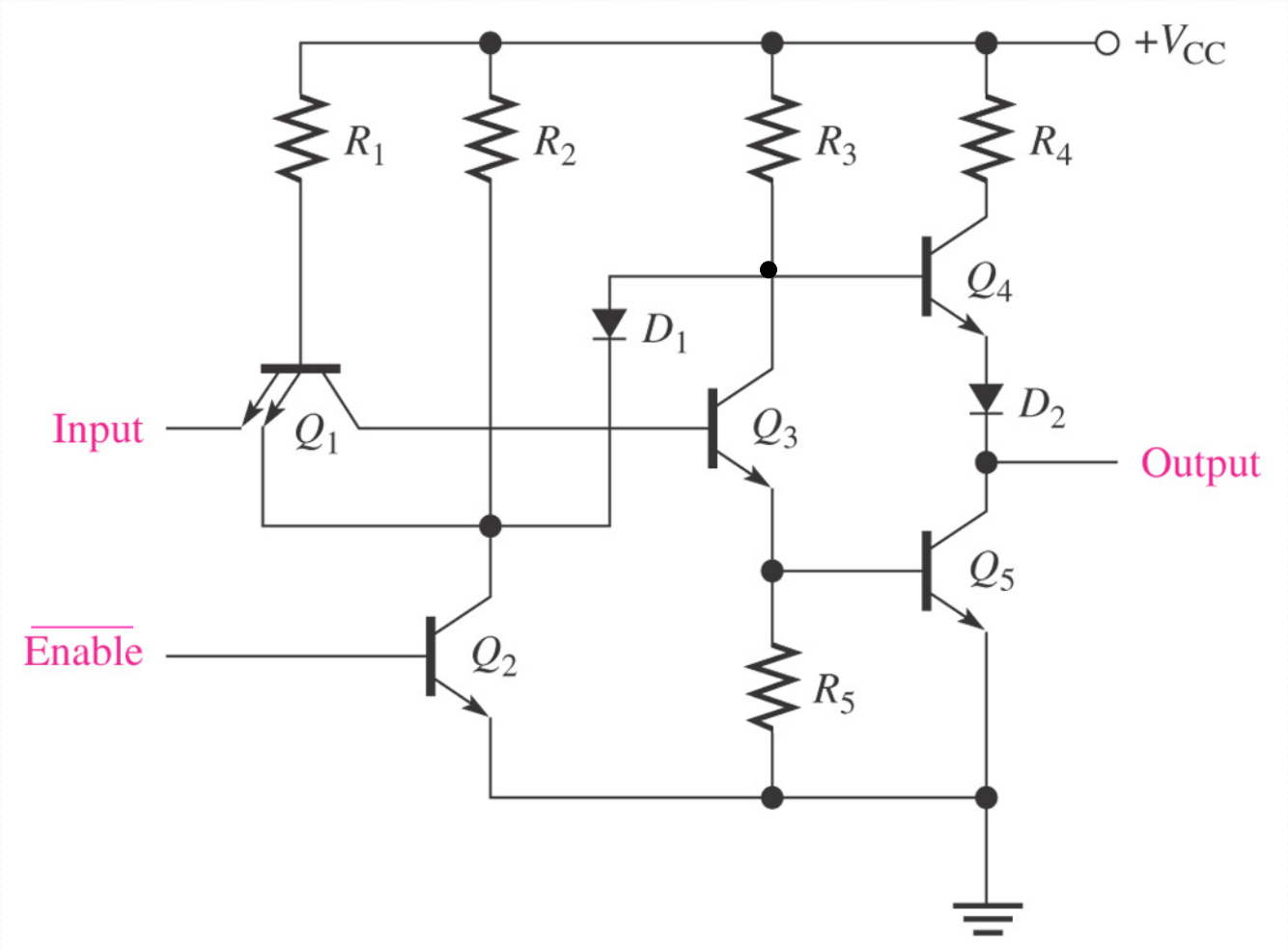



(a) Open-collector inverter circuit

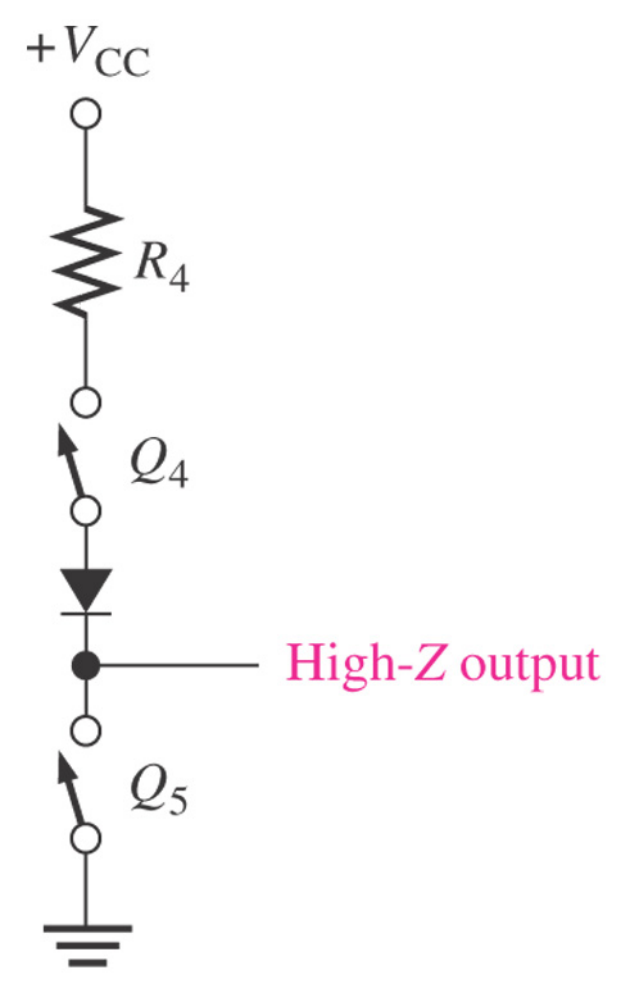



(b) With external pull-up resistor

# Basic tristate inverter circuit.

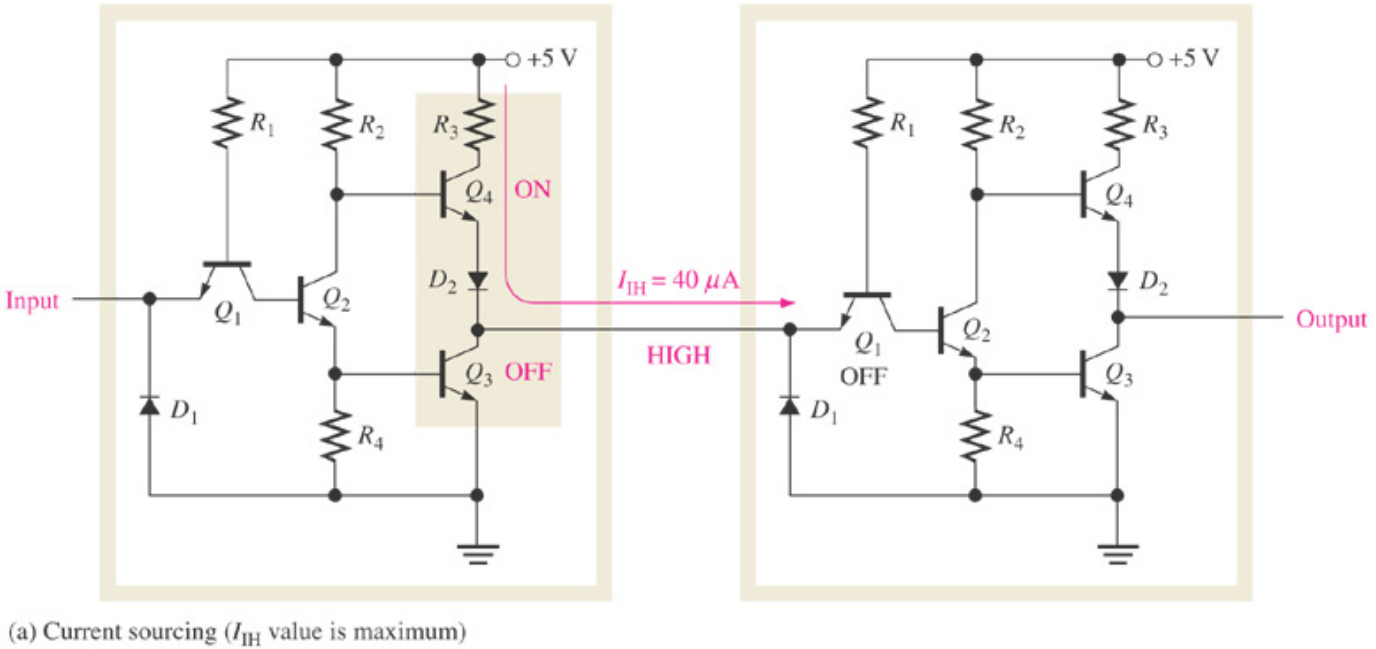


# An equivalent circuit for the tristate output in the high-Z state

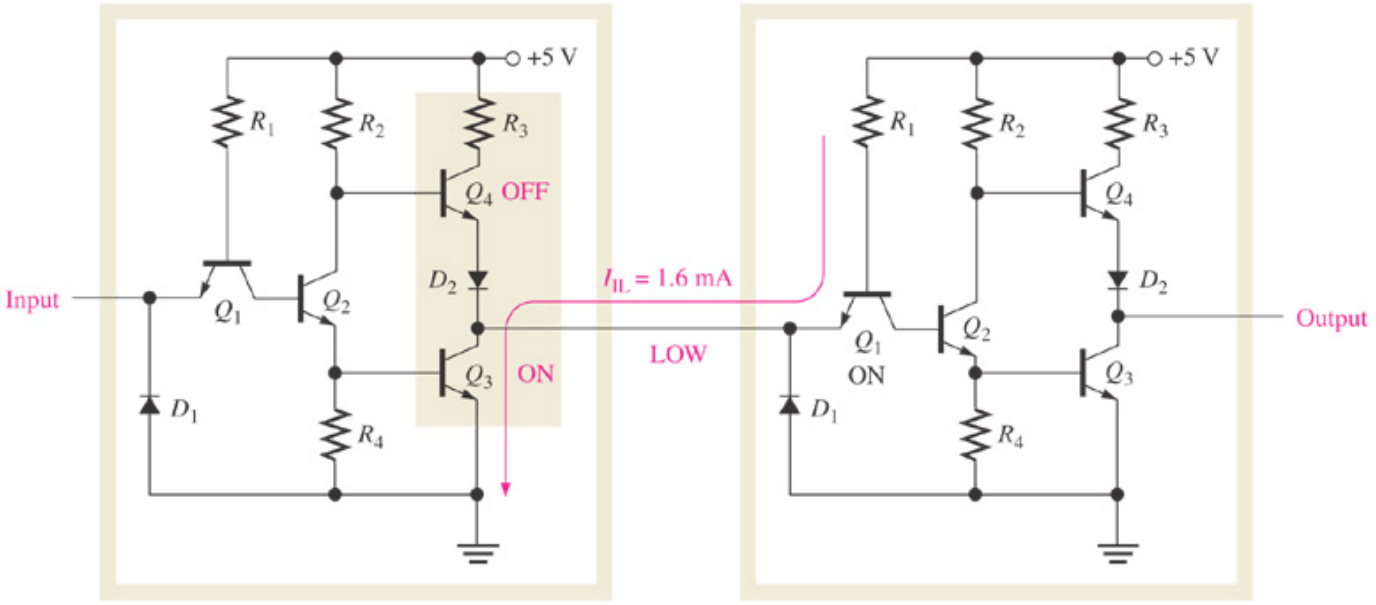


# 12.4 Practical Considerations in the Use of TTL

# Current sinking and sourcing action in TTL.

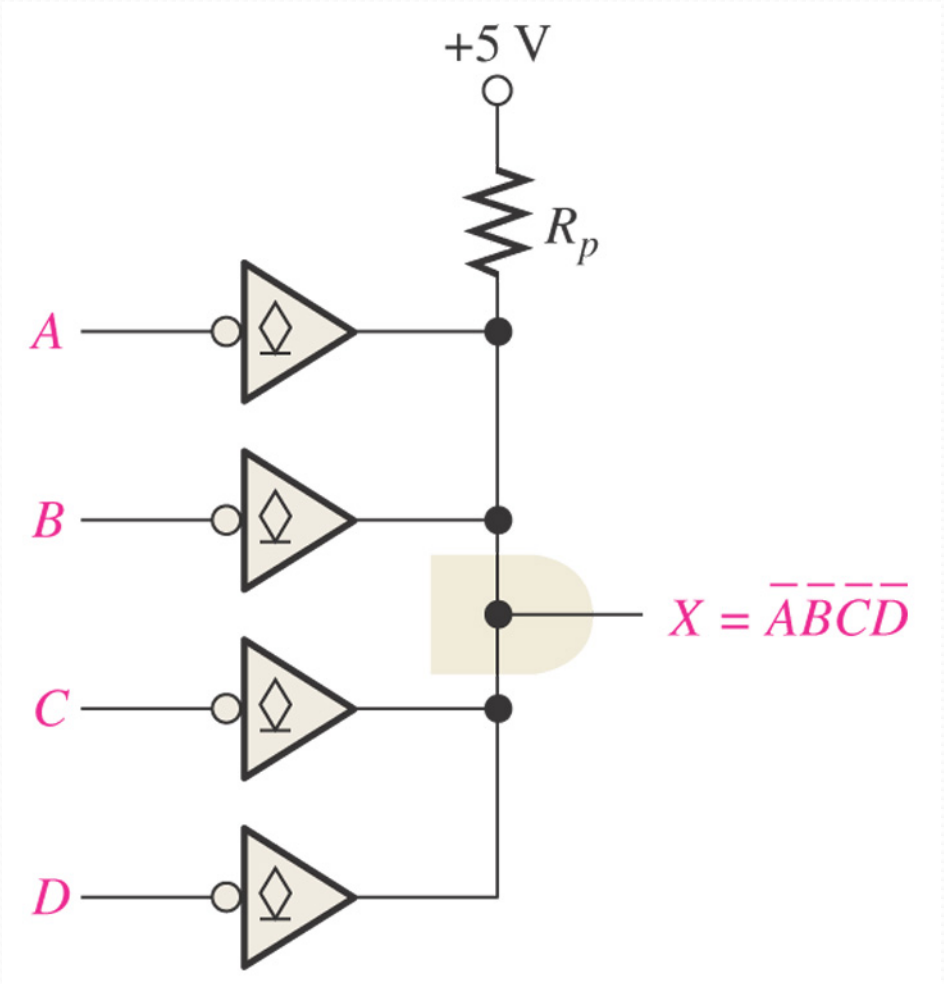



(a) Current sourcing ($I_{IH}$ value is maximum)



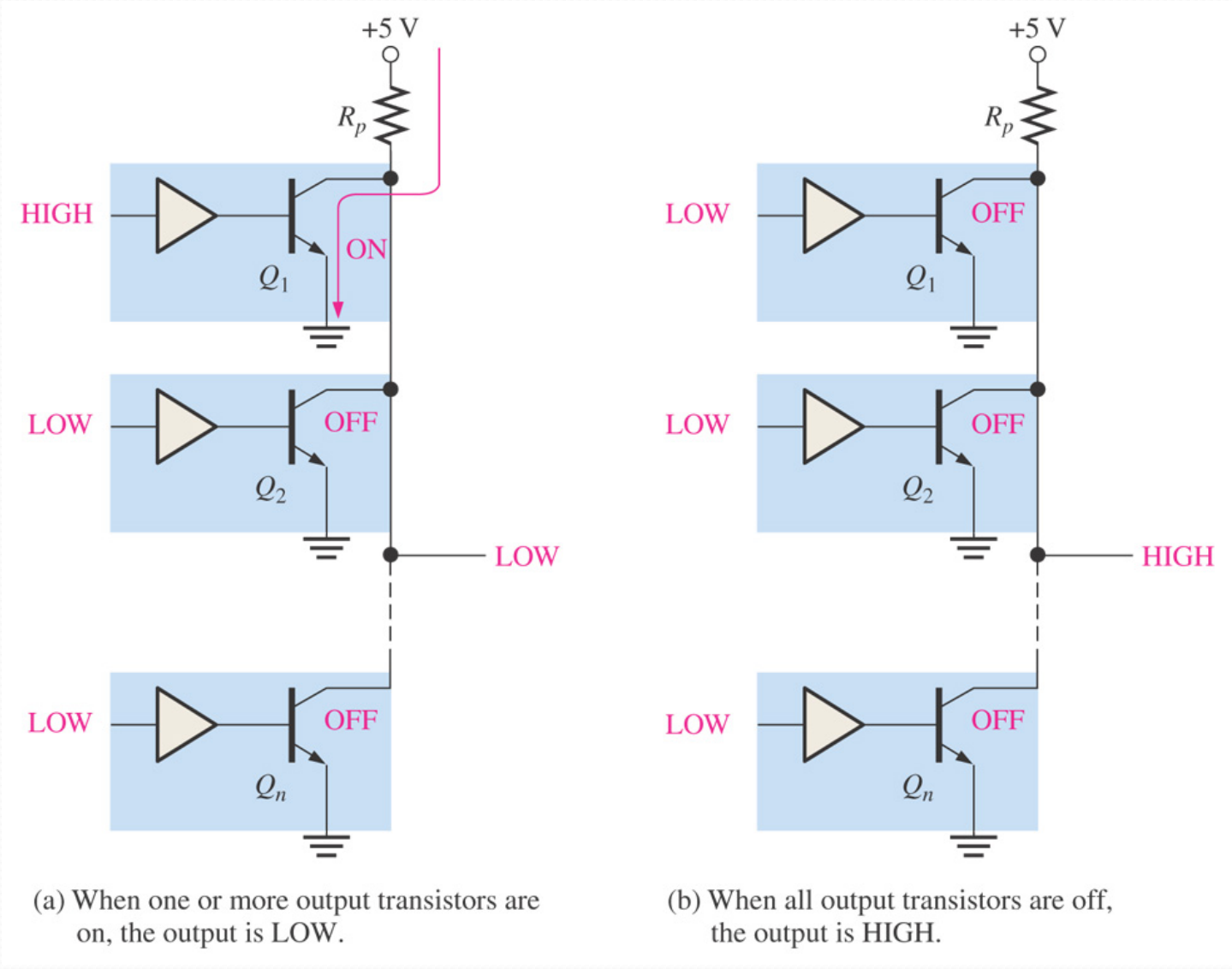

(b) Current sinking ($I_{IL}$ value is maximum)

# A wired-AND configuration of four inverters




Wired-AND: The output of open-collector gates are wired together.

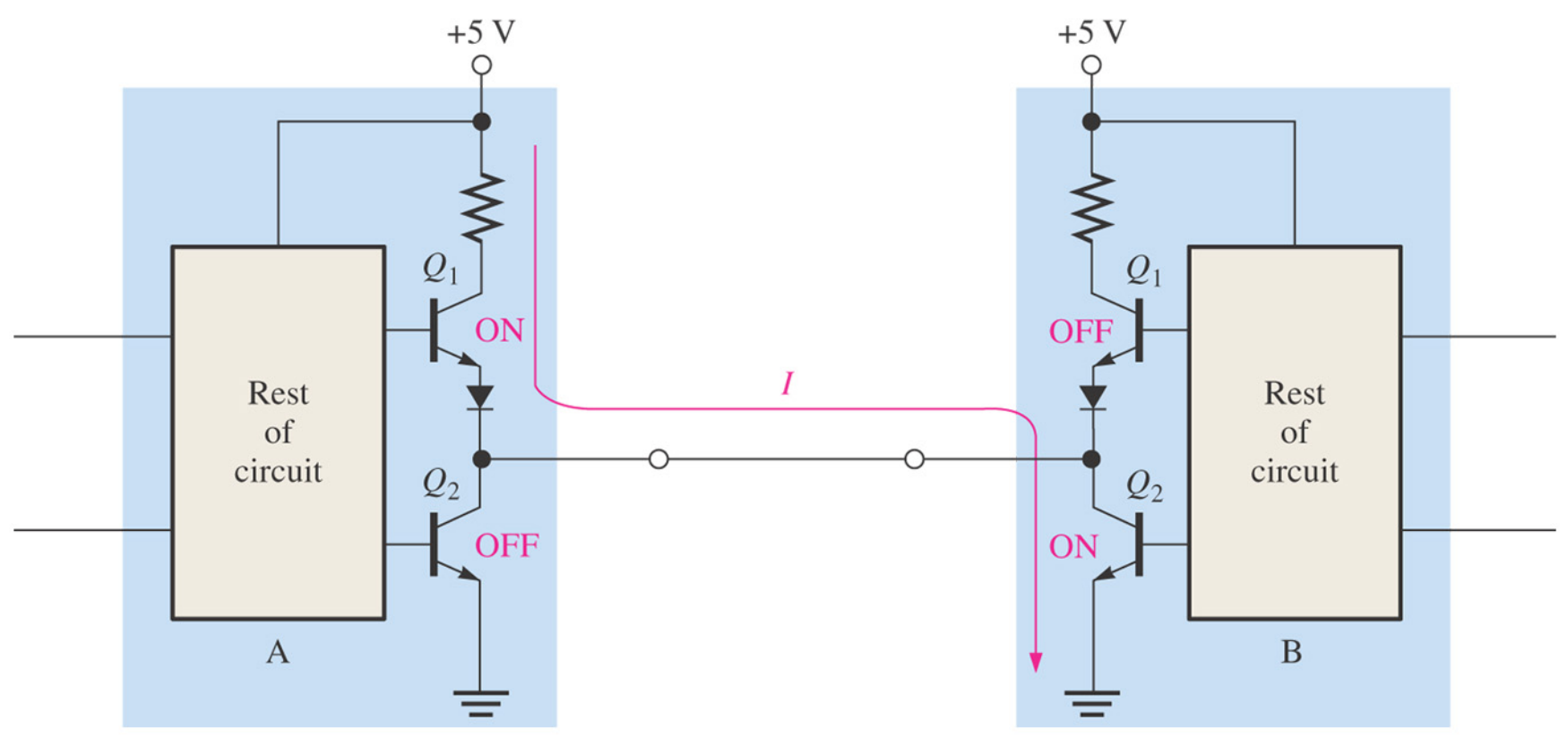
# Open-collector wired negative-AND operation with inverters.




(a) When one or more output transistors are on, the output is LOW.

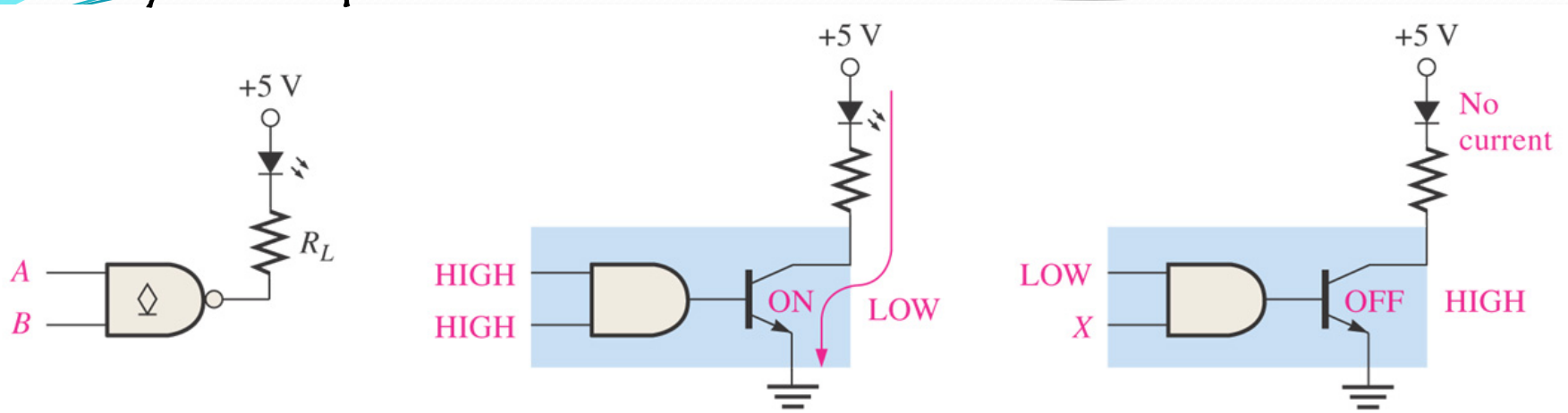
(b) When all output transistors are off, the output is HIGH.

# If the outputs of Totem-Pole are connected, …?

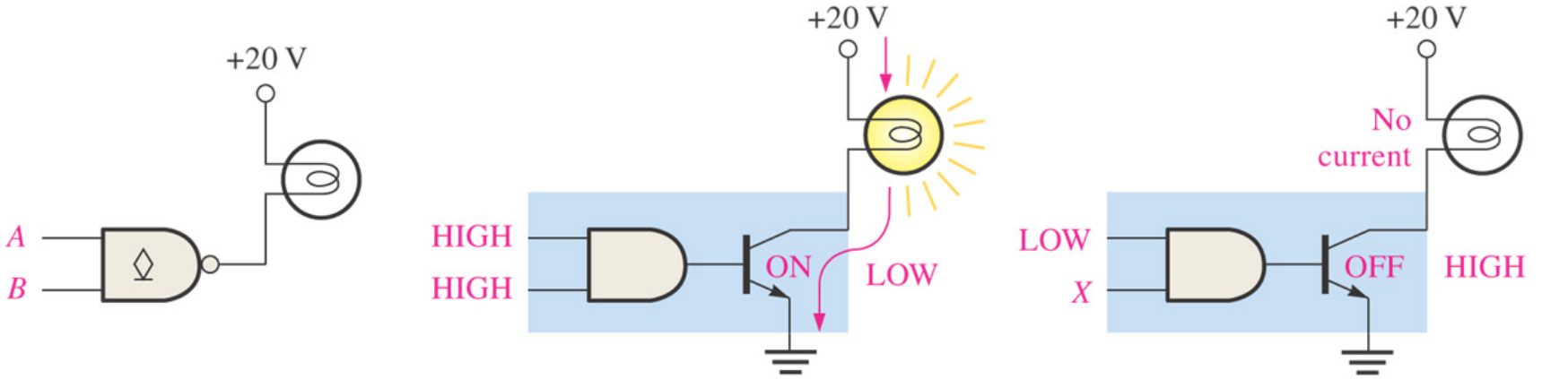



Totem-pole outputs wired together. Such a connection may cause excessive current through $Q_1$ of device A and $Q_2$ of device B and should never be used.

# Why an open-collector driver is so useful?




(a) Driving an LED



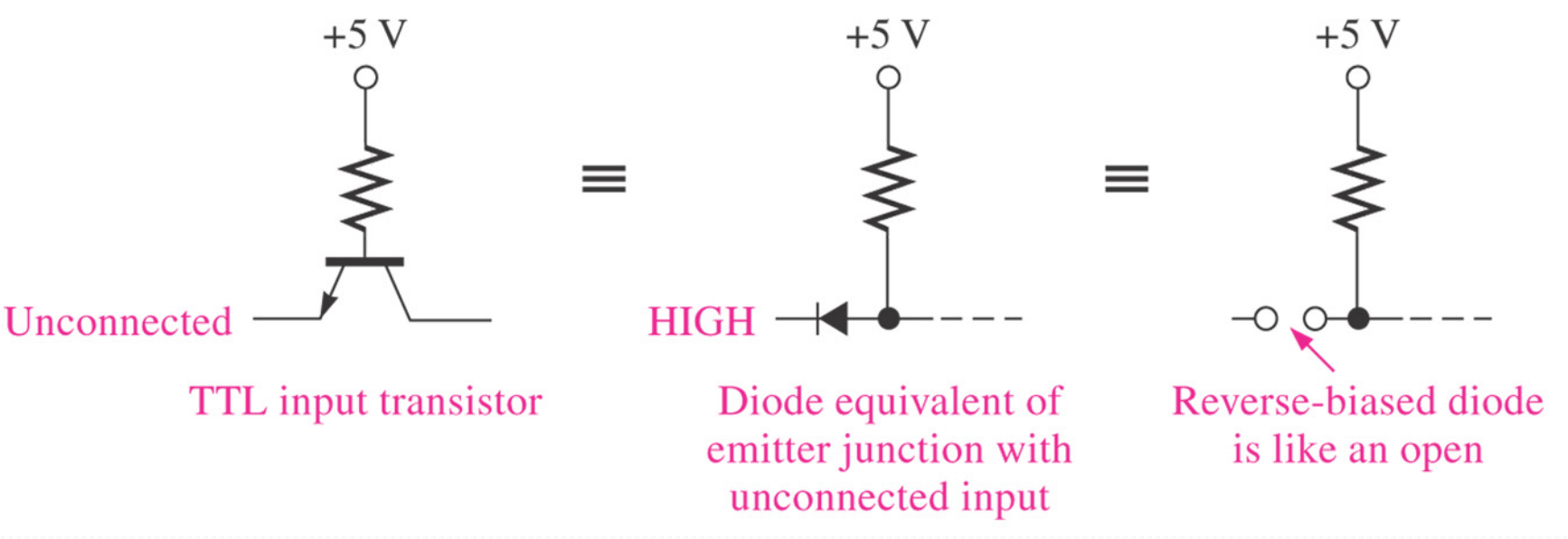

(b) Driving a low-current lamp

**Some applications of open-collector drivers**

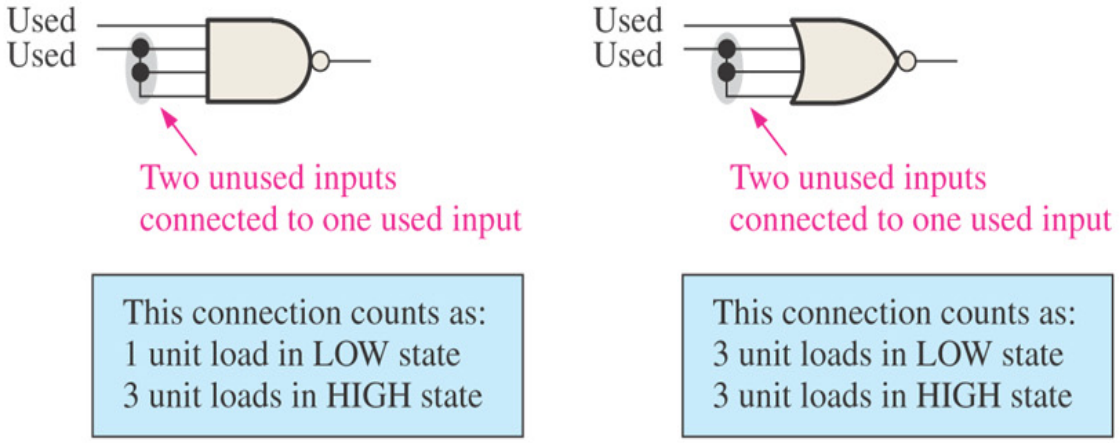
# How do we set those unused TTL inputs?

- An unconnected input on a TTL gate acts as a **HIGH**
- An open input results in a reverse-biased emitter junction on the input transistor
- It is best **NOT** to leave unused TTL inputs unconnected.

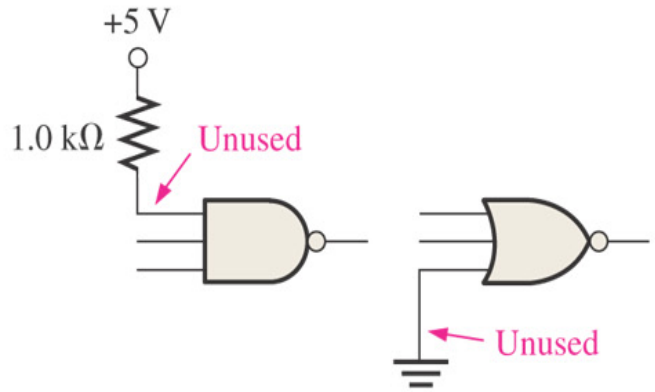
## Comparison of an open TTL input and a HIGH-level input.



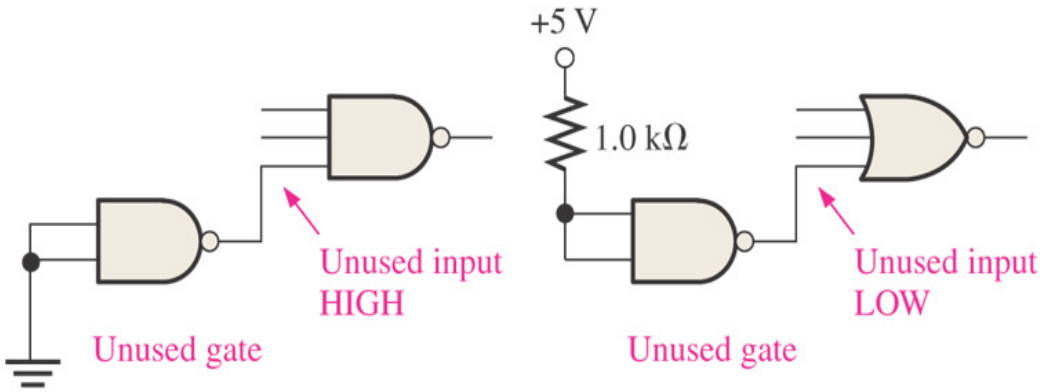
# Methods for handling unused TTL inputs




(a) Tied-together inputs




(b) Inputs to $V_{CC}$ or ground




(c) Inputs to unused output