Chapter 5 Combinational Logic Analysis

OUTLINE

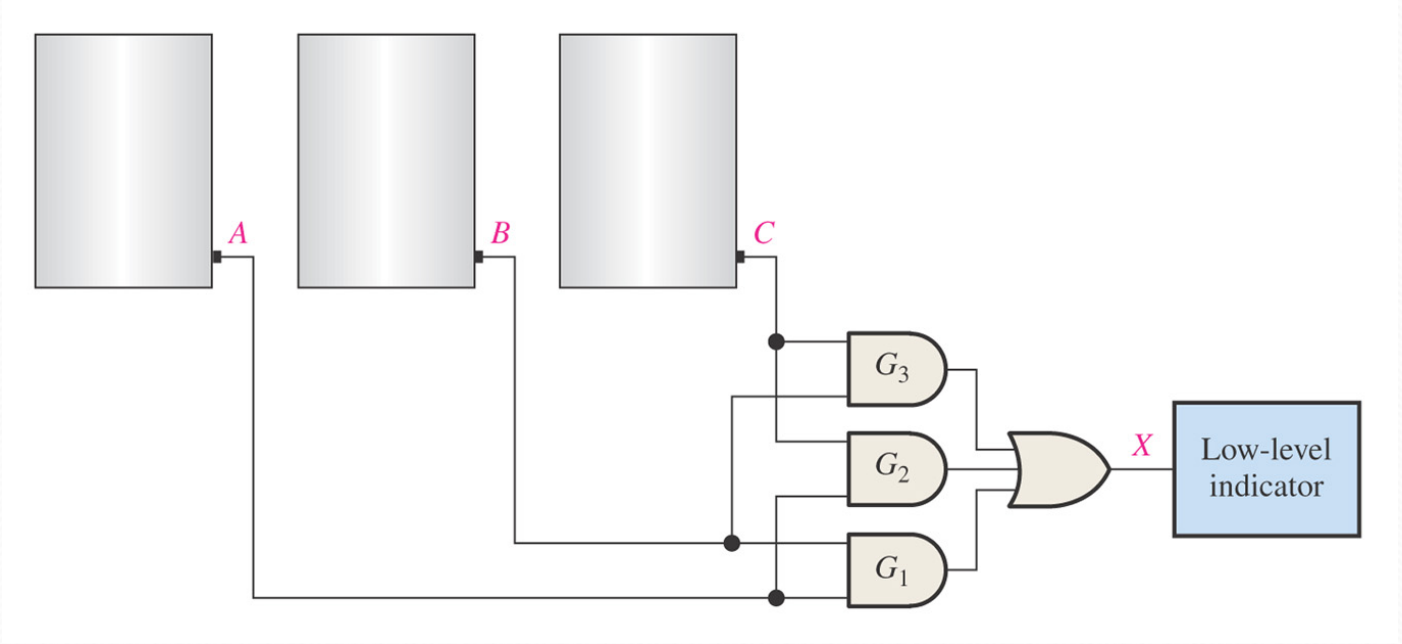
- Basic Combinational Logic Circuits
- Implementing Combinational Logic
- The Universal Property of NAND and NOR Gates
- Combinational Logic Using NAND and NOR Gates
- Logic Circuit Operation with Pulse Waveform Inputs

5.1 Basic Combinational Logic Circuits

- AND-OR Logic
  - SOP expressions can be implemented with
    - an AND gate for each product term
    - One OR gate for summing all of the product terms
  - The basic form for realizing standard Boolean functions

$$X = AB + BC + AC$$

Example: Low-level indicator for chemical tanks



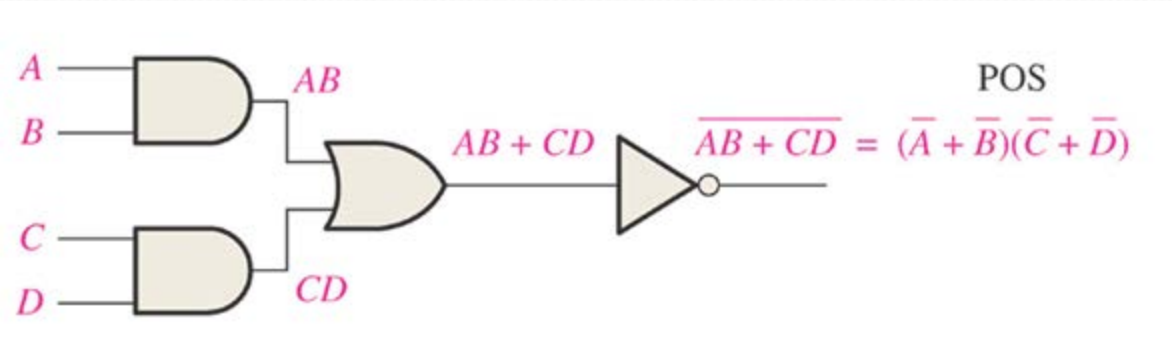
$$X = AB + BC + AC$$

X indicates the level in any two of the tanks drops below the specified point.

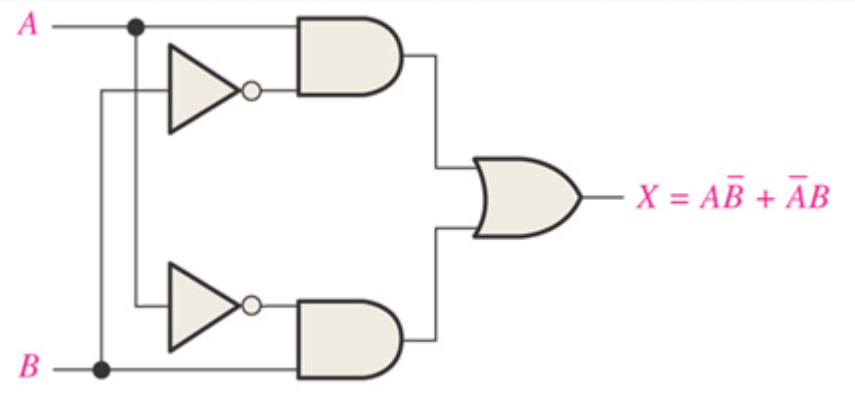
- AND-OR-Invert Logic
  - SOP can be implemented with AND-OR logic directly
  - POS expressions can be implemented with AND-OR-Invert logic

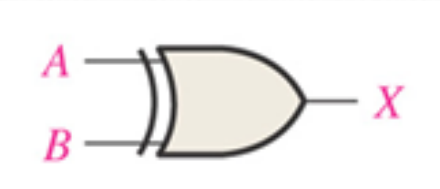
$$X = (\overline{A} + \overline{B})(\overline{C} + \overline{D}) = (\overline{AB})(\overline{CD})$$

$$= \overline{\overline{(\overline{AB})(\overline{CD})}} = \overline{\overline{AB} + \overline{CD}} = \overline{AB + CD}$$



- Exclusive-OR Logic

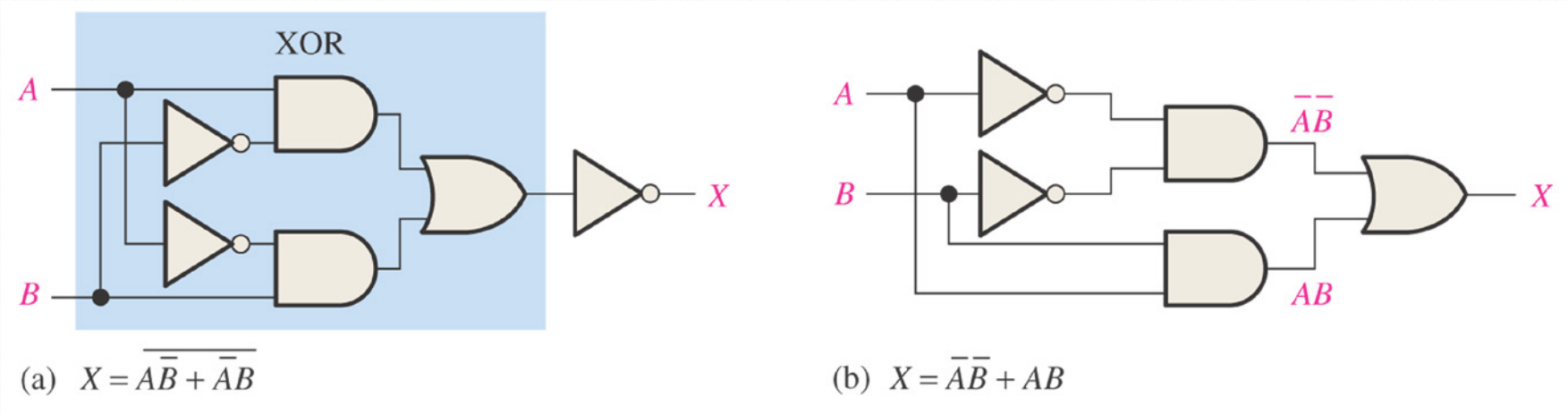




$$X = A\overline{B} + \overline{A}B$$

$$X = A \oplus B$$

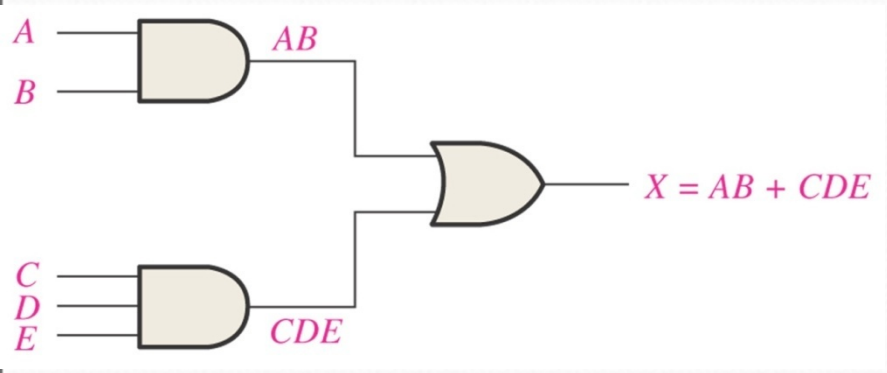
- Exclusive-NOR Logic



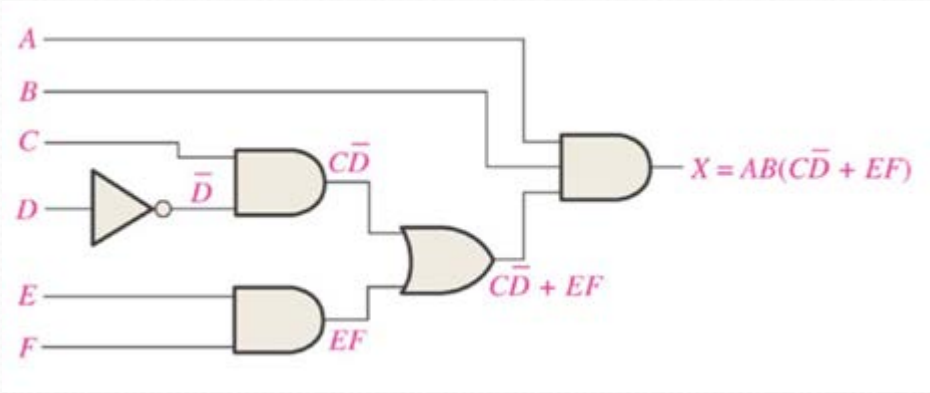
$$X = \overline{A\overline{B} + \overline{A}B} = \overline{(A\overline{B})}\,\overline{(\overline{A}B)} = (\overline{A} + B)(A + \overline{B}) = \overline{A}\overline{B} + AB$$

5.2 Implementing Combinational Logic

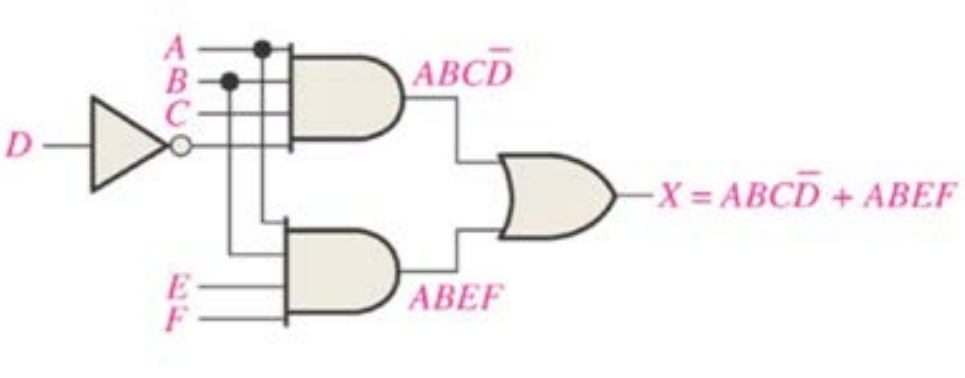
- From a Boolean Expression to a Logic Circuit



Logic circuit for $X = AB + CDE$.



$$X = AB(C\bar{D} + EF) = ABC\bar{D} + ABEF$$



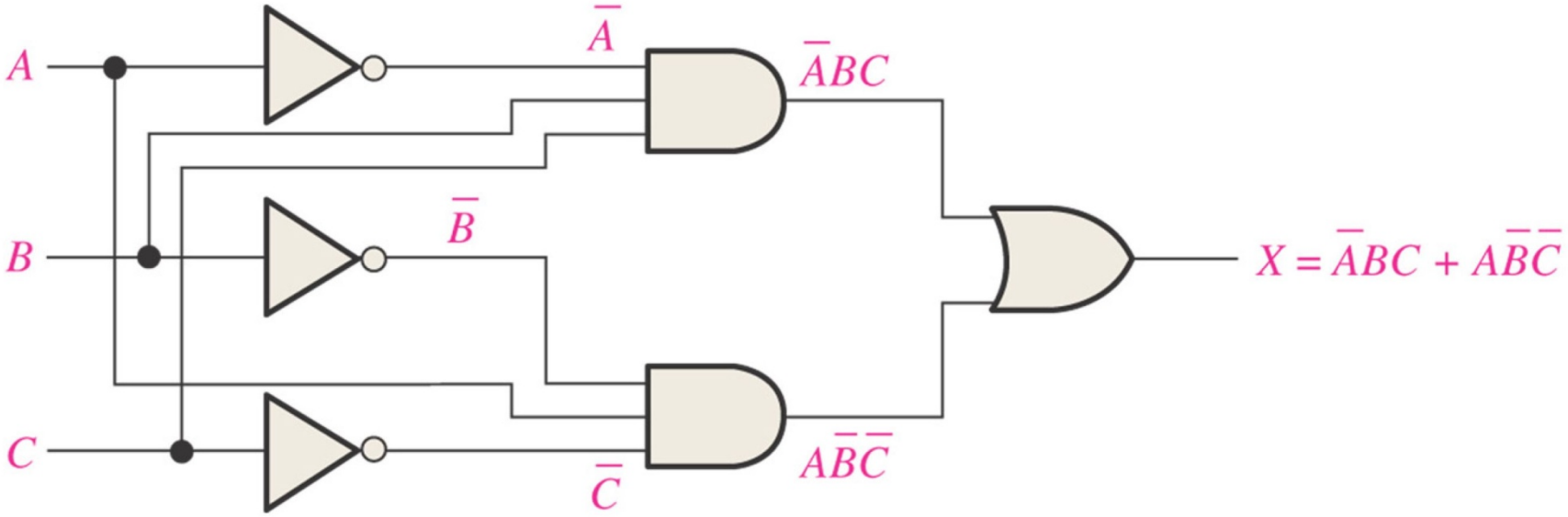
- From a Truth Table to a Logic Circuit

Input			Output	Product Term
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	1	$A\overline{B}\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

$$X = \overline{A}BC + A\overline{B}\overline{C}$$

ORing the product terms for which X=1

Figure 5–9 Logic circuit for $X = \overline{A}BC + A\overline{BC}$. Open file F05-09 to verify the operation.



Example: Design a logic circuit to implement the operation specified in the following truth table.

Input			Output	Product Term
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\rightarrow \overline{A}BC$
1	0	0	0	
1	0	1	1	$\rightarrow A\overline{B}C$
1	1	0	1	$\rightarrow AB\overline{C}$
1	1	1	0	

$$X = \overline{A}BC + A\overline{B}C + AB\overline{C}$$

$$X = \overline{A}BC + A\overline{B}C + AB\overline{C}$$

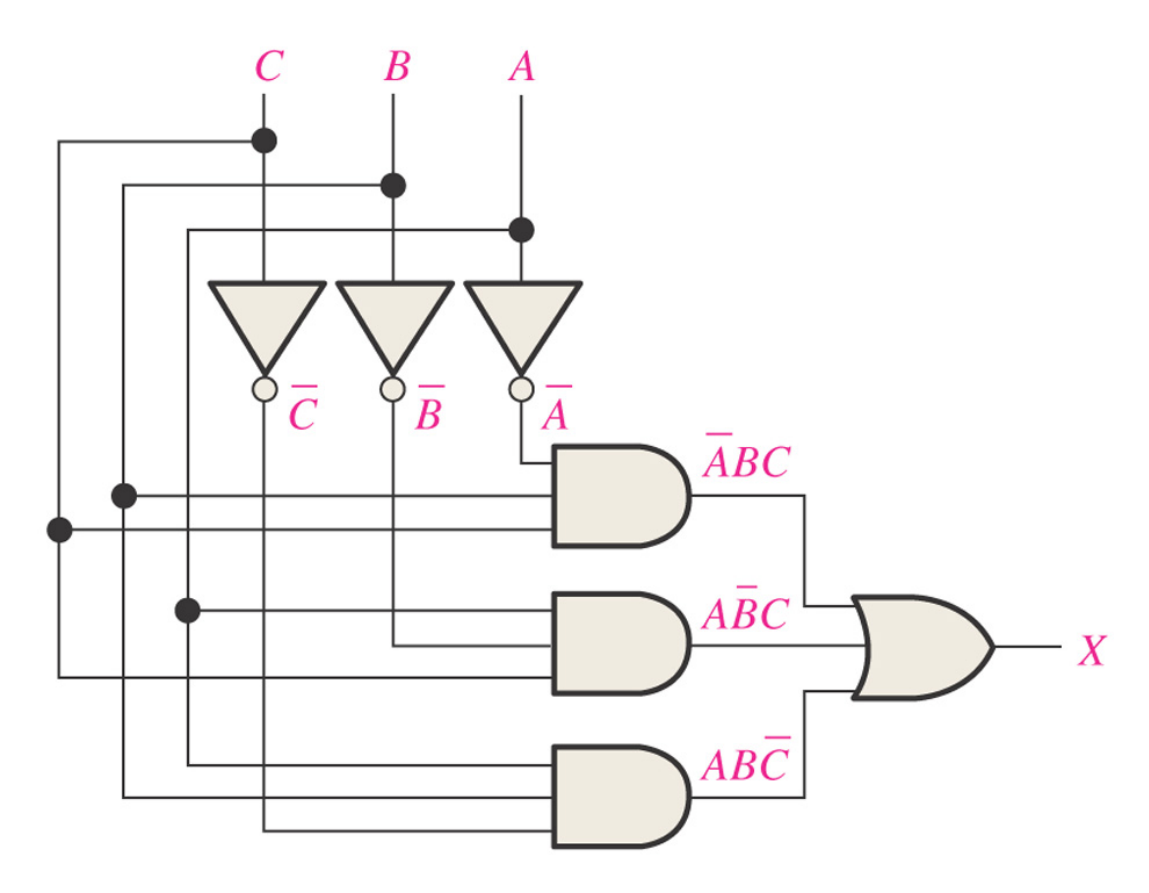
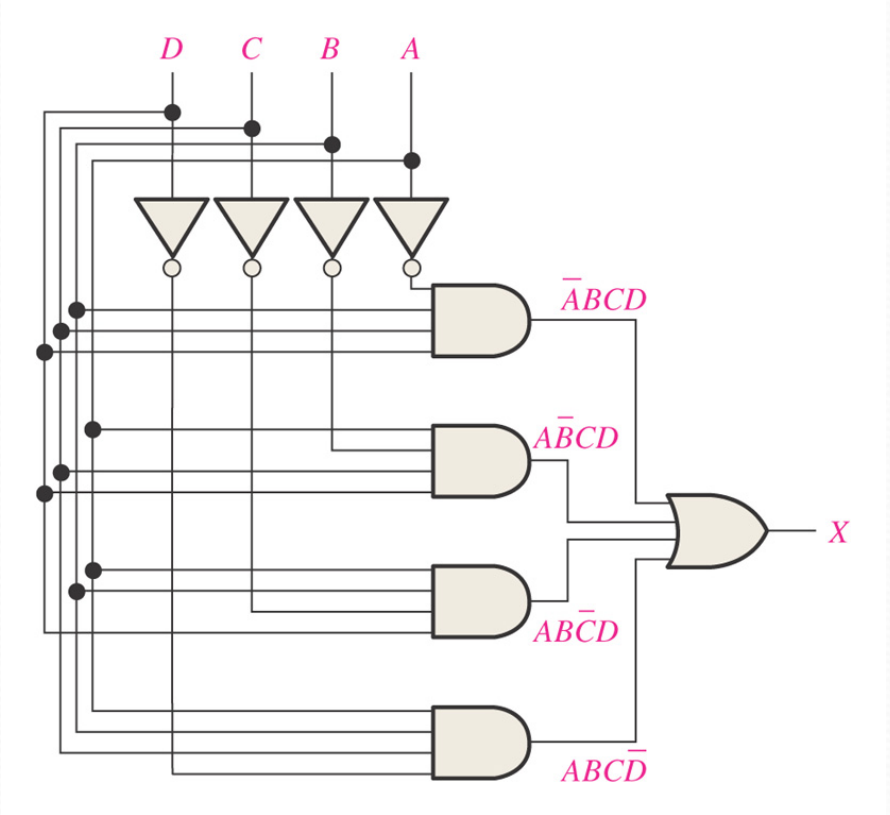


Figure 5–10 Implementation .

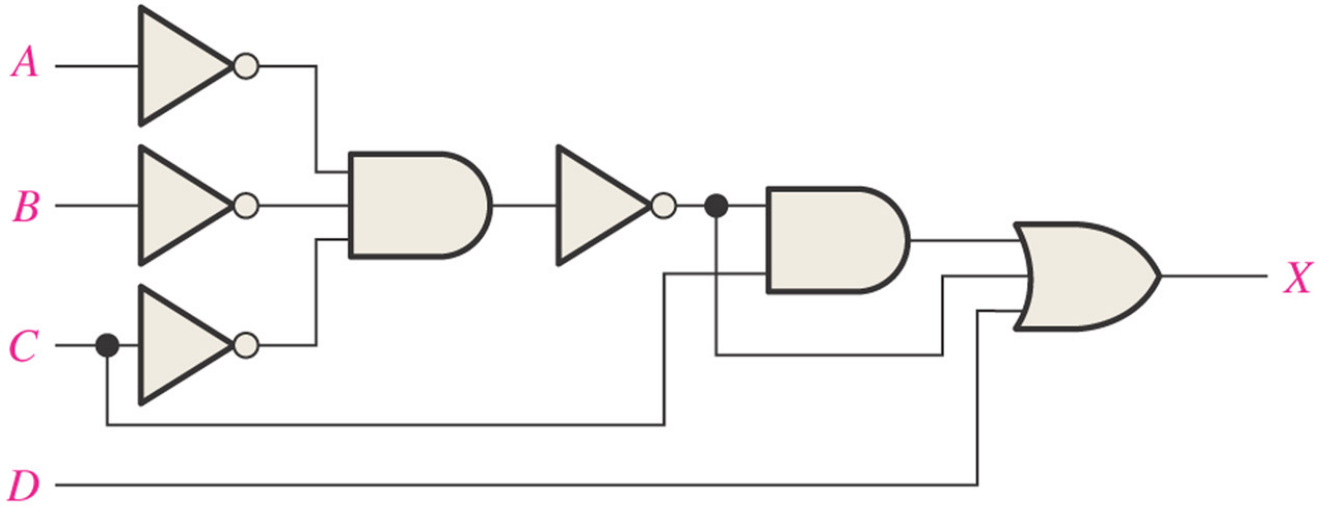
Example: Design a logic circuit to implement the operation specified in the following truth table.

A	B	C	D	Product Term
0	1	1	1	$\overline{A}BCD$
1	0	1	1	$A\overline{B}CD$
1	1	0	1	$AB\overline{C}D$
1	1	1	0	$ABC\overline{D}$



$$X = \overline{A}BCD + A\overline{B}CD + AB\overline{C}D + ABC\overline{D}$$

Example: **Reduce the combinational logic circuit to a minimum form**



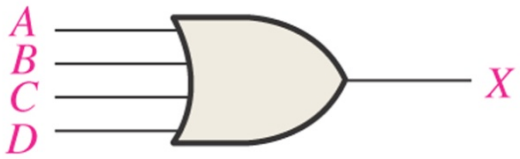
$$X = (\overline{\overline{\overline{\overline{ABC}}}})C + \overline{\overline{\overline{\overline{ABC}}}} + D$$

$$= (\overline{\overline{A} + \overline{B} + \overline{C}})C + \overline{\overline{A} + \overline{B} + \overline{C}} + D$$

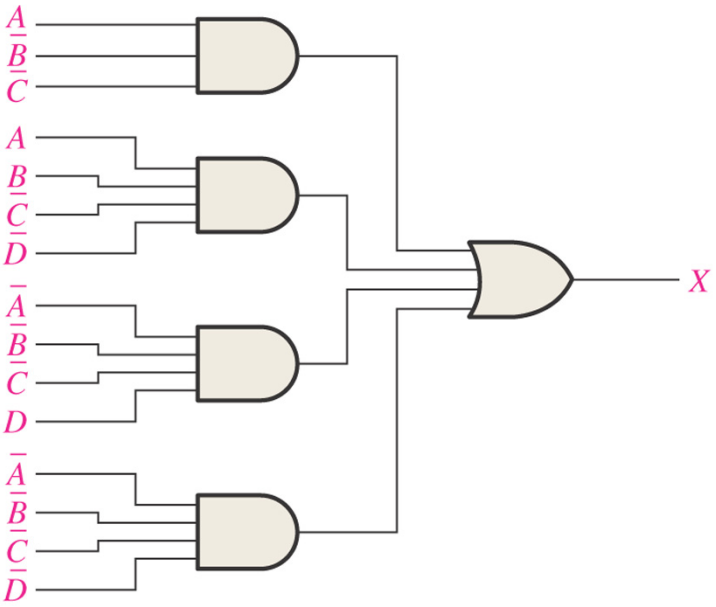
$$= AC + BC + CC + A + B + C + D$$

$$= C(A + B + 1) + A + B + D$$

$$= A + B + C + D$$

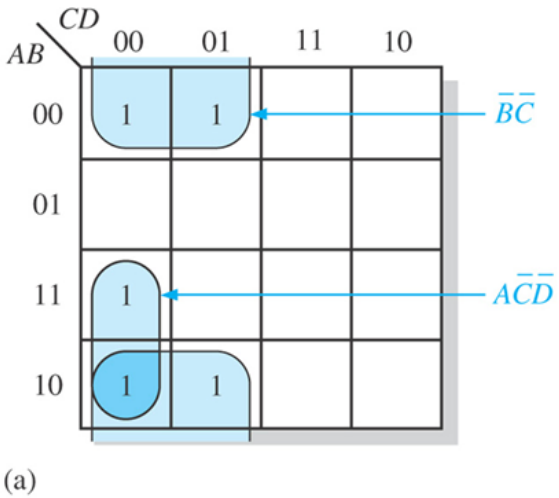


Example: **Minimize the combinational logic circuit shown in the following figure.**



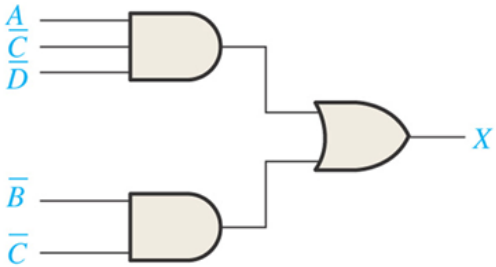
$$X = A\overline{B}\overline{C} + AB\overline{C}D + \overline{A}BCD + \overline{A}BC\overline{D}$$

$$= A\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BC\overline{D}$$



(a)

$$X = A\overline{C}\overline{D} + \overline{B}\overline{C}$$

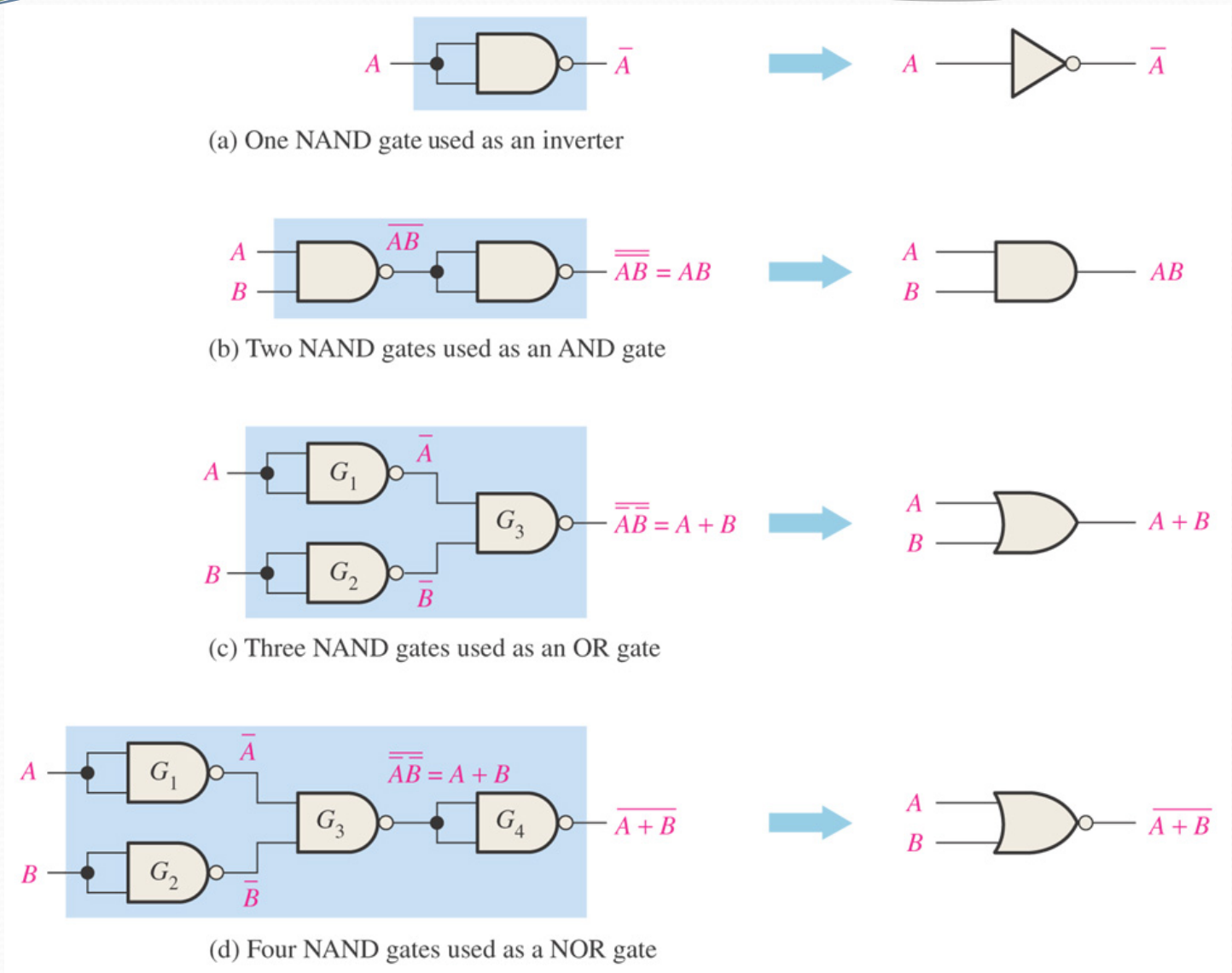


(b)

5.3 The Universal Property of NAND and NOR Gates

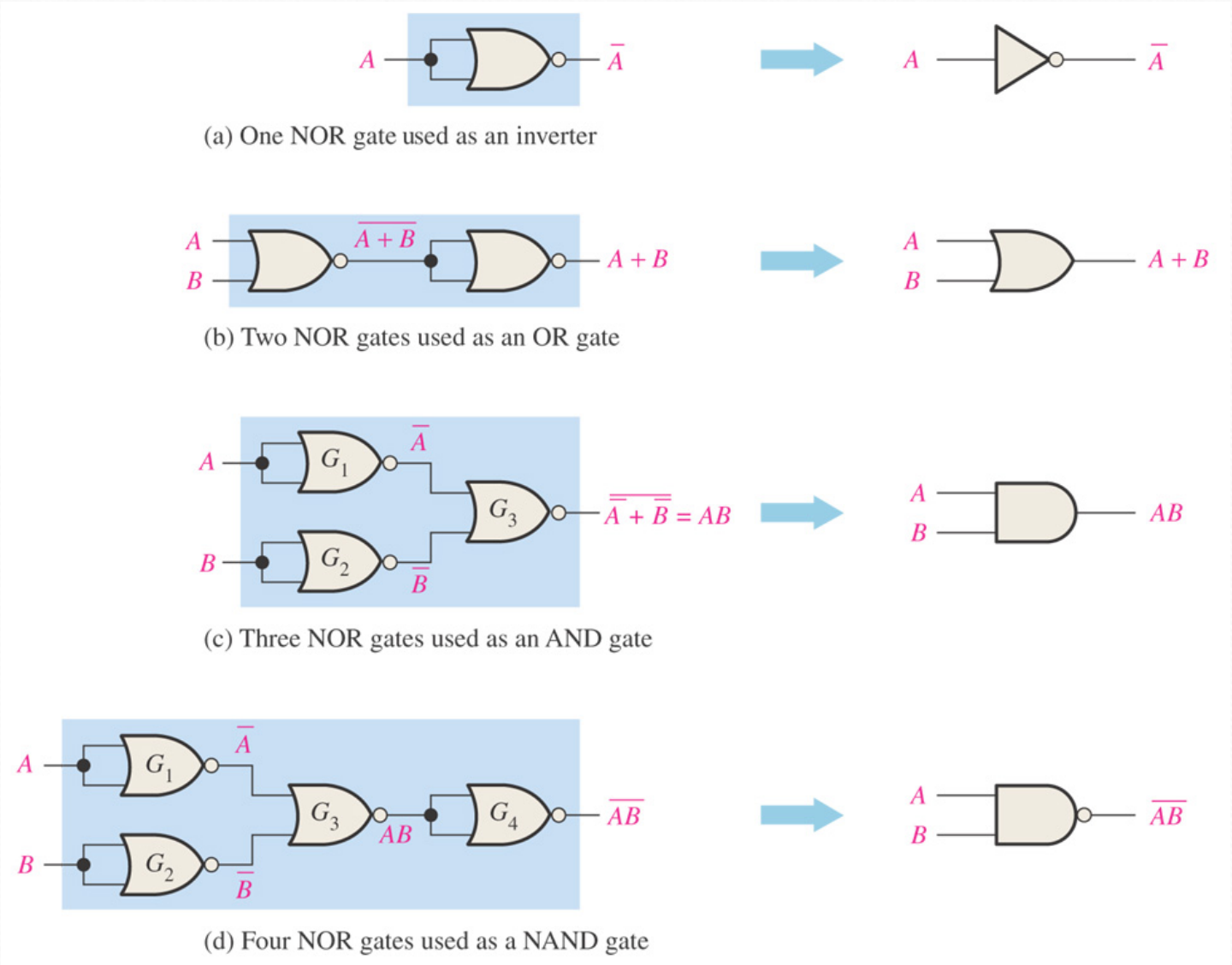
- The NAND Gate as a Universal Logic Element
  - Be used to produce the NOT, the AND, the OR, and the NOR functions.

Figure 5–16 Universal application of NAND gates.



- The NOR gate as a universal logic element
  - Be used to produce the NOT, the AND, the OR, and the NAND functions.

Figure 5–17 Universal application of NOR gates.



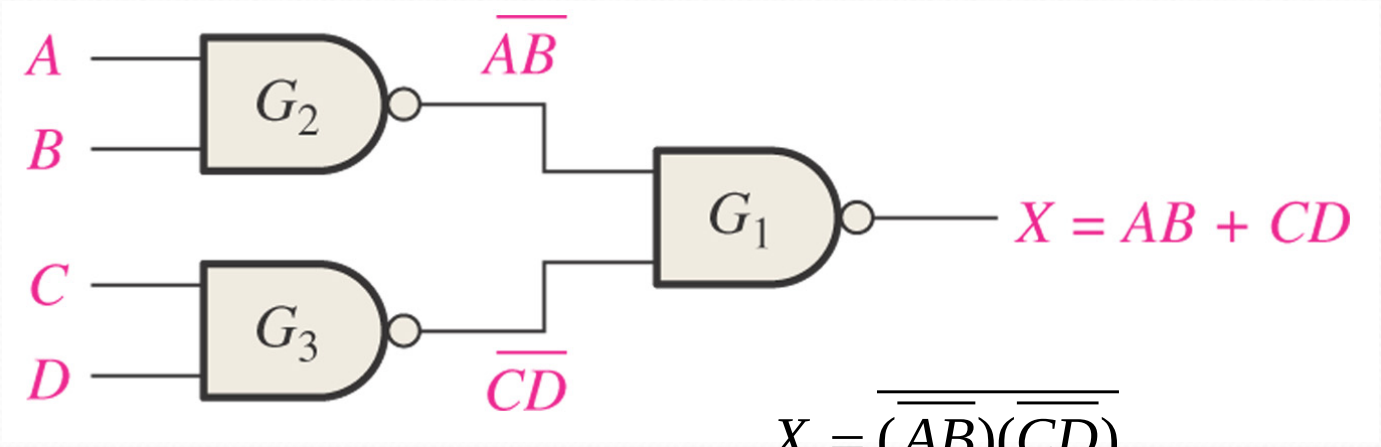
5.4 Combinational Logic Using NAND and NOR Gates

- How can NAND and NOR gates be used to implement a logic function?

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A}\,\overline{B}$$

Figure 5–18 NAND logic for $X = AB + CD$.



$$X = \overline{(\overline{AB})(\overline{CD})}$$

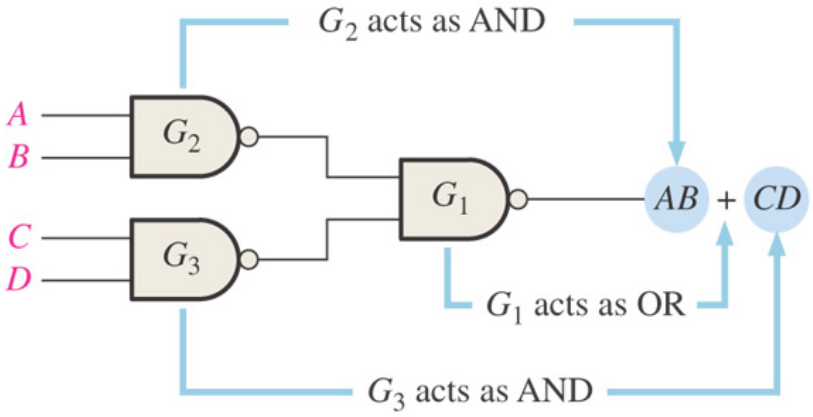
$$= \overline{(\overline{A} + \overline{B})(\overline{C} + \overline{D})}$$

$$= \overline{(\overline{A} + \overline{B})} + \overline{(\overline{C} + \overline{D})}$$

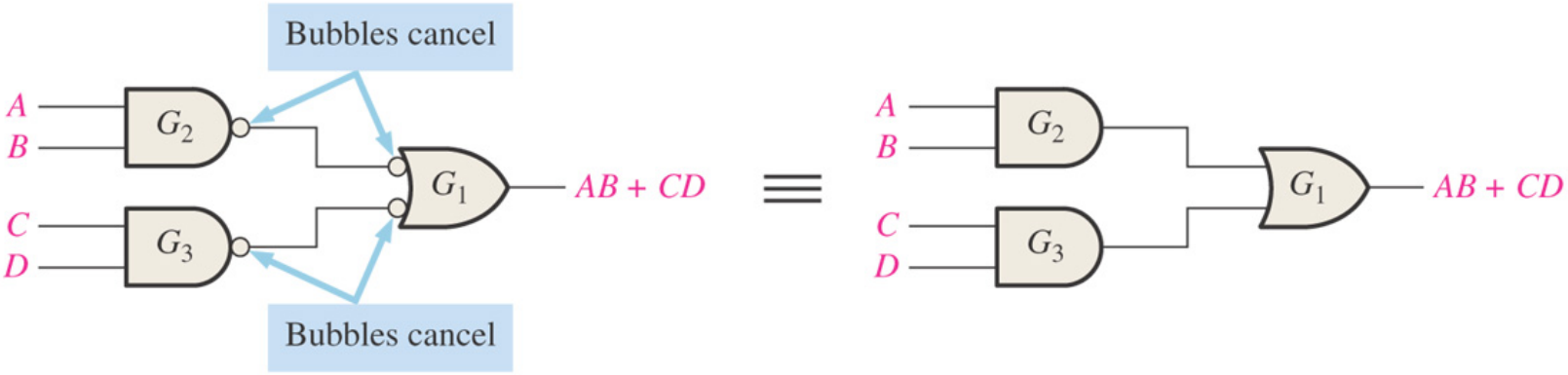
$$= \overline{\overline{AB}} + \overline{\overline{CD}}$$

$$= AB + CD$$

Figure 5–19 Development of the AND-OR equivalent of the circuit in Figure 5–18.



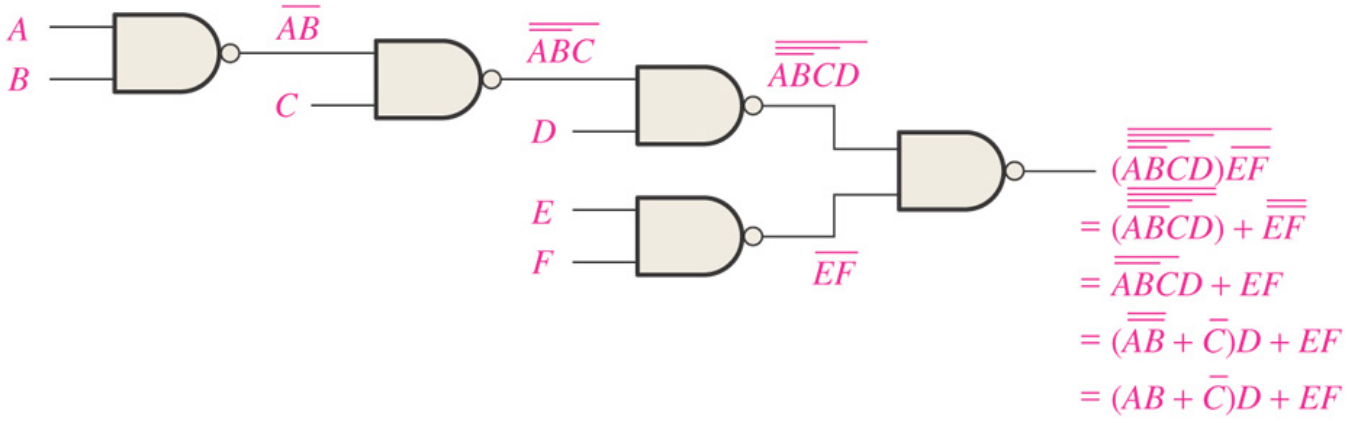
(a) Original NAND logic diagram showing effective gate operation relative to the output expression



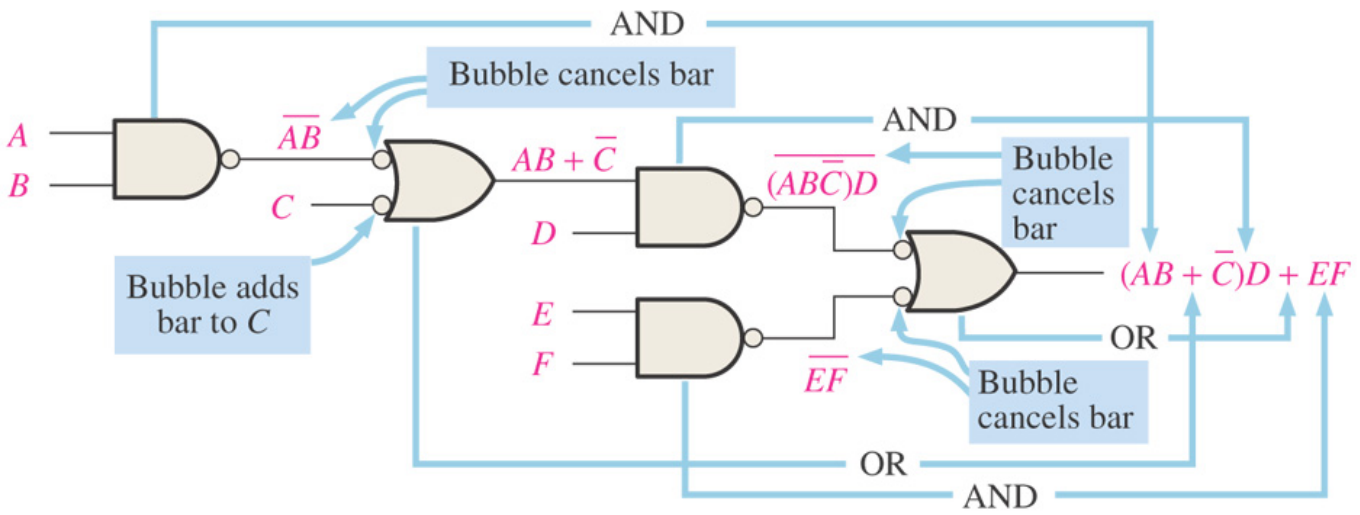
(b) Equivalent NAND/Negative-OR logic diagram

(c) AND-OR equivalent

Figure 5–20 Illustration of the use of the appropriate dual symbols in a NAND logic diagram.

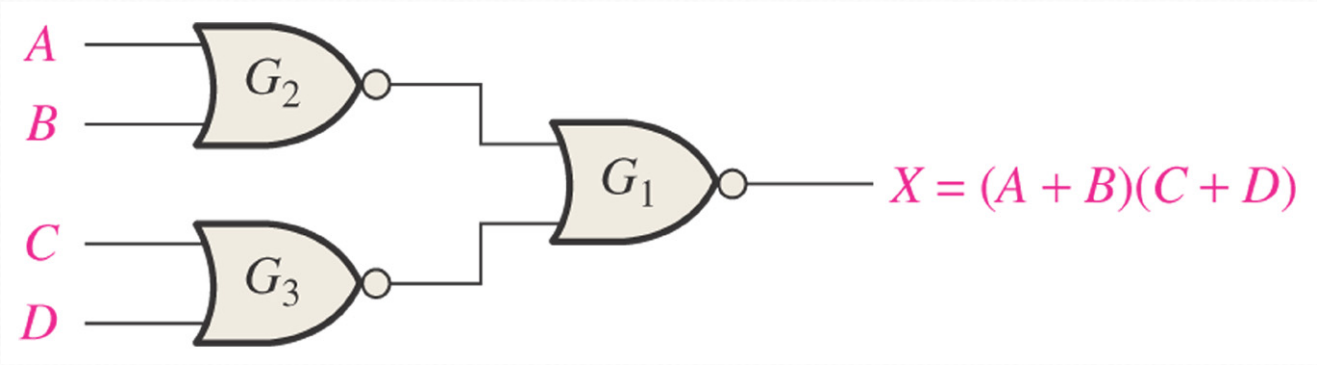


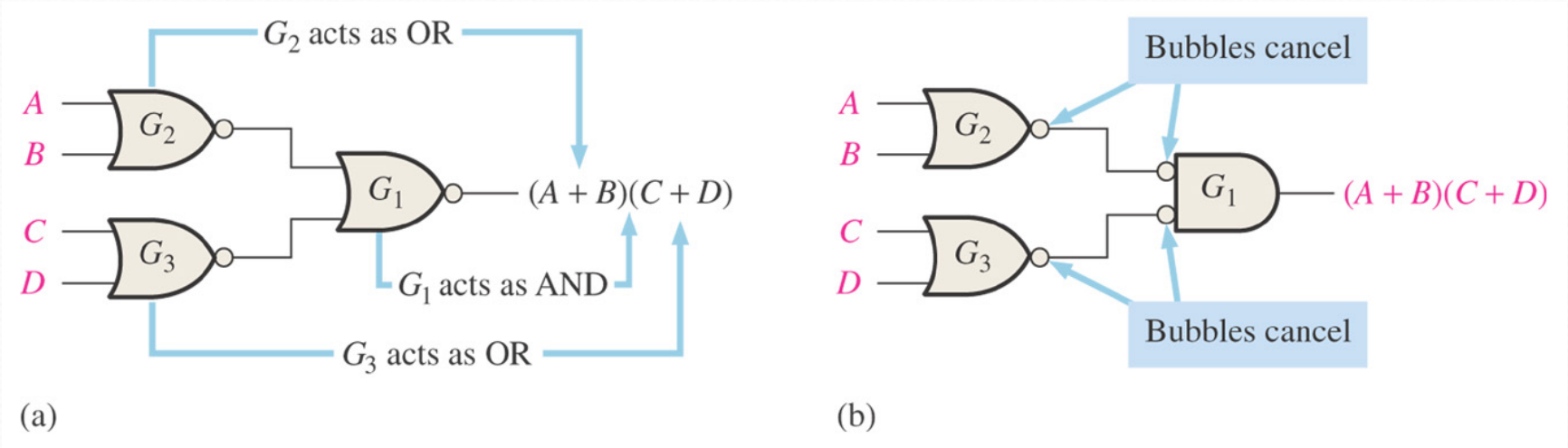
(a) Several Boolean steps are required to arrive at final output expression.



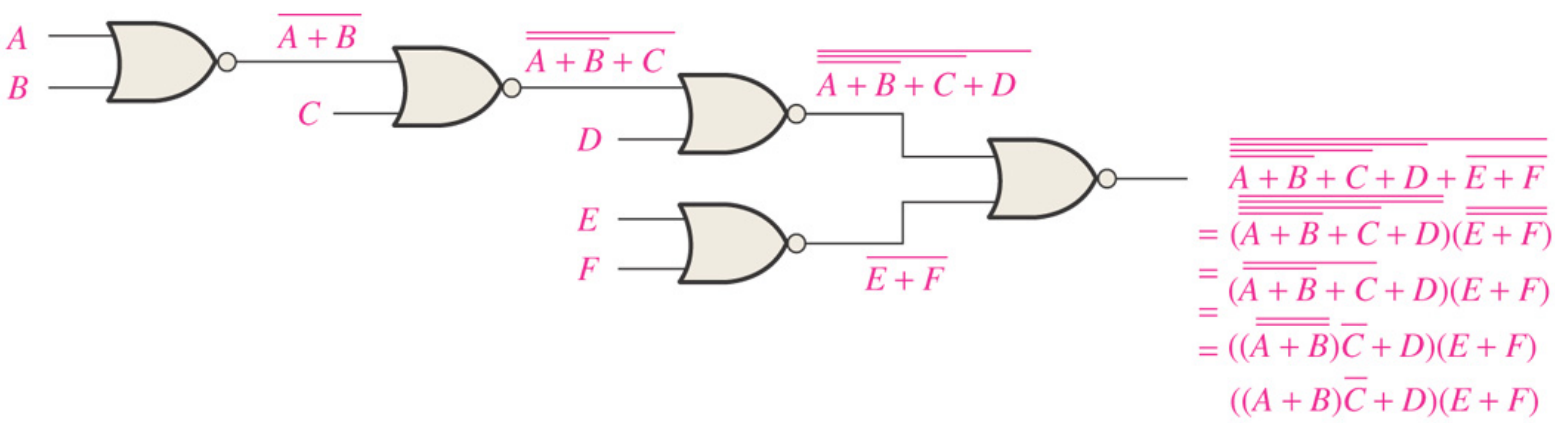
(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Figure 5–24 NOR logic for $X = (A + B)(C + D)$.

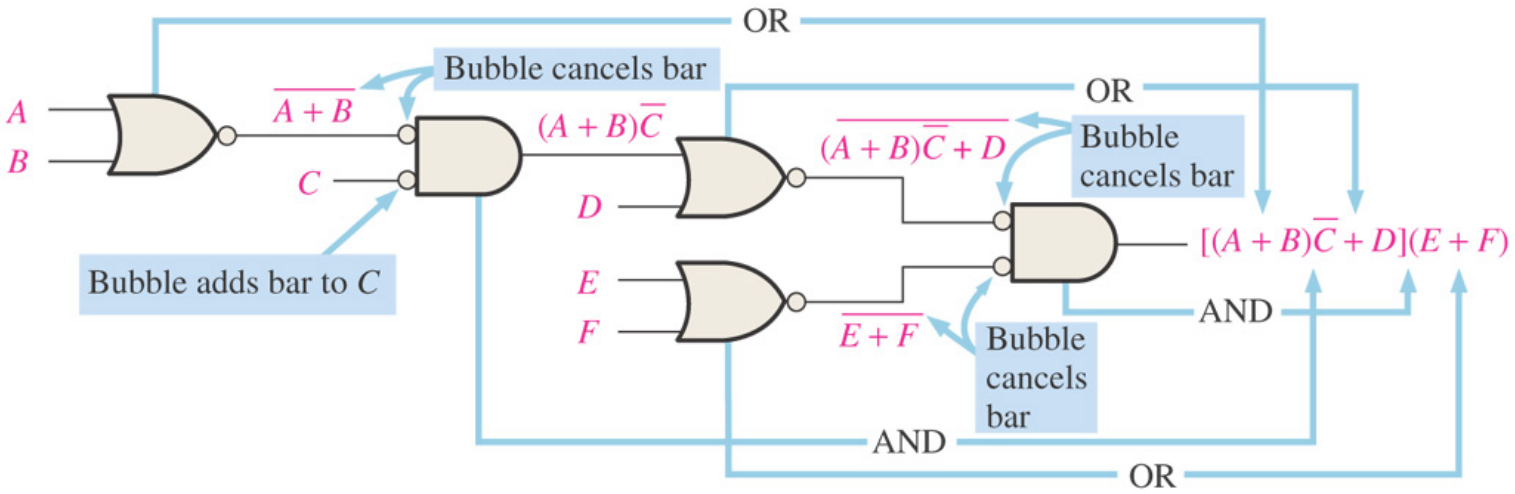




Example: Illustration of the use of the appropriate dual symbols in a NOR logic diagram.

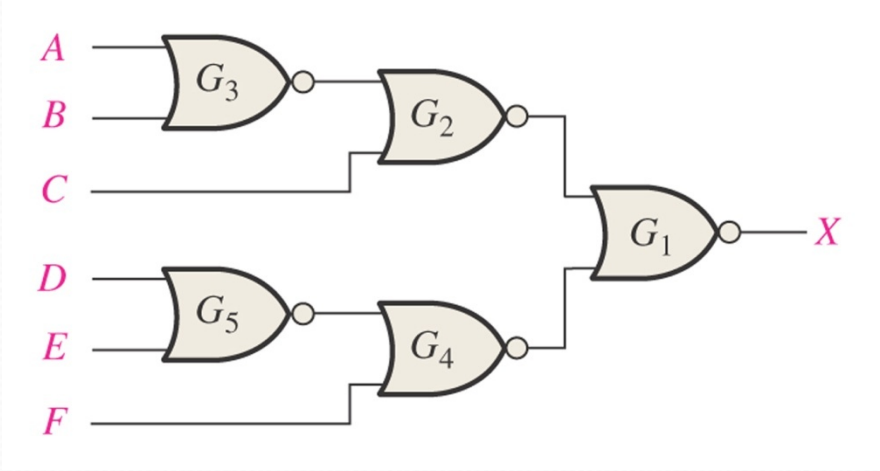


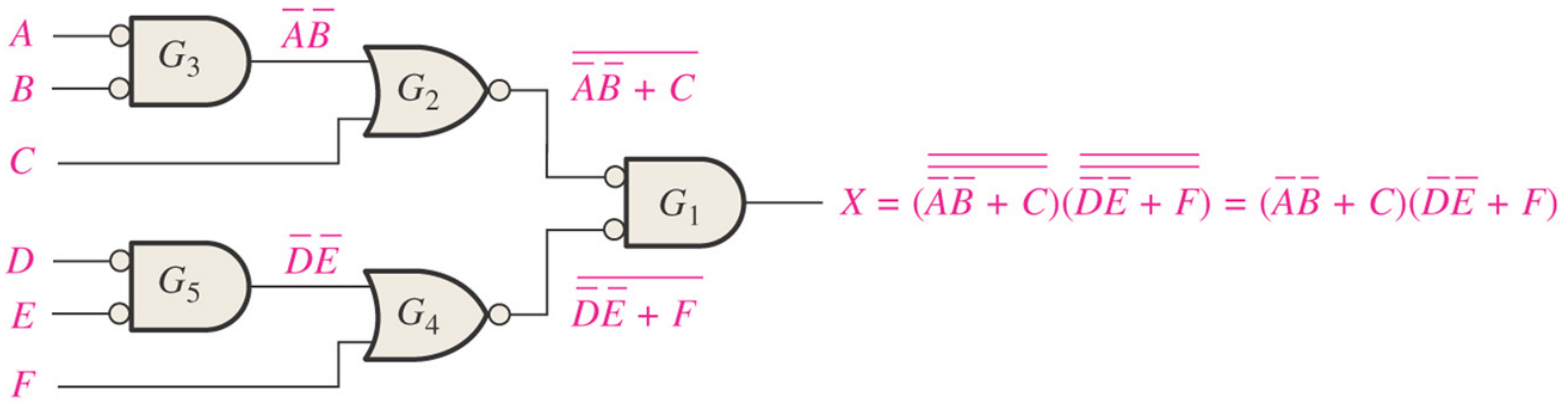
(a) Final output expression is obtained after several Boolean steps.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Example: Using appropriate dual symbols, redraw the logic diagram and develop the output expression for the circuit in the following figure.

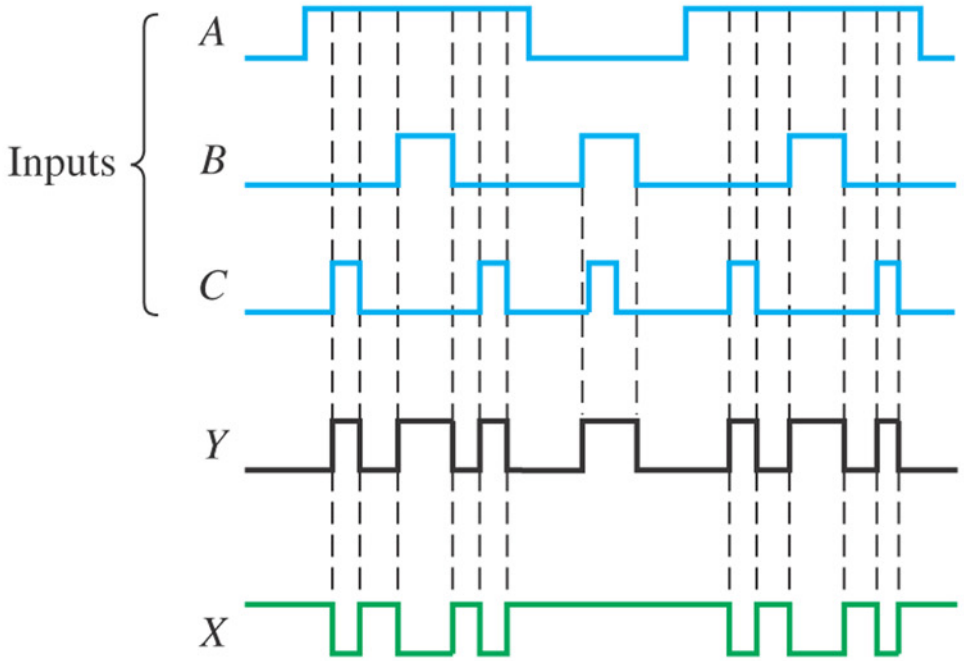


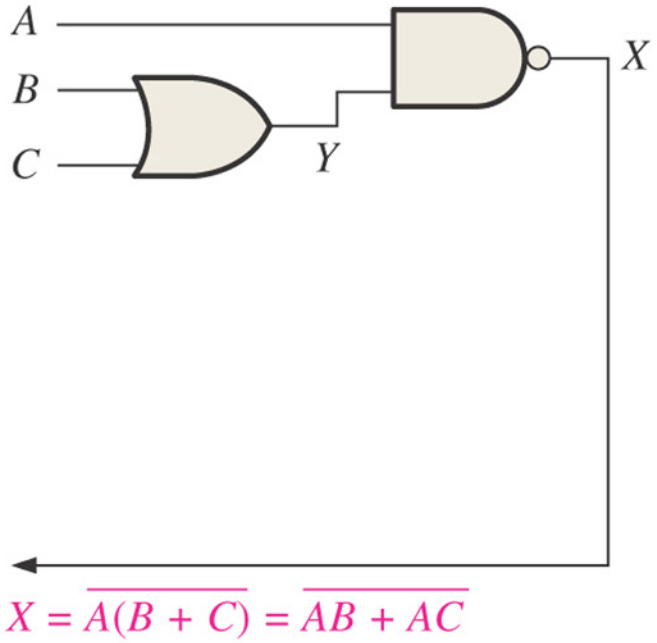


5.5 Logic Circuit Operation with Pulse Waveform Inputs

- The output of an AND gate is ***HIGH*** only when all inputs are ***HIGH*** at the same time;
- The output of an OR gate is ***HIGH*** only when at least one of its inputs is ***HIGH***;
- The output of a NAND gate is ***LOW*** only when all inputs are ***HIGH*** at the same time;
- The output of a NOR gate is ***LOW*** only when at least one of its inputs is ***HIGH***.

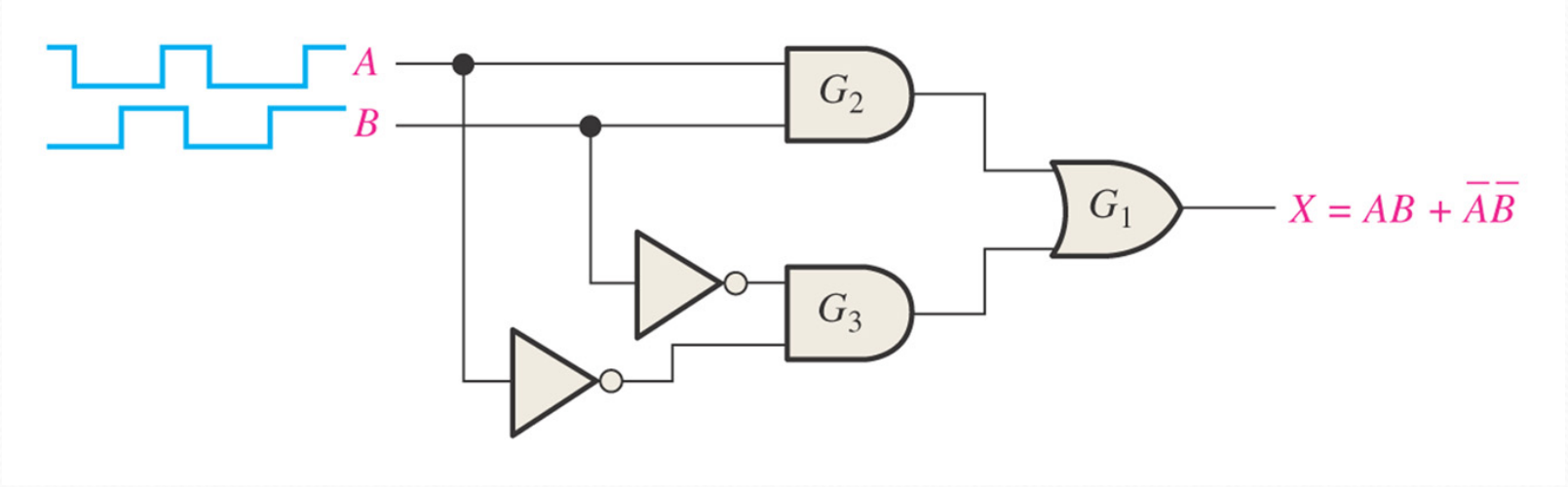
Example: **Determine the final output waveform X for the circuit in the following figure, with input waveforms A, B, and C as shown.**

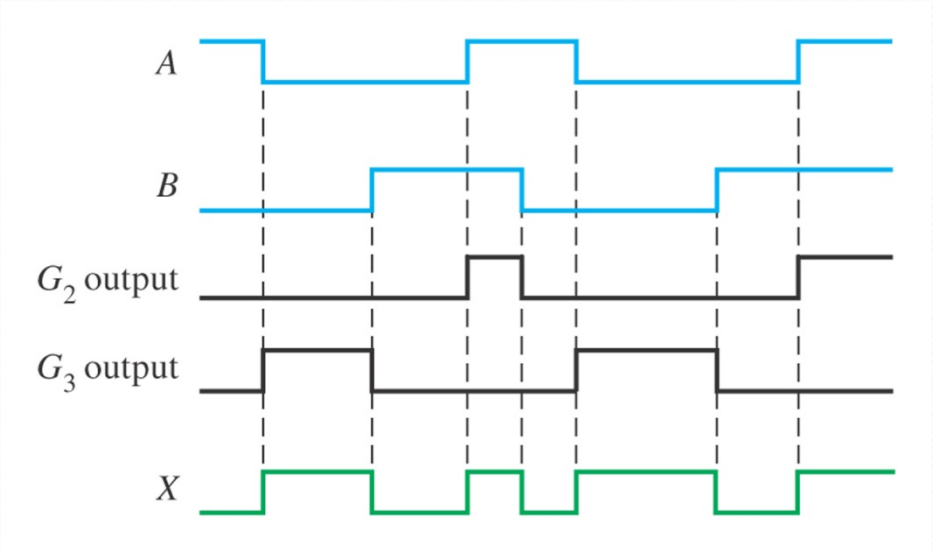




$$X = \overline{A(B + C)} = \overline{AB + AC}$$

Example: **Determine the final output waveform X for the circuit in the following figure, with input waveforms A, B, and C as shown.**





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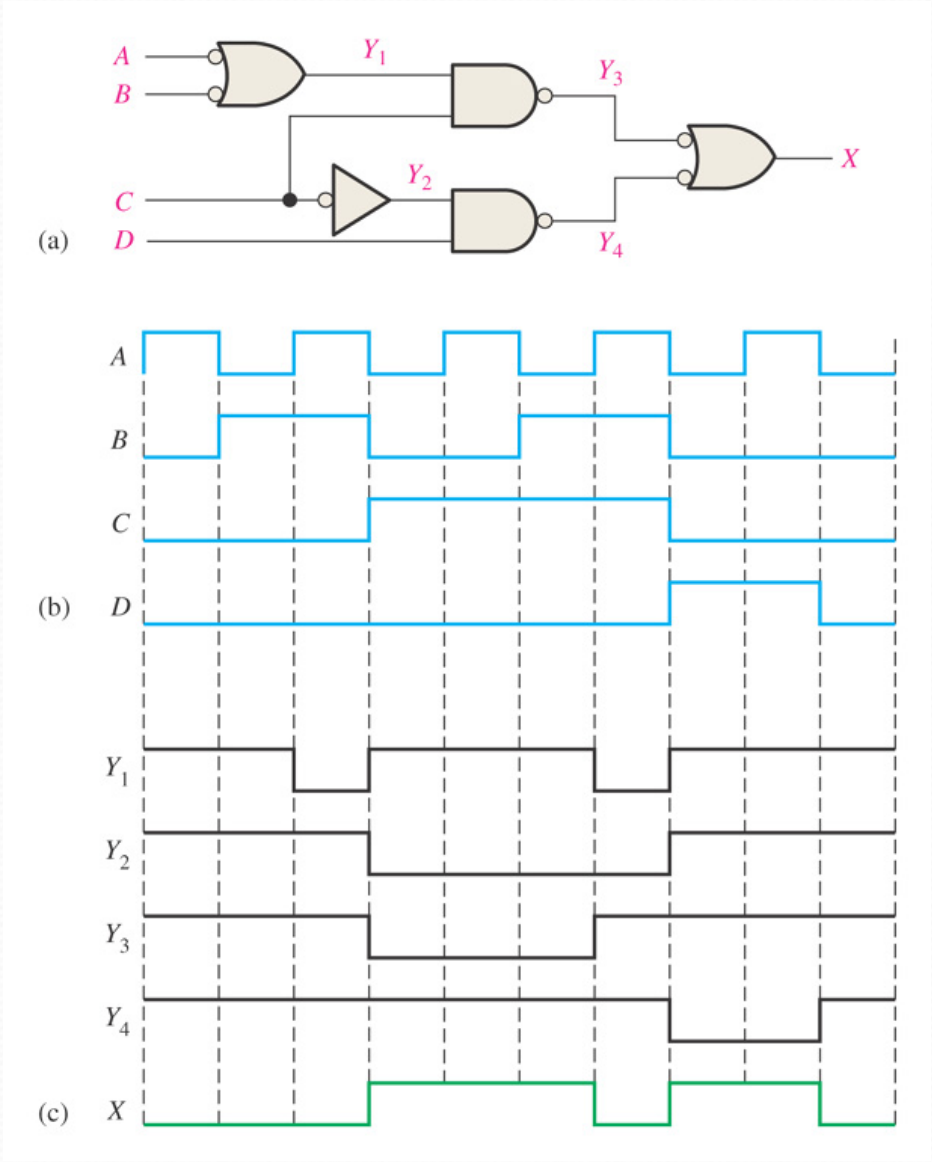
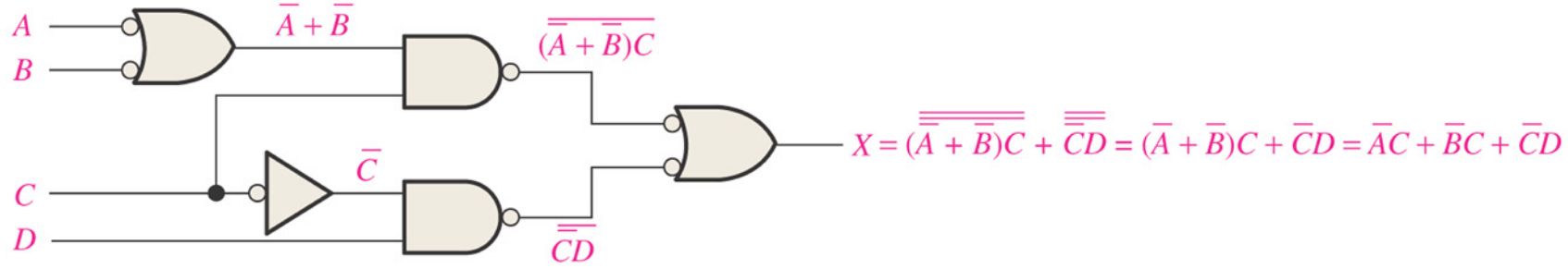
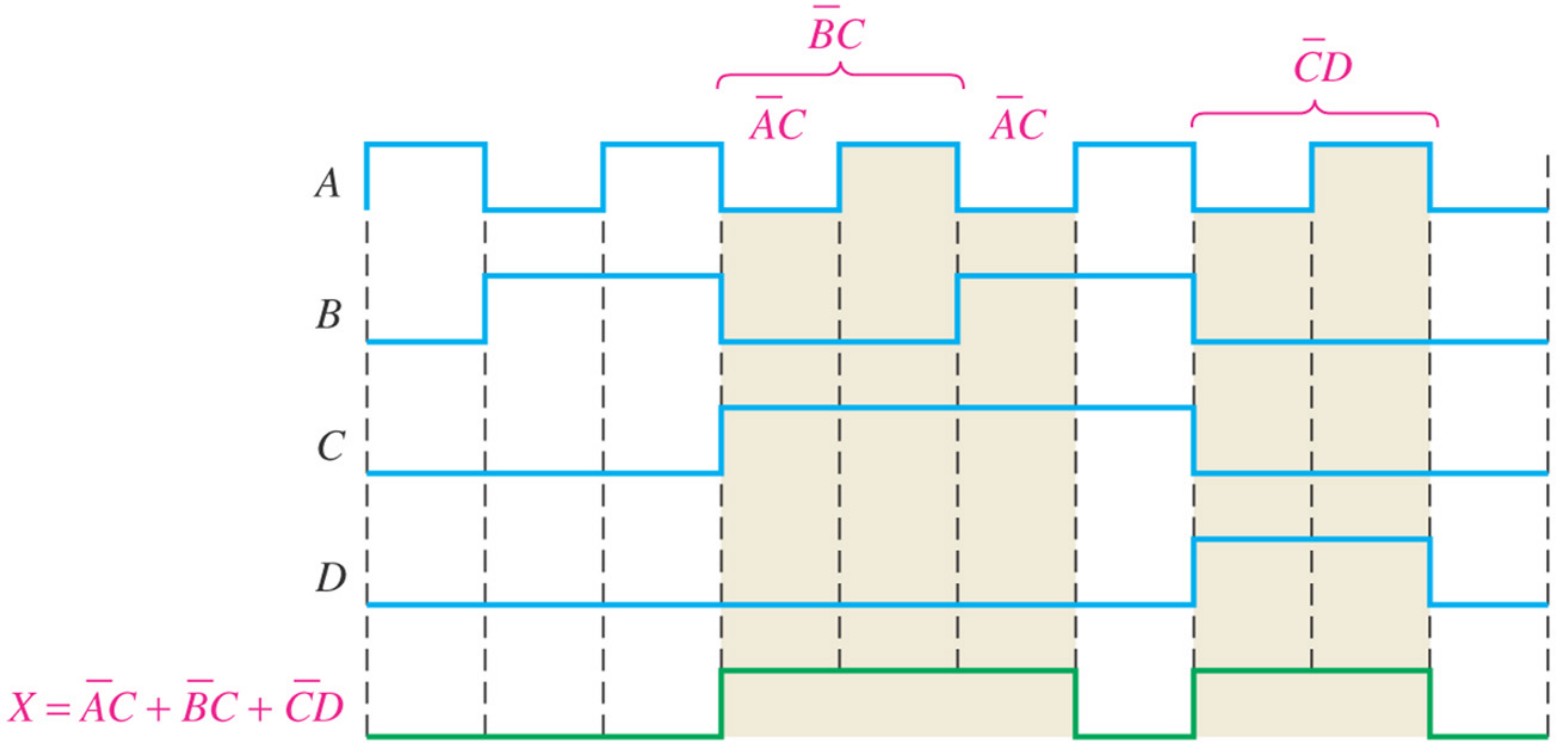


Example: **Determine the final output waveform X for the circuit in the following figure, with input waveforms A, B, and C as shown.**





Summary

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- Implementing Combinational Logic
  - From a Boolean expression to a Logic Circuit
  - From a Truth Table to a Logic Circuit
- The Universal Property of NAND and NOR Gates
- Logic Circuit Operation with Pulse Waveform Inputs
- How to design a combinational Logic?

HW

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