Chapter 11 Introduction to Digital Signal Processing

Outline

- Digital Signal Processing Basics
- Converting Analog Signals to Digital
- Analog-to-Digital Conversion Methods
- Digital-to-Analog Conversion Methods

11.1 Digital Signal Processing Basics

- Naturally occurred signals are usually analog
- Analog signals should be converted to digital form before being further processed
- Digital signals should be converted back to analog form sometimes

Figure 11–1 An original analog signal (sine wave) and its "stairstep" approximation.

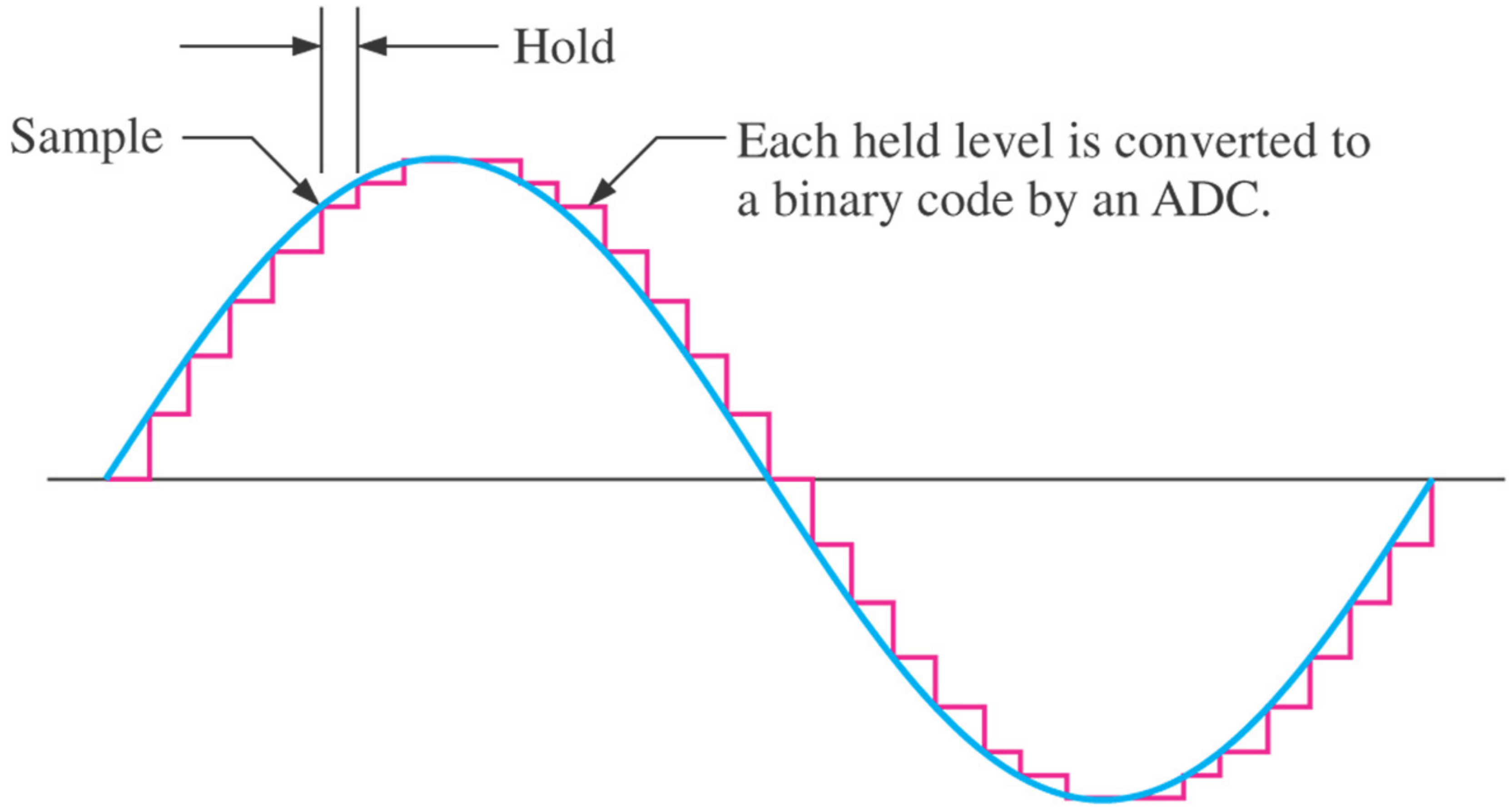
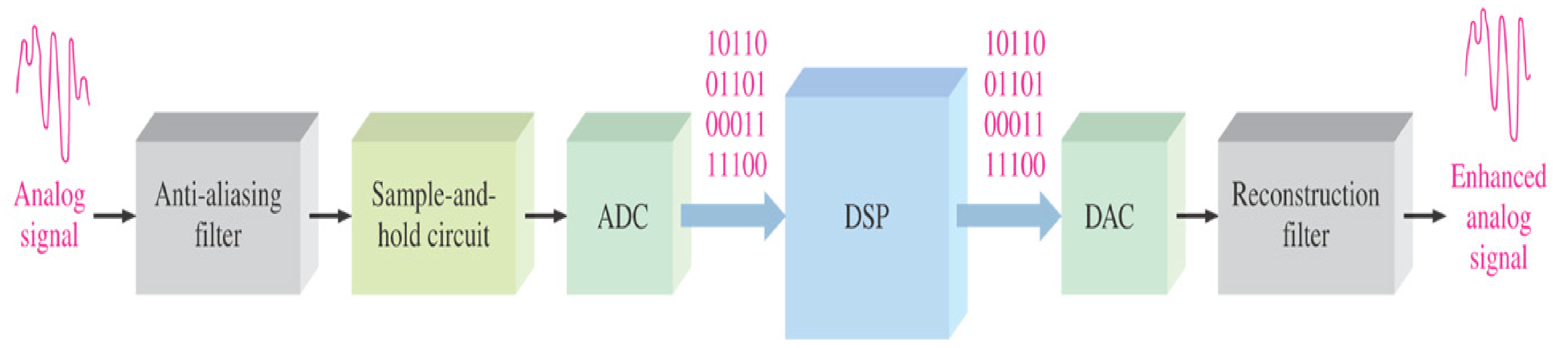


Figure 11–2 Basic block diagram of a typical digital signal processing system.



11.2 Converting analog signals to digital

- Sampling and filtering
- Holding the sampled value
- Analog-to-digital conversion

Sampling and Filtering

- Sampling
  - Take a sufficient number of discrete values at points on a waveform that defines the shape of waveform
  - Converts an analog signal into a series of impulses
- Filtering
  - Sampling theorem
    - The sampling frequency must be at least twice the highest frequency component of the analog signal
  - Nyquist frequency

Figure 13–3 Illustration of the sampling process.

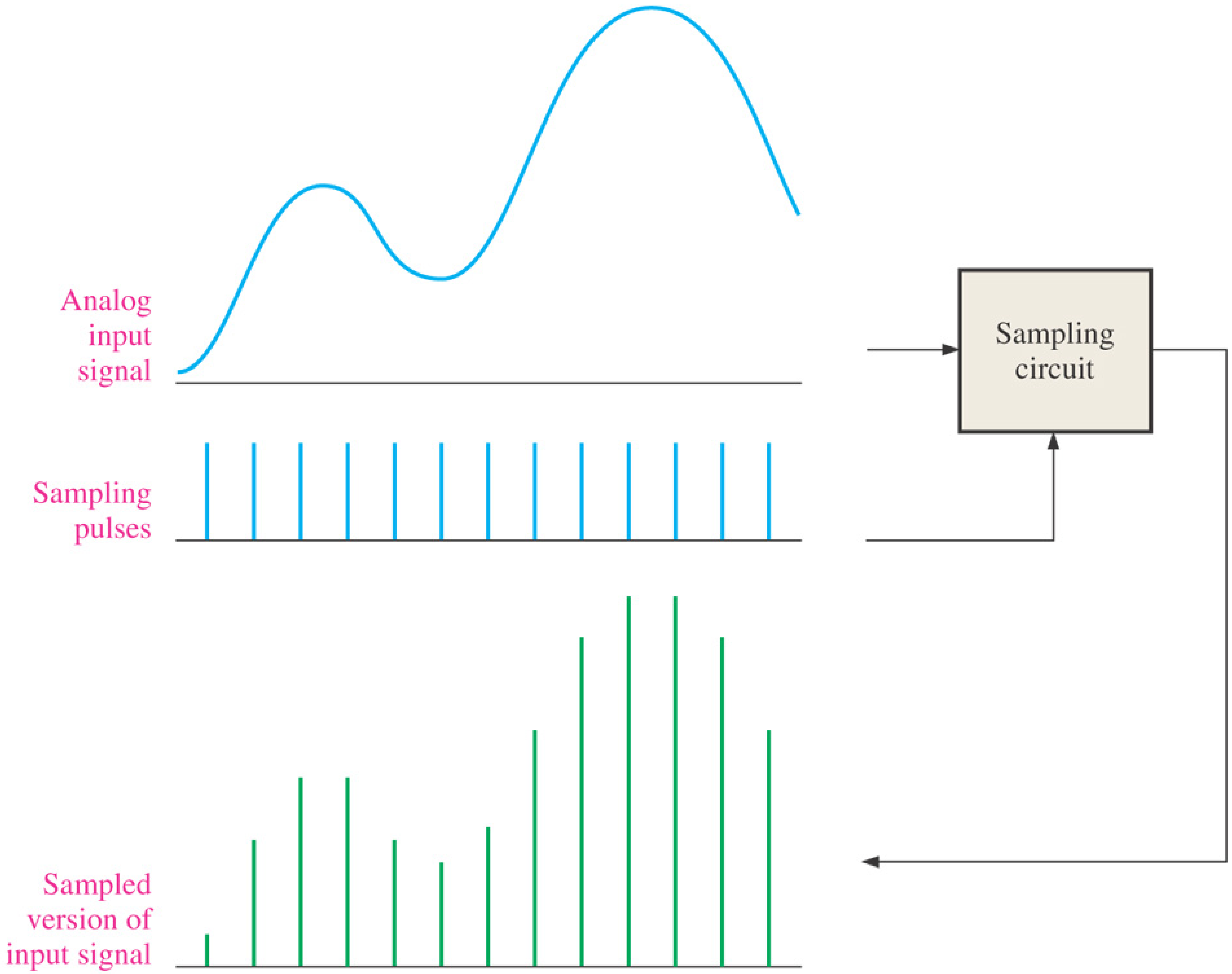
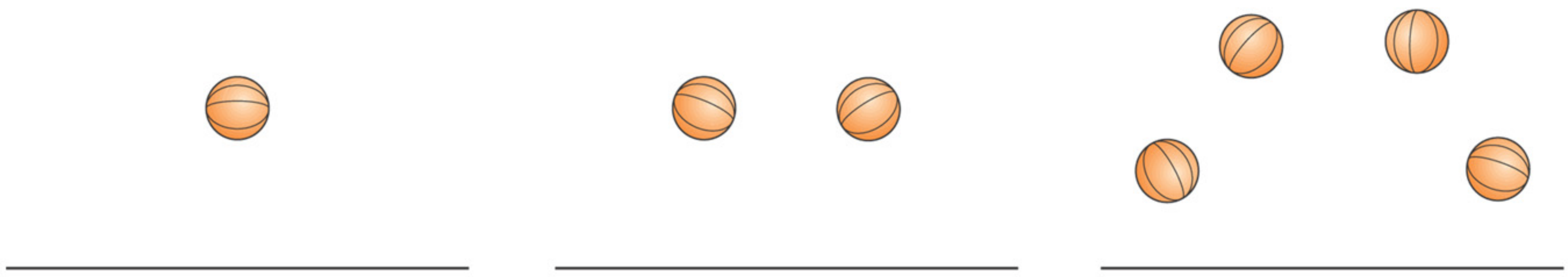


Figure 13–4 Bouncing ball analogy of sampling theory.



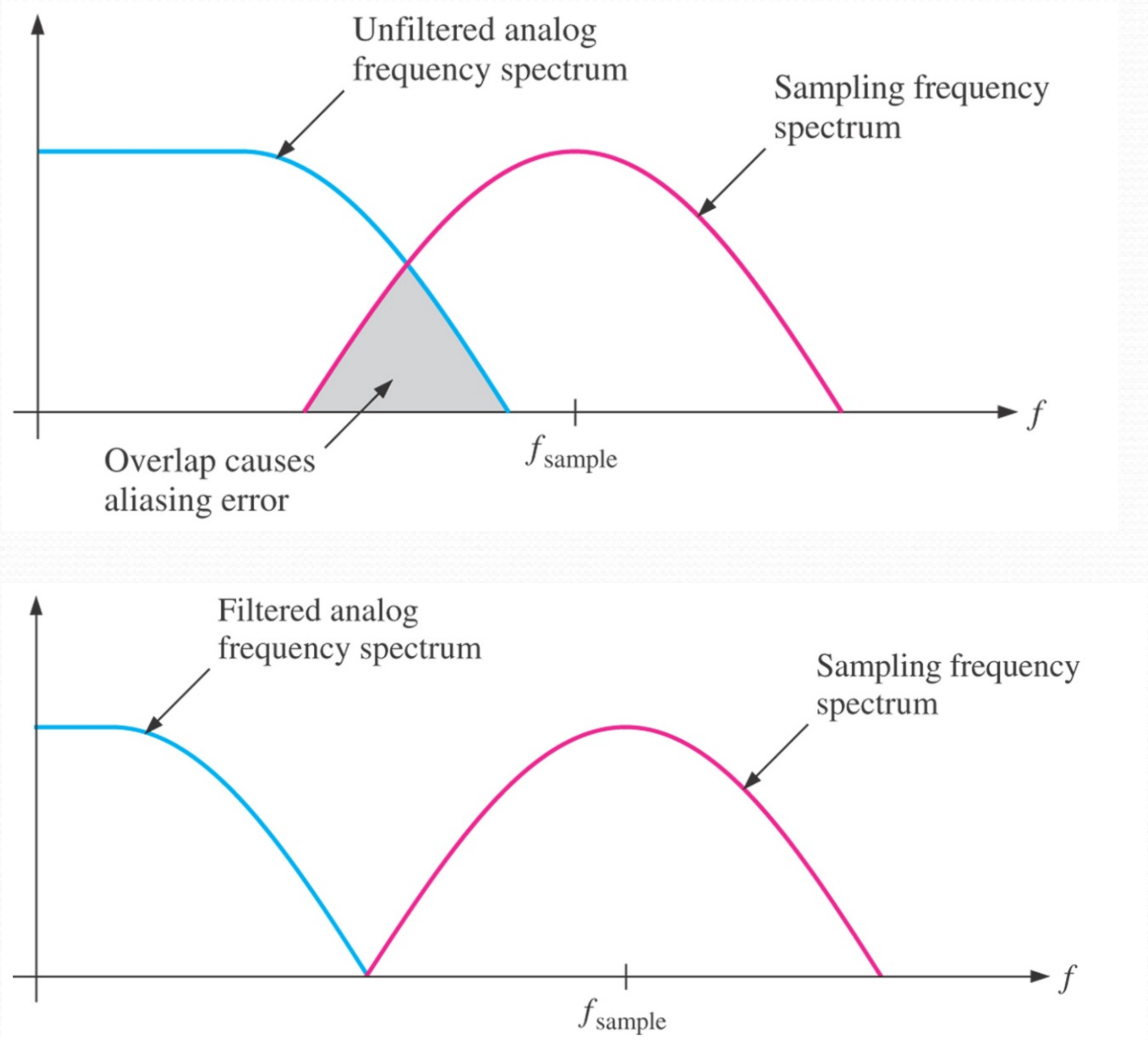
(a) One sample of a ball during a single bounce

(b) Two samples of a ball during a single bounce. This is the absolute minimum required to tell anything about its movement, but generally insufficient to describe its path.

(c) Four samples of a ball during a single bounce form a rough picture of the path of the ball.

How many photos need to be taken to keep the path of the ball?

Figure 11–6 After low-pass filtering, the frequency spectra of the analog and the sampling signals do not overlap, thus eliminating aliasing error.



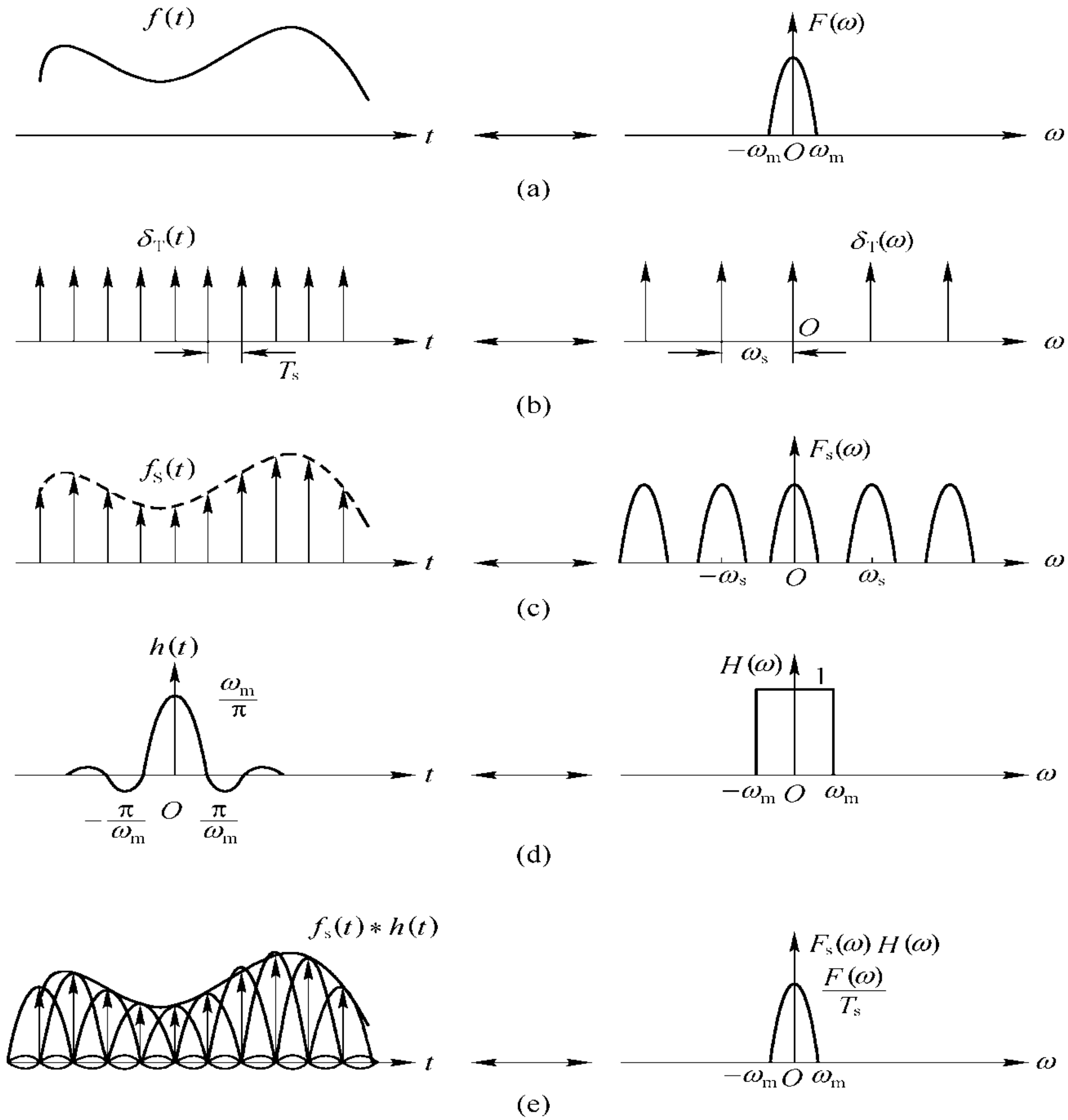


Fig. The sampling and restoring of a Low-pass signal

Holding the Sampled Value

- The sampled level must be held constant until the next sample occur.
- It is necessary for ADC to have time to process the sampled value.

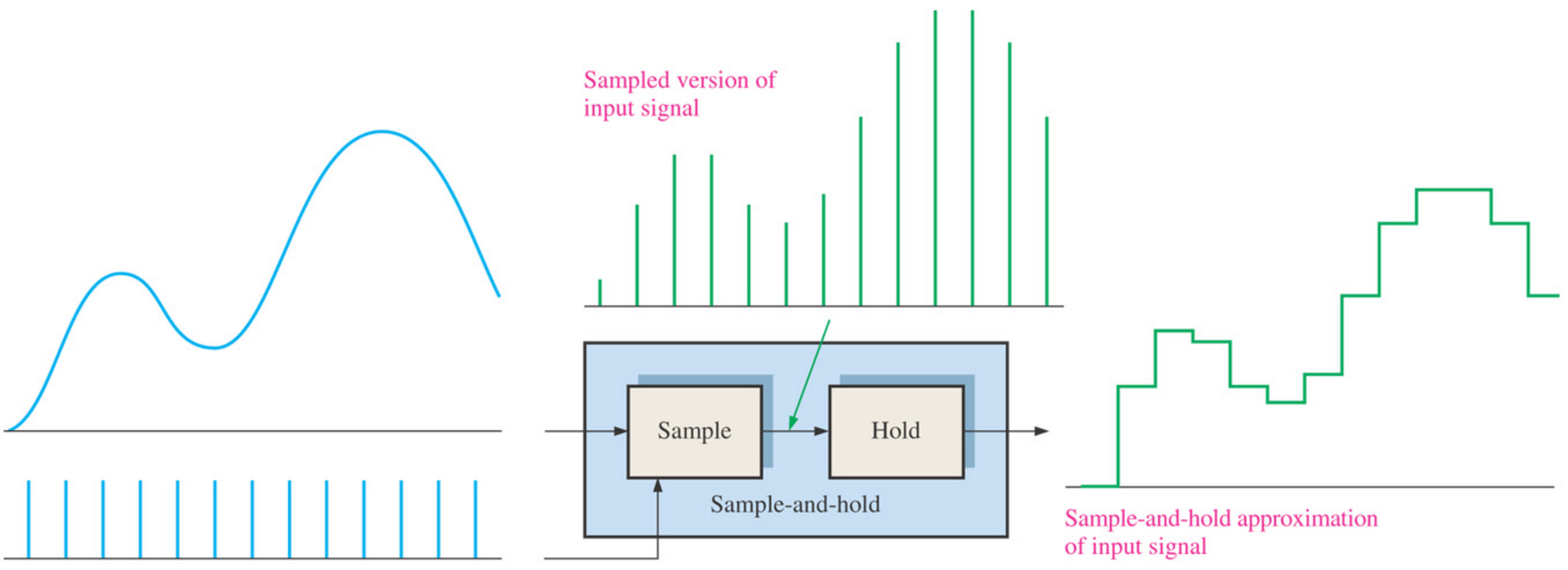


Figure 11–7 Illustration of a sample-and-hold operation.

Analog-to-Digital Conversion

- Convert the output of the sample-and-hold circuit to a series of binary codes.
- ADC must complete the conversion between sample pulses (within the conversion interval).

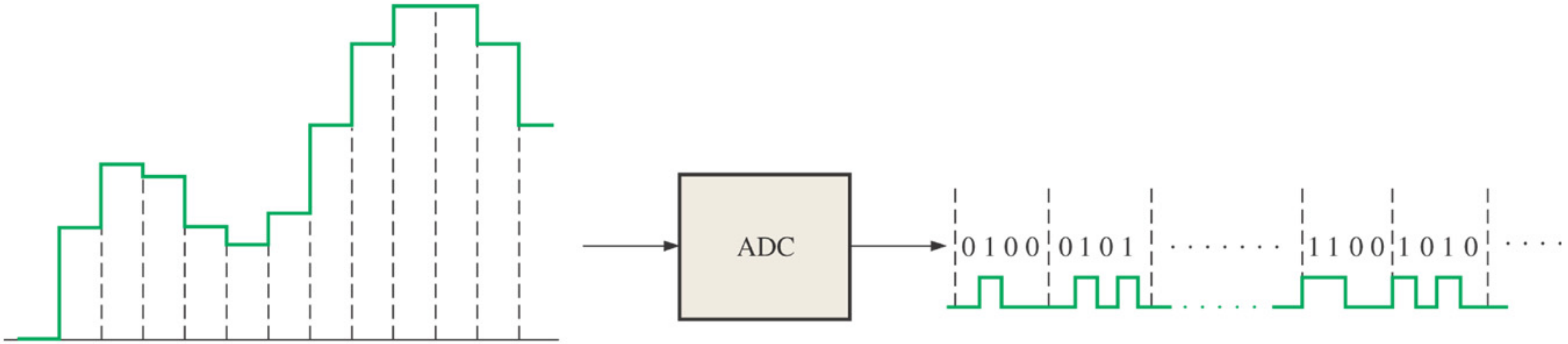


Figure 11–8 Basic function of an analog-to-digital (ADC) converter (The binary codes and number of bits are arbitrarily chosen for illustration only). The ADC output waveform that represents the binary codes is also shown.

Figure 11–9 Sample-and-hold output waveform with four quantization levels. The original analog waveform is shown in light gray for reference.

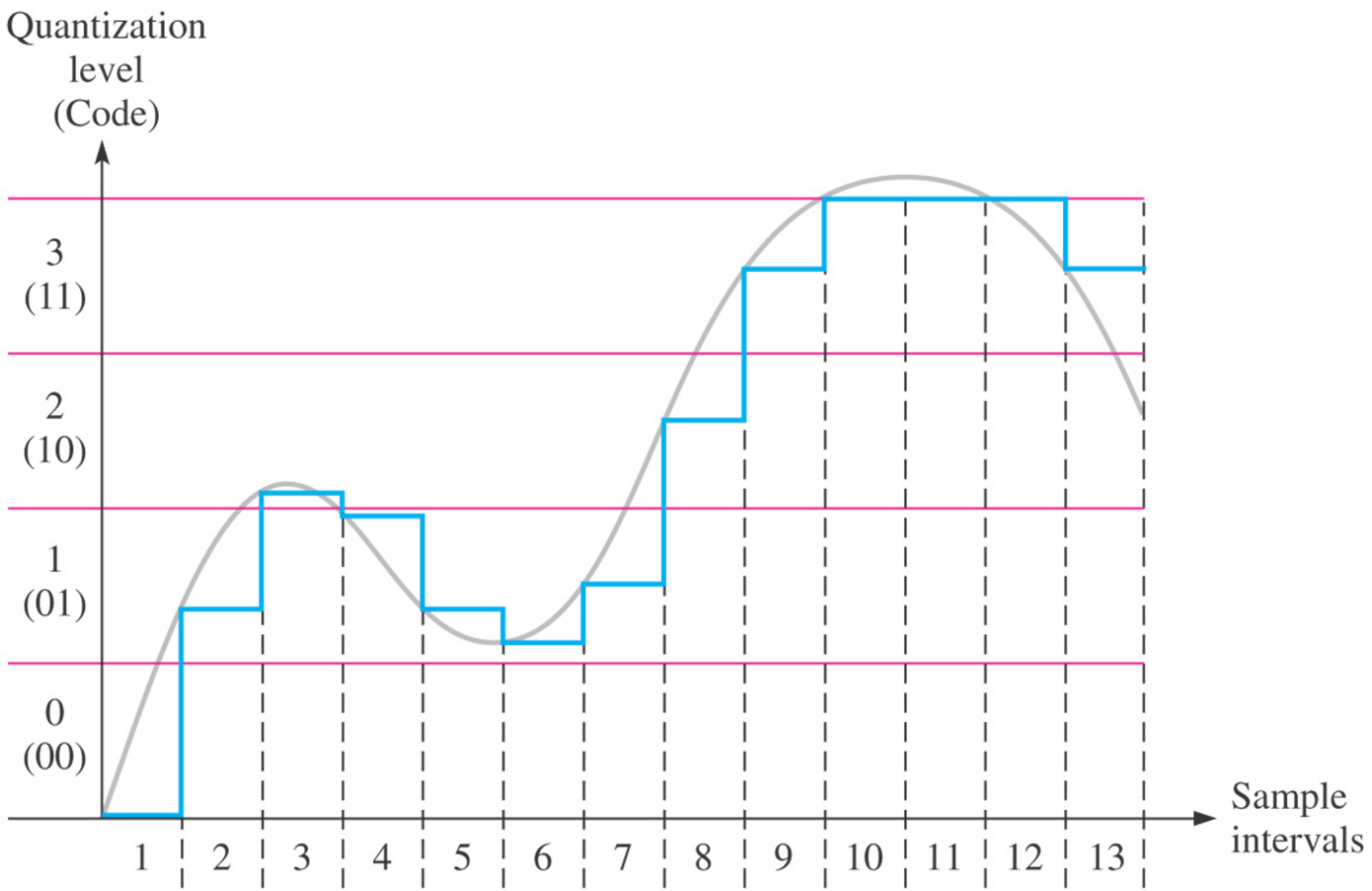


Figure 11–10 The reconstructed waveform in Figure 11–9 using four quantization levels (2 bits). The original analog waveform is shown in light gray for reference.

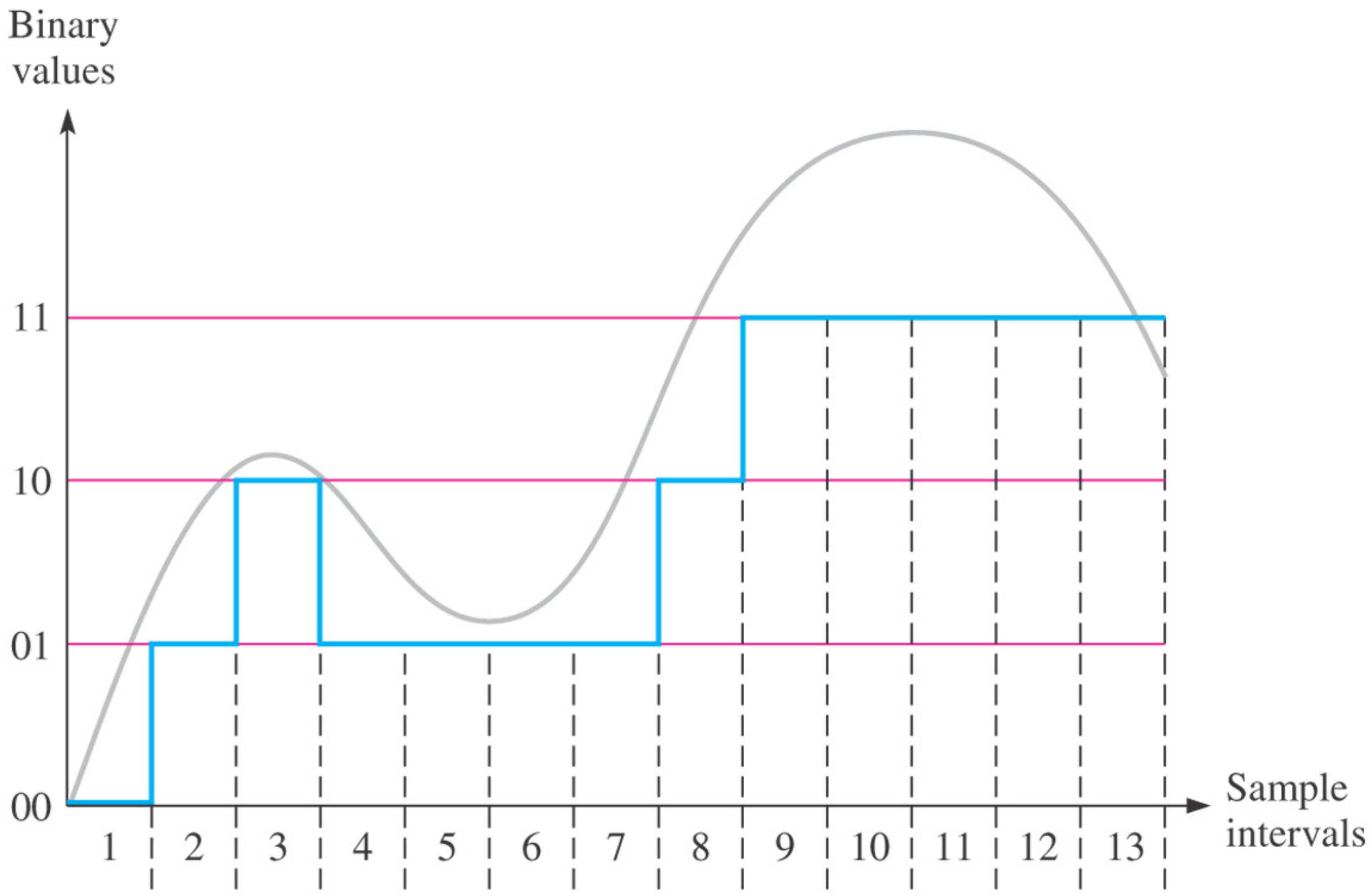


Figure 11–11 Sample-and-hold output waveform with four quantization levels. The original analog waveform is shown in light gray for reference.

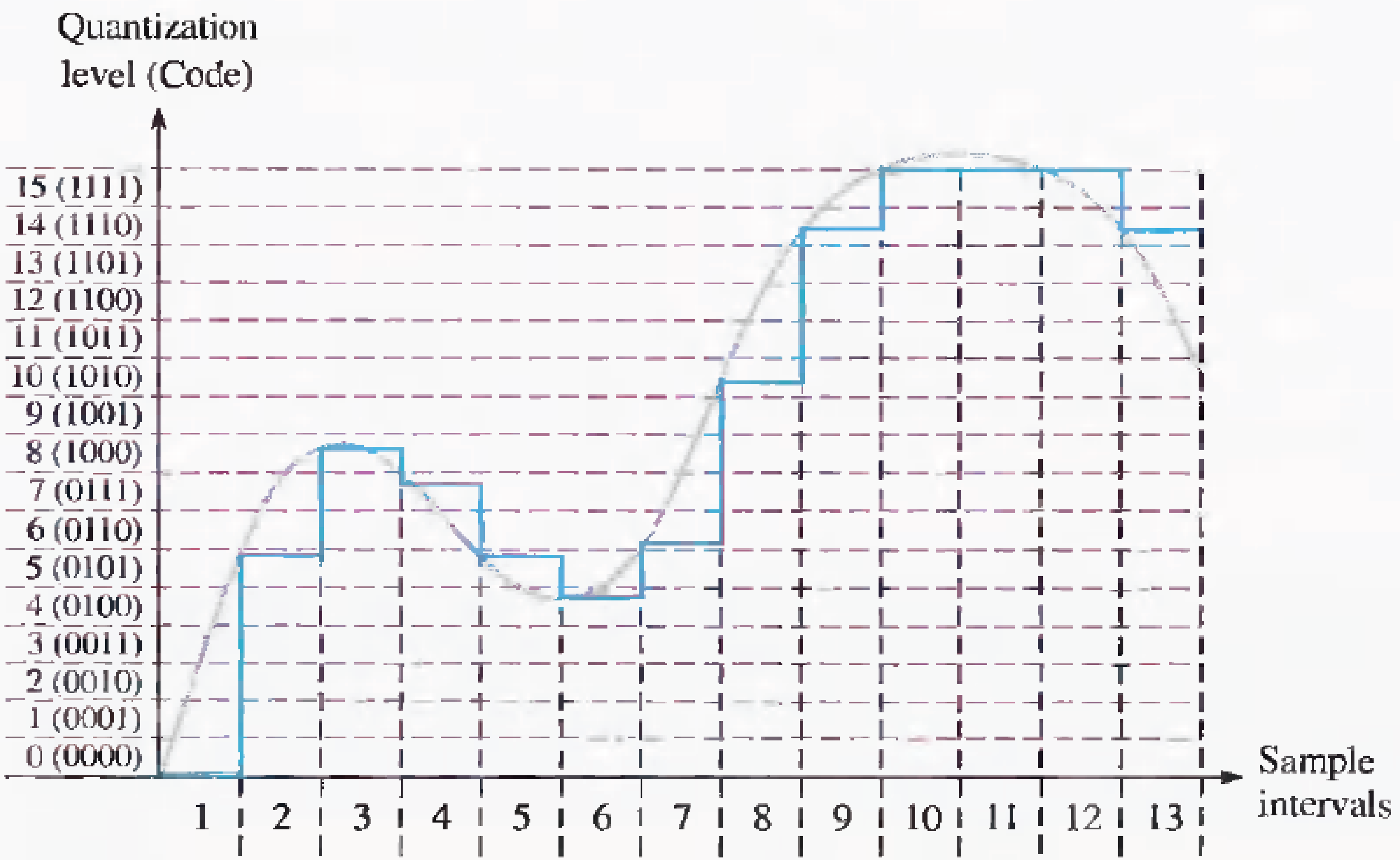
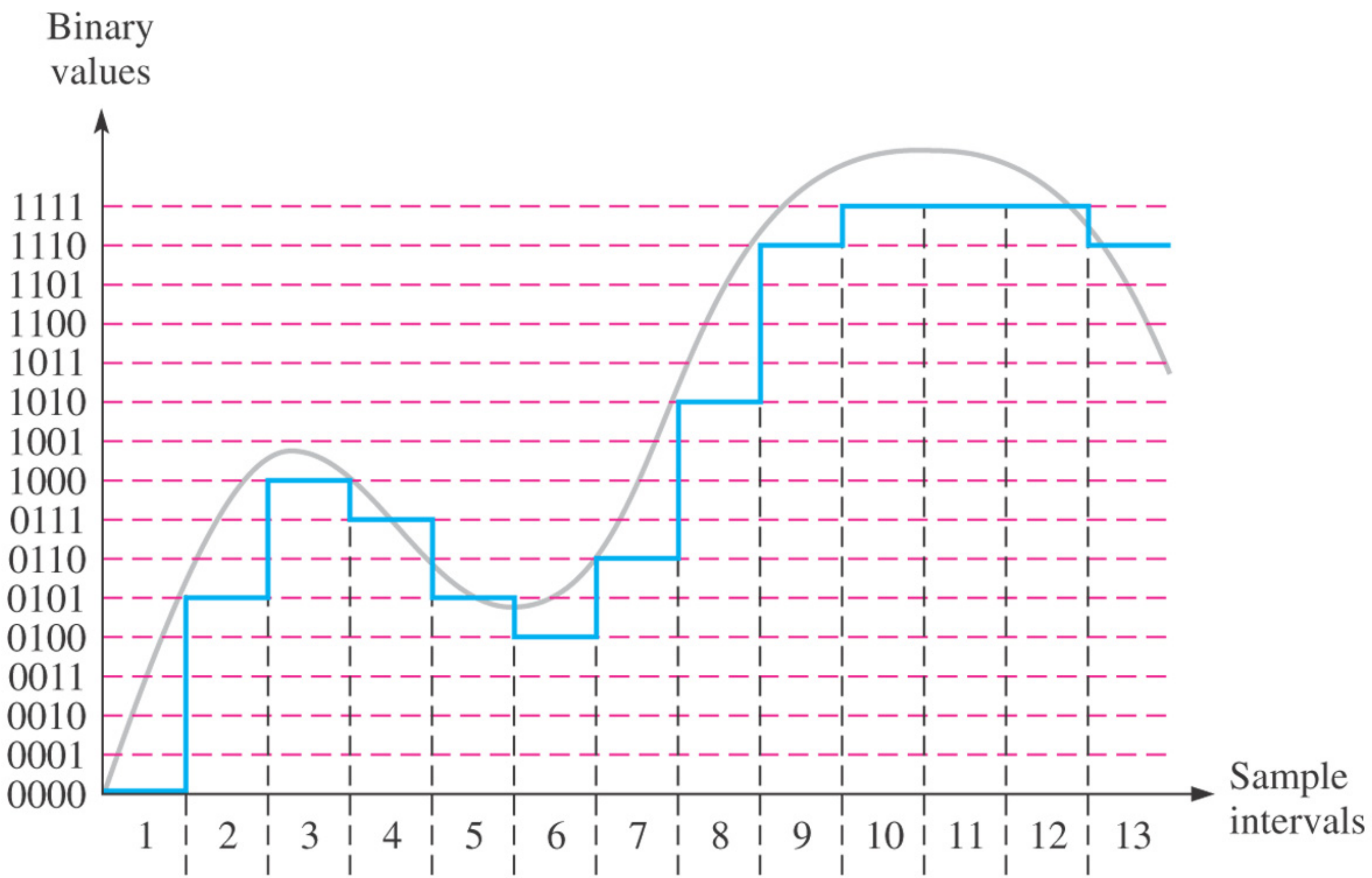


Figure 11–12 The reconstructed waveform in Figure 11–11 using sixteen quantization levels (4 bits). The original analog waveform is shown in light gray for reference.



As a summary for the procedure of A/D conversion

- Sampling
- Holding
- Quantization
- Coding

11.3 Analog-to-digital conversion methods

- Operational Amplifier
- A/D conversion methods
- ADC parameters
  - resolution – the number of bits
  - Throughput – the sampling rate an ADC can handle in units of samples per second (sps)

Operational Amplifier

- Virtual ground
- Working as a comparator
    - The op-amp is driven into one of its two saturated output states, either HIGH of LOW, depending on which input voltage is greater

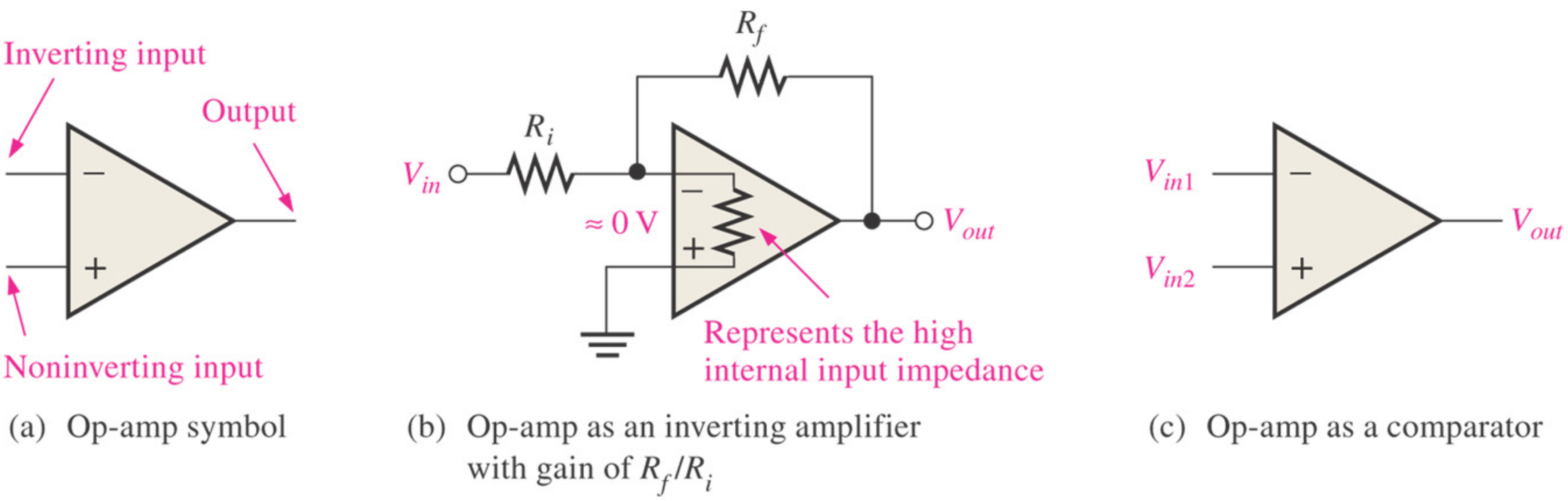


Figure 11–13 The operational amplifier (op-amp).

Figure 11–14 A 3-bit flash ADC.

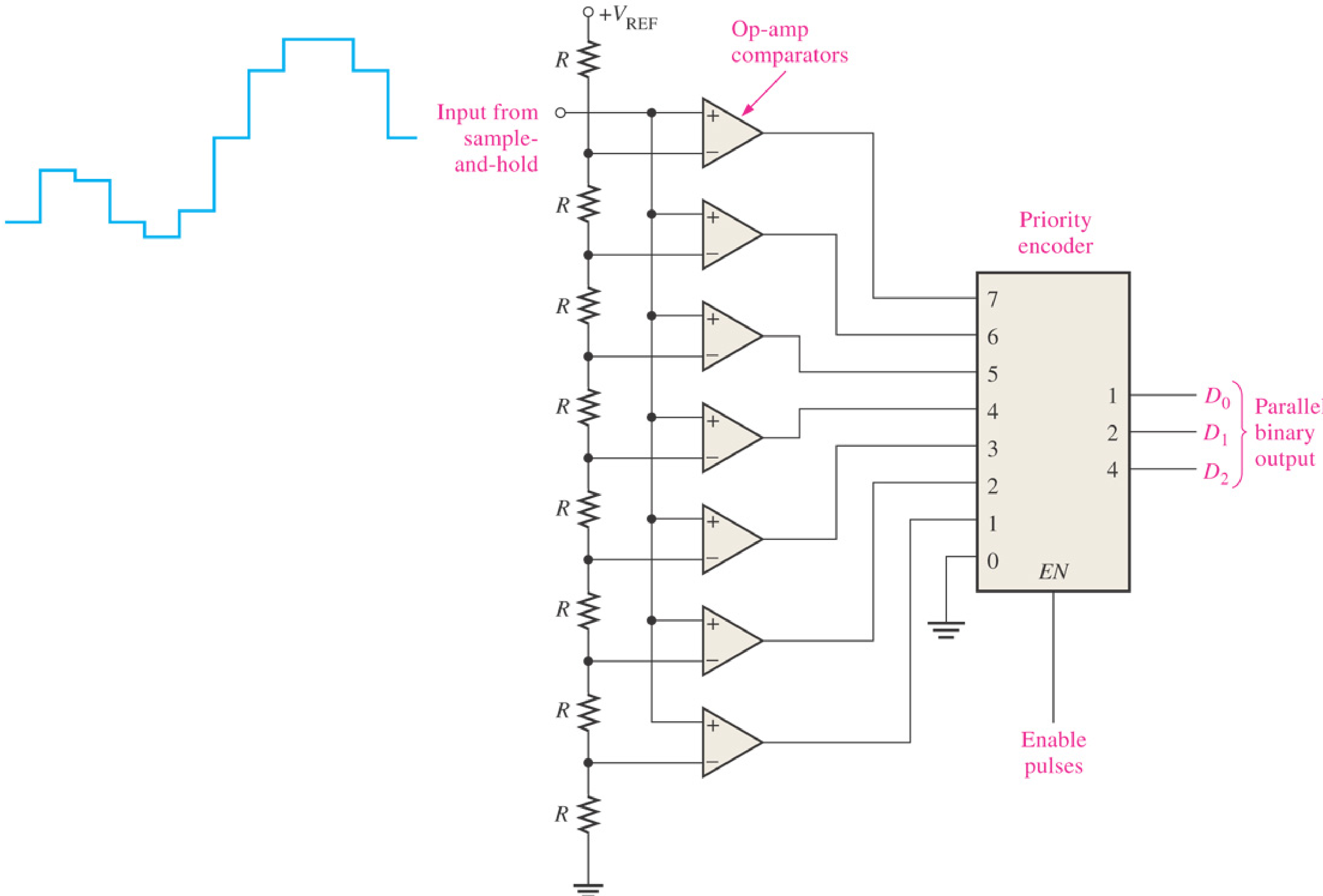
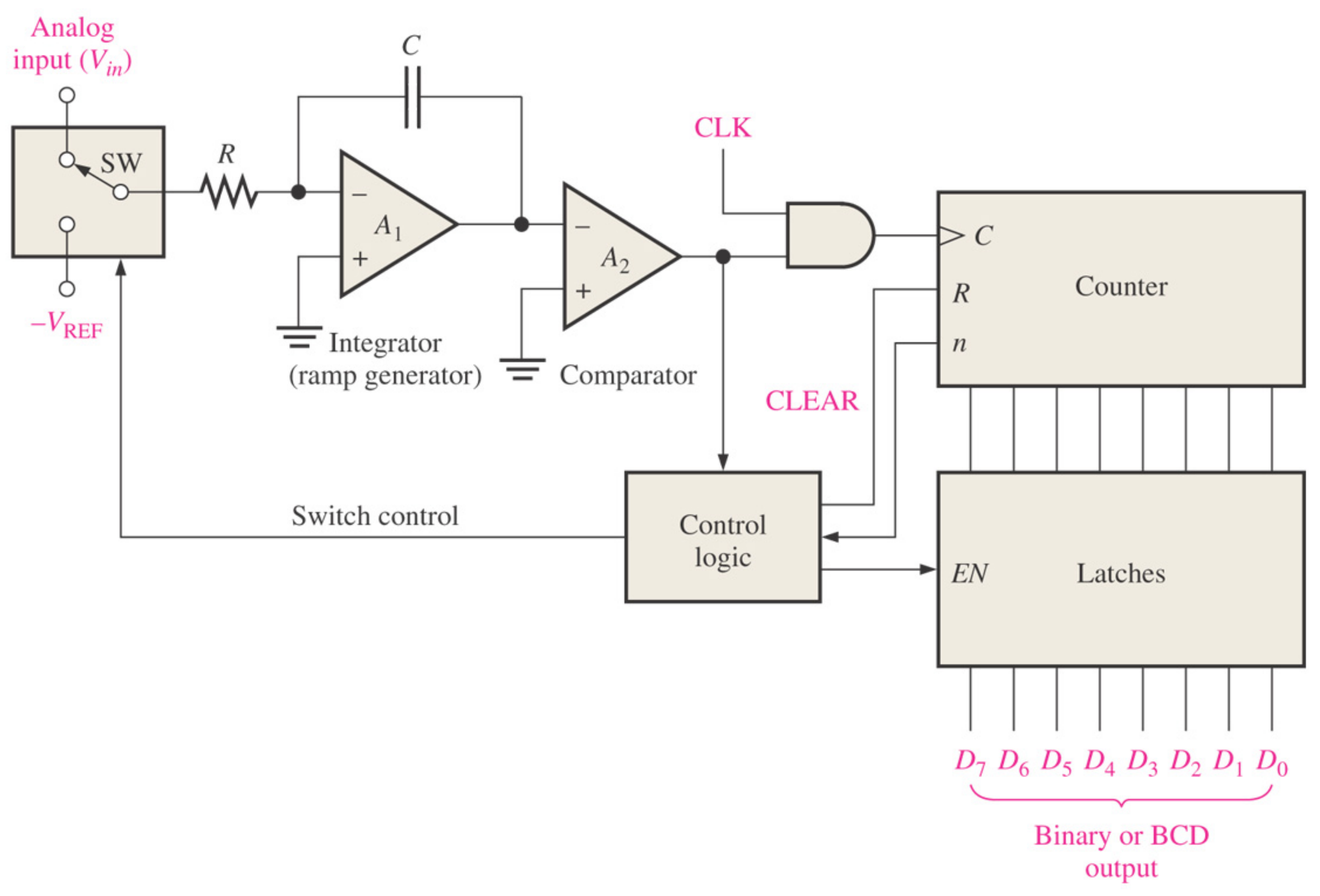
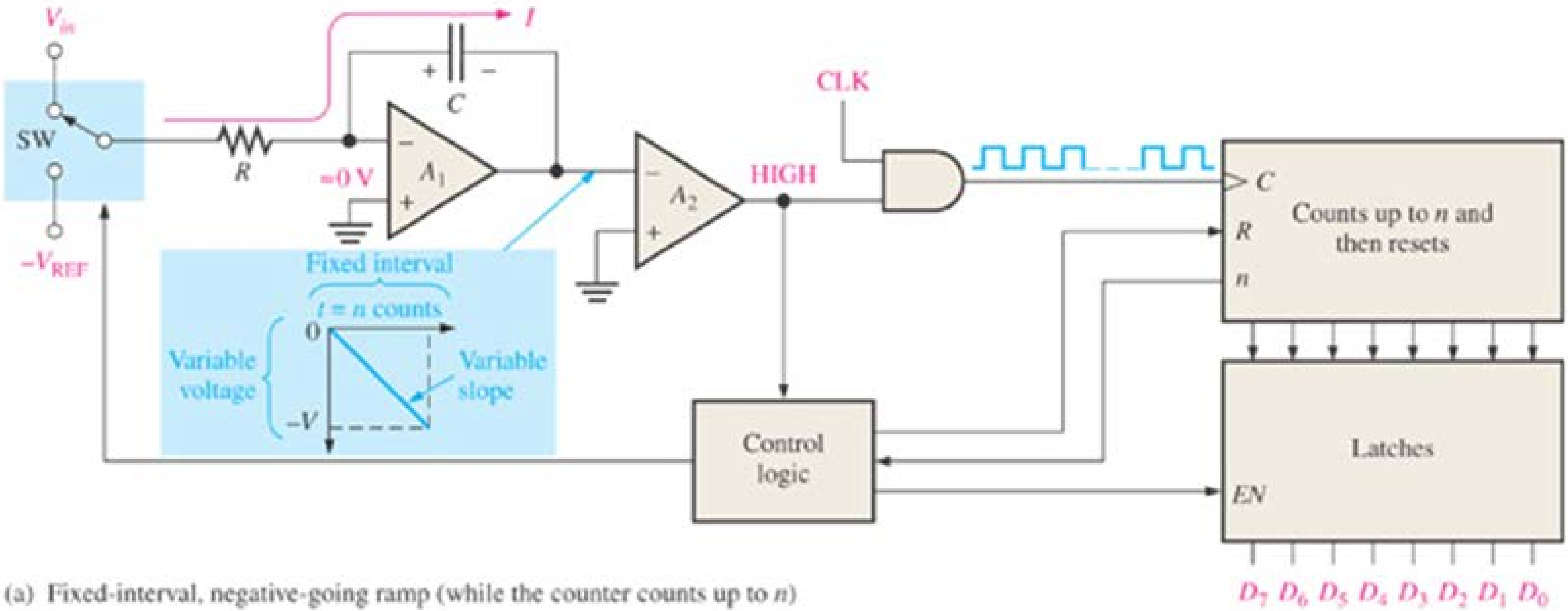
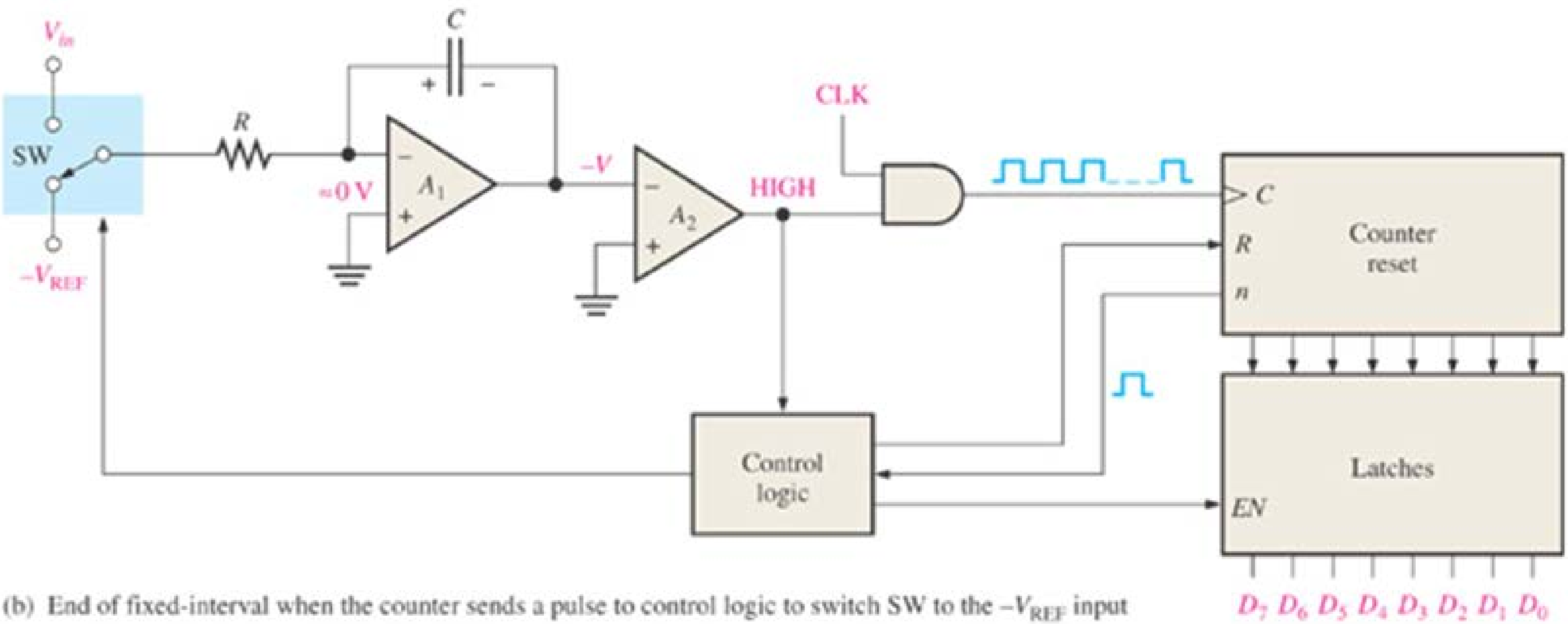


Figure 13–17 Basic dual-slope ADC.

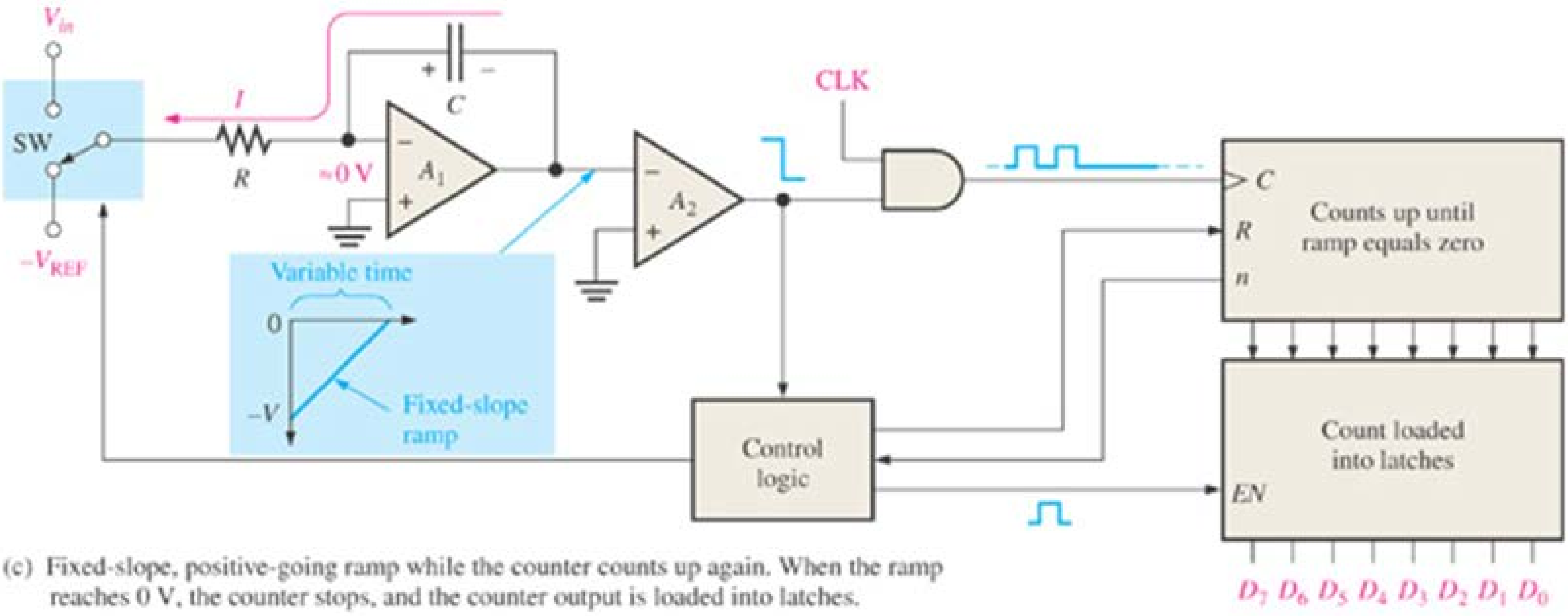




(a) Fixed-interval, negative-going ramp (while the counter counts up to n)



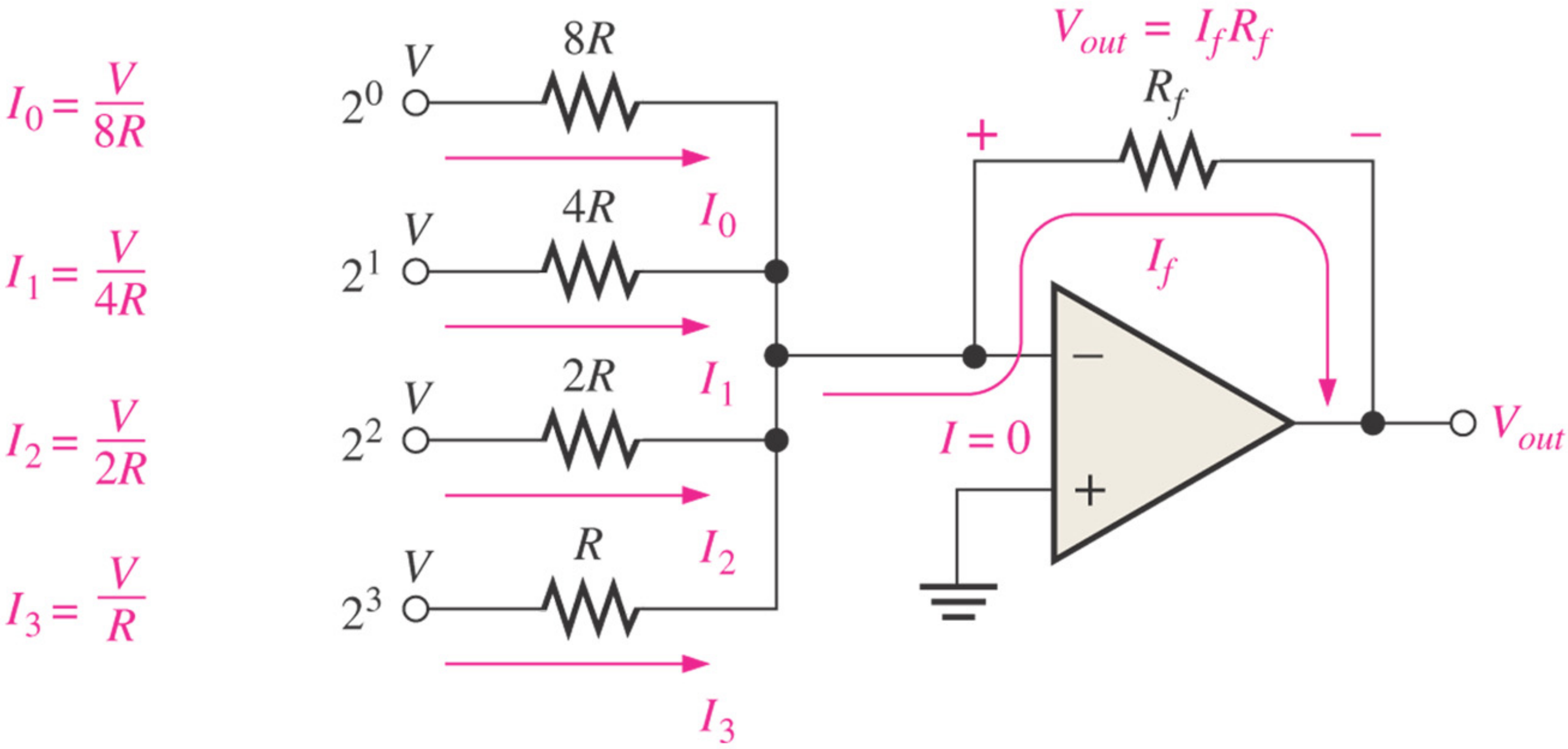
(b) End of fixed-interval when the counter sends a pulse to control logic to switch SW to the $-V_{REF}$ input



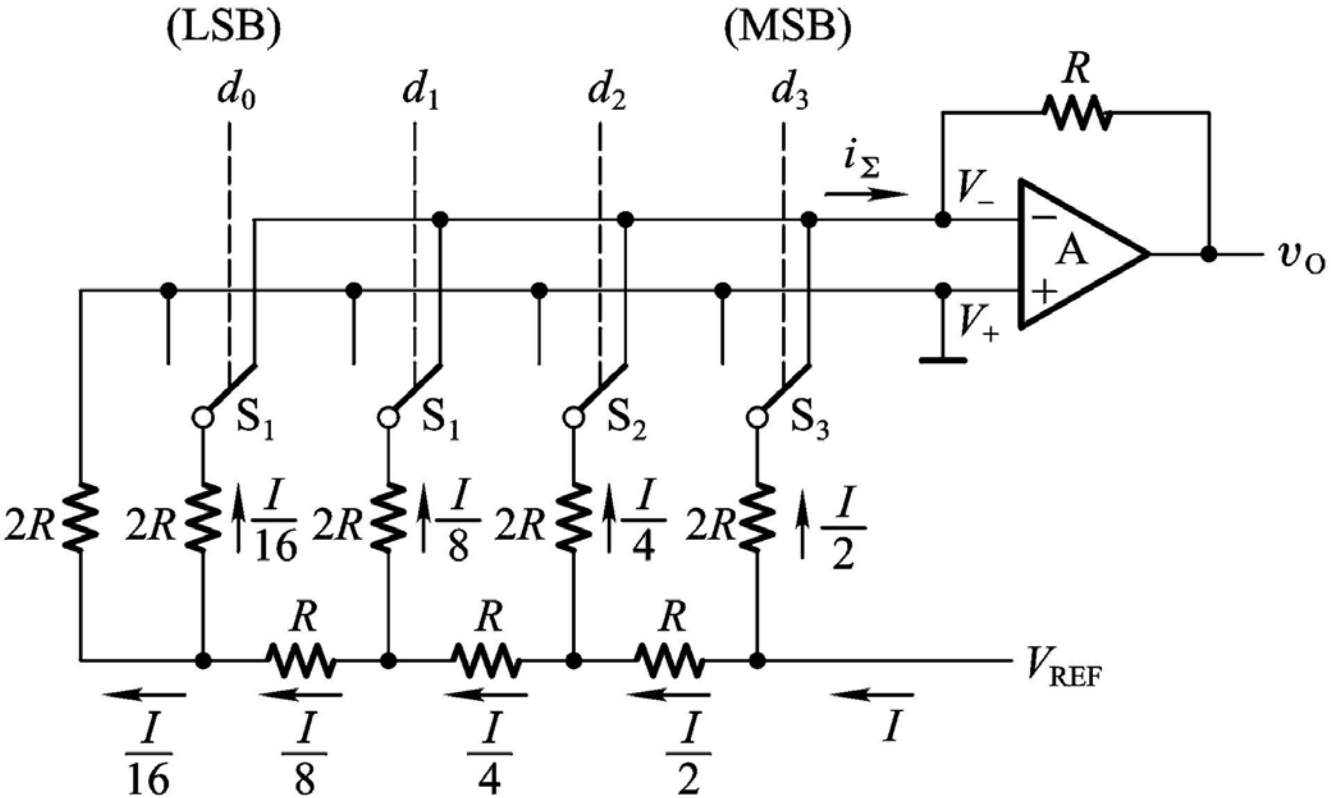
(c) Fixed-slope, positive-going ramp while the counter counts up again. When the ramp reaches 0 V, the counter stops, and the counter output is loaded into latches.

11.4 Digital-to-analog conversion methods

Figure 11–36 A 4-bit DAC with binary-weighted inputs.



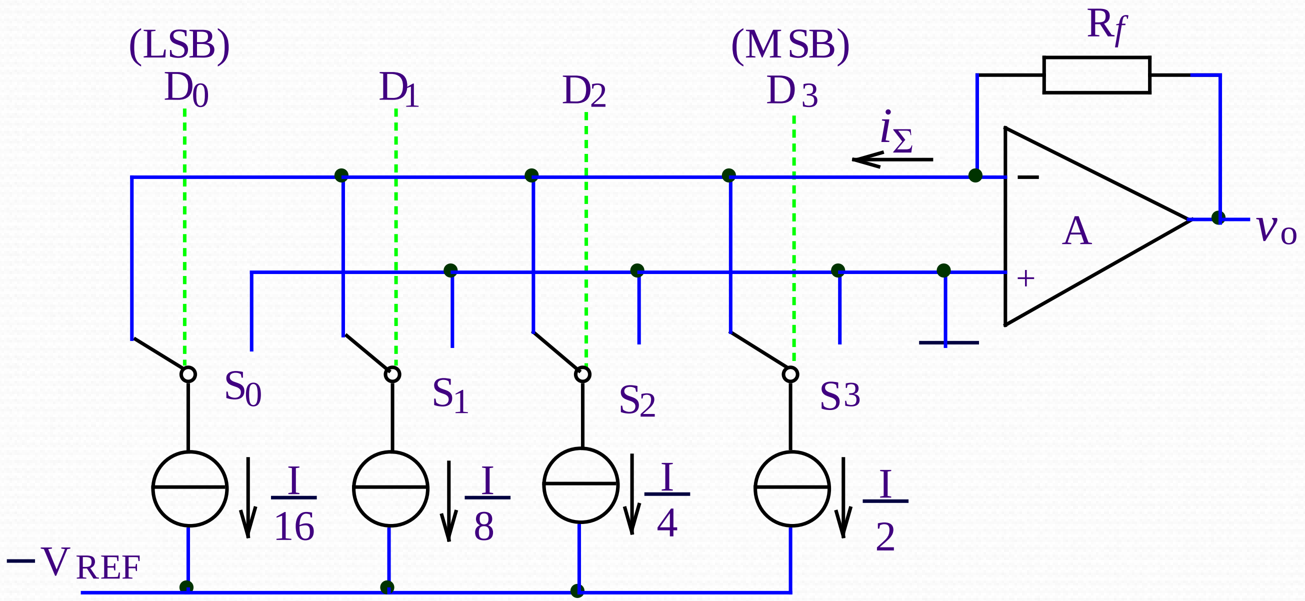
Some other DACs



11-2-3

$$i_\Sigma = \frac{V_{REF}}{R}\left(\frac{D_0}{2^4} + \frac{D_1}{2^3} + \frac{D_2}{2^2} + \frac{D_3}{2^1}\right) = \frac{V_{REF}}{2^4 \times R}\sum_{i=0}^{3}(D_i \cdot 2^i)$$

$$v_O = -i_\Sigma R_f = -\frac{R_f}{R} \cdot \frac{V_{REF}}{2^4}\sum_{i=0}^{3}(D_i \cdot 2^i)$$



$$v_O = i_\Sigma R_f = R_f\left(\frac{I}{2}D_3 + \frac{I}{4}D_2 + \frac{I}{8}D_1 + \frac{I}{16}D_0\right)$$

$$= \frac{I}{2^4}\cdot R_f\left(D_3\cdot 2^3 + D_2\cdot 2^2 + D_1\cdot 2^1 + D_0\cdot 2^0\right)$$

$$= \frac{I}{2^4}\cdot R_f\sum_{i=0}^{3} D_i\cdot 2^i$$

Summary

- Digital Signal Processing Basics
- Sampling and reconstruction
- AD and ADC
  - Sampling, holding, quantization, coding
- DA and DAC

Homework

- P488
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