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## THE EVOLUTION OF x86: FROM 32-BIT TO 64-BIT

The x86 PC

assembly language, design, and interfacing

fifth edition

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Prentice Hall

# OBJECTIVES

this chapter enables the student to:

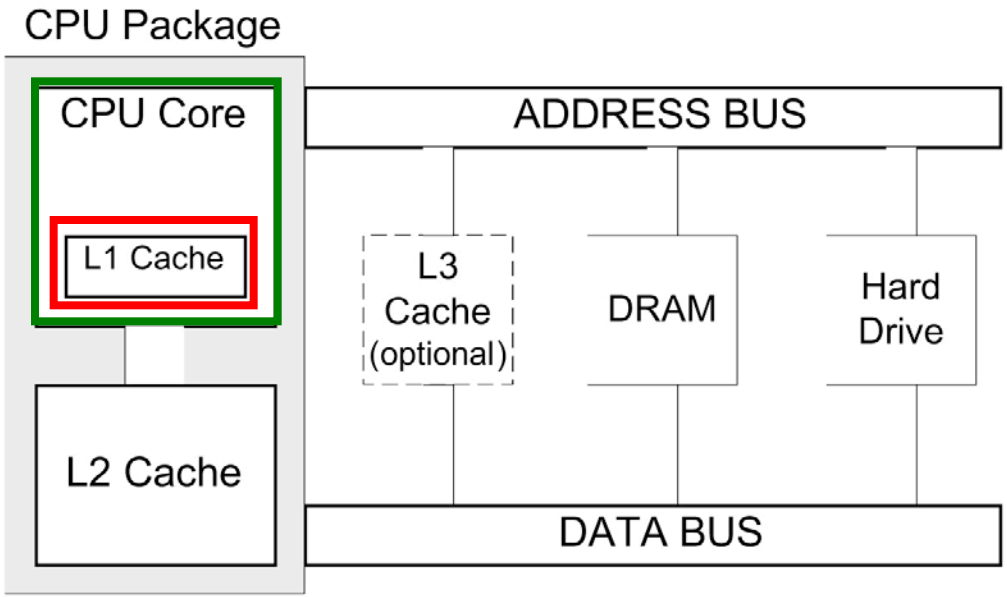
- Compare and contrast the variations of Pentium® processors.
- Compare and contrast the variations of x86 32-bit architecture.
- Describe the enhancements of 32-bit architecture in x86 processors.
- Describe the role of L1–L3 caches in x86 processors.
- Describe the role of multicore and multithreading features of x86.
- Describe 64-bit architecture of x86.

# 24.1: x86 PENTIUM® EVOLUTION
## Pentium® II to Pentium® IV: an overview

- x86 microprocessor architecture has gone through major changes since the introduction of the first Pentium® processor in 1993.
  - To increase processing power Intel added enhancements to each successive generation of Pentium® II, III, and IV.
    - Most involved internal architecture and did not change the 32-bit register size of the original 386.

# 24.1: x86 PENTIUM® EVOLUTION
## level 1 and level 2 caches

- Pentium® Pro had 8K of cache for code (instruction) & 8K for data, feeding code & data to the fetch unit.
  - Called **level 1** (**L1**) cache, it is on the **same die** as the CPU & works at the same clock speed.

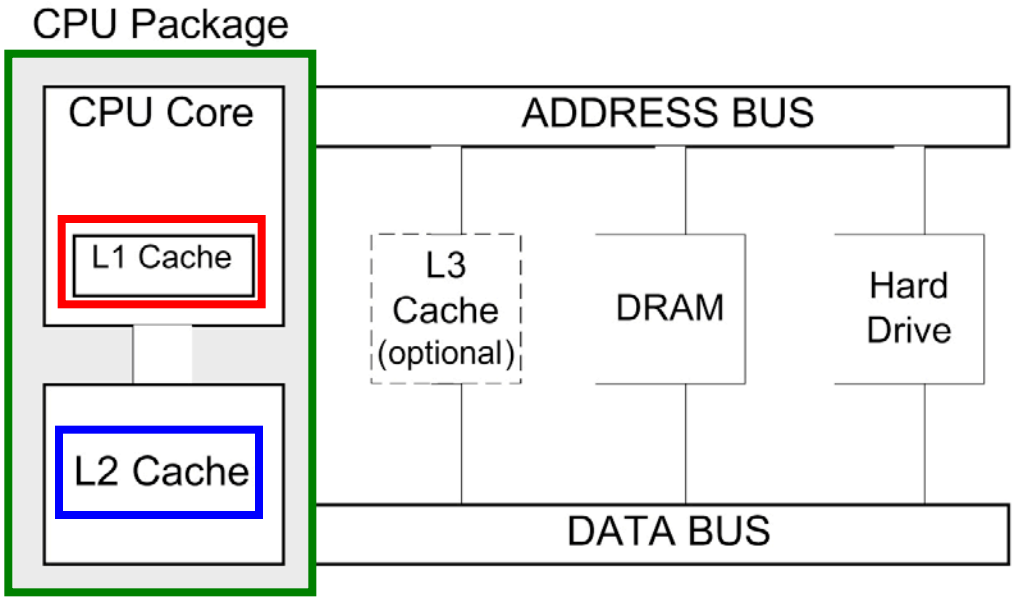



**L1** cache feeds code & data to the fetch/execution units and is part of the inner working of the CPU

**Fig. 24-1 L1**, L2 and L3 Cache

# 24.1: x86 PENTIUM® EVOLUTION
## level 1 and level 2 caches

- In Pentium® II, **level 2** (**L2**) cache was introduced.
  - **L1** cache was increased to 16K each for code & data.
  - 256K bytes of **L2** cache was added.




**L 2** cache is outside the CPU die, but still on the **same package** as the CPU itself.

**Fig. 24-1** L1, **L2** and L3 Cache

# 24.1: x86 PENTIUM® EVOLUTION
## level 1 and level 2 caches

- When a Pentium® with **L2** cache brings in code & data from external DRAM it places them in **L2** cache.
- The memory management unit of the CPU brings in the information from **L2** cache, separating code & data, placing each in **data** or **code** **L1** caches. (*Harvard architecture*)

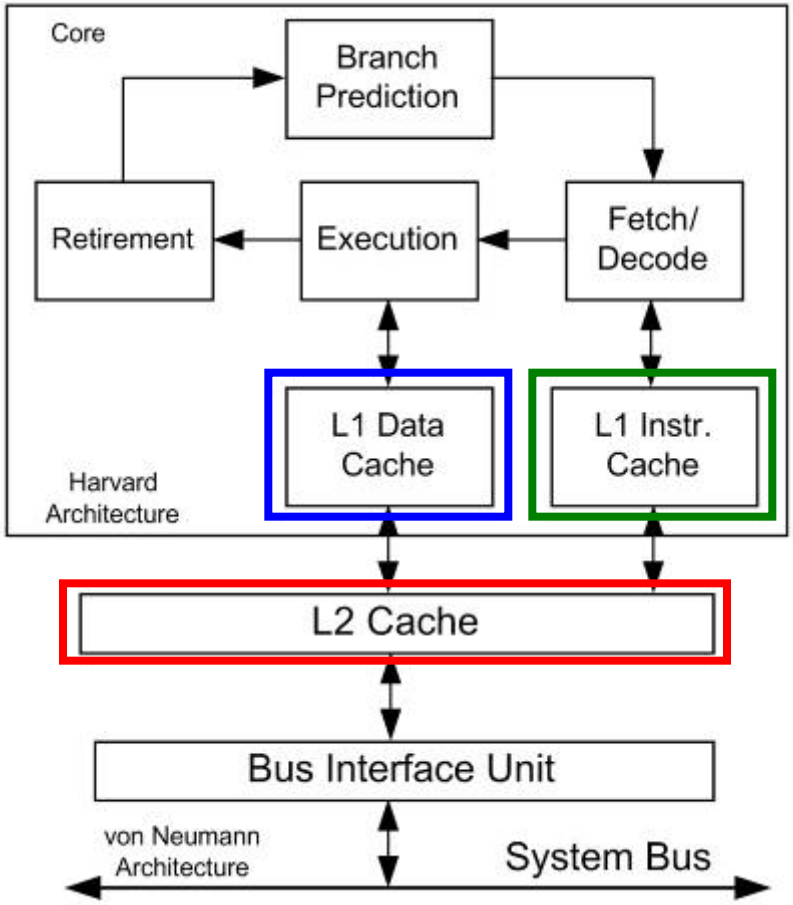



**Fig. 24-2**
Cache Feeding Code and Data to L1 Caches

# 24.1: x86 PENTIUM® EVOLUTION
## level 1 and level 2 caches

- L1 code & data caches are separate, as opposed to L2 cache, which is a unified cache.
  - Used for both code and data.
- The L2 amount allocated to data & code varies dynamically, depending on the program being run.
  - If the program being run is more data intensive, then more of the L2 cache is allocated to data.

# 24.1: x86 PENTIUM® EVOLUTION
## level 3 cache – multicore

- In some high-performance systems designers place **level 3** (**L3**) cache on the motherboard, outside the CPU, to speed up the external memory access
  - Between the **CPU** & **DRAM**

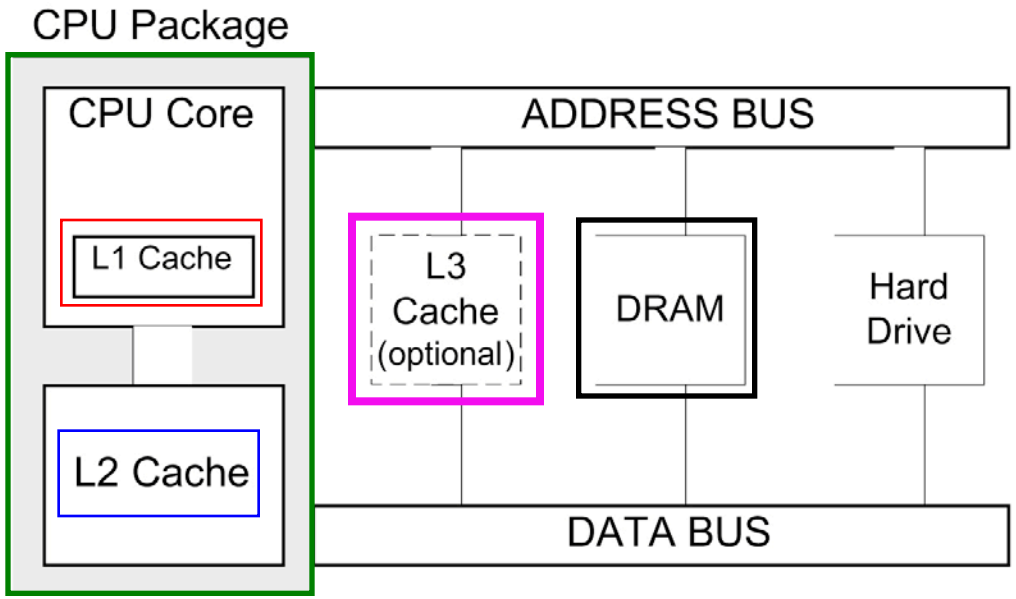



**Fig. 24-1** L1, **L2** and L3 Cache

**L1** cache speed is a multiple of CPU speed, since a CPU retires multiple instructions per clock cycle.

**L2** cache works at the same speed as the CPU since it is on the same package.

**L3** cache works at a fraction of CPU speed as it is located outside the CPU package.

# 24.1: x86 PENTIUM® EVOLUTION
## cache evolution

**Table 24-1: Pentium Cache Size and Speed**

| Product | Year | Transistors | CLK Speed | L1 Cache (Code) | L1 Cache (Data) | L2 Cache |
|---|---|---|---|---|---|---|
| 386 | 1985 | 275K | 20 MHz | 0 | 0 | 0 |
| 486 | 1989 | 1.2M | 25 MHz | 4 KB | 4 KB | 0 |
| Pentium | 1993 | 3.1M | 60 MHz | 8 KB | 8 KB | 0 |
| Pentium Pro | 1995 | 5.5M | 200 MHz | 8 KB | 8 KB | 0 |
| Pentium II | 1997 | 7M | 266 MHz | 16 KB | 16 KB | 256 KB |
| Pentium III | 1999 | 8.2M | 700 MHz | 16 KB | 16 KB | 512 KB |
| Pentium IV | 2000 | 42M | 1.5 GHz | 12 KB | 8 KB | 256 KB |
| Pentium M | 2004 | 140M | 2 GHz | 32 KB | 32 KB | 2 MB |
| Pentium IV | 2004 | 125M | 3.4 GHz | 12 KB | 16 KB | 1 MB |
| Pentium Duo | 2006 | 152M | 2.16 GHz | 32 KB | 32 KB | 2 MB |

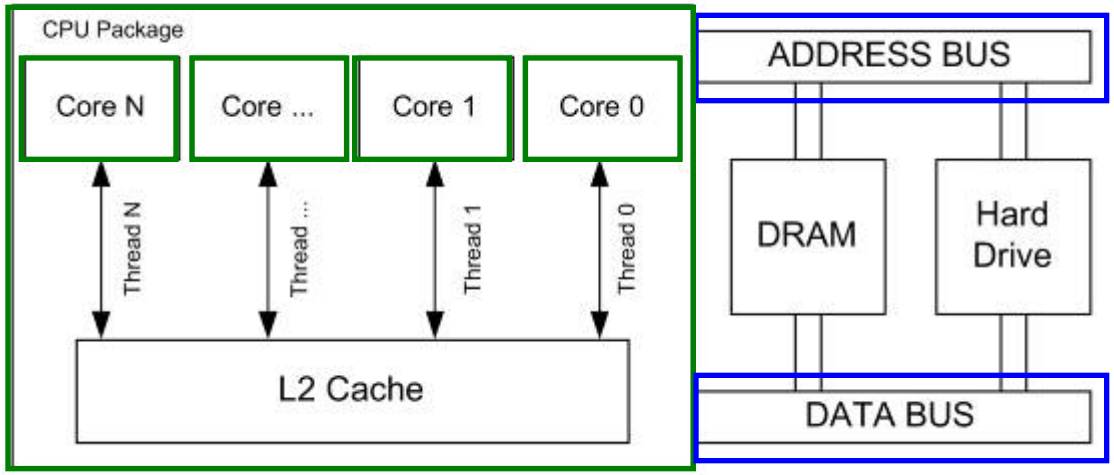
*Note*: The clock speed is the speed at the time of introduction.

# 24.1: x86 PENTIUM® EVOLUTION
## Hyper-Threading Technology (HTT)

- In Pentium® IV, multithreaded execution was introduced.
  - A *thread* is a series of parallel programs that can run on different CPUs simultaneously.
    - In a multiprocessor environment, each is given its own CPU and memory.
  - Intel placed multiple CPUs into a single chip, and called it hyper-threading.
- As far as the OS is concerned, a CPU with hyper-threaded capability appears to be multiple logical CPUs inside a single physical CPU.

# 24.1: x86 PENTIUM® EVOLUTION
## Hyper-Threading Technology (HTT)

- In threaded CPUs, internal logical CPUs must share the system bus access.

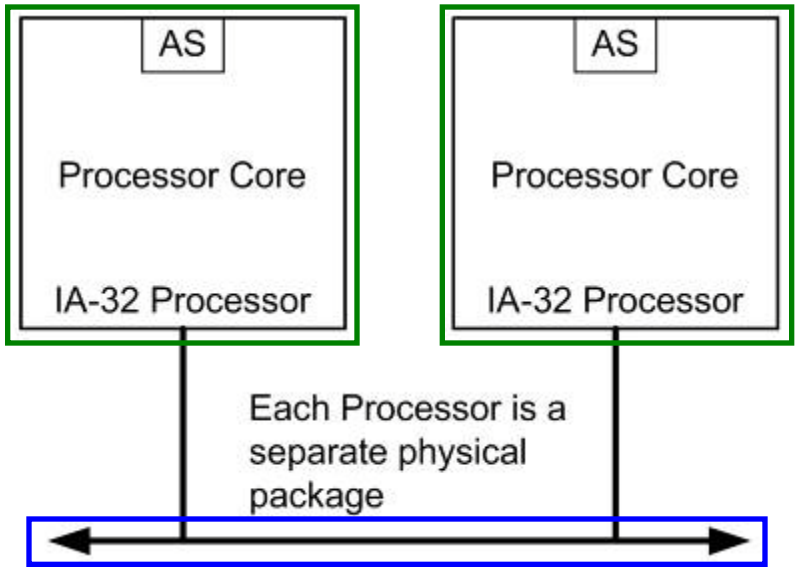


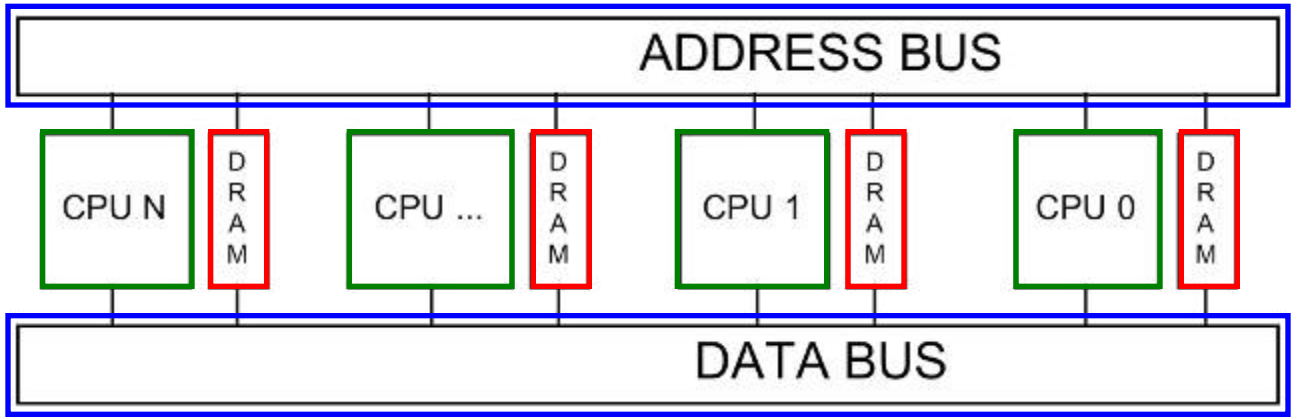

Since both **logical processors** inside the hyper-threaded CPU use the **same bus** to accesses memory, they can get in each other's way and slow down program execution.

**Fig. 24-3** Multithreading

# 24.1: x86 PENTIUM® EVOLUTION
## Hyper-Threading Technology (HTT)

- When using multiple processors, each **CPU** has its own access to the **system bus**.



# 24.1: x86 PENTIUM® EVOLUTION
## Hyper-Threading Technology (HTT)

- In x86 literature, the words *threads* and *tasks* are used interchangeably.
  - There is a difference between a task and a thread.
- Multitasking runs multiple tasks all on a single CPU.
  - The CPU switches from one task to another in a circular fashion, giving each task a slice of the CPU's time.
- True multithreading attempts to parallelize execution of a single program in order to speed up the execution of that program.

# 24.1: x86 PENTIUM® EVOLUTION
## multicore technology

- Many newer-generation Pentiums® have what is called multicore technology.
  - Two or more independent processors (called cores) into a single chip.
  - Many x86 CPUs come with dual- and quad-core features, and work is being done on processors with 8 cores.
- In the *multicore* CPU there is one pathway to the system memory for the CPU
- In the *multiprocessor* CPUs each processor has its own memory space independent of the others.

# 24.1: x86 PENTIUM® EVOLUTION
## multicore technology

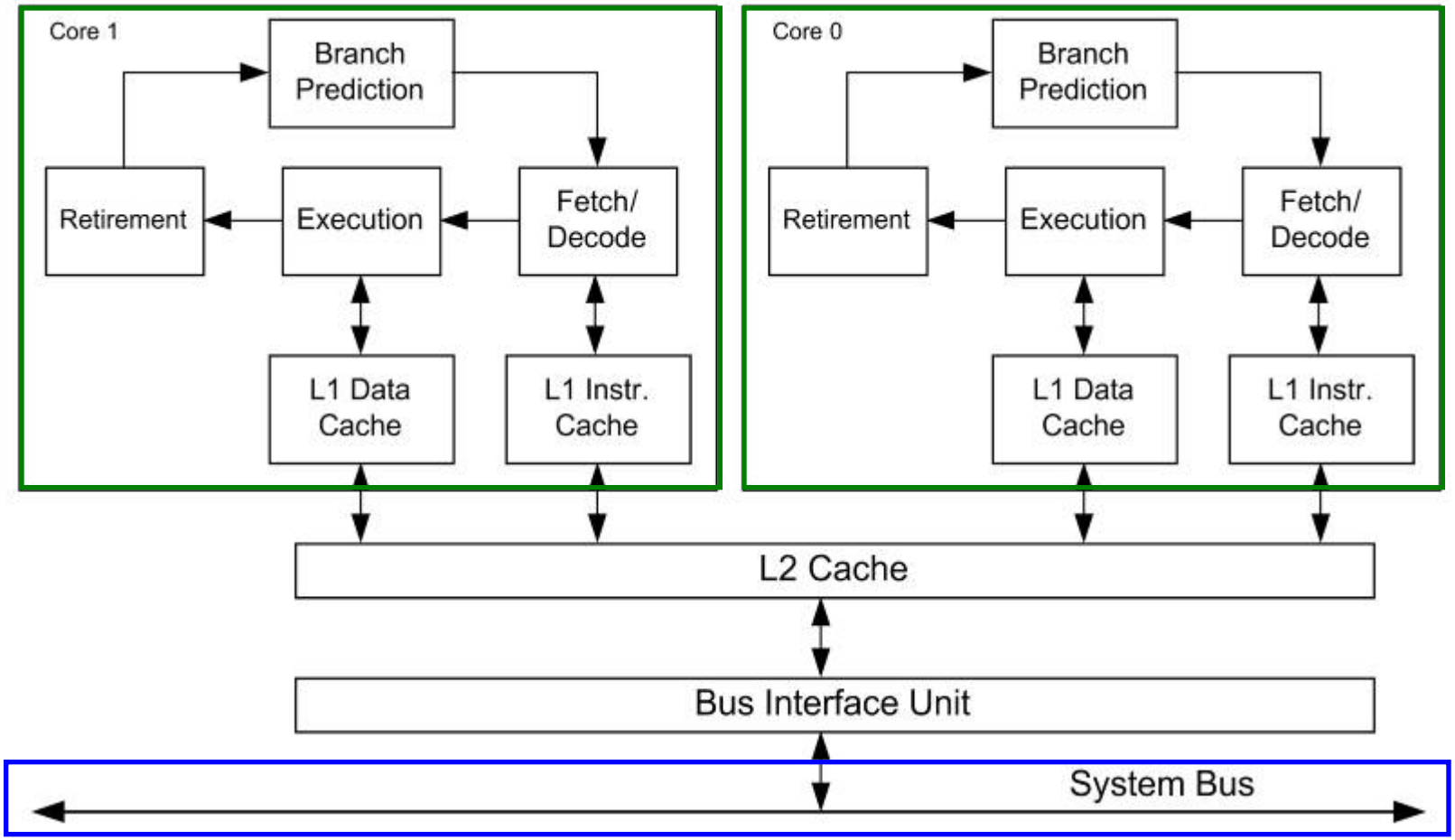
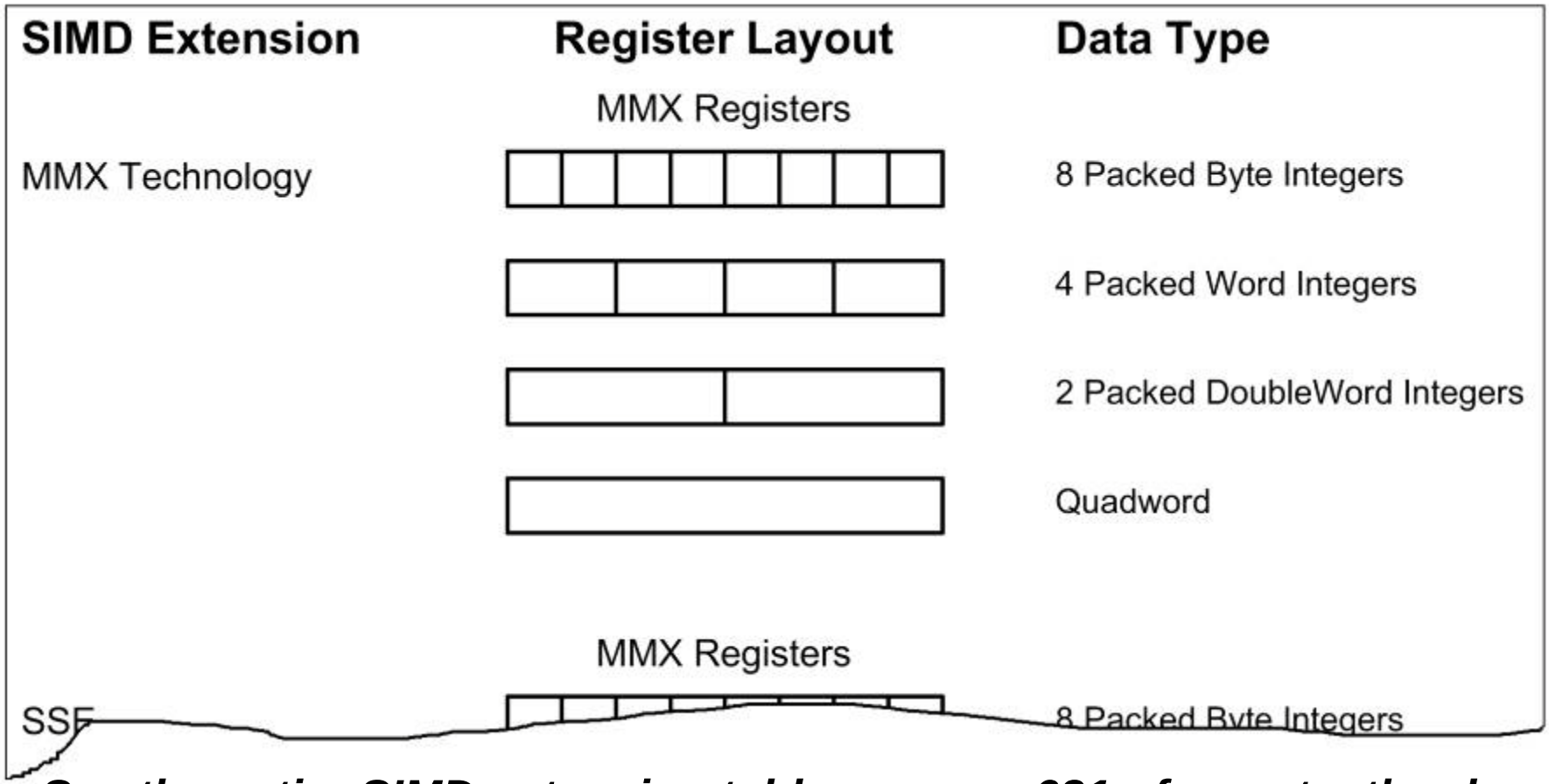



**Fig. 24-5** Dual Core Processor

# 24.1: x86 PENTIUM® EVOLUTION
## Streaming SIMD Extension (SSE)

- Single instruction multiple data (SIMD) was first incorporated into the Pentium® Pro with the introduction of MMX technology.
  - The MMX used SIMD operations on packed bytes of data
- Intel expanded SIMD to include floating-point data, and called it streaming SIMD extension (SSE).
  - SSE was expanded further to include both single and double double-precision floating points.
    - Referred to as SSE, SSE2, SSE3, and SSSE3.
  - Original SIMD had one set of MMX registers.
    - Extended SIMD has several sets of MMX registers in addition to a new set of 128-bit registers called XMM.

# 24.1: x86 PENTIUM® EVOLUTION
# Streaming SIMD Extension (SSE)




***See the entire SIMD extension table on page 631 of your textbook.***

**Fig. 24-6** SIMD Extension in x86 (*Courtesy of Intel Corp.*)

# 24.1: x86 PENTIUM® EVOLUTION
## other features of Pentium®

- Pentium® increased to 10 the number of pipeline stages, then 20, making a super-superpipeline CPU.
  - The instruction decoder units were expanded to four.
    - With a hugely expanded size of instruction queue.
- The enhancements were still insufficient to keep high-speed system designers happy, which left x86 CPU companies no choice but to expand the size of general-purpose registers to 64-bit.
  - The change to 64-bit architecture came about only when increase in performance of the 32-bit architecture was no longer possible.

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
## 64-bit architecture in x86

64-bit x86 processors needed to maintain compatibility with the earlier generations of 386 legacy software.

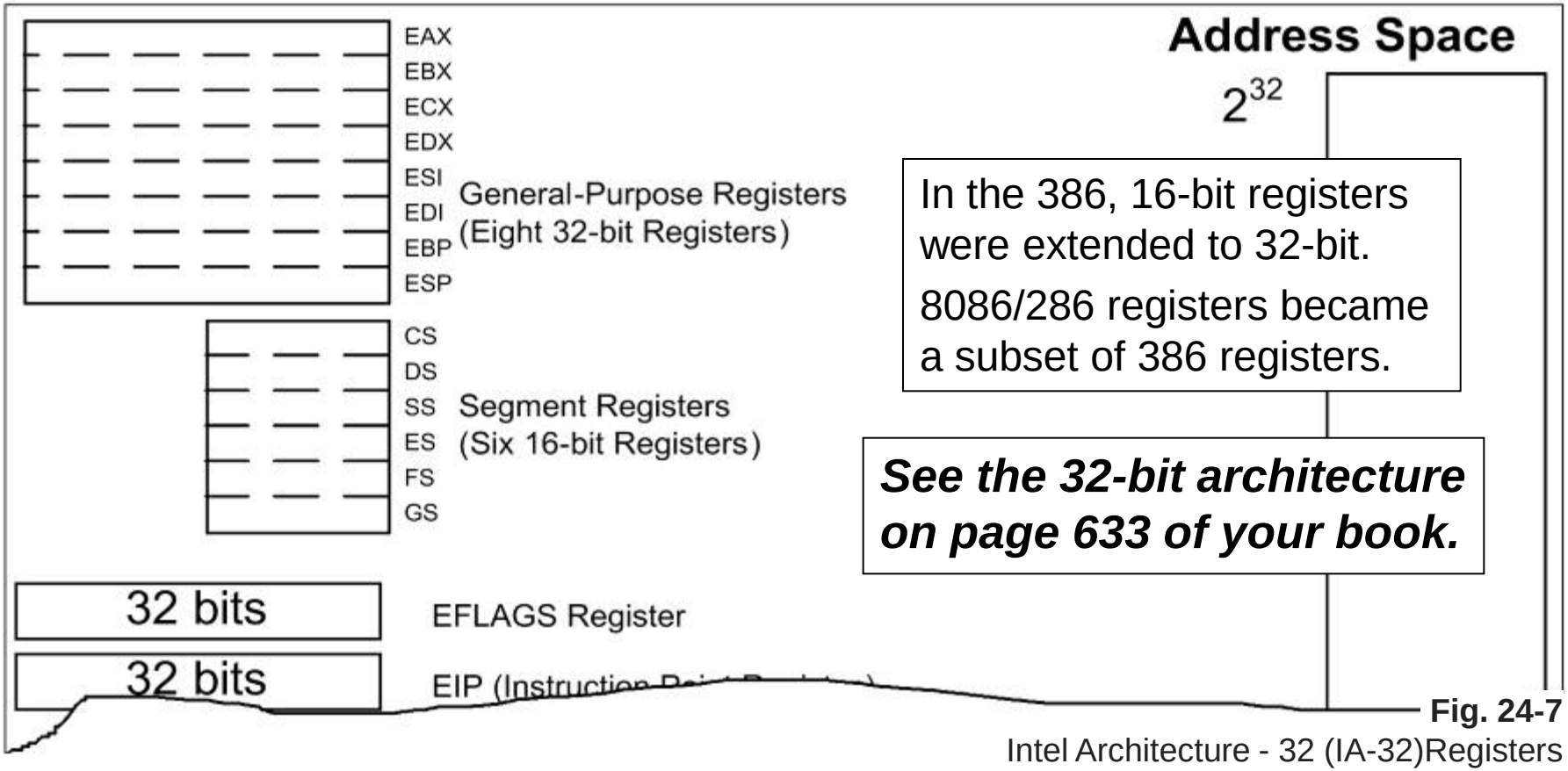



**Fig. 24-7**
Intel Architecture - 32 (IA-32)Registers

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
## 64-bit architecture in x86

- To make the transition from 32- to 64-bit data types easier, 64-bit architecture can work in two modes:
  - **Compatibility mode** - uses 8-, 16- & 32-bit data sizes and limits memory space to 4G bytes, like 386 architecture.
    - Most 16-bit & 32-bit legacy application software can be run without recompilation under 64-bit systems like Microsoft Vista.
  - **64-bit mode** - 386 registers **AEX** , **EBX**, etc., are expanded to 64-bit, and designated as **RAX** , **RBX**, etc.
    - Eight new 64-bit general purpose registers called R8–R15 were added, for a total of 16 64-bit registers.

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
## 64-bit architecture in x86

The new 64-bit **R8–R15** registers can also be accessed as 8-bit, 16-bit, and 32-bit registers.

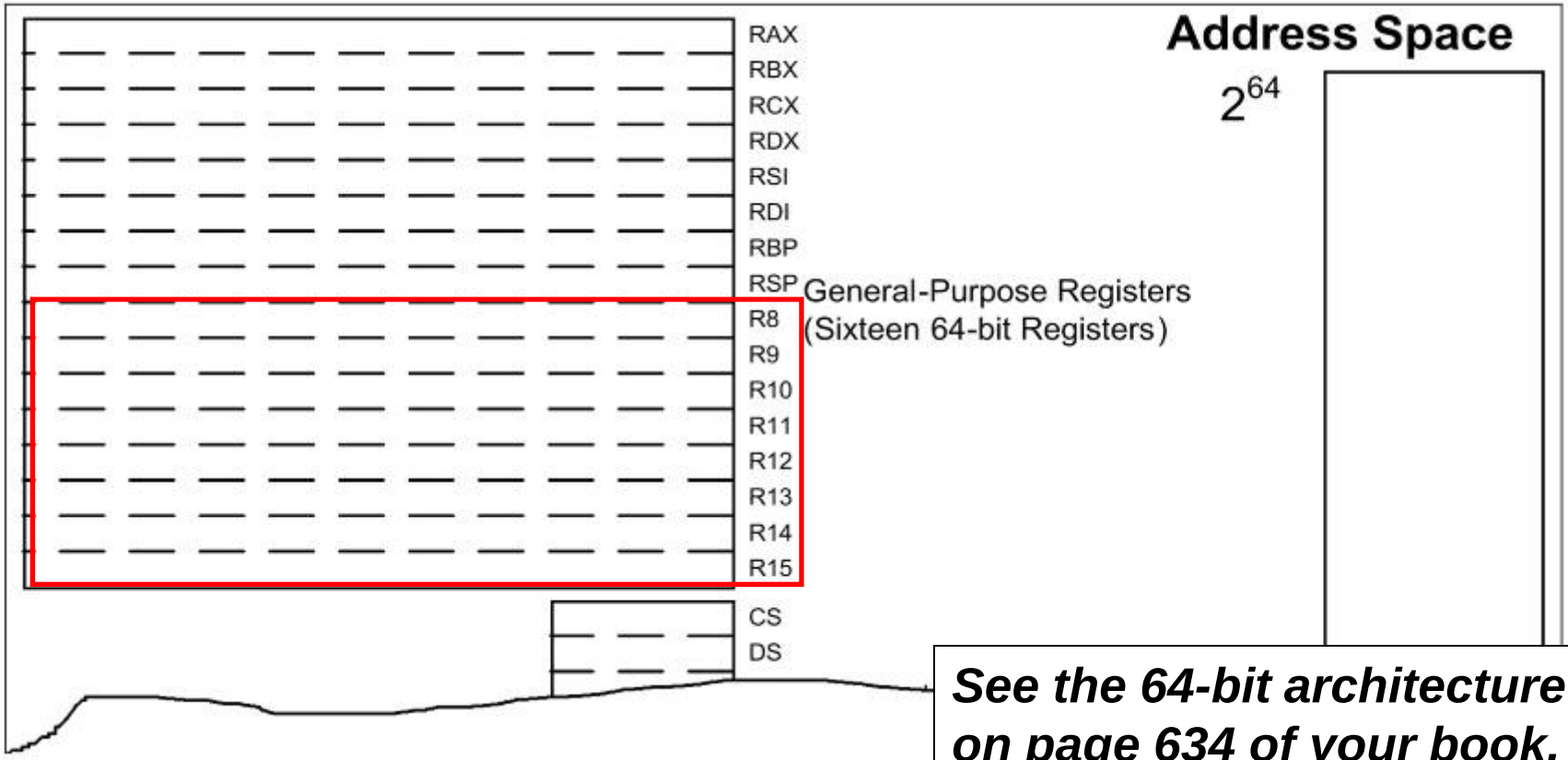



**Fig. 24-8** 64-Bit Registers in 64-Bit x86 Processors

***See the 64-bit architecture on page 634 of your book.***

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
## external memory of 64-bit architecture

- Pentium® 32-bit architecture limited the external memory space to 4G bytes.
  - It used segment registers to convert the linear addresses to physical addresses.
- 64-bit architecture largely stopped using segment registers, introducing a flat 264 byte memory space.
  - The **EIP** (instruction pointer) of the 386 has been expanded from 32-bit to 64-bit, and is called **RIP**.
    - It allows access of up to 264 bytes of code & data stored in external memory, using address A0–A63 pins.
  - A new 64-bit data pointer register allows access to external data memory using the A0–A63 address pins.

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
## external memory of 64-bit architecture

- Not all family members have all the 64 address pins.
  - Many 64-bit x86 processors have only 36 pins (A0–A35).
    - Allows access of up to 64 G bytes of external memory.
- In 32-bit architectures, register sizes match the 32-bit external data bus.
  - In Pentium® Pro, the external data bus was expanded to 64-bit, even though the registers were left at 32-bit.
  - For the 64-bit registers, the external data bus is also 64-bit.
- To increase the bus bandwidth of the 64-bit x86 processors, 128 pins for the data bus is very likely.

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86
# x86 64-bit processors and Vista

- Both Intel & AMD have been producing 64-bit x86 processors since the early 2000s.
  - Microsoft used some aspects of the architecture in Windows XP and called it XP x64.
  - Only on introduction of Vista did Microsoft take full advantage of 64-bit architecture.
- Due to legacy software & the need for the transition to the new 64-bit systems, there are two versions:
  - **Vista** - will run on any x86 32-bit architecture.
  - **Vista x64** - requires a 64-bit x86 processor and at least 1G byte of DRAM on the motherboard.

# 24.2: 64-BIT PROCESSORS & VISTA FOR x86 Moore's Law

In the mid 1960s, Intel cofounder Gordon Moore predicted:

> *"The number of transistors that would be incorporated on a silicon die would double every 18 months for the next several years."*

**Table 24-2: Some 64-Bit Processors in x86 Fam**

| Product | Year | Tr | |
|---|---|---|---|
| Xeon | 2004 | | |
| Xeon Processor MP | 2005 | | |
| Pentium 4 | 2005 | | |
| Pentium 840 | 2005 | 230 M | 64 GB |
| Dual-Core Xeon | 2005 | 321 M | 64 GB |
| Pentium 4 672 | 2005 | 164 M | 64 GB |
| Pentium 955 | 2006 | 376 M | 64 GB |
| Core 2 X6800 | 2006 | 291 M | 64 GB |
| Xeon 5160 | 2006 | 291 M | 64 GB |
| Xeon 7140 | 2006 | 1.3 B | 64 GB |
| Core 2 QX6700 | 2006 | 582 M | 64 GB |
| Quad-Core Xeon 5355 | 2006 | 582 M | 64 GB |

*Note*: For the registers associated with these 64-bit processors see Figure 24-6.

***See the 64-bit x86 family on page 635 of your textbook.***

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