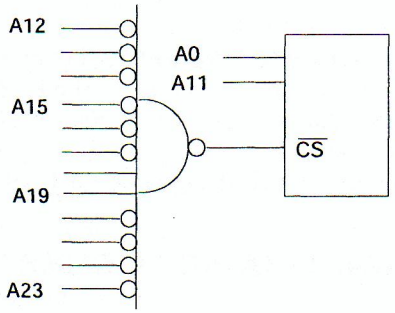
SOLUTIONS FOR CHAPTER 10 (2)

SECTION 10.1 (3.1): SEMICONDUCTOR MEMORY FUNDAMENTALS

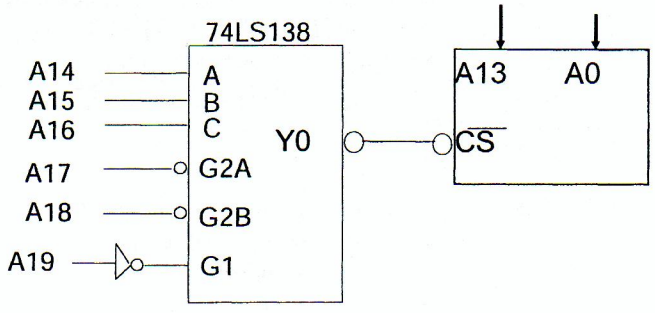
1. For memory it is 4 megabits, and for the computer it is 4 megabytes.
2. true
3. true
4. false, not necessarily
5. true
6. access time
7. true
8. It need not be removed from the system board to be erased and reprogrammed.
9. true
10. DRAM
11. SRAM
12. all of them, except UV-EPROM and NV-RAM
13. c
14. c
15. (a) 32Kx8, 256K
    (b) 8Kx8, 64K
    (c) 4Kx8, 32K
    (d) 8Kx8, 64K
    (e) 4Mx1, 4M
    (f) 8Kx8, 64K
    (g) 4Kx8, 32K
    (h) 2Kx8, 16K
    (i) 256Kx4, 1M
    (j) 64Kx8, 512K
16. (a) 128K, A0 - A13, D0 - D7
    (b) 256K, A0 - A14, D0 - D7
    (c) 512K, A0 - A15, D0- D7
    (d) 1M, A0 - A8, D0 - D3 plus RAS and CAS
    (e) 512K,A0-A15,D0-D7
    (f) 256K, A0 - A7, D0 - D3 plus RAS and CAS
    (g) 4M, A0- A9, D0 - D3 plus RAS and CAS
    (h) 16M, A0 - A10, D0 - D3 plus RAS and CAS
    (i) 512K, A0 - A7, D0 - D7 plus RAS and CAS

SECTION 10.2 (2.2): MEMORY ADDRESS DECODING

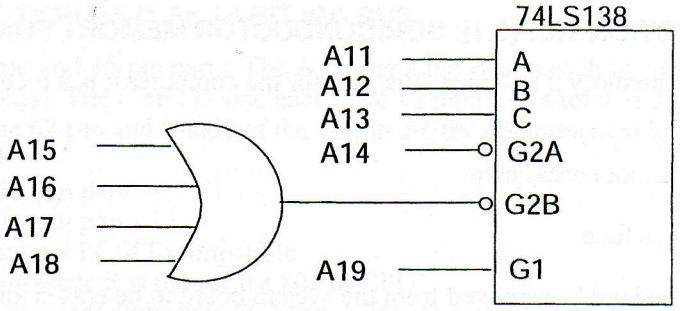
17. 98000H - 9FFFFH
18. The diagram follows.



19. for Y0 = F0000H - F1FFFH, Y3 = F6000H - F7FFFH, Y6 = FC000H - FDFFFH
20. The diagram follows. Each Y controls a 16K block.



21. Y3 = 0C000 - 0FFFF, Y6 = 18000 - 1BFFF, Y7 = 1C000 - 1FFFF.
22. The diagram follows. Each Y controls a 2K block.



23. Y1 = 80800 - 80FFF, Y4 = 82000 - 827FF, Y5 = 82800 - 82FFF.
24. low RD is also active low.
25. CPLD

SECTION 10.2 (2.2): IBM PC MEMORY MAP

26. 00000 - 9FFFFH, a total of 640K bytes for RAM; A0000H - BFFFFH, a total of 128K bytes for video RAM; C0000H - FFFFFH, a total of 256K bytes for ROM
27. from 00000 - 9FFFFH, a total of 640K bytes
28. No, DOS uses only the lowest 640K bytes. Furthermore, the addresses beyond 9FFFFH belong to video RAM; therefore, if we use them there will be a conflict with video.
29. CS = FFFFH IP = 0000
30. No. The address range 00000 - 9FFFFH is strictly managed by DOS. DOS uses whatever K bytes it needs and uses the rest for applications software. To use that area results in fragmentation of the 640K memory space and can result in a system crash.
31. From F000:FFF5 to F000:FFFD is the logical address and FFFF5 to FFFFD is the physical address.
32. Subtracting C0000 from C7FFF gives 7FFFH, but since the 0 is the first address location it will be 8000H bytes. Converting that to decimal and dividing by 1024 gives 32K bytes in ROM allocated space.
33. B0FFFH
34. BBFFFH
35. When the 8088 is powered up, the FFFF0H is the first physical location that the CPU fetches the op code from. Therefore the ROM (non-volatile) memory must be mapped at those addresses and not 00000. Furthermore, the 00000 belongs to the interrupt vector table.
36. FFFF0H; the opcode is EAH, the opcode for FAR JMP

SECTION 10.4 (2.4): DATA INTEGRITY IN RAM AND ROM

37. 34H+54H+7FH+11H+E6H+99H=297H. The 2 is dropped and then the 2's complement of 97H=69H. Therefore the checksum byte is 69H.
38. (a) 29H + 1CH + 16H + 38H + 6DH =00, dropping the carries from the upper nibble. Therefore, the data is not corrupted.
    (b) 29H +1CH + 16H + 30H + 6DH = F8H, which is not zero. Therefore, some bytes are corrupted.
39. ROM, RAM
40. true
41. 320K bytes is broken down to 256K and 64K bytes blocks. It means that we need 9 of the 64Kx1 and 9 of the 256Kx1 memory chips, a total of 18 chips.
42. That gives two 256Kx4 and one 256Kx1 chip for the 256KB block, and two 64Kx4 and one 64kx1 chip for the 64KB block, for a total of 6 memory chips.

43. A higher density chip means a lower parts count, which leads to a smaller printed circuit board. Also, a lower number of parts leads to a lower number of system defects.
44. true
45. true
46. even = 1 and odd = 0
47. even = 0 and odd = 1
48. even = 1 and odd = 0

SECTION 10.5 (2.5): 16-BIT MEMORY INTERFACING

49. 80286
50. 2 of each, a total of 8 chips
51. A0=1 and BHE=0
52. A0=0 and BHE=0
53. A0=0 and BHE=1
54. A0=1 and BHE=0
55. increases driving capability of the data pins
56. megabytes per second
57. the data bus width and bus cycle time
58. true
59. false
60. (a) 200 ns (2 × 100 ns) memory cycle gives (1/200 ns) × 2 bytes =10 megabytes/s
    (b) 125 ns (2 × 62.5 ns) memory cycle gives (1/125 ns) × 2 bytes = 16 megabytes/s

SECTION 10.6 (2.6): ISA BUS MEMORY INTERFACING

61. MEMW and MEMR on the 36-pin section of the ISA bus
62. 24 megabytes since we have A0 - A23
63. low, yes
64. The 8-bit D0 - D7 is the default mode in ISA. Therefore, to use the entire D0 - D15 data bus we must assert the MEMCS16 pin low.
65. low, yes
66. The ZEROWS pin is used to tell the system board to perform the read and write cycle time with zero wait states. For 16-bit ISA, memory read and write has 1 WS, unless the ZEROWS pin is aserted low. For 8-bit ISA, if ZEROWS is asserted low, the read/write cycle has 1 WS instead of 4 WS.
67. D0 - D7 portion
68. the entire D0 - D15
69. 6 × 125 ns = 750 ns (4WS + 2)
70. 3 × 125 ns = 375 ns (1WS + 2)
71. 2 × 125 ns = 250 ns (0WS + 2)
72. 3 × 125 ns = 375 ns (1WS + 2)
73. Both need to be asserted low.
74.

MEMCS16	ZEROWS	Data bus used	Read Cycle Time	Bus Bandwidth
0	0	D0 - D15	250 ns	8MB/sec
0	1	D0 - D15	375 ns	5.33MB/sec
1	0	D0 - D7	375 ns	2.66 MB/sec
1	1	D0 - D7	750 ns	1.33MB/sec

75. More memory on smaller cards and much shorter access time than the ISA bus.