计算机组成原理习题 10/22

一、将下列MIPS指令翻译成机器代码，并描述这些指令在图4.17所示的单周期MIPS CPU中的执行过程，列出控制信号的值。

1. add $s1,$s2,$s3

2. sub $s4,$t5,$t9

3. and $t1,$t2,$s3

4. or

5. slt $t0, $s3, $s4

6. lw $ra,4($sp)

7 sw $a0, 8($sp)

8. j 20000

9.

20000H BEQ $S3,$S4,EXIT ;BEQ指令所在地址为20000H

......

40000H ;EXIT指令所在地址为40000H

二、Provide the type, assembly language instruction, and binary representation of instruction described by the following MIPS f elds: op=0, rs=3, rt=2, rd=3, shamt=0, funct=34

三。Provide the type, assembly language instruction, and binary representation of instruction described by the following MIPS f elds: op=0x23, rs=1, rt=2, const=0x4

四、 In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| IF | ID | EX | MEM | WB |  |
| 250ps | 350ps | 150ps | 300ps | 200ps |  |

What is the clock cycle time in a pipelined and non-pipelined processor?