# ILI9882T+HSD10.51 For HQ Sleep in/Out abnormal display Analysis Report



2023.08.01



Customer: HQ

❖ LCM: ILI9882T+HSD10.51

**❖** Abnormal phenomenon:

➤ Sleep in/Out Abnormal Display



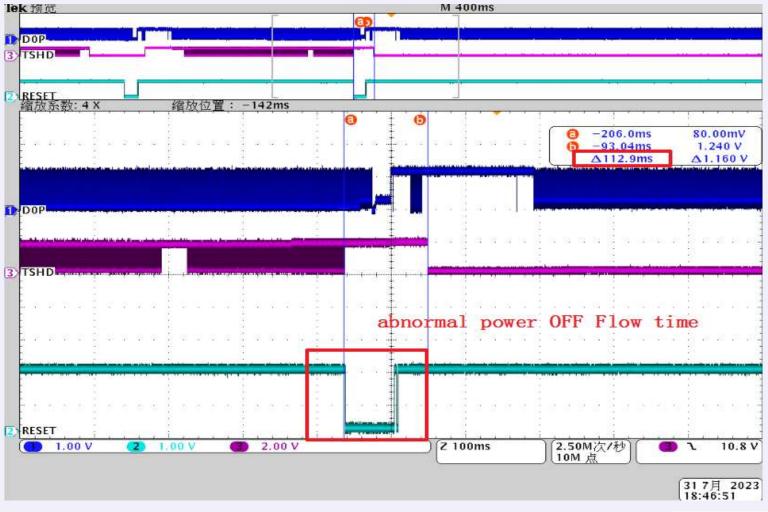
#### ❖ NG & OK Code Comparison

When abnormal conditions, the read back value of the register is the IC default value.

```
NG花屏
                                                                                                                                                       OK显示正常
2023/7/26 14:19:04 22,687 字节 其它一切 ▼ ANSI ▼ UNIX
                                                                                            2023/7/26 14:24:13 22.687 字节 其它一切 ▼ ANSI ▼ UNIX
    Disable report
                                                                                                Disable report
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x00, data =
(ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x00, data = 0x00,
   (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x01, data = 0x40,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x01, data =
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x02, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x02, data =
                                                                                                                                                                       0x00,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x03, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x03, data =
                                                                                                                                                                        0x00.
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x04, data =
(ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x04, data = 0x00,
                                                                                                                                                                        0x01,
   (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x05, data = 0x40,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x05, data =
                                                                                                                                                                       0x11,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x06, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x06, data =
                                                                                                                                                                       0x00,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x07, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x07, data =
                                                                                                                                                                       0x00.
(ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x08, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x08, data =
                                                                                                                                                                       0x80,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x09, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x09, data =
                                                                                                                                                                       0x81,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0A, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0A, data =
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0B, data = 0x01,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0B, data =
                                                                                                                                                                        0x00,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0C, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0C, data =
(ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0E, data = 0x00.
                                                                                            (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x0E, data = 0x1A.
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x24, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x24, data = 0x00,
(ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x25, data = 0x10,
                                                                                            (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x25, data = 0x00.
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x26, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x26, data = 0x00,
    (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x27, data = 0x00,
                                                                                                (ili ddi reg read, 555): Read master ddi page = 0x01, reg = 0x27, data = 0x00,
```



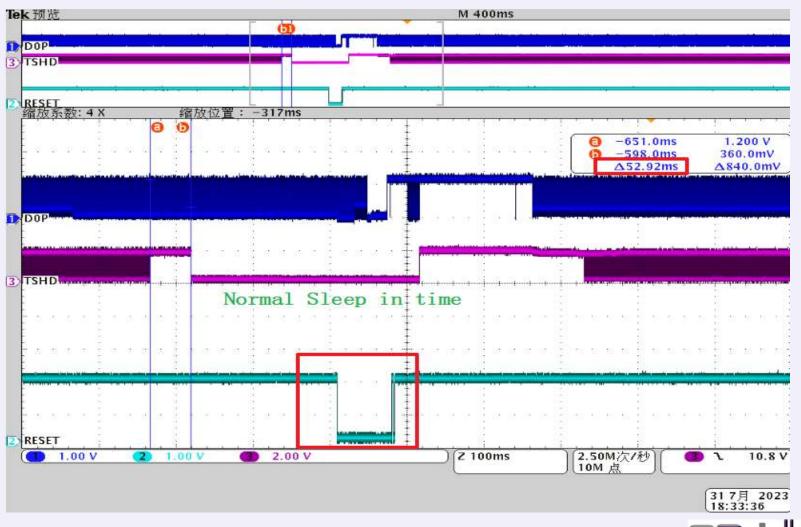
❖ Abnormal Display Waveform : Abnormal Power OFF Flow=112.9ms



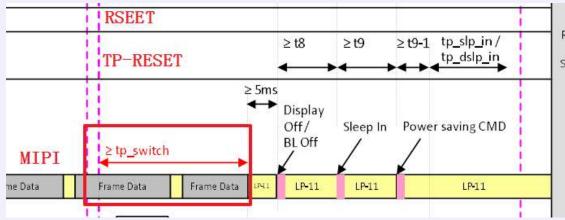
### **Analysis-Waveform**



❖ Normal display Waveform: Normal Sleep in Flow=52.92ms



- **When the OS wakes up, the screen is abnormal. Analyze the root causes:** 
  - > Entering the suspend sequence, the host side needs to first notify the TP to enter the scan stop.



- ➤ When the suspend timing can't meet the spec , then 28/10 will not take effect.
- When the IC doesn't in sleep in mode, then reset function follow APO sequence. (Timing =120ms)
- > In APO flow, IC cannot effectively execute MIPI command



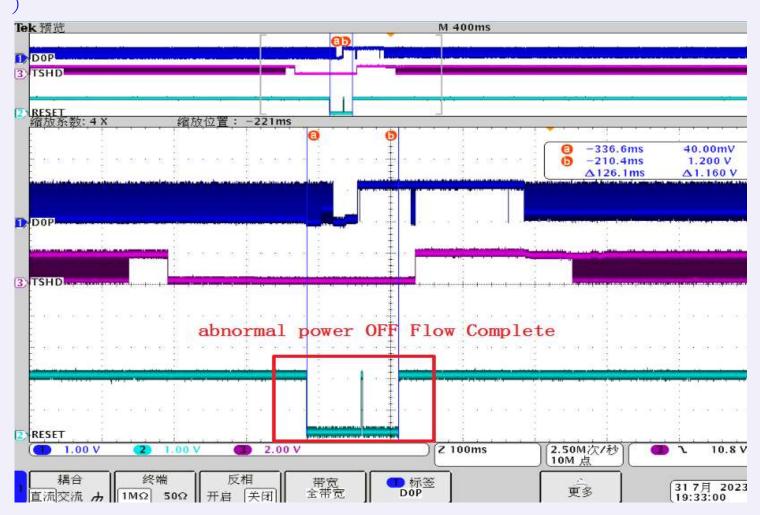
#### **Solution**

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❖ Entering the resume sequence → extend the reset timing from 2ms to 50ms to avoid APO flow.



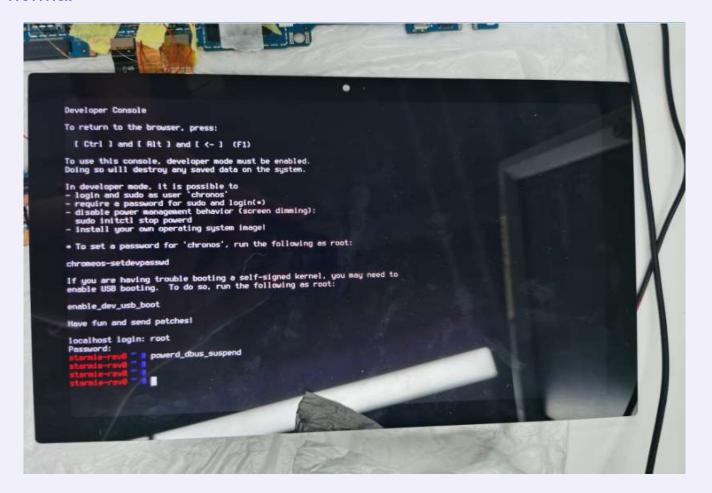
Resume Waveform : Sleep out time=126.1ms > 120ms (Abnormal Power OFF Flow





#### **Solution**

After the solution was combined, the Sleep out NG display improved and returned to normal





#### Summary

- **❖ NG&OK Code Comparison**: When abnormal conditions, the read back value of the register is the IC default value.
- The suspend timing can't meet the spec, then IC can't entering to sleep in mode.
- ❖ When the IC doesn't in sleep in mode , then reset function follow APO sequence.(Timing =120ms)
- Currently suspend to resume is only 112ms.
- Extend the reset timing from 2ms to 50ms to avoid APO flow.



## Thank you

