ILI9882T+HSD10.51 For HQ Sleep in&Out Abnormal Display_Analysis_Report

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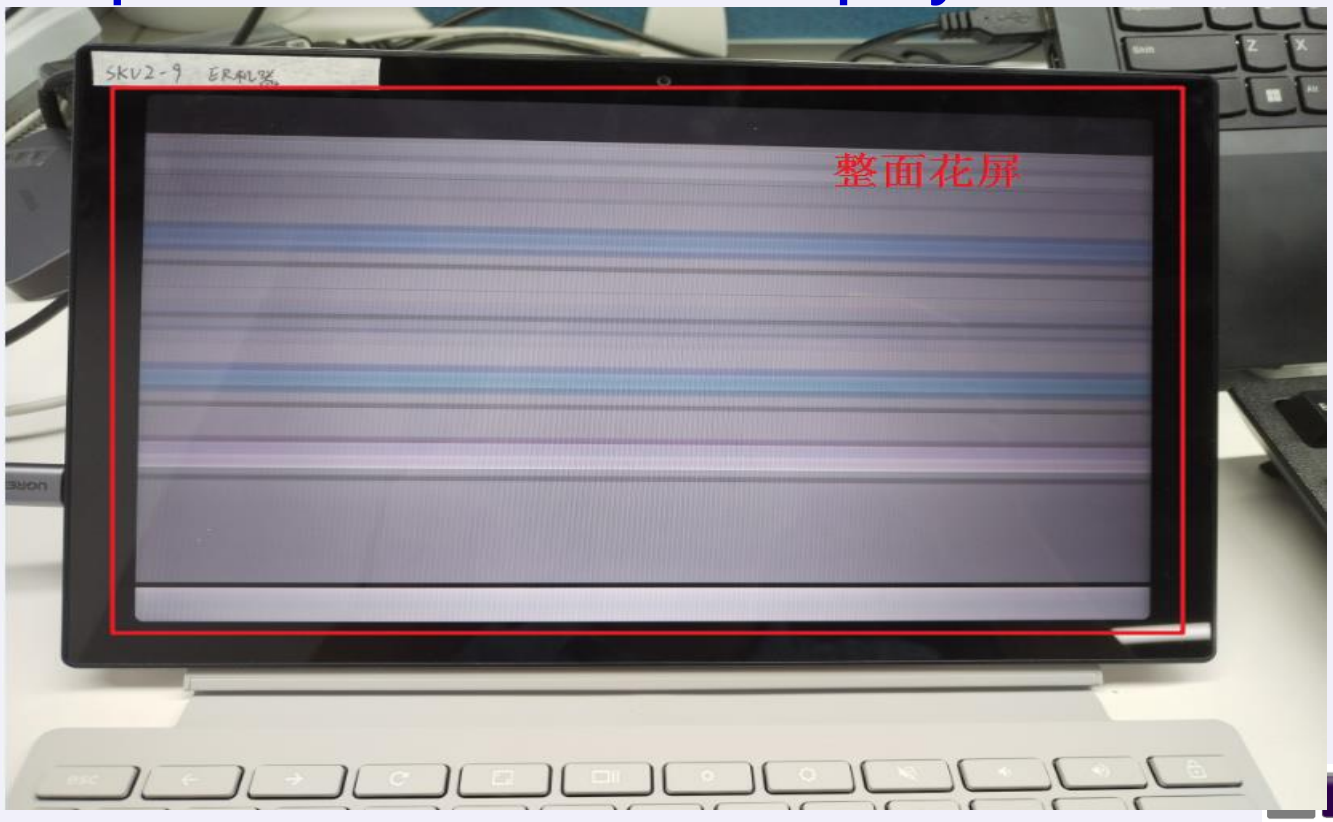
Sample Description

- 客户：HQ
- 模块：ILI9882T+HSD10.51
- 异常现象:
  - Sleep in&Out Abnormal Display



Analysis-Code Comparison

❖ NG&OK Code Comparison

- ➢ The IC register is the default value when the NG screen is displayed, and the system Code is not accessed.

2023/7/26 14:19:04 22,687 字节 其它一切 ▾ ANSI ▾ UNIX NG花屏

```
Disable report
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x00, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x01, data = 0x40,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x02, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x03, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x04, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x05, data = 0x40,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x06, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x07, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x08, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x09, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0A, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0B, data = 0x01,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0C, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0E, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x24, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x25, data = 0x10,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x26, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x27, data = 0x00,
```

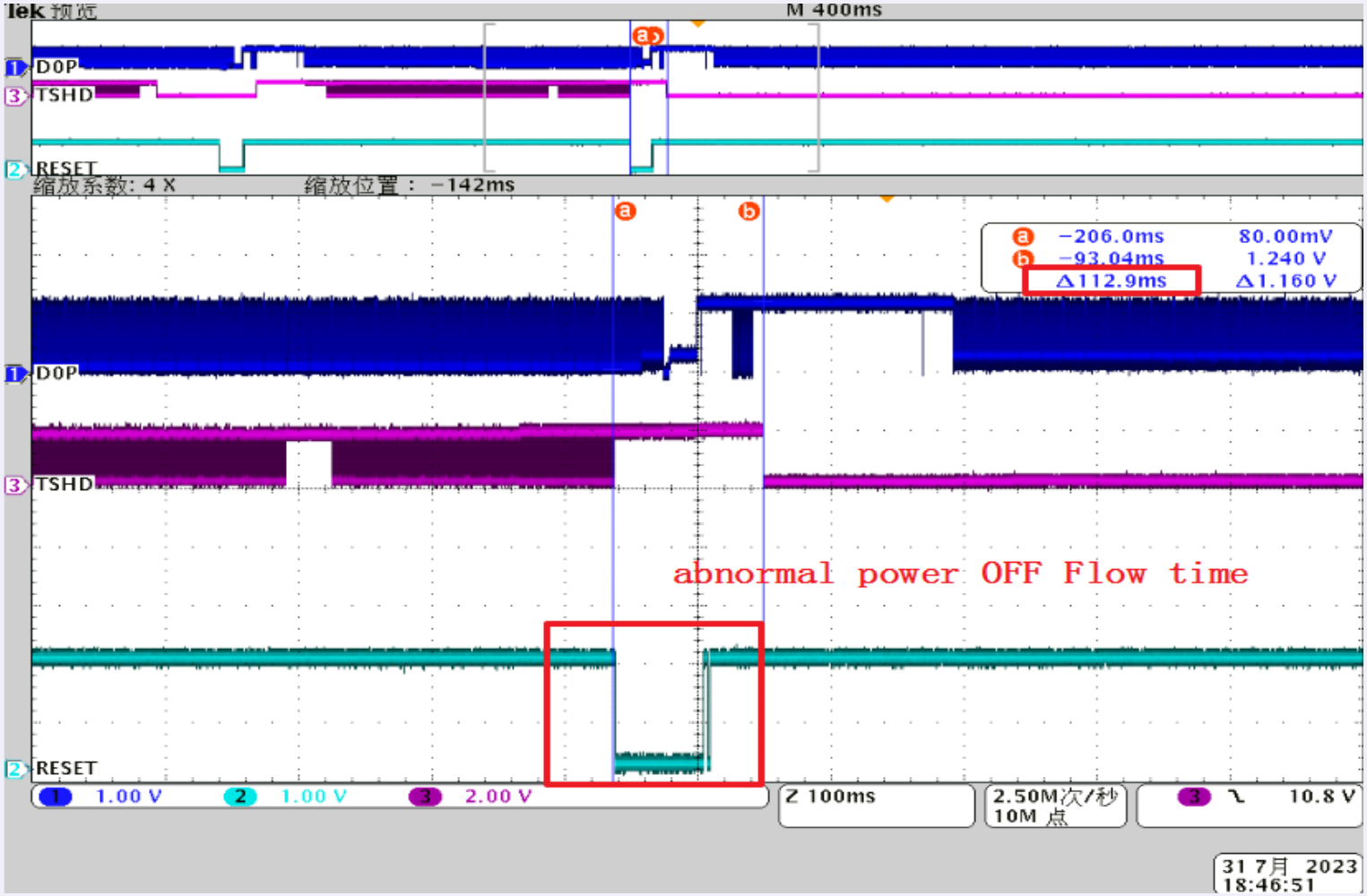
2023/7/26 14:24:13 22,687 字节 其它一切 ▾ ANSI ▾ UNIX OK显示正常

```
Disable report
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x00, data = 0x42,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x01, data = 0x11,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x02, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x03, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x04, data = 0x01,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x05, data = 0x11,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x06, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x07, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x08, data = 0x80,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x09, data = 0x81,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0A, data = 0x71,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0B, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0C, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x0E, data = 0x1A,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x24, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x25, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x26, data = 0x00,
(ili_ddi_reg_read, 555): Read master ddi page = 0x01, reg = 0x27, data = 0x00,
```

Analysis-Waveform

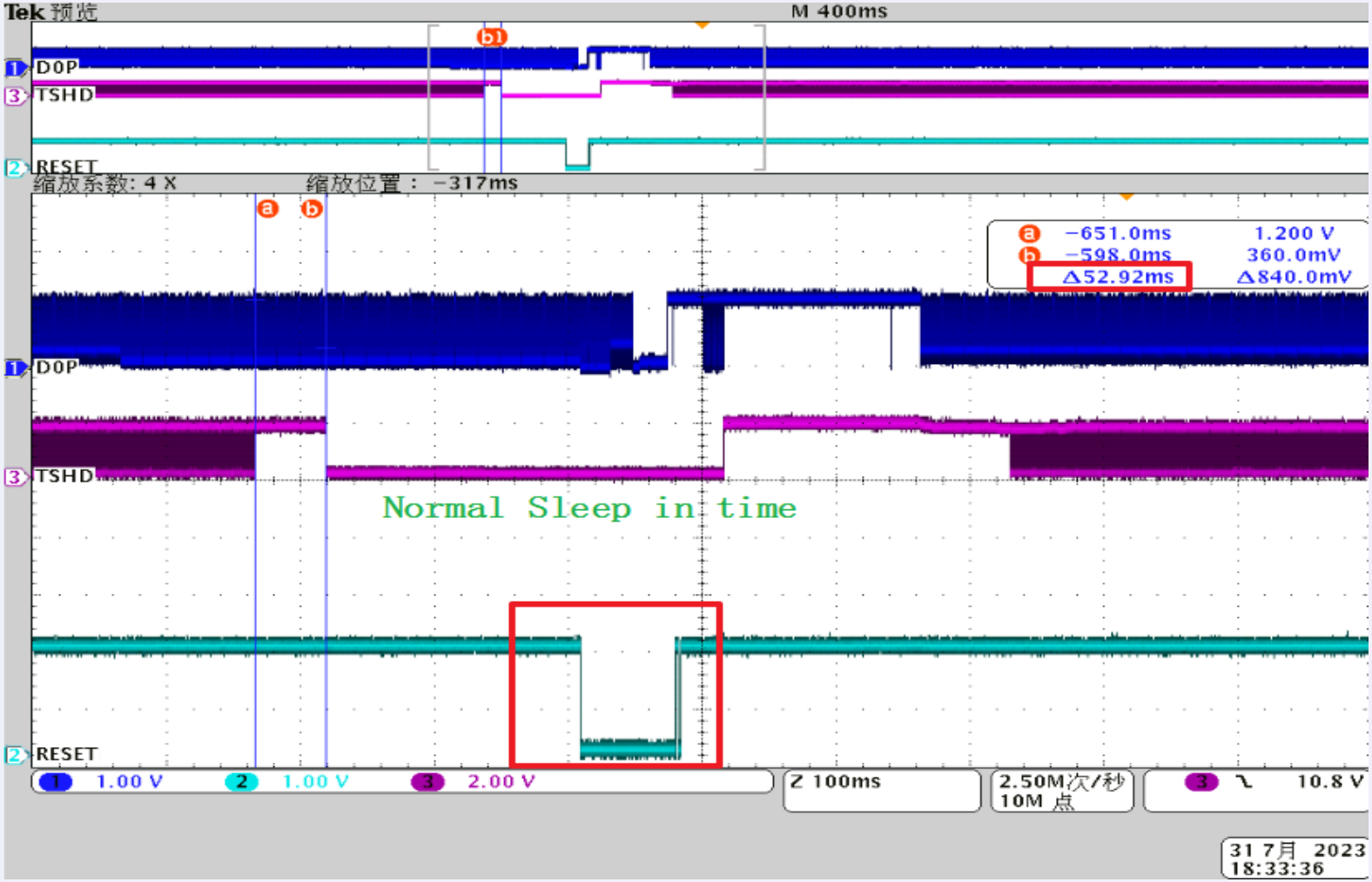
I ❤ Innovation

- NG screen is displayed Waveform：Abnormal Power OFF Flow=112.9ms



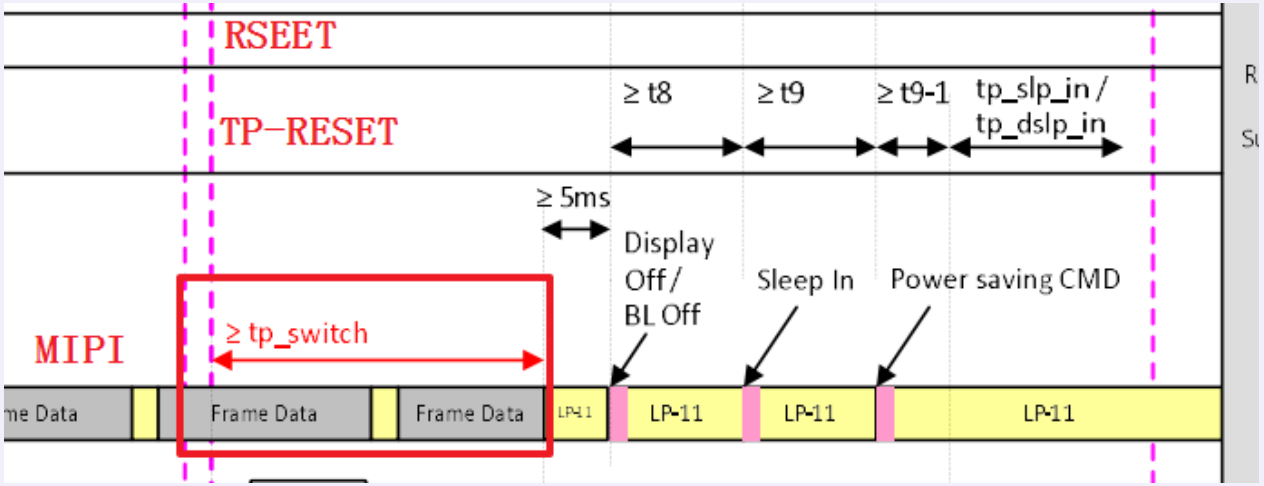
Analysis-Waveform

- OK screen is displayed Waveform：Normal Sleep in Flow=52.92ms



Root Cause

- When the OS wakes up, the screen is abnormal. Analyze the root causes:
  - When the OS goes to sleep, it cannot inform the IC that it is going to sleep in advance and needs to stop scanning;



  - When the suspend timing cannot meet the spec, then 28/10 will not take effect.
  - The IC did not enter the real Sleep in state, but because the RESET had been pulled down to a Low level to power off, the IC went through the abnormal power off Flow(Time=112.9ms).
  - When the OS wakes up again, the Code has been started normally, but the IC is in an abnormal power failure Flow, can not eat the Code under the OS, IC can not work normally, there will be an abnormal screen phenomenon.

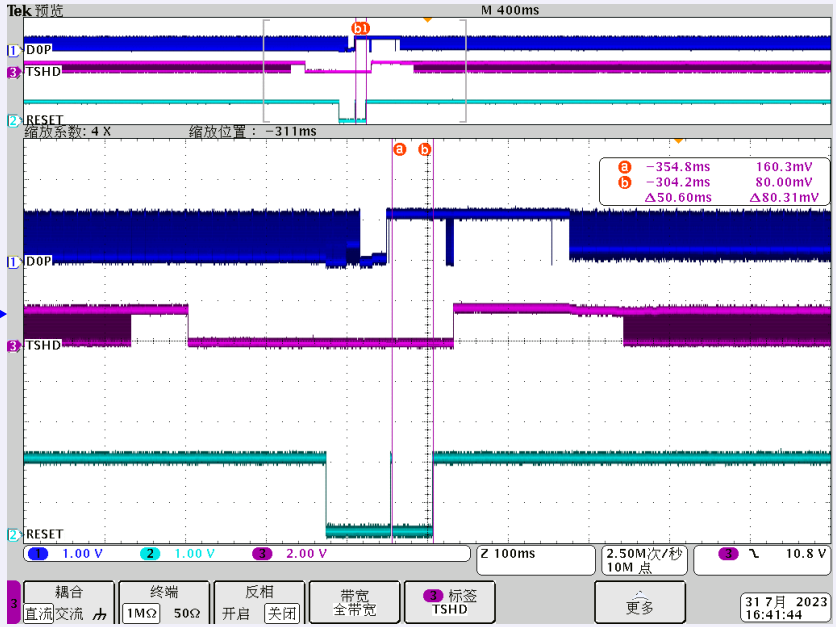
Solution

I ❤ Innovation

- When the OS wakes up, extend the RESET low time from 2ms to 50ms to allow the IC to power on after running abnormal power off Flow.

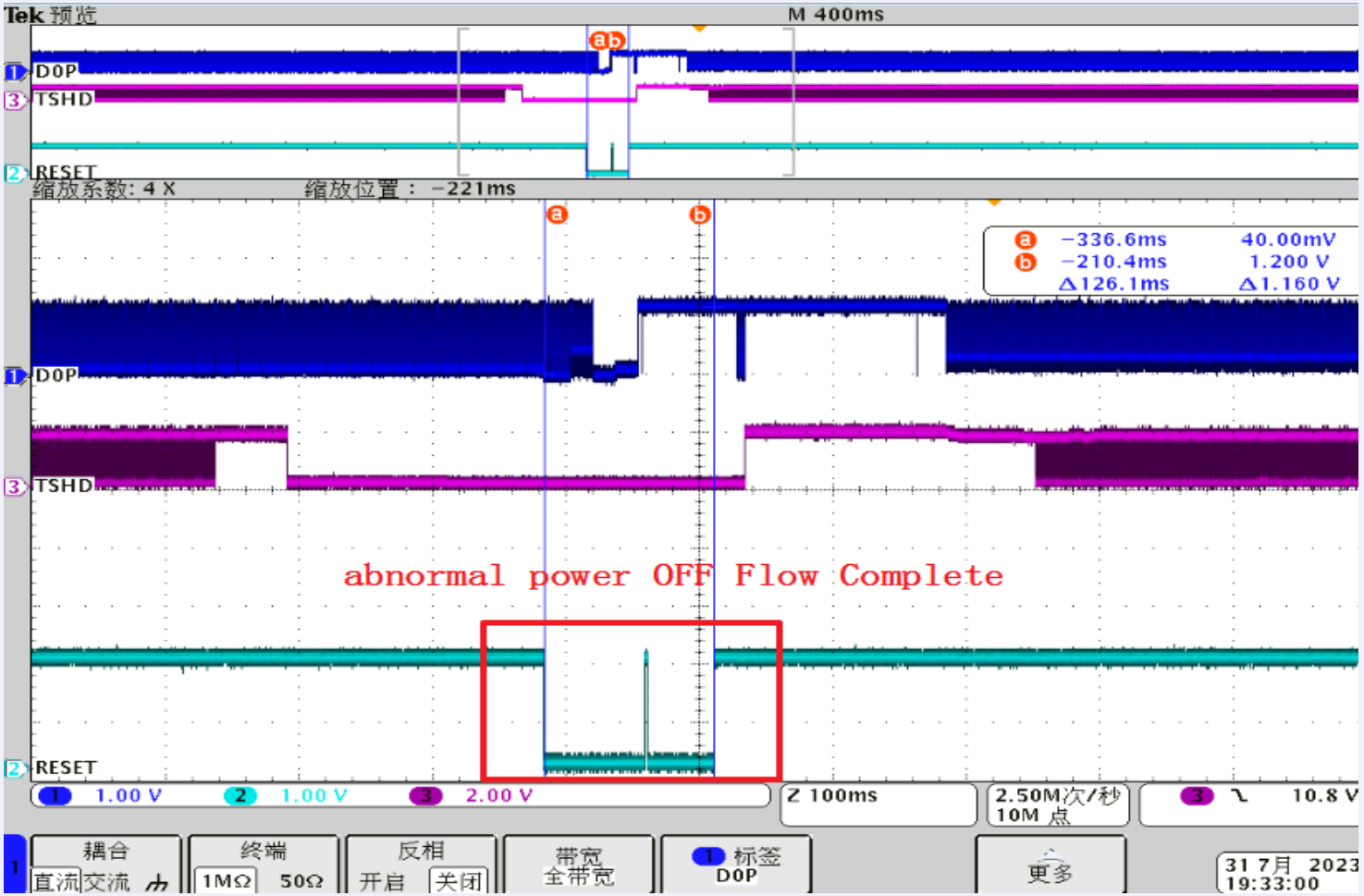
before modification（2ms）

after modification（50ms）



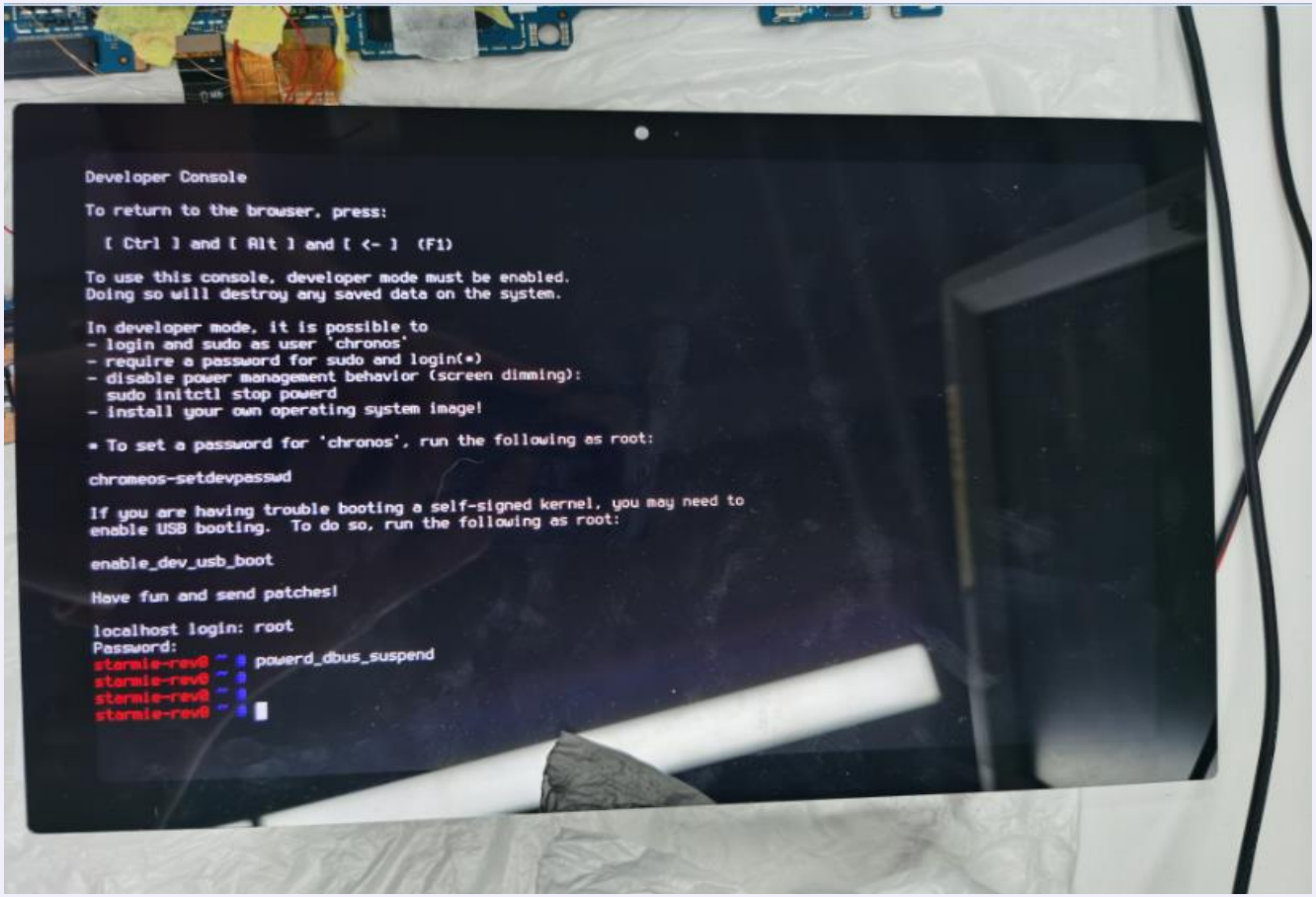
Solution

- Retest Sleep out Waveform：Sleep out time=126.1ms＞112.9ms（Abnormal Power OFF Flow）



Solution

- After the solution was combined, the Sleep out NG display improved and returned to normal



Summary

- NG&OK Code Comparison：The IC register is the default value when the NG screen is displayed, and the system Code is not accessed.
- The IC did not enter the real Sleep in state, but because the RESET had been pulled down to a Low level to power off, the IC went through the abnormal power Flow(Time=112.9ms).
- When the OS wakes up again, the Code has been started normally, but the IC is in an abnormal power failure Flow, can not eat the Code under the OS, IC can not work normally, there will be an abnormal screen phenomenon.
  - When the OS wakes up, extend the RESET low time from 2ms to 50ms to allow the IC to power on after running abnormal power off Flow.
- Improve Sleep out NG display.

Thank you