Southern Luzon State University
College of Engineering
Computer Engineering Department

CPE 09 INTRODUCTION TO HDL

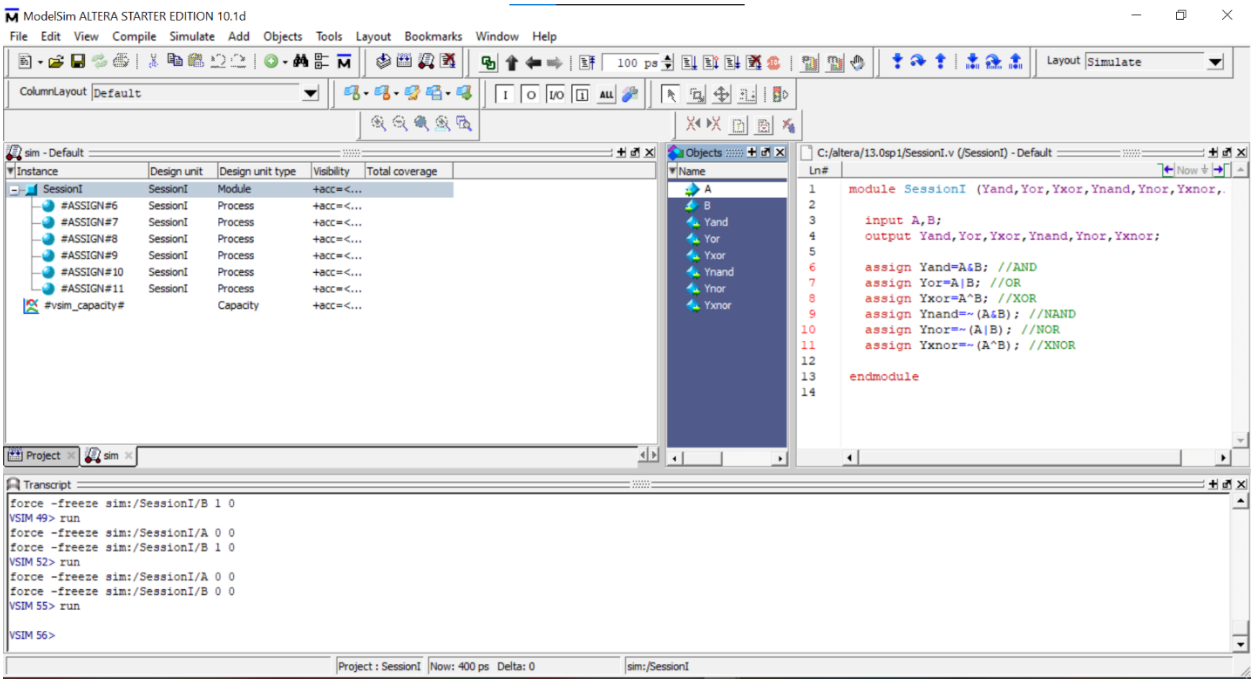
Name: REIMARC G. CORPUZ

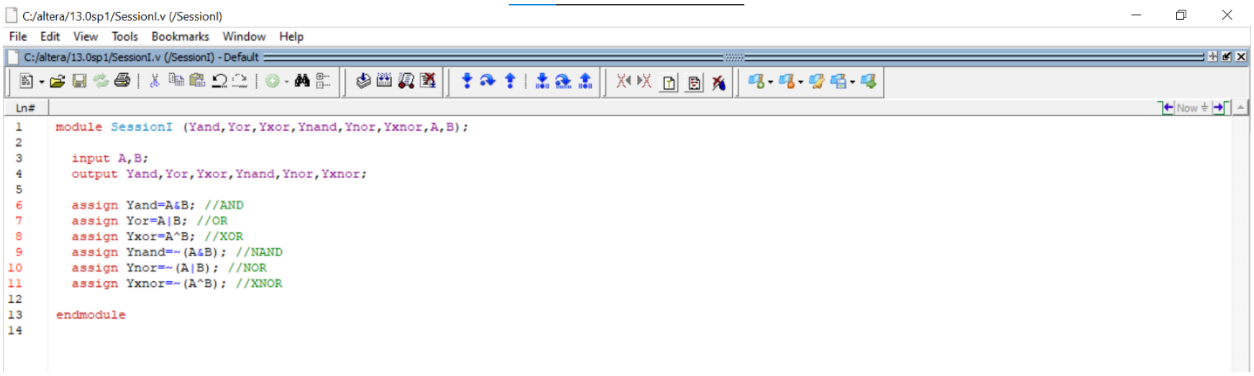
Date: Sept 27, 2022

Course and Year: BSCpE III GF

Score:

Verilog Code





Testbench Code

C:/altera/13.0sp1/SessionI_Struct_tb.v (/SessionI_Struct_tb)

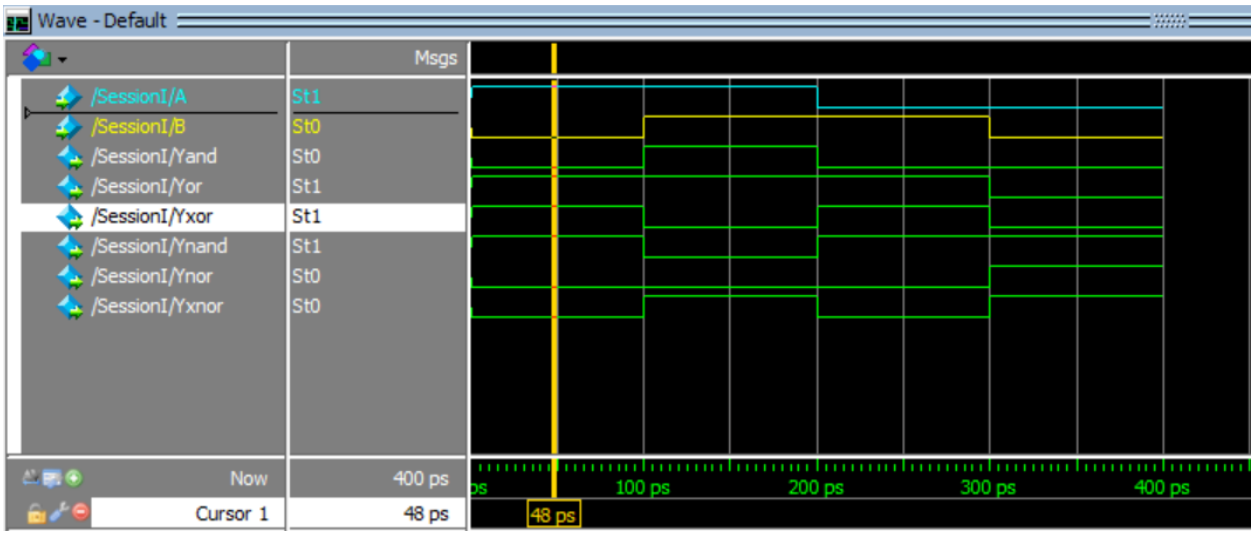
File Edit View Tools Bookmarks Window Help

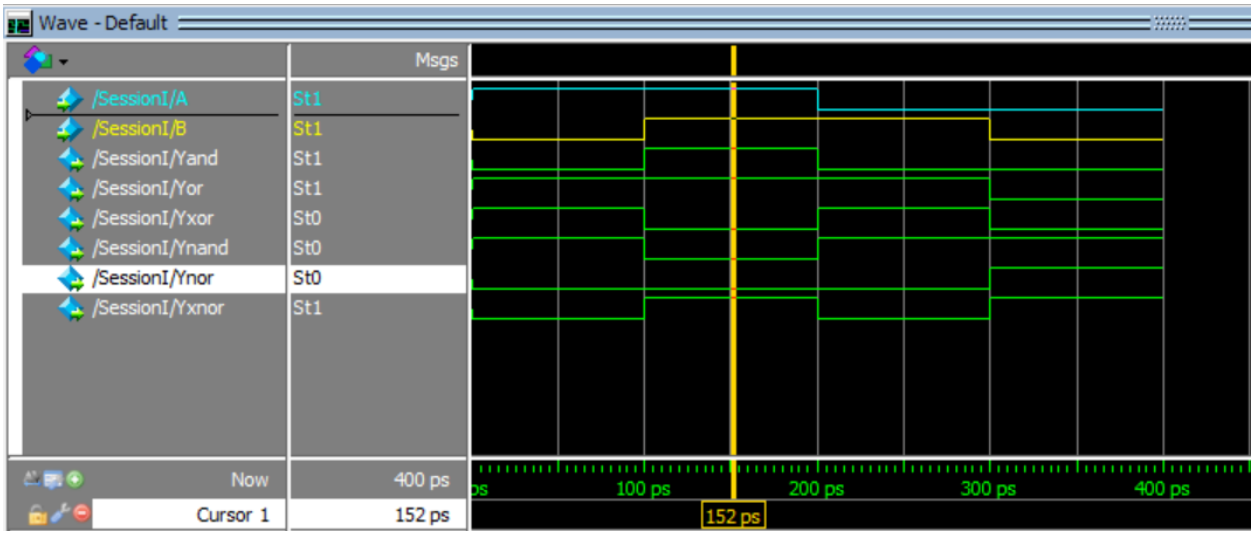
C:/altera/13.0sp1/SessionI_Struct_tb.v (/SessionI_Struct_tb) - Default

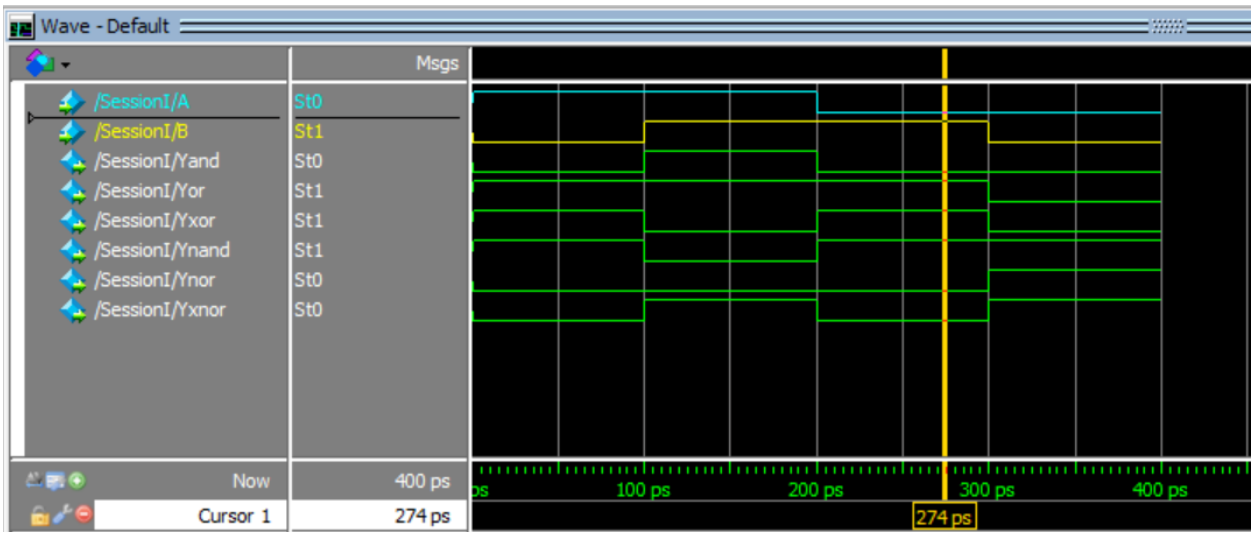
Step Over

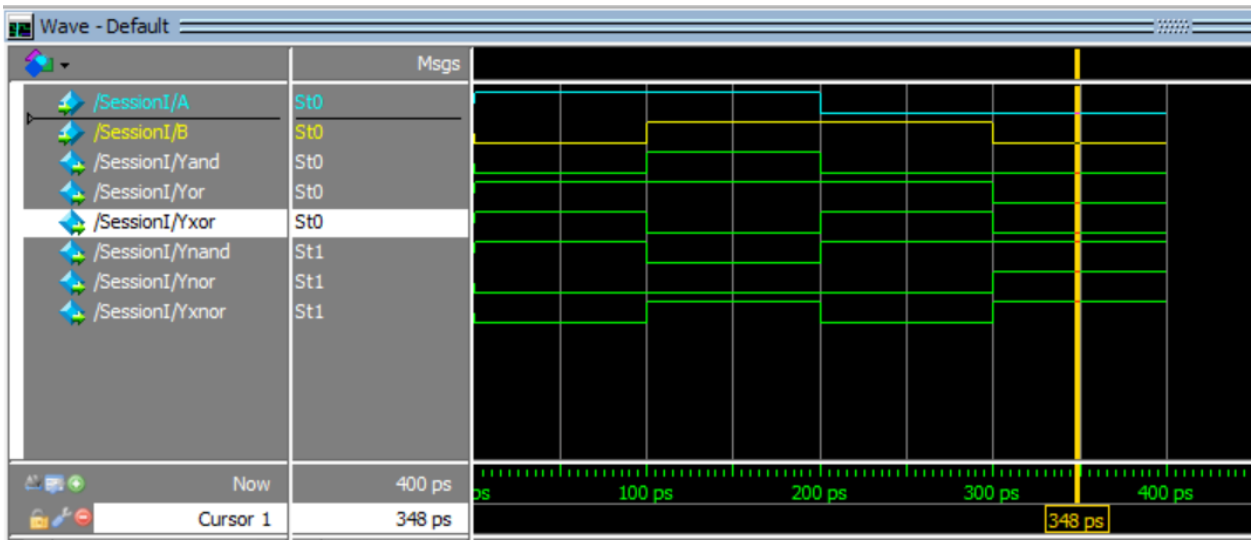
```
1   module SessionI_Struct_tb;
2
3     reg A,B;
4     wire Yand,Yor,Yxor,Ynand,Ynor,Yxnor;
5
6     SessionI MUT(Yand,Yor,Yxor,Ynand,Ynor,Yxnor,A,B);
7
8     initial
9     begin
10
11      A = 0; B = 0;
12      #100 A = 0; B = 1;
13      #100 A = 1; B = 0;
14      #100 A = 1; B = 1;
15
16    end
17    endmodule
```

Waveform Simulation

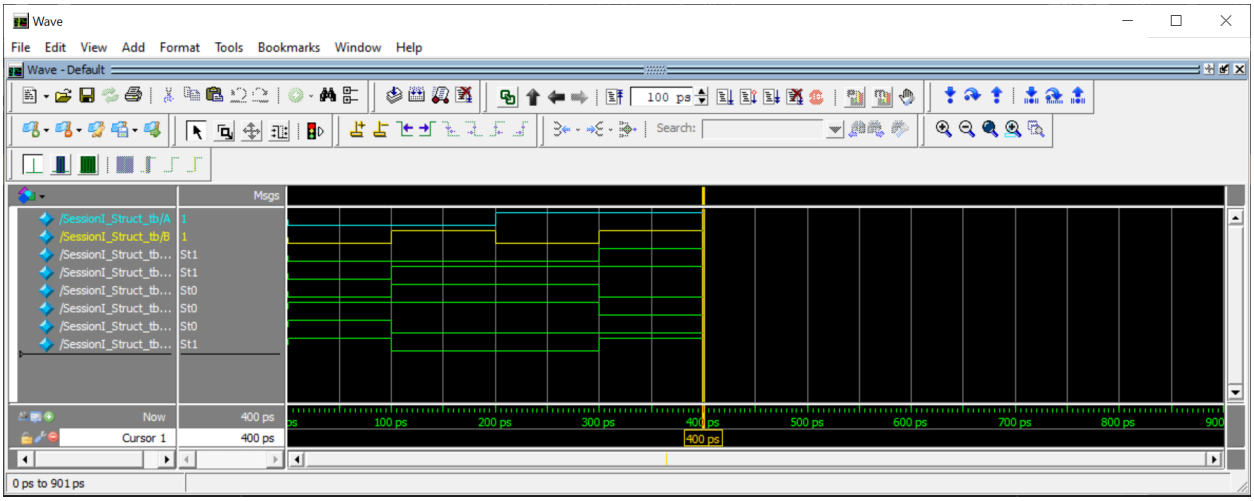








Waveform Simulation using Testbench



ID

Business Affairs Office
Southern Luzon State University

Lucban, Quezon

September 19,2022

Dear Ma'am/ Sir,

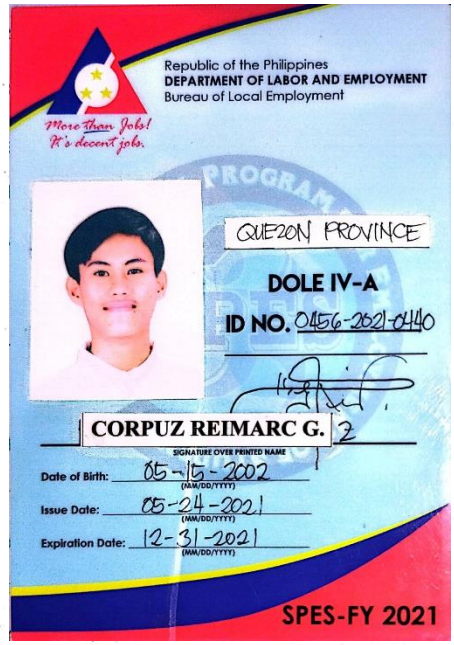
Good Day!

This is to inform you that the id of **Mr/Ms.** REIMARC G. CORPUZ was not yet process due to reschedule of ID processing for all freshmen (1st year), Kindly use this for his/her scholarship purposes.

Hoping for your understanding on this matter.

Yours truly,

ROMAME CABRERA
Business Affairs Office - Staff



Reflection

AFTER THE ACTIVITY USING MODELSIM, I UNDERSTAND THAT THE SIMULATION OF VERILOG CODE SHOWS THE WAVEFORM THAT TELLS THE LOGIC GATE EQUIVALENT TO 0 AND 1. AS SHOWN IN THE WAVE FORM SIMULATION, I HAVE THREE SETS OF INPUT FOR VARIABLE A AND B. I ALSO HAVE SIX OUTPUT VARIABLES DEPENDING TO THE TYPES OF LOGIC GATES (Yand, Yor, Yxor, Ynand, Ynor, Yxnor). IN THE FIRST SET INPUT (1 AND 0), THE OUTPUT WAVEFORM ARE FALLING, RISING, RISING, RISING, FALLING AND FALLING. THE ARRANGEMENT IS BASE ON THE ASSIGNED OUTPUT IN MY VERILOG CODE, THE DIRECTIONS OF THE WAVEFORM, SHOWS THAT IF IT IS RISING IT IS EQUIVALENT TO 1, AND IF IT IS FALLING IT IS 0. AND AS WE CAN SEE I HAVE FOUR SETS OF INPUT AND OUTPUT, 100 PICOSECOND PER SET WITH THE TOTAL OF 400 PS. THAT IS WHY I HAVE THAT WAVEFORM SIMULATION. THE DEFAULT DELAY THA I USED IS 1 NS THAT IS EQUAL TO 100 PS. IN MY VERILOG CODE I USED ASSIGN WITH THE BOOLEAN EXPRESSIONS & FOR AND, | FOR OR, ^ FOR XOR, AND ~ FOR NOT INSTEAD OF USING THE WORD AND, OR, XOR, NOT, NAND, NOR, XNOR. I INCLUDE IT ALL IN ONE MODULE OR VERILOG CODE. ALSO I REALIZE THAT, I CANNOT HAVE OR IT IS ERROR TO HAVE ONLY ONE OUTPUT VARIABLE (Y) FOR ALL LOGIC GATES, THAT IS WHY I GREATED SIX VARIABLE NAME.

FOR CONCLUSION, USING MODEL SIM I CAN EASILY IDENTIFY THE OUTPUT EQUIVALENT FOR LOGIC GATES OR IN A CIRCUIT DESIG AND SINCE IT ONLY HAVE TWO CHOICES WETHER IT IS 0 OR 1.