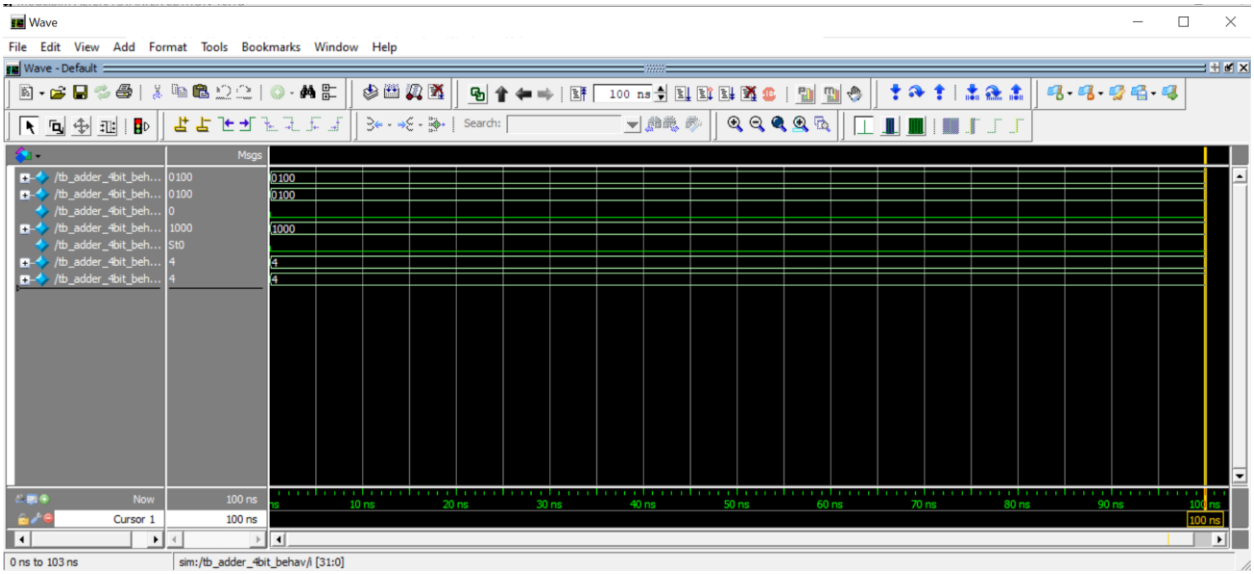
NAME: REIMARC G. CORPUZ DATE: OCTOBER 27, 2022

COURSE, YR & SECTION: BSCPE 3GF SCORE:

adder_4bit_bahavioral

Wave:

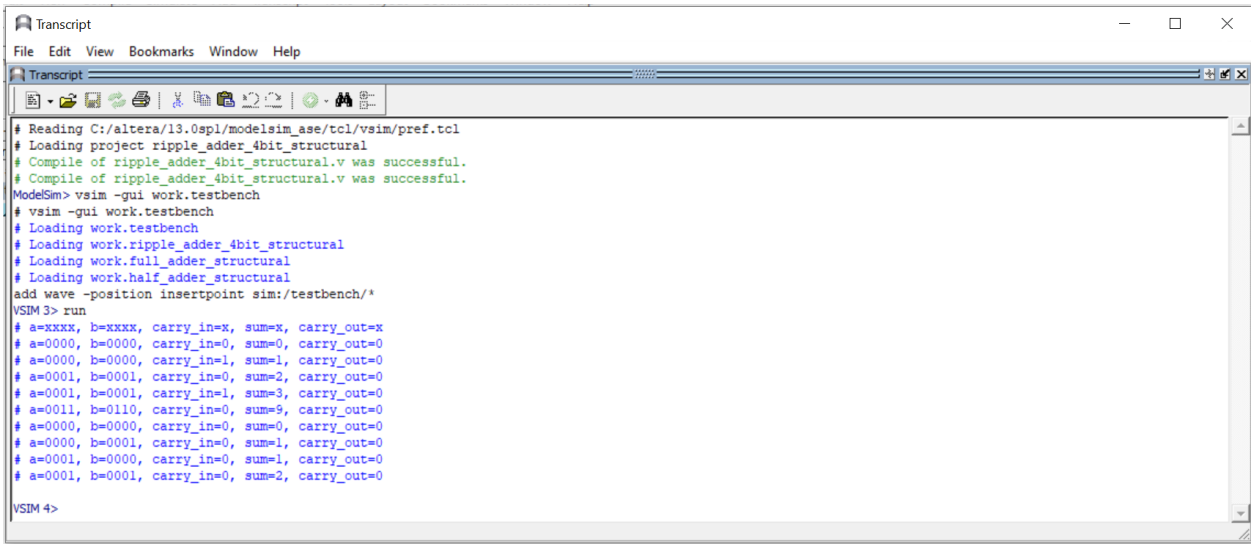


Reflection:

In the Verilog coding style of a 4-bit adder using behavioral, the statement is assigned together with the output variable carry_out and sum enclosed in a curly bracket. In the testbench, it uses a parameter for the condition to satisfy the 4-bit adder. As always it will initiate the variable within the two connecting modules.

ripple_adder_4bit_structural

Transcript:



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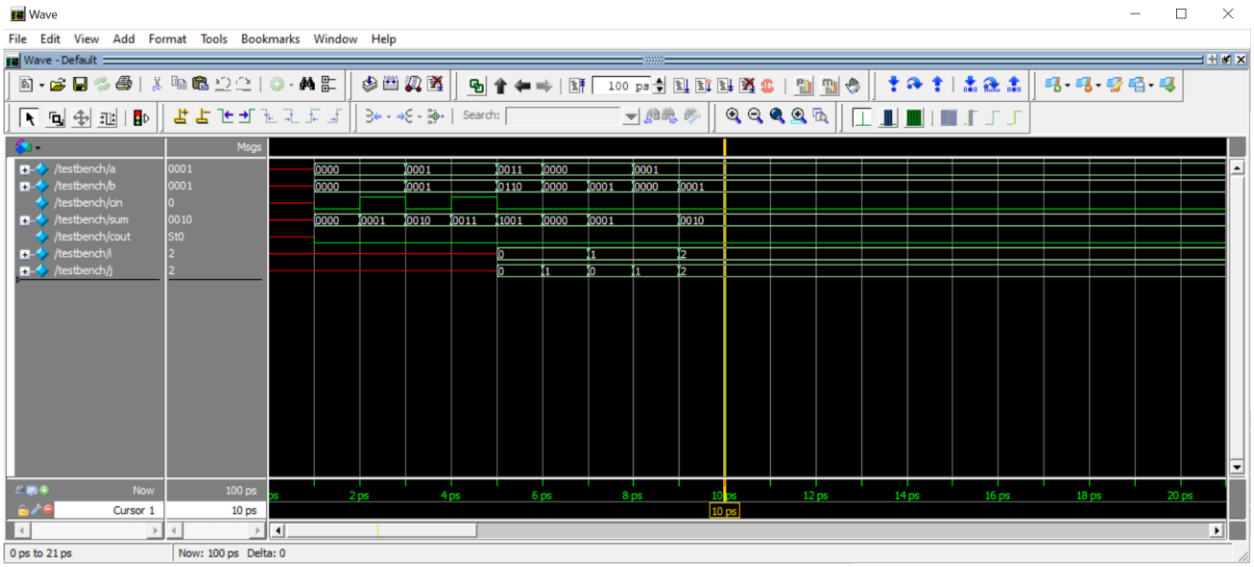
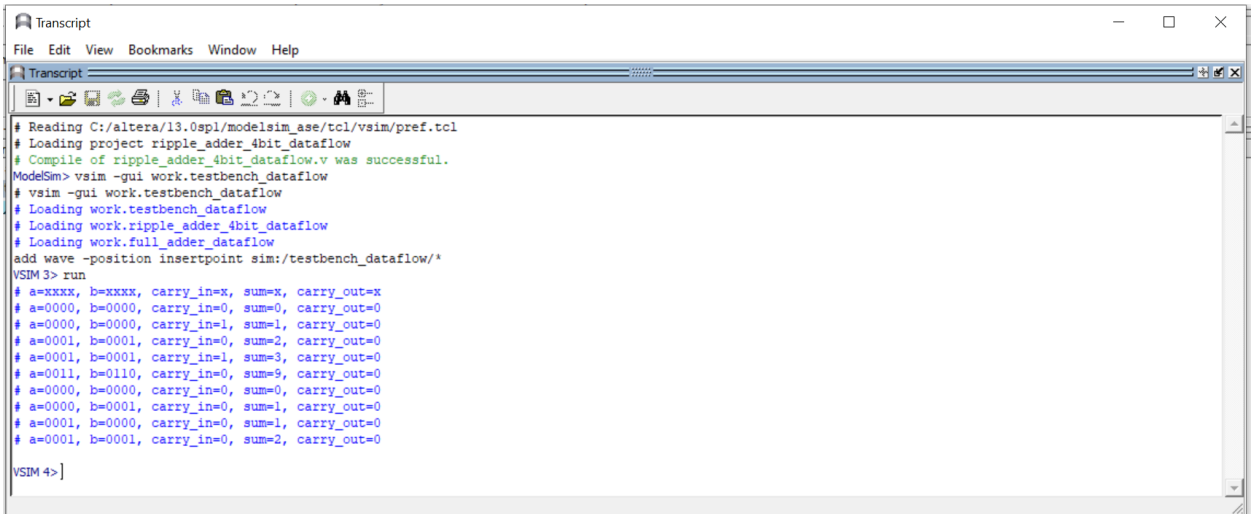


Reflection:

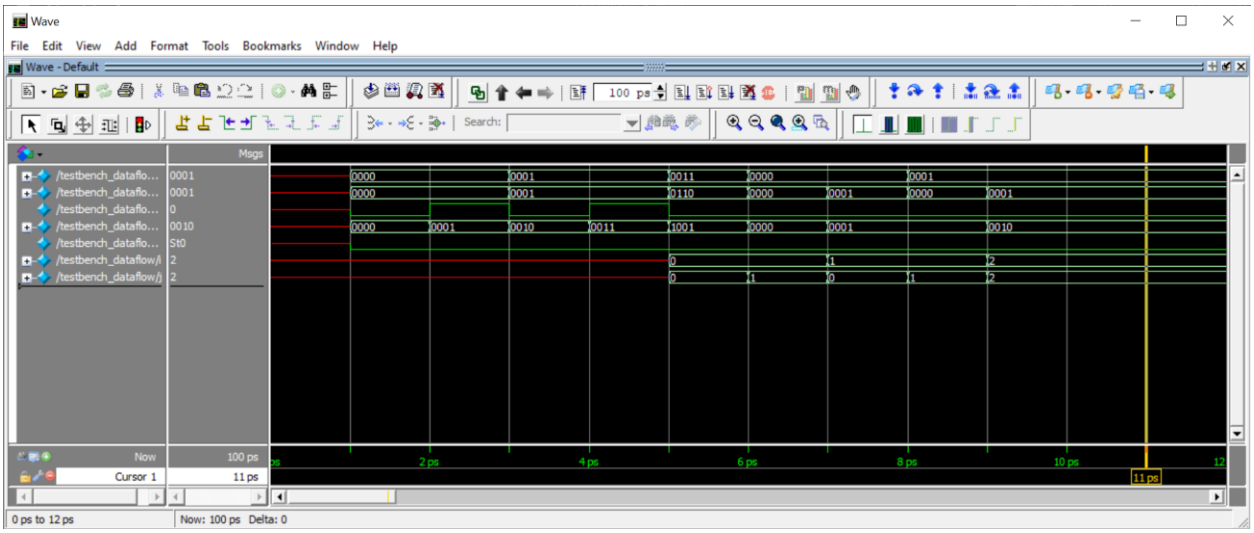
In the Verilog coding style of a 4-bit ripple adder using structural, it has 4 modules and it uses internal nets to connect those four. It also used a declaration and primitives to simulate the test bench. Within the testbench, the condition will satisfy to observe the effect in the module ports.

Ripple_adder_4bit_dataflow

Transcript:



Wave:



Reflection:

In a Verilog coding style using data flow, the wire output is assigned by the data flow style of the implement circuit in the modules. It also uses internal nets to connect four full adders using data flow. The data is transferred by the assigned value of the input to the wire/output variable.