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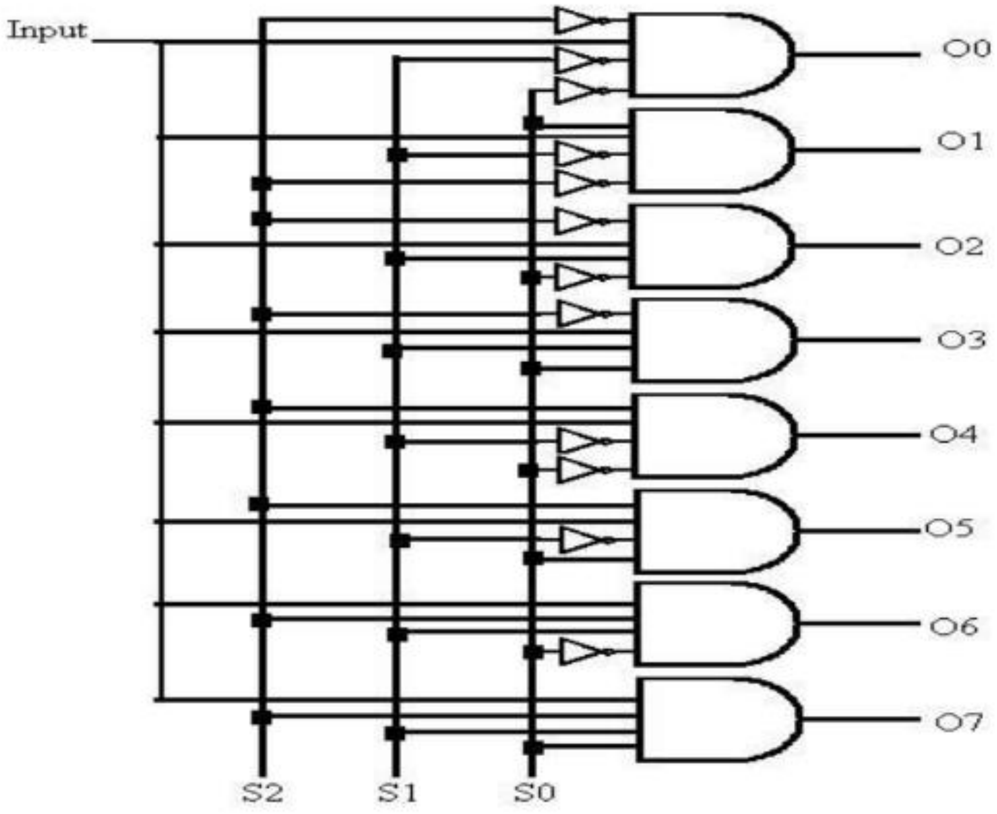
Course/Sec: BSCPE 3GF	Time/Day: 11:56 WEDNESDAY

Date Sub: NOVEMBER 16, 2022

III. LEARNING ACTIVITIES

A 1:8 de multiplexer is below. You may modify your previous codes.

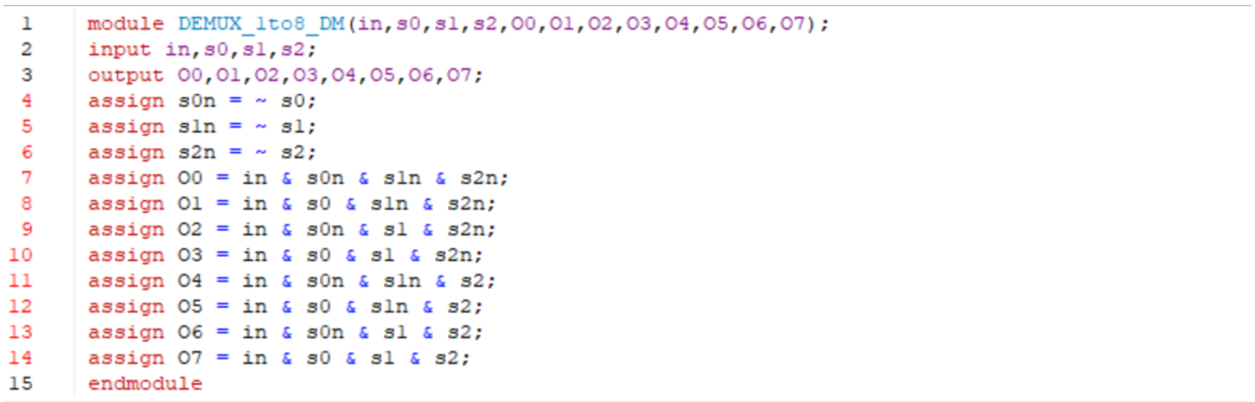


a. What is a demultiplexer?

A De multiplexer is a circuit that receives a single input signal and selects one of the multiple possible output routes to which to transmit the signal.

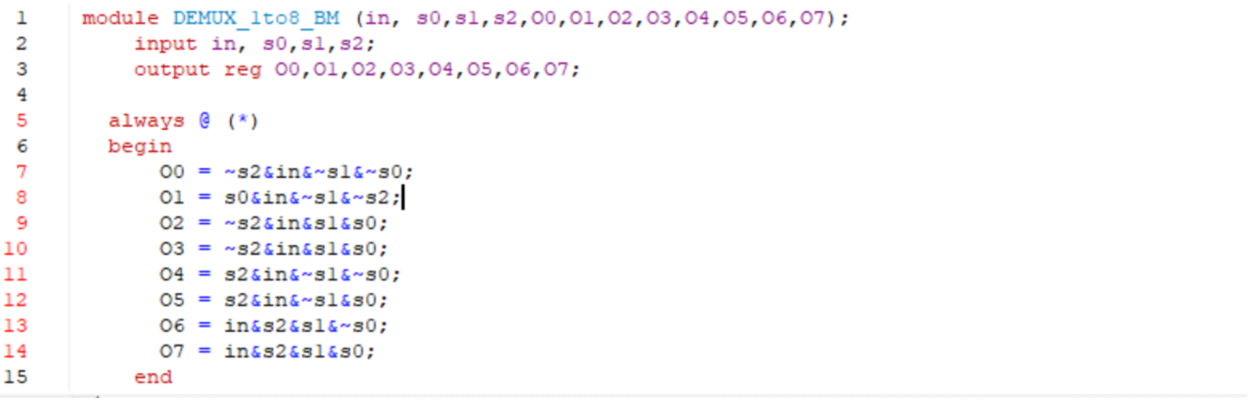
b. Create a Verilog code written in Data flow and behavioral modeling.

Data Flow Modeling



```
module DEMUX_1to8_DM(in,s0,s1,s2,O0,O1,O2,O3,O4,O5,O6,O7);
input in,s0,s1,s2;
output O0,O1,O2,O3,O4,O5,O6,O7;
assign s0n = ~ s0;
assign s1n = ~ s1;
assign s2n = ~ s2;
assign O0 = in & s0n & s1n & s2n;
assign O1 = in & s0 & s1n & s2n;
assign O2 = in & s0n & s1 & s2n;
assign O3 = in & s0 & s1 & s2n;
assign O4 = in & s0n & s1n & s2;
assign O5 = in & s0 & s1n & s2;
assign O6 = in & s0n & s1 & s2;
assign O7 = in & s0 & s1 & s2;
endmodule
```

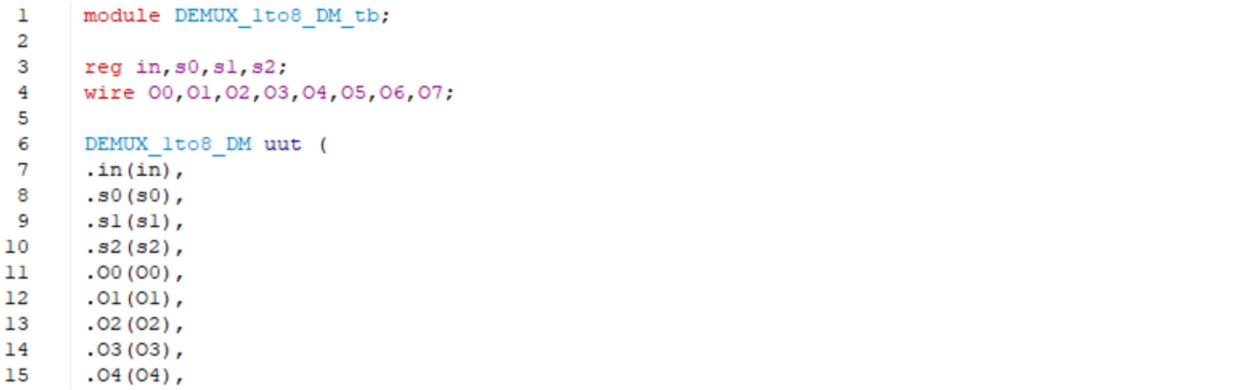
Behavioral Modeling

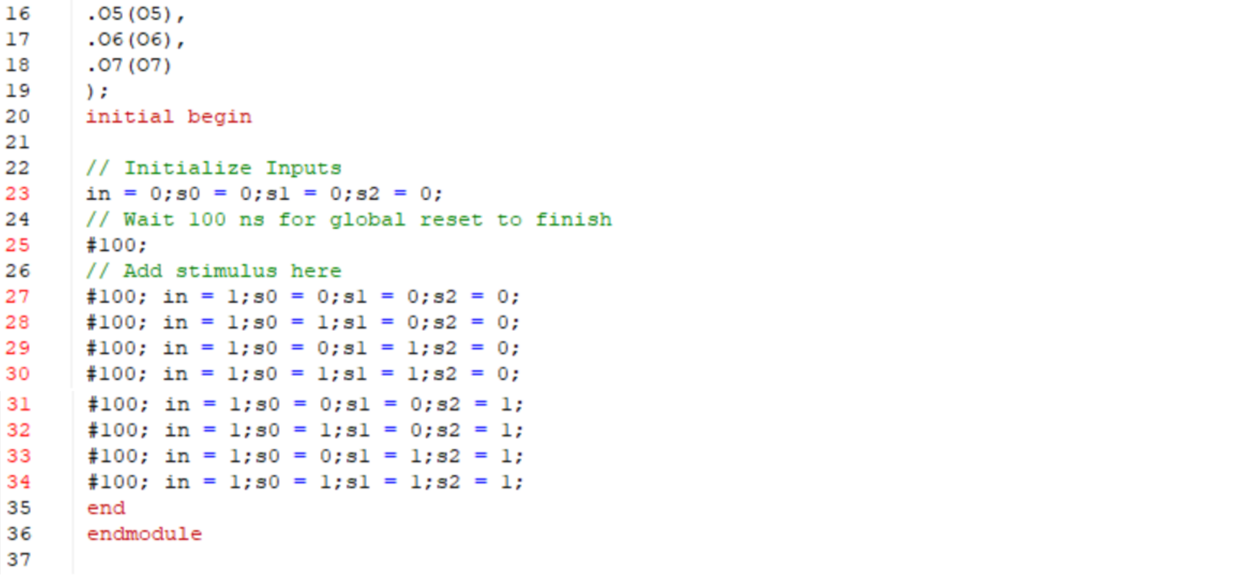


```
module DEMUX_1to8_BM (in, s0,s1,s2,O0,O1,O2,O3,O4,O5,O6,O7);
    input in, s0,s1,s2;
    output reg O0,O1,O2,O3,O4,O5,O6,O7;

  always @ (*)
  begin
      O0 = ~s2&in&~s1&~s0;
      O1 = s0&in&~s1&~s2;
      O2 = ~s2&in&s1&s0;
      O3 = ~s2&in&s1&s0;
      O4 = s2&in&~s1&~s0;
      O5 = s2&in&~s1&s0;
      O6 = in&s2&s1&~s0;
      O7 = in&s2&s1&s0;
    end
```

c. Provide a Test bench of the code.

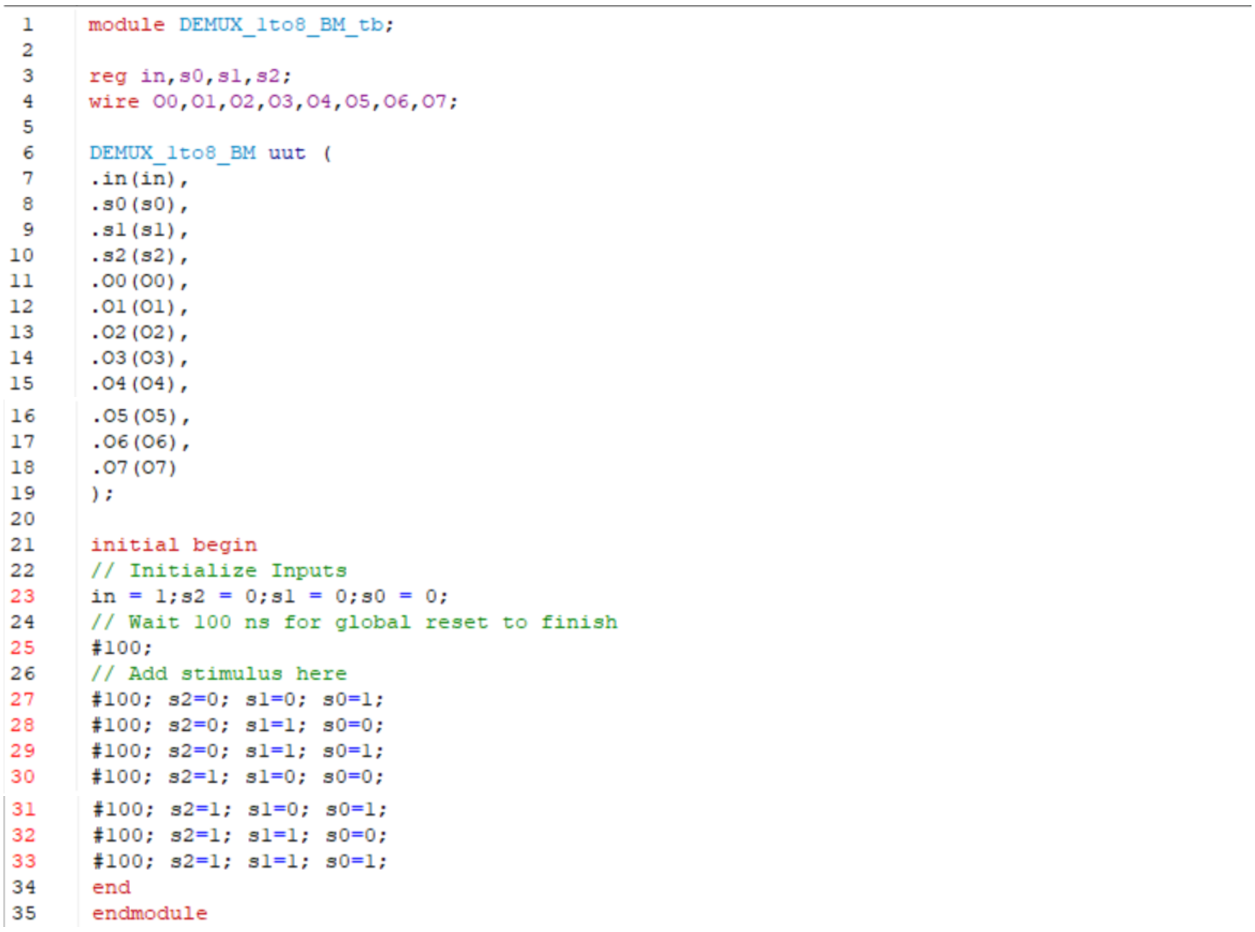
Data Flow Modeling





```
module DEMUX_1to8_DM_tb;

reg in,s0,s1,s2;
wire O0,O1,O2,O3,O4,O5,O6,O7;

DEMUX_1to8_DM uut (
.in(in),
.s0(s0),
.s1(s1),
.s2(s2),
.O0(O0),
.O1(O1),
.O2(O2),
.O3(O3),
.O4(O4),
.O5(O5),
.O6(O6),
.O7(O7)
);
initial begin

// Initialize Inputs
in = 0;s0 = 0;s1 = 0;s2 = 0;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
#100; in = 1;s0 = 0;s1 = 0;s2 = 0;
#100; in = 1;s0 = 1;s1 = 0;s2 = 0;
#100; in = 1;s0 = 0;s1 = 1;s2 = 0;
#100; in = 1;s0 = 1;s1 = 1;s2 = 0;
#100; in = 1;s0 = 0;s1 = 0;s2 = 1;
#100; in = 1;s0 = 1;s1 = 0;s2 = 1;
#100; in = 1;s0 = 0;s1 = 1;s2 = 1;
#100; in = 1;s0 = 1;s1 = 1;s2 = 1;
end
endmodule
```

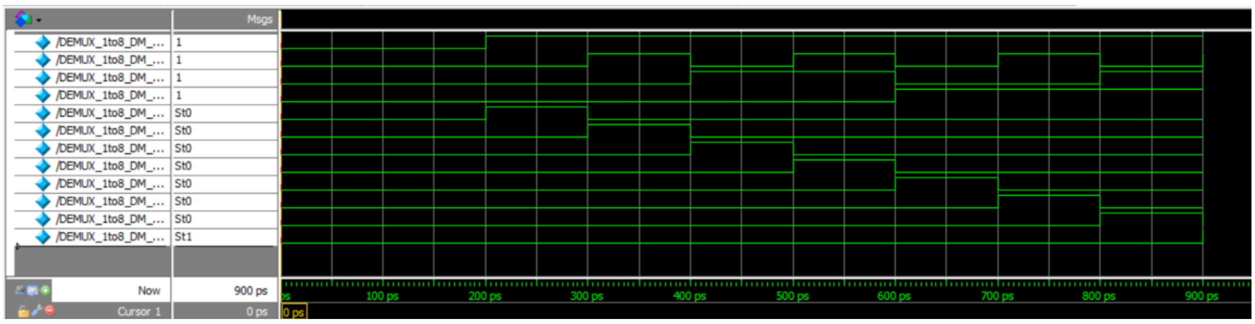
Behavioral Modeling



```
module DEMUX_1to8_BM_tb;

reg in,s0,s1,s2;
wire O0,O1,O2,O3,O4,O5,O6,O7;

DEMUX_1to8_BM uut (
.in(in),
.s0(s0),
.s1(s1),
.s2(s2),
.O0(O0),
.O1(O1),
.O2(O2),
.O3(O3),
.O4(O4),
.O5(O5),
.O6(O6),
.O7(O7)
);

initial begin
// Initialize Inputs
in = 1;s2 = 0;s1 = 0;s0 = 0;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
#100; s2=0; s1=0; s0=1;
#100; s2=0; s1=1; s0=0;
#100; s2=0; s1=1; s0=1;
#100; s2=1; s1=0; s0=0;
#100; s2=1; s1=0; s0=1;
#100; s2=1; s1=1; s0=0;
#100; s2=1; s1=1; s0=1;
end
endmodule
```

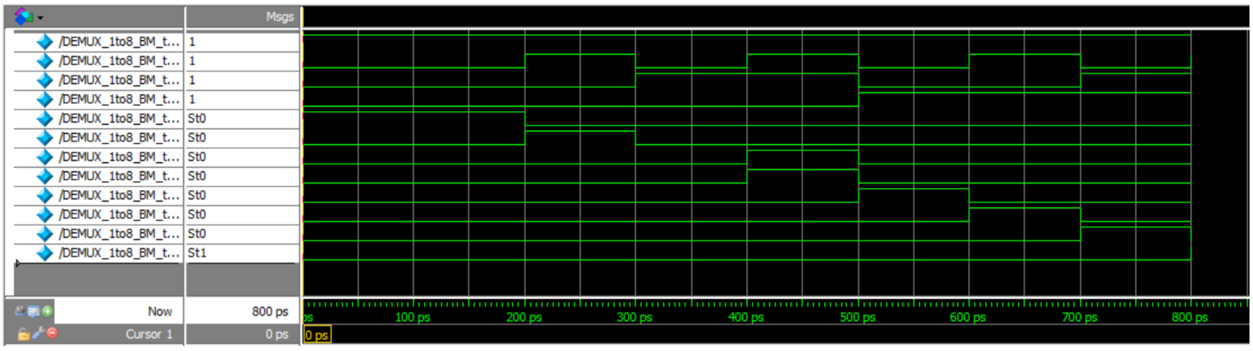
d. Provide simulation result of a waveform

Data Flow Modeling



	Msgs
/DEMUX_1to8_DM_...	1
/DEMUX_1to8_DM_...	1
/DEMUX_1to8_DM_...	1
/DEMUX_1to8_DM_...	1
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St0
/DEMUX_1to8_DM_...	St1
Now	900 ps
Cursor 1	0 ps

Behavioral Modeling



	Msgs
/DEMUX_1to8_BM_t...	1
/DEMUX_1to8_BM_t...	1
/DEMUX_1to8_BM_t...	1
/DEMUX_1to8_BM_t...	1
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St0
/DEMUX_1to8_BM_t...	St1
Now	800 ps
Cursor 1	0 ps