ECE 465: Digital System design

Summer 2021

Project 2: Sequence Detector

Due: July 26, 2021

A sequential circuit has two inputs (x1, x2) and one output (z). The output remains constant till one of the following input sequences occur:

a) Input sequence x1,x2 = 01, 11 causes the output to become 0
b) Input sequence x1,x2 = 10, 11 causes the output to become 1
c) Input sequence x1,x2 = 10, 01 causes the output to change value

Drive a Moore state graph for the circuit and implement it in Verilog and demonstrate the working using Modelsim based simulation.

Submission guidelines:

- Please use exactly the same port names as defined above (It helps us in grading!)
- Submit the compressed version of Quartus project on blackboard.
  - The Project should also have a waveform file that demonstrates the working of your design
- A lab report (in hard form) should be submitted in class. It should have the following contents:
  - Design description using a block diagram
  - Snapshots of the netlist viewer-based state machine, RTL schematic and simulations
  - Explanation of the simulation waveforms (You may want to add internal registers to the simulation waveform. For example, you can add state of the state-machine and counter value for better explanation).
  - Conclusion
  - Verilog/VHDL code (You can use smaller font size to reduce the number of pages)