

# MIPS reference card

<b>add</b>	rd, rs, rt	Add	rd = rs + rt	R 0 / 20	<b>registers</b> \$0 \$zero \$1 \$at \$2-\$3 \$v0-\$v1 \$4-\$7 \$a0-\$a3 \$8-\$15 \$t0-\$t7 \$16-\$23 \$s0-\$s7 \$24-\$25 \$t8-\$t9 \$26-\$27 \$k0-\$k1 \$28 \$gp \$29 \$sp \$30 \$fp \$31 \$ra hi — lo — PC — c0 \$13 c0_cause c0 \$14 c0_epc						
<b>sub</b>	rd, rs, rt	Subtract	rd = rs - rt	R 0 / 22							
<b>addi</b>	rt, rs, imm	Add Imm.	rt = rs + imm±	I 8							
<b>addu</b>	rd, rs, rt	Add Unsigned	rd = rs + rt	R 0 / 21							
<b>subu</b>	rd, rs, rt	Subtract Unsigned	rd = rs - rt	R 0 / 23							
<b>addiu</b>	rt, rs, imm	Add Imm. Unsigned	rt = rs + imm±	I 9							
<b>mult</b>	rs, rt	Multiply	{hi, lo} = rs * rt	R 0 / 18							
<b>div</b>	rs, rt	Divide	lo = rs / rt; hi = rs % rt	R 0 / 1a							
<b>multu</b>	rs, rt	Multiply Unsigned	{hi, lo} = rs * rt	R 0 / 19							
<b>divu</b>	rs, rt	Divide Unsigned	lo = rs / rt; hi = rs % rt	R 0 / 1b	<b>syscall codes for MARS/SPIM</b> 1 print integer 2 print float 3 print double 4 print string 5 read integer 6 read float 7 read double 8 read string 9 sbrk/alloc. mem. 10 exit 11 print character 12 read character 13 open file 14 read file 15 write to file 16 close file						
<b>mfhi</b>	rd	Move From Hi	rd = hi	R 0 / 10							
<b>mflo</b>	rd	Move From Lo	rd = lo	R 0 / 12							
<b>and</b>	rd, rs, rt	And	rd = rs & rt	R 0 / 24							
<b>or</b>	rd, rs, rt	Or	rd = rs   rt	R 0 / 25							
<b>nor</b>	rd, rs, rt	Nor	rd = ~(rs   rt)	R 0 / 27							
<b>xor</b>	rd, rs, rt	eXclusive Or	rd = rs ^ rt	R 0 / 26							
<b>andi</b>	rt, rs, imm	And Imm.	rt = rs & imm0	I c							
<b>ori</b>	rt, rs, imm	Or Imm.	rt = rs   imm0	I d							
<b>xori</b>	rt, rs, imm	eXclusive Or Imm.	rt = rs ^ imm0	I e							
<b>sll</b>	rd, rt, sh	Shift Left Logical	rd = rt << sh	R 0 / 0	<b>syscall codes for MARS/SPIM</b> 1 print integer 2 print float 3 print double 4 print string 5 read integer 6 read float 7 read double 8 read string 9 sbrk/alloc. mem. 10 exit 11 print character 12 read character 13 open file 14 read file 15 write to file 16 close file						
<b>srl</b>	rd, rt, sh	Shift Right Logical	rd = rt >> sh	R 0 / 2							
<b>sra</b>	rd, rt, sh	Shift Right Arithmetic	rd = rt >> sh	R 0 / 3							
<b>sllv</b>	rd, rt, rs	Shift Left Logical Variable	rd = rt << rs	R 0 / 4							
<b>srlv</b>	rd, rt, rs	Shift Right Logical Variable	rd = rt >> rs	R 0 / 6							
<b>srav</b>	rd, rt, rs	Shift Right Arithmetic Variable	rd = rt >> rs	R 0 / 7							
<b>slt</b>	rd, rs, rt	Set if Less Than	rd = rs < rt ? 1 : 0	R 0 / 2a							
<b>sltu</b>	rd, rs, rt	Set if Less Than Unsigned	rd = rs < rt ? 1 : 0	R 0 / 2b							
<b>slti</b>	rt, rs, imm	Set if Less Than Imm.	rt = rs < imm±? 1 : 0	I a							
<b>sltiu</b>	rt, rs, imm	Set if Less Than Imm. Unsigned	rt = rs < imm±? 1 : 0	I b							
<b>j</b>	addr	Jump	PC = PC&0xF0000000   (addr0<< 2)	J 2	<b>exception causes</b> 0 interrupt 1 TLB protection 2 TLB miss L/F 3 TLB miss S 4 bad address L/F 5 bad address S 6 bus error F 7 bus error L/S 8 syscall 9 break a reserved instr. b coproc. unusable c arith. overflow						
<b>jal</b>	addr	Jump And Link	\$ra = PC + 8; PC = PC&0xF0000000   (addr0<< 2)	J 3							
<b>jr</b>	rs	Jump Register	PC = rs	R 0 / 8							
<b>jalr</b>	rs	Jump And Link Register	\$ra = PC + 8; PC = rs	R 0 / 9							
<b>beq</b>	rt, rs, imm	Branch if Equal	if (rs == rt) PC += 4 + (imm±<< 2)	I 4							
<b>bne</b>	rt, rs, imm	Branch if Not Equal	if (rs != rt) PC += 4 + (imm±<< 2)	I 5							
<b>syscall</b>		System Call	c0_cause = 8 << 2; c0_epc = PC; PC = 0x80000080	R 0 / c							
<b>lui</b>	rt, imm	Load Upper Imm.	rt = imm << 16	I f							
<b>lb</b>	rt, imm(rs)	Load Byte	rt = SignExt(M1[rs + imm±])	I 20							
<b>lbu</b>	rt, imm(rs)	Load Byte Unsigned	rt = M1[rs + imm±] & 0xFF	I 24	<b>exception causes</b> 0 interrupt 1 TLB protection 2 TLB miss L/F 3 TLB miss S 4 bad address L/F 5 bad address S 6 bus error F 7 bus error L/S 8 syscall 9 break a reserved instr. b coproc. unusable c arith. overflow						
<b>lh</b>	rt, imm(rs)	Load Half	rt = SignExt(M2[rs + imm±])	I 21							
<b>lhu</b>	rt, imm(rs)	Load Half Unsigned	rt = M2[rs + imm±] & 0xFFFF	I 25							
<b>lw</b>	rt, imm(rs)	Load Word	rt = M4[rs + imm±]	I 23							
<b>sb</b>	rt, imm(rs)	Store Byte	M1[rs + imm±] = rt	I 28							
<b>sh</b>	rt, imm(rs)	Store Half	M2[rs + imm±] = rt	I 29							
<b>sw</b>	rt, imm(rs)	Store Word	M4[rs + imm±] = rt	I 2b							
<b>ll</b>	rt, imm(rs)	Load Linked	rt = M4[rs + imm±]	I 30							
<b>sc</b>	rt, imm(rs)	Store Conditional	M4[rs + imm±] = rt; rt = atomic ? 1 : 0	I 38							
<b>pseudo-instructions</b>											
<b>bge</b>	rx, ry, imm	Branch if Greater or Equal	<div><div>6 bits</div><div>5 bits</div><div>5 bits</div><div>5 bits</div><div>5 bits</div><div>6 bits</div></div> <table><tr><td>R</td><td>op</td><td>rs</td><td>rt</td><td>rd</td><td>sh</td><td>func</td></tr></table>	R	op	rs	rt	rd	sh	func	
R	op	rs		rt	rd	sh	func				
<b>bgt</b>	rx, ry, imm	Branch if Greater Than		<div><div>6 bits</div><div>5 bits</div><div>5 bits</div><div>16 bits</div></div> <table><tr><td>I</td><td>op</td><td>rs</td><td>rt</td><td>imm</td></tr></table>	I	op	rs	rt	imm		
I	op	rs			rt	imm					
<b>ble</b>	rx, ry, imm	Branch if Less or Equal									
<b>blt</b>	rx, ry, imm	Branch if Less Than									
<b>la</b>	rx, label	Load Address	<div><div>6 bits</div><div>26 bits</div></div> <table><tr><td>J</td><td>op</td><td>addr</td></tr></table>	J	op	addr					
J	op	addr									
<b>li</b>	rx, imm	Load Immediate									
<b>move</b>	rx, ry	Move register									
<b>nop</b>		No Operation									