ECEN 5613 | **Embedded System Design**
Lab #2 Signoff Sheet | **Fall 2019**

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 27, 2019 (Part 1 Elements) and Friday, October 4, 2019 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Nitik Gupta

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: Gupta

Signoff Checklist

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

Tanmay 9/28/2019
TA signature and date

Part 2 Required and Supplemental Elements

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☐ ~~74LS374 debug port functional~~ NO
- ☑ Understands timing analysis, setup/hold/propagation TALKED ABOUT IT, DECENT UNDERSTANDING
- ☑ MSP432 code build process, LED program, version control

10/4/19
TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY **Part 1 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Part 1 Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☑	☐	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐ ✓	☐	☐

FOR INSTRUCTOR USE ONLY **Part 2 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
SEE COMMENTS Schematics, SPLD code GOOD	☐	☐	– ☑	☐	☐
Hardware physical implementation	☐	☐	☐	✓ ☐	☐
Part 2 Required Elements functionality	☐	☐	☐	✓ ☐	☐
Supplemental Elements functionality	☒ ✓	☐	☐	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐	✓ ☐	☐
Overall Demo Quality (Part 2 Elements)	☐	☐	☐	✓ ☐	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.

* comments on next page

* directly connected $\overline{OE}$ and $\overline{PSEN}$.
* checking for time delay in main code LED
* made some calculation mistakes in delay calculation
* Data fetched has some bits different in logic analyzer

9/28/2019

PTZ

SCHEMATIC MISSING DECOUPLING, MAX232 WRONG
BOARD OK, SOME LONG WIRES + UNCLIPPED LEADS
KNOWS ~~[illegible]~~ SOME BASIC TIMING ANALYSIS
GOOD DEBOUNCE UNDERSTANDING
HAS GIT, COMMITS ONLY SHORTLY BEFORE SIGNOFF THOUGH