XIA LLC
31057 Genstar Rd.
Hayward CA 94544
Phone: (510) 401-5760
FAX: (510) 401-5761

Instruments that advance the art

User's Manual

Pixie-16 Trigger Board

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1. Introduction

The Pixie-16 Trigger (P16Trigger) board facilitates distribution of clock and trigger signals between Pixie-16 chassis. It connects to the rear of the backplane in the Pixie-16 chassis. The P16Trigger does not have any programmable logic and does not interface to the host computer; its mode of operation is configured by setting jumpers on the boards.

The P16Trigger hardware has two sections:

1. A *transmission* section which takes clock and trigger signals from the backplane of the clock/trigger master chassis and sends them out to all chassis in the system as LVDS signals on one or more CAT-5 cables. This section is only used in the director chassis that controls the triggers.
2. A *receiver* section which receives clock and trigger signals from CAT-5 cables and puts them on the chassis backplane for distribution to all modules. This section is used in all chassis.

Notes:

1. To minimize skew between chassis, the P16Trigger in the director chassis always acts as both a transmission board and a receiver board, i.e. one of the CAT-5 cables is looped back into the same board so that the director chassis receives trigger signals at the same time (same cable delay) as the other chassis.

2. Though nominally called transmission and receiver sections, it is possible to reverse the signaling direction. Each P16Trigger "receiver" section can thus send signals *to* the P16Trigger "transmission" section in the director chassis, which builds a logic OR of all signals and sends it to the Pixie-16 director chassis backplane.

2. Installation and Power

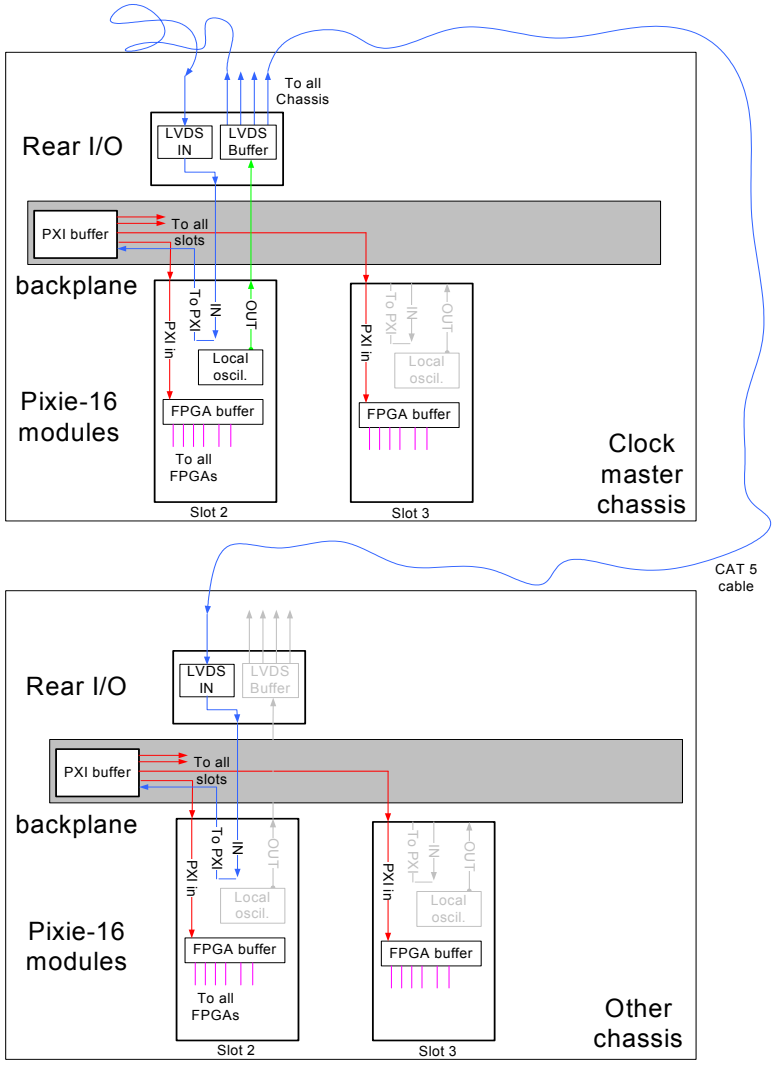
The Pixie-16 Trigger board plugs into the rear of the backplane in a Pixie-16 chassis. Currently only 14-slot chassis have the rear pins and the rear card cage required to connect to P16Trigger boards. Cables connected to the P16Trigger board can be brought out through the cutouts in the hinged door panel on the back of the chassis.

The P16Trigger board is powered from the chassis backplane and chassis power supply, but through a Pixie-16 module. Thus at least one Pixie-16 module has to be present in the same PXI bus segment at the P16Trigger board(s), preferably in the same slot.

For clock distribution purposes, the P16Trigger board should be inserted in the same slot on the rear backplane as the Pixie-16 acting as the chassis clock master (e.g. in PXI clock mode in rear slot 2 to be able to connect to a Pixie-16 in slot 2 that in turn connects to the PXI clock distribution path of the chassis).

3. Clock Distribution

The transmission section of the P16Trigger takes a clock signal from a local oscillator (or from the Pixie-16 module in the same slot), converts it into a LVDS signal, makes 8 copies, and send them out through 8 CAT-5 cables. The receiver section receives an LVDS clock signal from the CAT-5 input "IN A", converts it into a single ended signal, and sends it to the chassis clock master.



P16Trigger settings: On the P16Trigger director board, the clock source can be selected to be either a local oscillator or a clock signal from the Pixie-16 module in the same slot. This function is controller by Jumper JP1: set to "loc" for local clock and to "P16" for Pixie-16 clock

Pixie-16 settings: In multi-module systems with distributed clocks, the Pixie-16 modules will be operated either in PXI clock mode or in daisy-chained clock mode with one module (in slot 2 or the leftmost slot, respectively) configured as the chassis clock master and the other modules configured as clock slaves (see Pixie-16 user manual). In multi-chassis systems the clock slaves will be unchanged, but the chassis clock master will only repeat a clock signal it receives from the P16Trigger board. In addition, unless the local clock on the P16Trigger director board is used as the system master clock, one Pixie-16 will send its clock to the P16Trigger director for distribution:

PXI clock mode: The Pixie-16 module in slot 2 is the chassis clock master. It receives the clock signal from the P16Trigger board in rear slot 2 on the "left neighbor input". Therefore the shunts on J101 have to be set such that pins 4 and 6 as well as pins 1 and 3 are connected (sending the clock from 'left' to the PXI clock input on the backplane and using the PXI clock from the backplane for distribution on board).

The Pixie-16 module acting as the chassis clock master in the director chassis can also be the clock source for the system as a whole. To do so, connect additionally pins 8 and 10 on J101 to send this module's local clock signal to the P16Trigger module for distribution (and select "P16" for the P16Trigger module input with JP1).

Daisy-chain clock mode: The Pixie-16 module in the leftmost slot is the chassis clock master. It receives the clock signal from the P16Trigger board in the *same rear slot* on the "left neighbor input". Therefore the shunts on J101 have to be set such that pins 3 and 4 as well as pins 9 and 10 are connected (using the clock from 'left' for distribution on board and sending it out to the right). This mode will introduce a clock delay from module to module.

4. Trigger Distribution

4.1. Backplane Input -> LVDS Output Connections

The transmission section of the P16Trigger connects to the backplane with 6 nominal input lines in the J5 connector. The input lines are organized as 3 signal pairs: (A1, B1), (A2, B2), and (A3, B3). Each pair may be connected to 8 LVDS outputs "OUT0-7". By settings shunts on JP20 (JP40, JP60), line A can be connected to outputs OUT0-3, line B can be connected to outputs OUT4-7, or either line can be connected to all 8 outputs.

Function	Connect pins on JP20/40/60	Notes
line A to OUT0-3	2-3	
line A to OUT0-7	2-3, 4-5	
line B to OUT4-7	6-7	
line B to OUT0-7	6-7, 4-5	

One LVDS signal from each pair (plus a clock signal) is sent out in each of the 8 CAT-5 cables (to the local board's receiver section and up to 7 receivers in remote chassis). A single board can thus send out 3 independent signals to itself and 7 remote chassis or 6 independent signals to itself and 3 remote chassis. (If the director chassis contains two P16trigger boards, 6 independent signals can be sent to 7 remote chassis.)

4.2. LVDS Input -> Backplane Output Connections

The P16Trigger receiver section connects to one or two CAT-5 cables from the director chassis' transmission section; either 3 trigger signals from director lines A1-3 on "IN A" or 6 trigger signals from director lines A1-3 and B1-3 on "IN A" and "IN B". (Only "IN A" carries the clock signal, so use of "IN B" alone is not recommended.

These 6 LVDS trigger signals are converted into CMOS logic signals and connected to the backplane on 6 nominal output lines in the either the J4 or the J5 connector. In XIA's 14-slot PXI chassis, output lines in J4 connect to all slots, output lines in J5 only connect to the slots of the same PXI segment (slots 1-7 or 8-14). To select J4 or J5 outputs, set Jumpers JP100-105 to "J4" or "J5"

4.3. Reverse Signaling

In reverse signaling mode, each P16Trigger "receiver" section can send signals *to* the P16Trigger "transmission" section in the director chassis, which builds a logic OR of all signals and sends it to the Pixie-16 director chassis backplane. To put a pair of trigger signals in this mode, set JP21 (41, 61) to "reverse" and on JP20 (40, 60) connect pins 1-2 and 7-8.

5. Summary of Jumper Settings

Jumper	Function	Default	MSU DDAS
JP1	select clock source local ("loc") or from Pixie-16 in front slot ("P16")	"loc"	"loc"
JP20/40/60	select source A, B or both for outputs 0-7	2-3, 6-7	JP20/40: 2-3, 6-7 JP60: 1-2, 7-8
JP100-105	select output to J4 or J5	"J4"	all "J4"
JP21/41/61	select normal or reverse signaling	"normal"	JP21/41: "normal" JP61: "reverse"