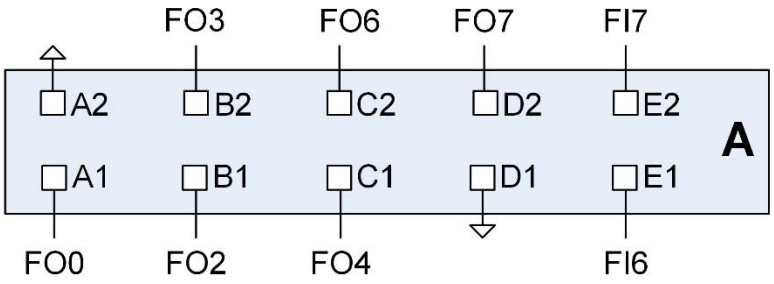
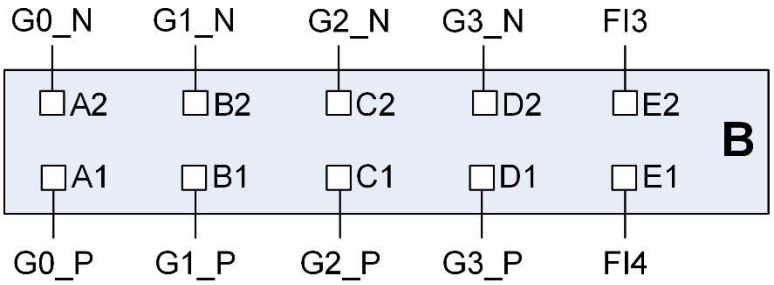
Pixie-16 PKU Custom Firmware Setup Guide

Multiplicity triggers M1 and M2 are generated for selected channels among 1-3 modules. M1 and M2 are outputted to external units through front panel connector A: M1 is connected to pin C2 (FO6) and M2 is connected to pin D2 (FO7), respectively.



Multiplicity triggers M1 and M2 are corresponding to ChanTrig0 and ChanTrig1, respectively. ChanTrig0 and ChanTrig1 are described in document “Pixie-16-ChanValidationTrigIllustration.pdf” (page 5). The different ways to generate ChanTrig0 and ChanTrig1 are also described in the same document.

With the help of external logic modules, M1/M2 for more channels can be configured. In addition, triggers from other detectors can also be included to make the external trigger. After the external trigger is generated in external logic modules, it is sent to the pin E1 (FI4) of front panel connector B.



More information about front panel test pins

1. Front panel connectors and ports

a. Front panel LVDS I/O port

Figure 1 shows the layout of the front panel LVDS I/O port (J101). This port can be configured to either input or output 4 differential pair LVDS signals. Each pair consists of two complementary signals with the annotation of ”p” and ”n”, respectively. Please note that pins #3 and #6 form one LVDS pair even though they are not neighboring pins. Pins #9 and #10 are both connected to ground.

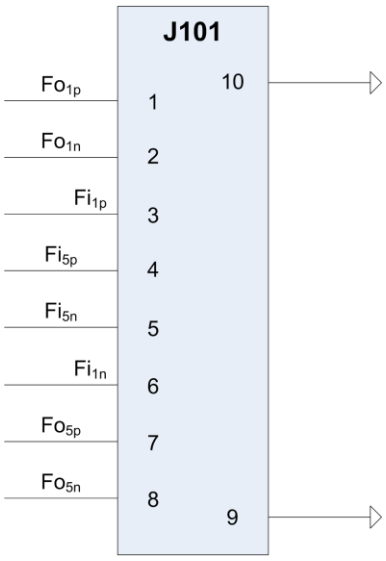


Figure 1: Layout of Pixie-16 front panel LVDS I/O port (J101).

b. Front panel test outputs

To aid system setup by a user or for debugging purpose, Pixie-16 provides up to six test output pins through the front panel connector J155 (labeled with red letter "**A**" on the front panel). This connector is the har-link® connector from HARTING.

These test pins can be connected to various internal signals of the Pixie-16 to provide insight of the current status of the system. **Figure 2** shows the layout of these test pins. Pins A1, B1, B2, C1, C2, and D2 are six test pins. Pins A2 and D1 are connected to ground. Pins E1 and E2 are connected to single-ended TTL external input signals, FI6 and FI7, respectively.

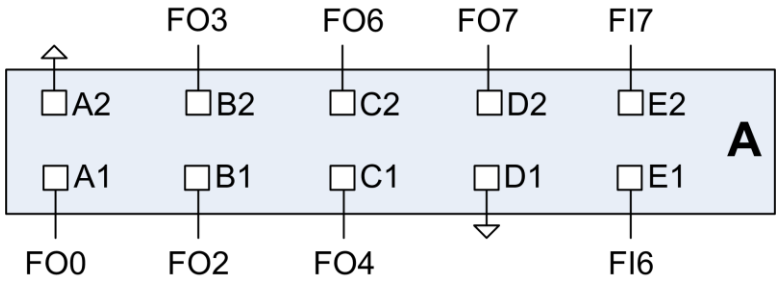


Figure 2: Layout of Pixie-16 front panel 3.3V I/O port (J200).

c. Front panel gate inputs

The next four har-link® connectors on the Pixie-16 front panel are J151 – J154 and labeled with red letters "**B**", "**C**", "**D**", and "**E**", respectively. They are "Gate Inputs" of the Pixie-16 module and can be used to accept gate signals for each of the 16 channels of a Pixie-16 module as well as a module gate signal, which applies to all 16 channels. **Figure 3** shows the layout of the front panel gate inputs on these connectors. All gate signals are differential LVDS signals. Gx_P and Gx_N (x=0, 1, ..., 15) form one differential pair for the gate input for Channel #x. MG_P and MG_N form the differential pair for the module gate input. The differential pair formed by SG_P and SG_N is not in use currently.

J151 ("**B**") and J152 (("**C**") can also accept 4 single-ended TTL external input signals, FI0, FI2, FI3 and FI4, respectively.

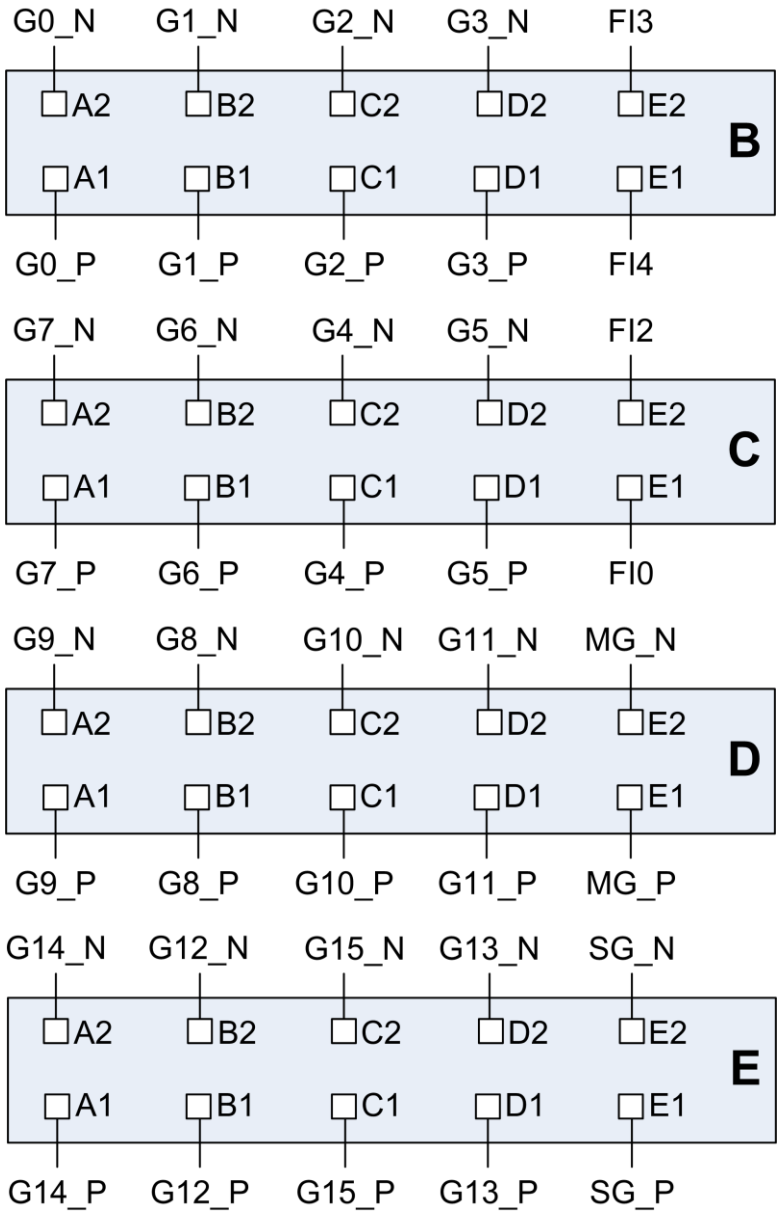


Figure 3: Layout of Pixie-16 front panel gate inputs and external signal inputs.

2. Output of test signals to front panel connector A

DAQ parameter TrigConfig0 is mainly used to configure the test signal outputs to the Pixie-16 front panel Test Header "A" (J200). Bits [14:12] are used to select the group of 4 test signals from the signal processing FPGA (more detailed explanation of these test signals are shown below). Bit 15 is used to enable or disable the output of test signals to J200 from the System FPGA, while bits [19:16] are used to select which channel's group of 4 test signals are output to the first 4 test pins (FO0, FO2, FO3, FO4) of J200 test header.

Value of Bits [14:12] of TrigConfig0	Selected Test Signals from the Signal Processing FPGA
0	FTRIG_DELAY, FTRIG_VAL, GLBETRIG_CE, CHANETRIG_CE
1	FTRIG_DELAY, VETO_CE, LDPMFULL, SDPMFULL
7 - 2	FTRIG_DELAY, FTRIG_VAL, GLBETRIG_CE, CHANETRIG_CE

Value of Bit [15] of TrigConfig0	Value & Description
0	Disable System FPGA to send test signals to Test Header "A" (J200)
1	Enable System FPGA to send test signals to Test Header "A" (J200)

Value of Bits [19:16] of TrigConfig0	Selected Test Signals from the Signal Processing FPGA
0	Test signals from Channel #0
1	Test signals from Channel #1
2	Test signals from Channel #2
…	...
15	Test signals from Channel #15

Definition of Test Signals from the Signal Processing FPGA

Pin Number	PIN Name	Signal Name	Description
A1	Fo_0	FTRIG_DELAY	Delayed local fast trigger
B1	Fo_2	FTRIG_VAL	Validated, delayed local fast trigger
B2	Fo_3	GLBETRIG_CE	Stretched global validation trigger
C1	Fo_4	CHANETRIG_CE	Stretched channel validation trigger
A1	Fo_0	FTRIG_DELAY	Delayed local fast trigger
B1	Fo_2	VETO_CE	Stretched veto signal
B2	Fo_3	LDPMFULL	Module's data memory full signal
C1	Fo_4	SDPMFULL	System-wide data memory full signal