Semiconductor Devices
Lab Session Report:
Metal Oxide Semiconductor Field Effect Transistor
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31/12/2023

Introduction :

This lab session aims to demonstrate MOSFET properties through software, enhancing our understanding of semiconductor devices' efficiency and quality for improved interpretation.

I. Preparation

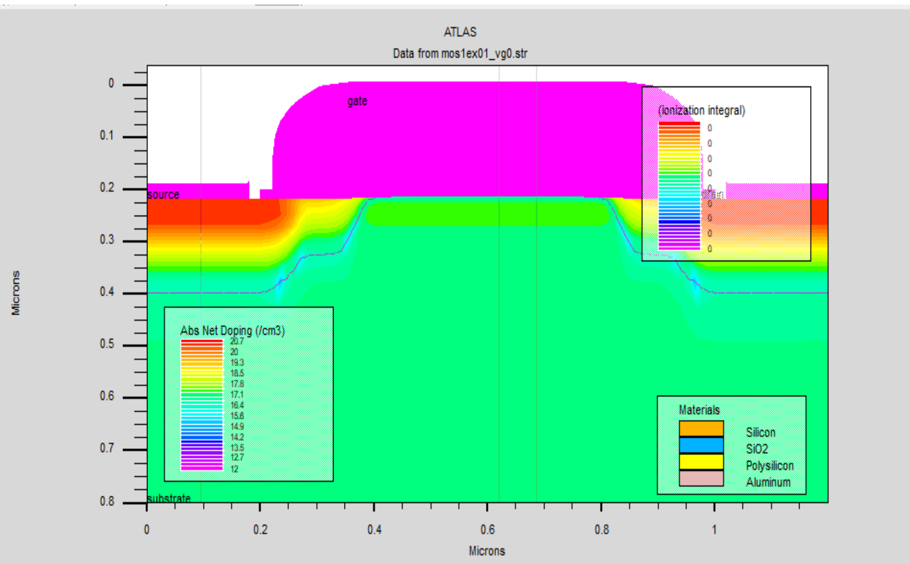

Figure 1: doping view of the transistor

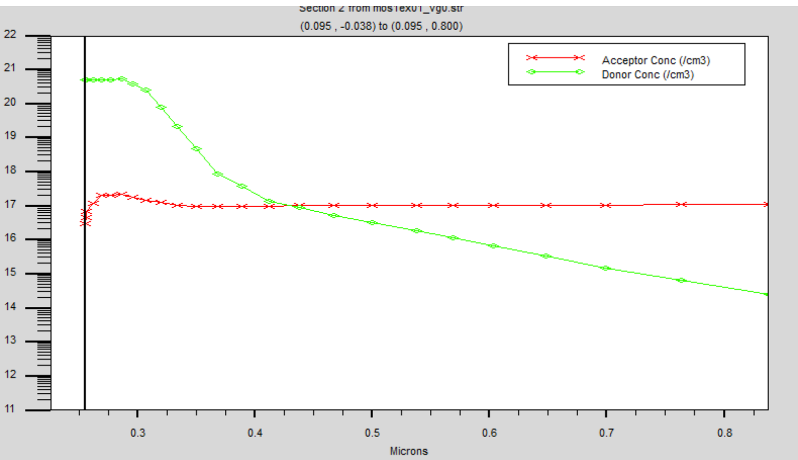

Figure 2: doping concentratration under source

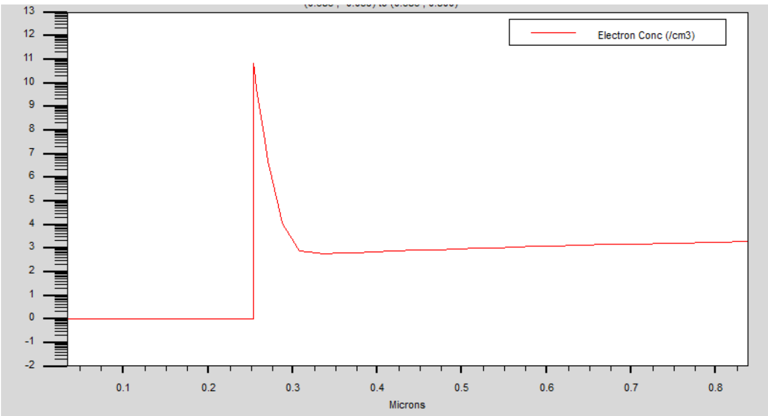

Figure 3: electron concentration for Vg=0V

1. For an N-Channel MOSFET

The gate doping is P-type (on the figure below we notice that the fermi level is close to the valence band
the drain and source doping is N-type

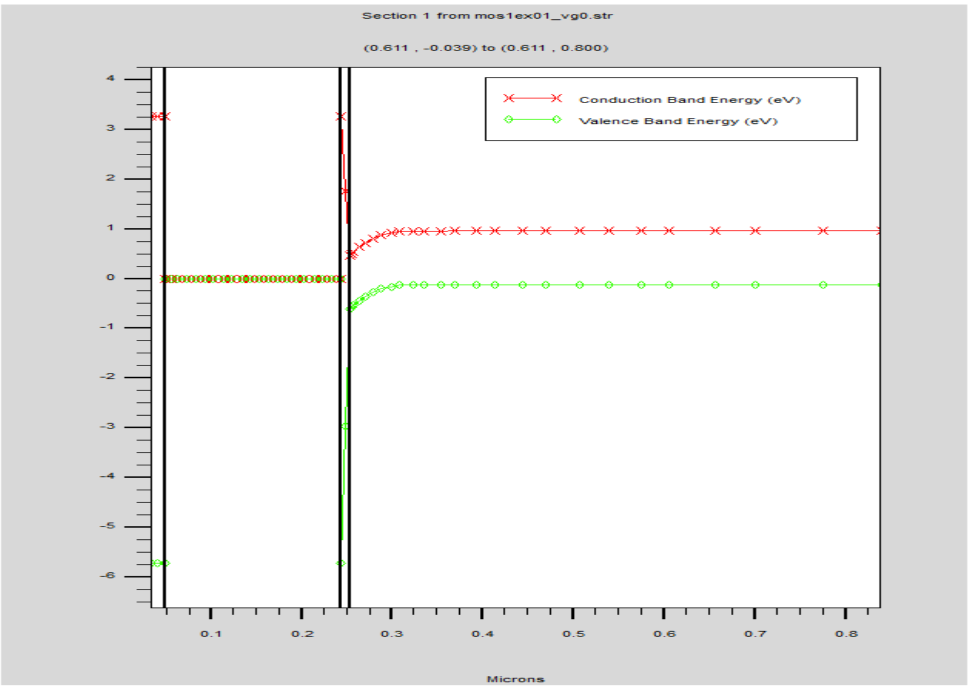

Figure 4: energy band diagram

2. For the Silicon
electron affinity is : 4.17eV
Work function of the polysilicon is : 6eV
3. The flatband voltage is
Vfb = electron affinity(Si) - Work function(SC)
Vfb= -173meV
The threshold voltage
Vth= 0.38V

II.Simulation

1.the curve bellow (figure 5) show a Vth of 0.5 V
V th theorically is 0.38

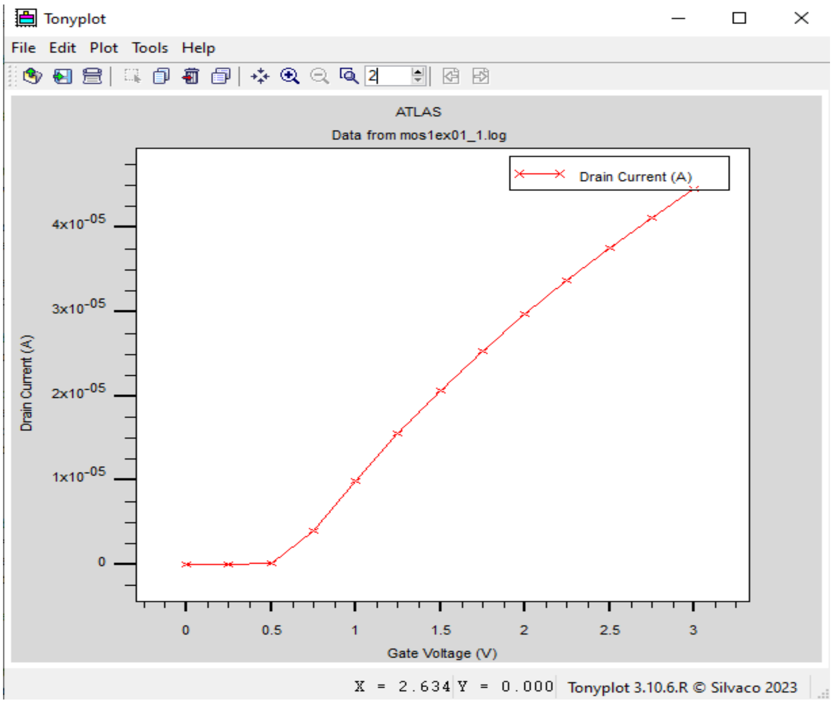

Figure 5: electrical characteristic

2.Plots (see figure 3 for electron ceoncentration at Vg=0V)

Here at Vg =3V the electron concentration has been highly increased

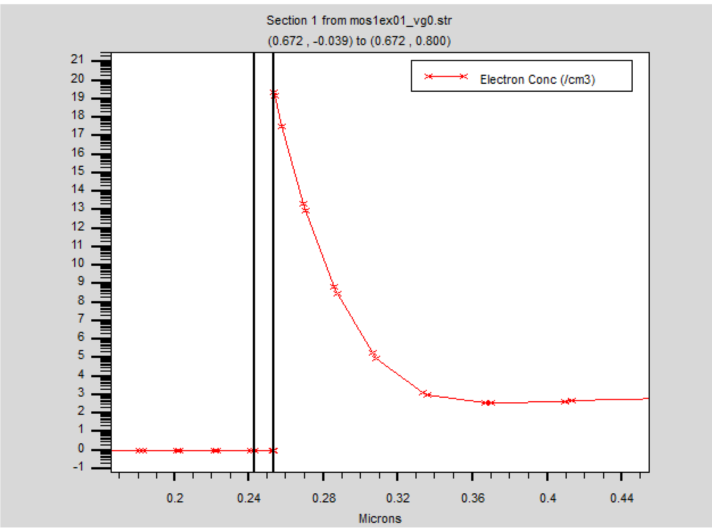

Figure 6: electron concentration for Vg= 3V

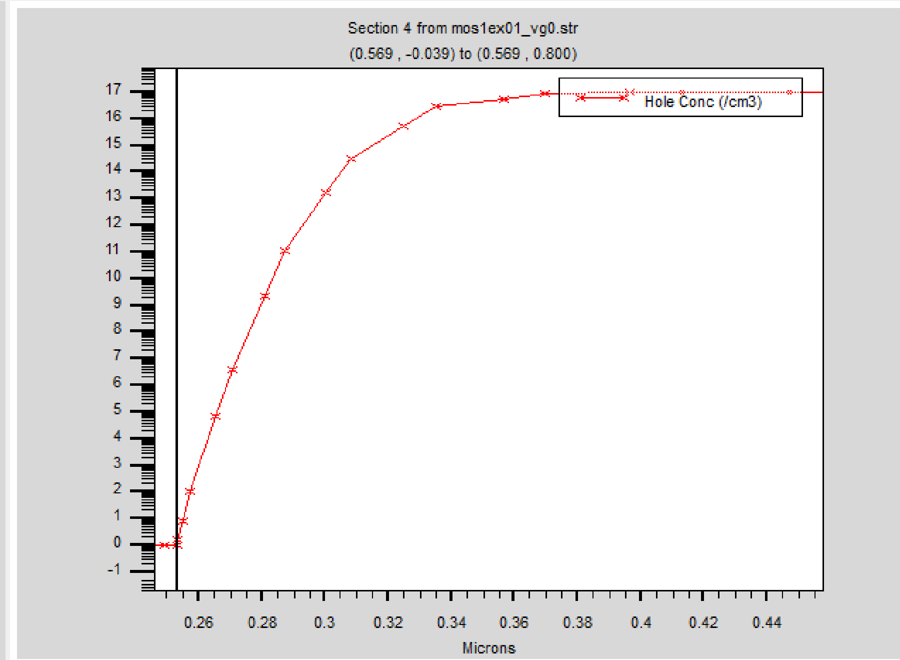

Figure 7: hole concentration

the slope is due to the depletion region from 0.24 to 0.36

III.SIMULATION

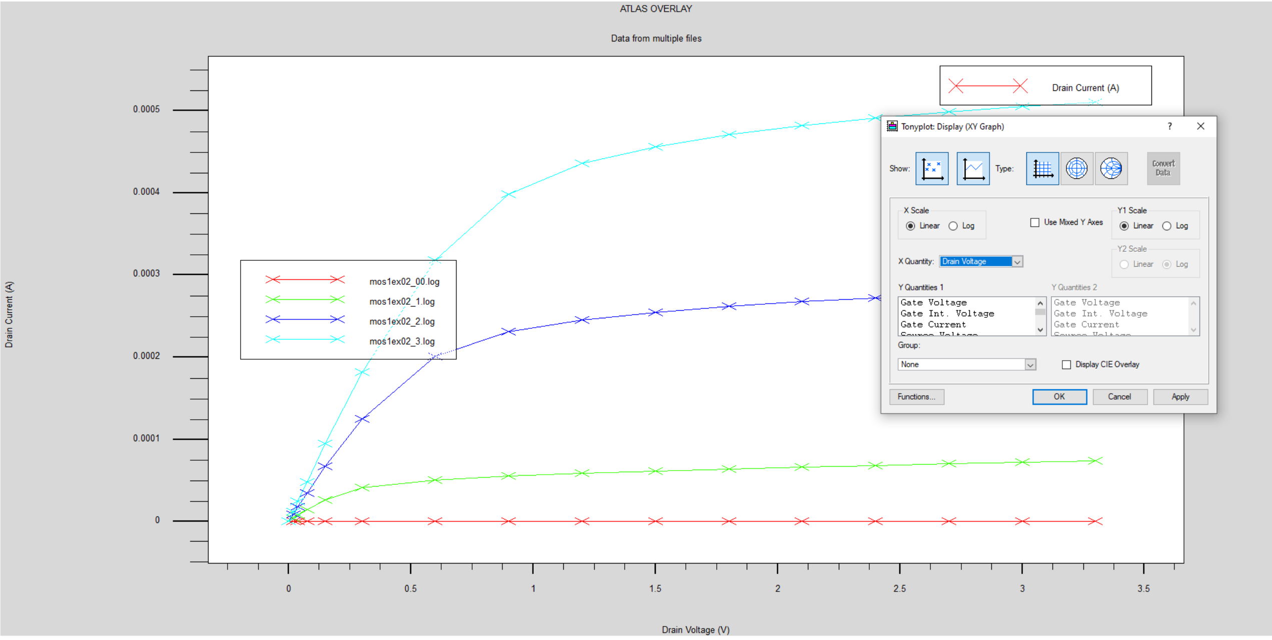

Figure 8: electrical charateristic Id(Vd,Vg) for different Vg

1. Determination of the maximum current density

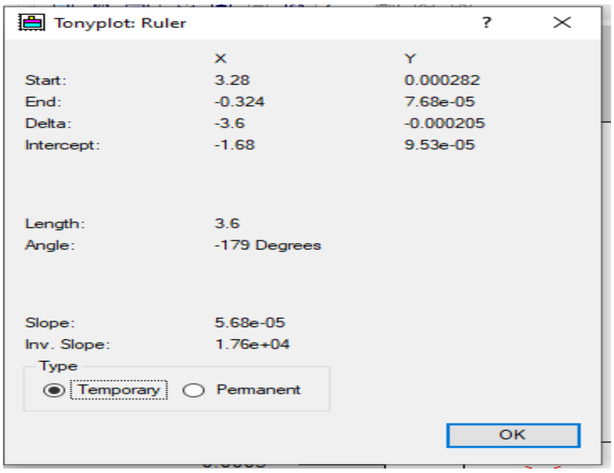

Figure 9: current density and transconductance determination

The max current density has been evaluated for 0.5 uA/um (see figure

2. The transconductance

$$g=\frac{\Delta Id}{\Delta Vgs}=\frac{0.2\,mA}{1.1\,V}=0.181\,mS$$

IV.Extraction of the subtreshold slope

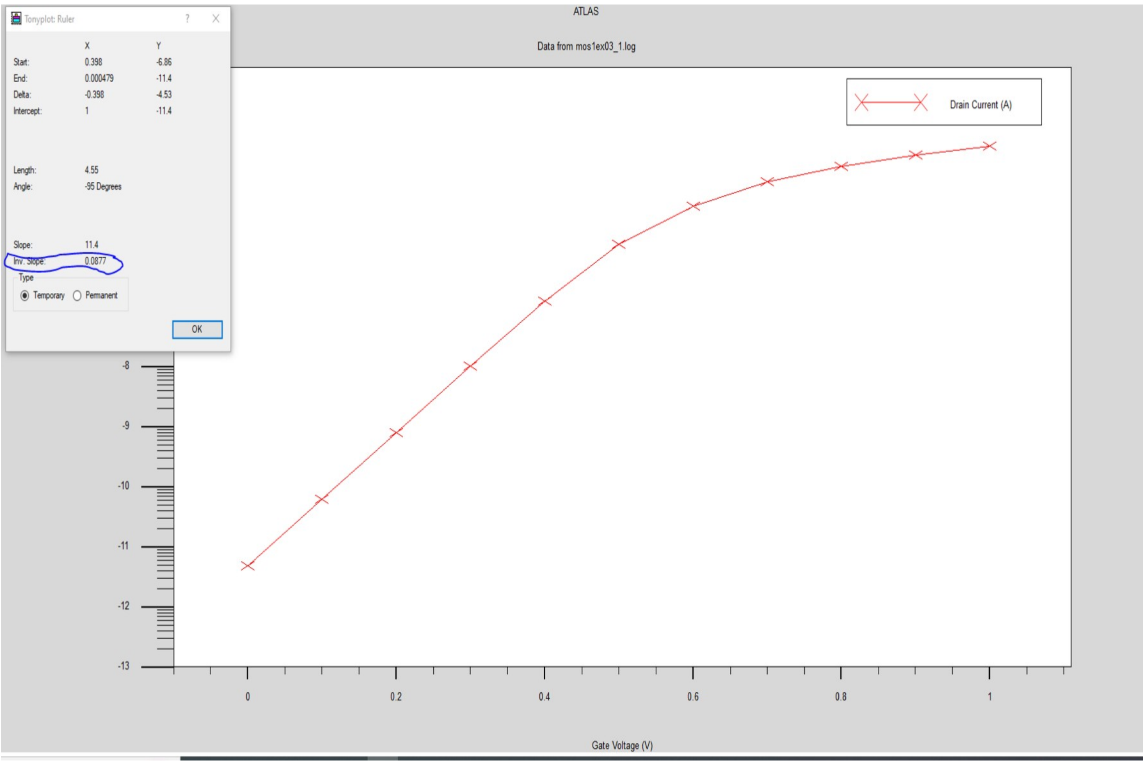

Figure 10: subtreshold slope deduction

a. From the previous figure we deduced that the slope is 0.087 with the ruler
b. the Drain Induced Barrier Lowering (DIBL)

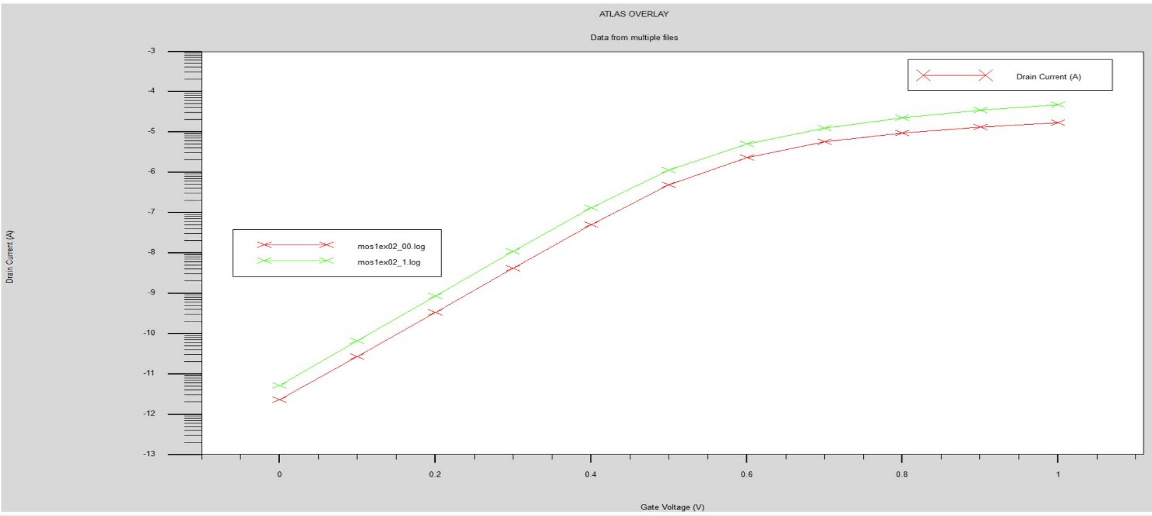

Figure 11: Drain Induced Barrier Lowering deduction

$$DIBL=\frac{0.5\,mA}{1.01\,V}=50\,mA/V$$

Conclusion :

The lab session employing Silvaco software proved instrumental in comprehensively exploring MOSFET characteristics. Through analysis of polarization, current density, transconductance, subthreshold slope, and the Drain Induced Barrier Lowering (DIBL) , we gained valuable insights into the intricate behaviors and performance metrics of MOSFETs. This hands-on experience illuminated the critical factors influencing their operation, contributing significantly to our understanding of semiconductor device behavior and potential optimizations for future applications.