Chapter 19: Logic circuits and Boolean algebra: Answers to coursebook

Exam-style Questions

1 a i 1 mark for any of the following and 2 marks for all three: OR (1), AND (1) and NOT (1).

ii Examination of the circuit shows that the R output comes directly from an AND gate fed by A and B as inputs. This allows the column for R to be completed without considering intermediate points.

The S output needs an intermediate after the OR gate (X), one after the AND gate (Y), which is a copy of the R output, and one after the NOT gate (Z). The truth table is as follows. 1 mark for each correct new column:

Inputs		Intermediate points			Outputs	
A	B	X	Y	Z	S	R
0	0	0	0	1	0	0
0	1	1	0	1	1	0
1	0	1	0	1	1	0
1	1	1	1	0	0	1

b 1 mark each for any of the following up to a maximum of 3: A combinational circuit (1), a half-adder (1), S is the sum (1) and R is the carry (1).

2 a i 1 mark each for any of the following up to a maximum of 3: $\overline{A}.\overline{B} + A.\overline{B} + A.B$

ii One option must be A. Note that $A.\overline{B} + A.B$ can be easily converted to A because $(\overline{B} + B) = 1$. (2)

b i A.B (2)

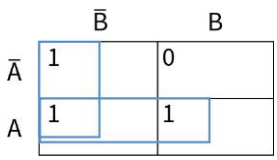
ii Using sum of products gives $A.\overline{B} + A.B + \overline{A}.B$ (3)

iii NOT gate inverts, inversion of a sum gives a product of the inverses which in this case are inverses of products, so becoming sums. The result is:

$(\overline{A} + B).(\overline{A} + \overline{B}).(A + \overline{B})$

Multiplying this out gives many terms equal to zero and leaves just $\overline{A}.\overline{B}$. Note that there is of course a shortcut which starts with A + B for OR, and which inverted gives the same answer (4)

3 a i 2 marks for the correct matrix, 2 marks for each pair of correct cell values: This is the Karnaugh map with the groups of 1 identified.



ii $A + \overline{B}$ (3)

b i $\overline{A}.\overline{B} + A.\overline{B} + A.B$ (3)

ii To convert this, add a second $A.\overline{B}$. Then combine $A.\overline{B} + A.B$ to produce A and $\overline{A}.\overline{B} + A.\overline{B}$ to get $\overline{B}$ (4)

4 This is Question 5 in 9608 Paper 31 June 2016. At the time of writing the published mark scheme is available on the Cambridge International School Support Hub (requires registration). The Examiners Report for the June 2016 series is also available there and this may contain comments specific to this question.

The following are what the author of this chapter in the Teacher Resource would suggest as reasonable answers with alternatives suggested where appropriate.

a

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

b i

S	R	Q	$\overline{Q}$
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

ii The S = 0 and R = 0 combination

This combination produces a 1 for both outputs. The outputs are supposed to be different. This combination of outputs would result in an unstable state.

c **i** A clock pulse

ii Any combination of inputs produces two different outputs. An unstable state cannot occur. Although not needed learners can mention that two 1 inputs toggle the output values.

d A flip-flop can achieve a stable state and this state can be toggled by an appropriate input. This means that it can act as a memory component storing a value for 1 bit.

Cambridge International AS & A Level Computer Science 9608 paper 31 Q5 June 2016

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The following are what the author of this chapter in the Teacher Resource would suggest as reasonable answers with alternatives suggested where appropriate.

a **i** It should be noted that the half-adder shown in the diagram has the outputs reversed from the normal presentation. It is normal to show the sum top right and the carry bottom right. This is also true for the full adder circuit. However, this does not affect the answers for the different parts of this question.

The following shows the answers for the J and K outputs plus a suggestion as to how the working space might be used.

P	Q	R		A1		X2	A2	B2		J	K
0	0	0		0		0	0	0		0	0
0	0	1		0		0	0	1		0	1
0	1	0		0		1	0	1		0	1
0	1	1		0		1	1	0		1	0
1	0	0		0		1	0	1		0	1
1	0	1		0		1	1	0		1	0
1	1	0		1		0	0	0		1	0
1	1	1		1		0	0	1		1	1

Here the column headed A1 is the output from the first half adder. X2 is the input to the second half adder and A2 and B2 are the outputs from it. B2 is then the K output and the J output is produced by the OR operation on A1 and A2.

ii A full adder

iii J is the carry output and K is the sum output.

If an addition involves two 1 bits there is a carry and the sum is zero. If there is only one 1 bit in the three bits there is no carry. If there is an odd number of 1 bits the sum is 1.

b **i** A . (A + B) . C

Brackets might be included through the method used to interpret the circuit. The result would be presented as A . ((A + B) . C). This is still a correct answer. Brackets are sometimes necessary but also often useful in aiding understanding or reading of an expression even if they are not essential.

ii Assuming a starting point of A . (A + B) . C, the first step could be multiplying by A or by C. If the expression with the extra pair of brackets is used the multiplication by C has to be first.

So, (A + B) . C becomes A.C + B.C then this has to be multiplied by A which gives:

A . A . C + A . B. C

The next stages are not immediately obvious because having removed a brackets a different one has to be created.

A . A = A so we have A . C (1 + B)

Because 1 + B = 1 we get the final answer A . C

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