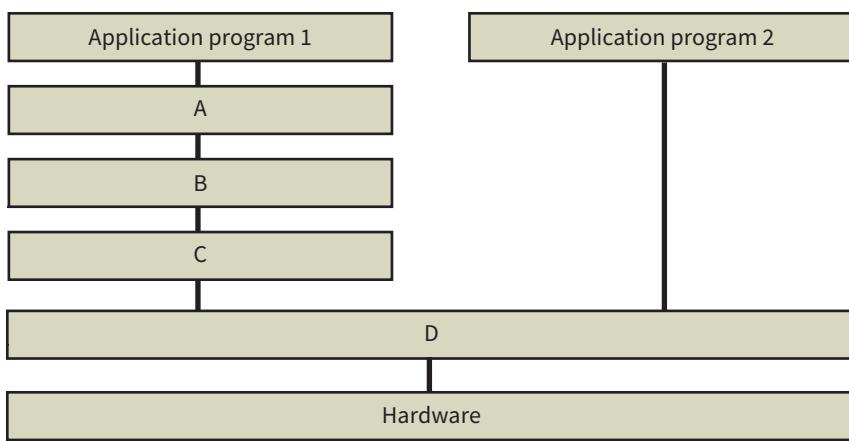


Exam-style Questions

- 1 a** Computer systems are now often constructed with RISC processors.
- i** State what the acronym RISC stands for. [1]
 - ii** State **four** characteristics to be expected of a RISC system. [4]
- b** A RISC processor is likely to be ‘hard-wired’.
- i** Explain what this term means and which specific part of the processor will be hard-wired. [3]
 - ii** State what the alternative to hard-wiring is and what hardware component is needed to be part of the processor to allow this alternative to be implemented. [2]
- 2** The following diagram represents a system which has implemented a virtual machine.



- a** For each of A, B, C, D give a suitable name. [4]
- b** For each of A, B, C and D give a brief description of the function of the feature. [8]
- c** Explain why the diagram is different for Application 2 [2]
- 3 a** Parallelism can be achieved in a number of ways.
- i** Identify **three** different types of parallelism. [3]
 - ii** Identify which type pipelining belongs to. [1]
 - iii** Using a diagram, explain how pipelining works. [5]
- b** Interrupt handling is not so straightforward in a pipelined system. Explain why this is so and give a brief account of how problems can be avoided. [3]
- 4 a** Three descriptions and two types of processor are shown below.

Draw a line to connect each description to the appropriate type of processor.

| Description | Type of processor |
|--|-------------------|
| Makes extensive use of general purpose registers | RISC |
| Many addressing modes are available | CISC |
| Has a simplified set of instructions | [3] |

- b** In a RISC processor three instructions (A followed by B, followed by C) are processed using pipelining. The following table shows the five stages that occur when instructions are fetched and executed.

- i The “A” in the table indicates that instruction A has been fetched in time interval 1.

Complete the table to show the time interval in which each stage of each instruction (A, B, C) is carried out.

| Stage | Time interval | | | | | | | | |
|--------------------------|---------------|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| Fetch instruction | A | | | | | | | | |
| Decode instruction | | | | | | | | | |
| Execute instruction | | | | | | | | | |
| Access operand in memory | | | | | | | | | |
| Write result to register | | | | | | | | | |

[3]

- ii The completed table shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.

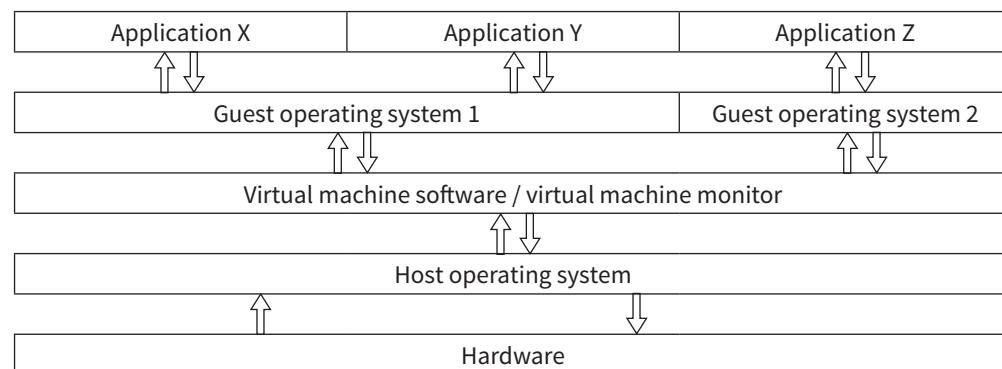
Calculate how many clock cycles are saved by the use of pipelining in the above example.

Show your working.

[3]

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- 5 a** The following diagram shows how applications X, Y and Z can run on a virtual machine system.



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- i The virtual machine software undertakes many tasks.

Describe **two** of these tasks.

[2]

- ii Explain the difference between a guest operating system and a host operating system.

[2]

- b** A company uses a computer as web server. The manufacturer will no longer support the computer’s operating system (OS) in six months time. The company will then need to decide on a replacement OS.

The company is also considering changing the web server software when the OS is changed.

Whenever any changes are made, it is important that the web server service is not disrupted.

In developing these changes, the company could use virtual machines.

- i Describe **two** possible uses of virtual machines by the company.

[4]

The web server often has to handle many simultaneous requests.

- ii The company uses a virtual machine to test possible solutions to the changes that they will need to make.

Explain **one** limitation of this approach.

[2]

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