4-Bit Ring Counter

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***Abstract* – This paper describes about the design of four bit ring counter. A ring counter consists of flip-flops which are connected to shift register, where the last output of flip-flop is connected to input of the first flip-flop making a ring structure.**

Index Terms – Flip-flop, shift register, clock, pre-set, clear.

I. Introduction

A ring counter is a typical application of shift register. Ring counter is like shift counter the only difference is that in ring counter the output of last flip-flop is connected to input of first flip-flop whereas in shift register the output of last flip-flop is connected to output of first flip-flop.

A ring counter is a synchronous counter thus it consists of common clock which activates all the flip-flops at the same time. Ring counter consists of D flip-flops connected in a cascade setup where the output of last flip-flop is connected to input of first flip-flop. In a ring counter number of flip-flops is equal to number of states in ring counter. Therefore, each flip-flop represents a stage. Therefore, 4 flip-flops are required for designing a 4-bit ring counter.

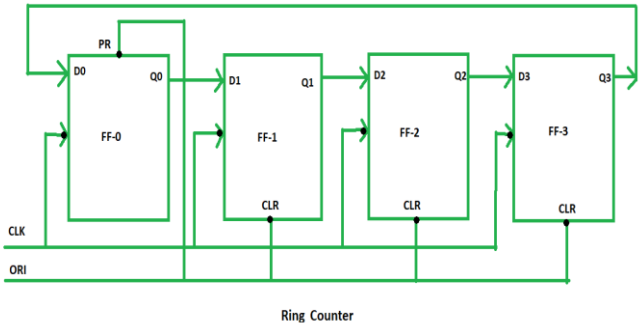

Fig.1 Circuit diagram of 4-bit ring counter

II. Working

From the fig.1 we can interpret that overriding input(ORI) is connected to every flip-flop and also clear(CLR) and pre-set(PR) are used as ORI. When PR is 0 output is 1 and when CLR is 0 output is 0. PR and CLR are active low signals and always operated with value 0.PR and CLR are independent of clock pulse(CLK) and value of input D.

From the fig.1 ORI is connected to Pre-set (PR) in FF-0 and it is connected to Clear (CLR) in FF-1, FF-2, and FF-3. Thus, output Q = 1 is generated at FF-0, and the rest of the flip-flop generates output Q = 0. This output Q = 1 at FF-0 is known as Pre-set 1. This pre-set 1 is generated by making ORI low and that time Clock (CLK) becomes don't care. Then ORI is made to high and apply low clock pulse signal as the Clock (CLK) is negative edge activated. Then at each clock pulse the pre-set 1 is shifted to the next flip-flop and thus forms a Ring.

PRESETED 1

ORI	CLK	Q0	Q1	Q2	Q3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

Table.1 Stage wise output of 4-bit ring counter

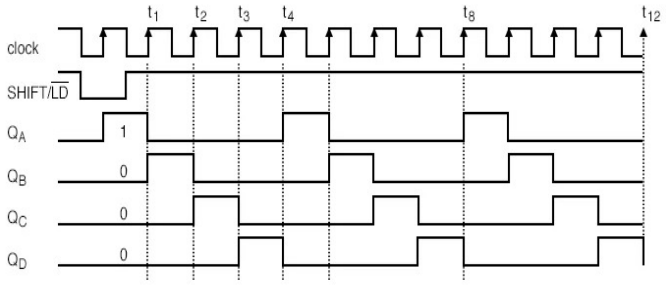

Fig. 2 Sample output of 4-bit ring counter

III. Applications

1. To count the data in a continuous loop.
2. Used in frequency divider circuits.

References

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