Assembly Language for x86 Processors

Seventh Edition





Chapter 2

x86 Processor Architecture



Chapter Overview

- General Concepts
- IA-32 Processor Architecture
- IA-32 Memory Management
- 64-bit Processors
- Components of an IA-32 Microcomputer
- Input-Output System



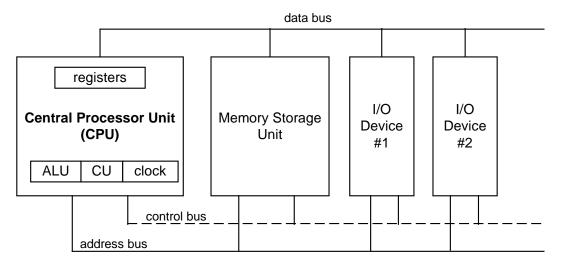
General Concepts

- Basic microcomputer design
- Instruction execution cycle
- Reading from memory
- How programs run



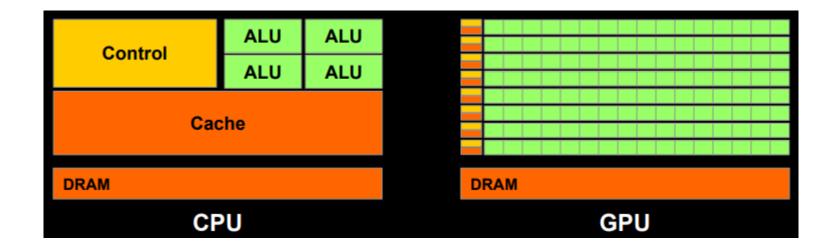
Basic Microcomputer Design

- clock synchronizes CPU operations
- control unit (CU) coordinates sequence of execution steps
- ALU performs arithmetic and bitwise processing





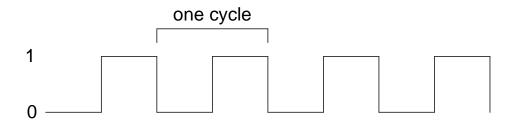
CPU vs GPU in ALU





Clock

- synchronizes all CPU and BUS operations
- machine (clock) cycle measures time of a single operation
- clock is used to trigger events

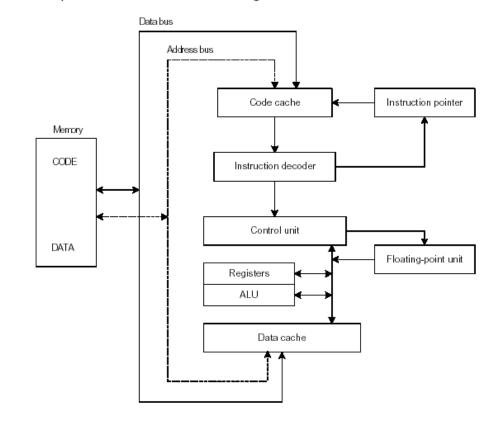




Instruction Execution Cycle

- Fetch
- Decode
- Fetch operands
- Execute
- Store output

Figure 2-2 Simplified Pentium CPU Block Diagram.





Reading from Memory

Multiple machine cycles are required when reading from memory, because it responds much more slowly than the C PU. The steps are:

- 1. Place the address of the value you want to read on the address bus.
- Assert (changing the value of) the processor's RD (read) pin.
- 3. Wait one clock cycle for the memory chips to respond.
- Copy the data from the data bus into the destination operand

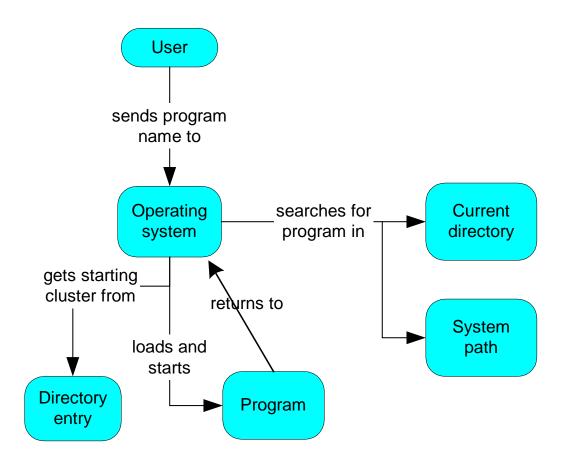


Cache Memory

- High-speed expensive static RAM both inside and outside the CPU.
 - Level-1 cache: inside the CPU
 - Level-2 cache: outside the CPU
- Cache hit: when data to be read is already in cache memory
- Cache miss: when data to be read is not in cache memory.



How a Program Runs





Basic Execution Environment

- Addressable memory
- General-purpose registers
- Index and base registers
- Specialized register uses
- Status flags
- Floating-point, MMX, XMM registers



Addressable Memory

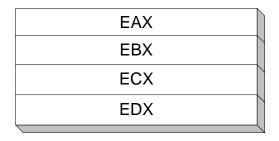
- Protected mode
 - 4 GB
 - 32-bit address
- Real-address and Virtual-8086 modes
 - 1 MB space
 - 20-bit address



General-Purpose Registers

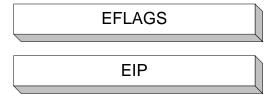
 Named storage locations inside the CPU, optimized for speed.

32-bit General-Purpose Registers





16-bit Segment Registers

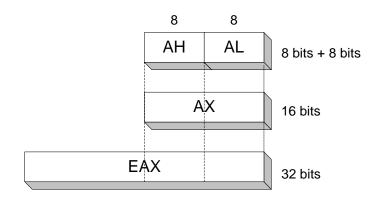


CS	ES
SS	FS
DS	GS



Accessing Parts of Registers

- Use 8-bit name, 16-bit name, or 32-bit name
- Applies to EAX, EBX, ECX, and EDX



32-bit	16-bit	8-bit (high)	8-bit (low)
EAX	AX	АН	AL
EBX	BX	ВН	BL
ECX	CX	СН	CL
EDX	DX	DH	DL



Index and Base Registers

 Some registers have only a 16-bit name for their lower half:

32-bit	16-bit
ESI	SI
EDI	DI
EBP	BP
ESP	SP



Some Specialized Register Uses (1 of 2)

- General-Purpose
 - EAX accumulator
 - ECX loop counter
 - ESP stack pointer
 - ESI, EDI index registers
 - EBP extended frame pointer (stack)



Some Specialized Register Uses (2 of 2)

- Segment
 - CS code segment
 - DS data segment
 - SS stack segment
 - ES, FS, GS additional segments
- EIP- instruction pointer
- EFLAGS
 - status and control flags
 - each flag is a single binary bit



Status Flags

- Carry
 - unsigned arithmetic out of range
- Overflow
 - signed arithmetic out of range
- Sign
 - result is negative
- Zero
 - result is zero
- Auxiliary Carry
 - carry from bit 3 to bit 4
- Parity
 - sum of 1 bits is an even number



IA-32 Memory Management

- Real-address mode
- Calculating linear addresses
- Protected mode
- Multi-segment model
- Paging



Protected Mode (1 of 2)

- 4 GB addressable RAM
 - (00000000 to FFFFFFFh)
- Each program assigned a memory partition which is protected from other programs
- Designed for multitasking
- Supported by Linux & MS-Windows



Components of an IA-32 Microcomputer

- Motherboard
- Video output
- Memory
- Input-output ports

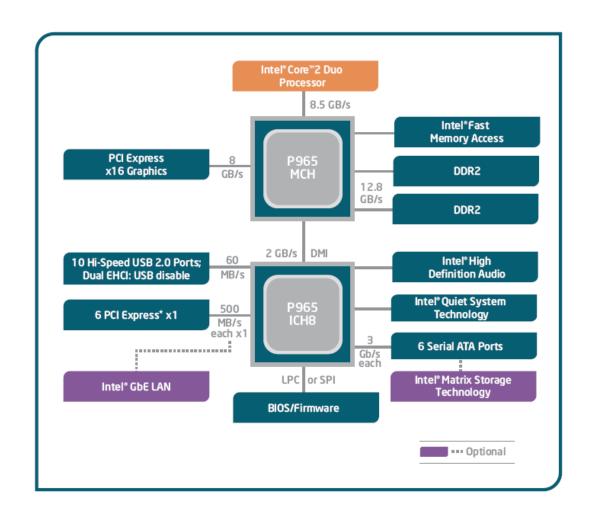


Motherboard

- CPU socket
- External cache memory slots
- Main memory slots
- BIOS chips
- Sound synthesizer chip (optional)
- Video controller chip (optional)
- IDE, parallel, serial, USB, video, keyboard, joystick, network, and mouse connectors
- PCI bus connectors (expansion cards)



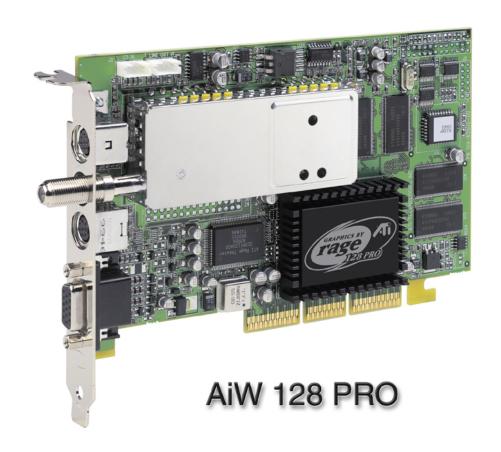
Intel 965 Express Chipset





Sample Video Controller (ATI Corp.)

- 128-bit 3D graphics performance powered by RAGE™ 128 PRO
- 3D graphics performance
- Intelligent TV-Tuner with Digital VCR
- TV-ON-DEMAND™
- Interactive Program Guide
- Still image and MPEG-2 motion video capture
- Video editing
- Hardware DVD video playback
- Video output to TV or VCR





Memory (1 of 2)

- ROM
 - read-only memory
- EPROM
 - erasable programmable read-only memory
- Dynamic RAM (DRAM)
 - inexpensive; must be refreshed constantly
- Static RAM (SRAM)
 - expensive; used for cache memory; no refresh required



Memory (2 of 2)

- Video RAM (VRAM)
 - dual ported; optimized for constant video refresh
- CMOSRAM
 - complimentary metal-oxide semiconductor
 - system setup information



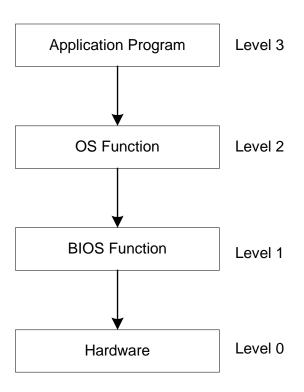
Levels of Input-Output

- Level 3: High-level language function
 - examples: C++, Java
 - portable, convenient, not always the fastest
- Level 2: Operating system
 - Application Programming Interface (API)
 - extended capabilities, lots of details to master
- Level 1: BIOS
 - drivers that communicate directly with devices
 - OS security may prevent application-level code from working at this level



Displaying a String of Characters

When a program displays a string of characters, the following steps take place:





Programming levels

 Assembly language programs can perform input-output at each of the following levels:

