

PMDPB30XN 20 V, dual N-channel Trench MOSFET

Product data sheet

Product profile 1.

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit		
Per transistor	Per transistor								
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	20	V		
V_{GS}	gate-source voltage			-12	-	12	V		
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	5.3	Α		
Static characteristics (per transistor)									
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	32	40	mΩ		

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



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Pinning information

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	6 5 4	D1 D2
2	G1	gate TR1		
3	D2	drain TR2	7 8	(」☆本本☆↓)
4	S2	source TR2		
5	G2	gate TR2	1 2 3	G1 S1 S2 G2
6	D1	drain TR1	Transparent top view DFN2020-6 (SOT1118)	017aaa254
7	D1	drain TR1	5.112020 3 (0011110)	
8	D2	drain TR2		

Ordering information

Table 3. **Ordering information**

Type number	Package					
	Name	Description	Version			
PMDPB30XN	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118			

Marking 4.

Marking codes Table 4.

Type number	Marking code
PMDPB30XN	1V

Limiting values 5.

Limiting values Table 5.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transis	tor					
V_{DS}	drain-source voltage	T _j = 25 °C		-	20	V
V_{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	5.3	Α
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	4	Α
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	2.6	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	12	Α
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Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1170	mW
		T _{sp} = 25 °C		-	8330	mW
Source-drain	n diode	,				
Is	source current	T _{amb} = 25 °C	[1]	-	1.2	Α
Per device		,				
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

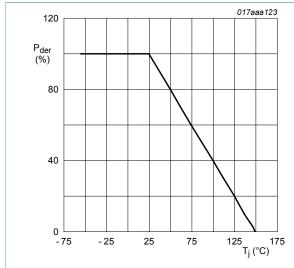


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

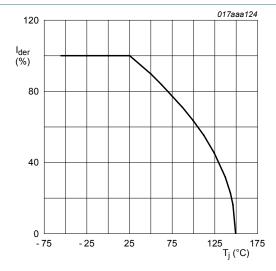


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

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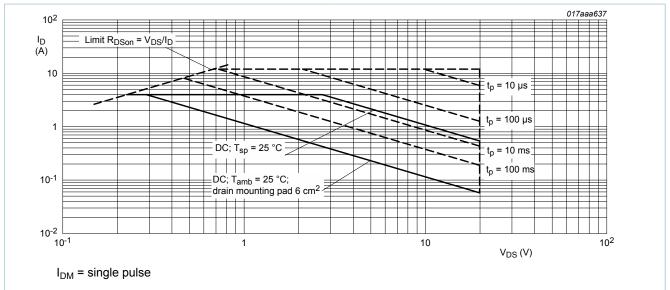


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient		[1]	-	223	256	K/W
			[2]	-	93	107	K/W
		in free air; t ≤ 5 s	[2]	-	55	63	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	10	15	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

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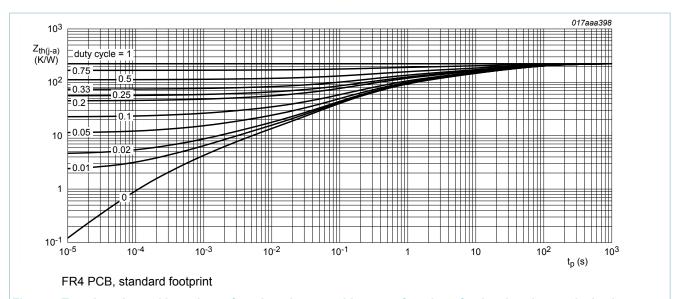


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

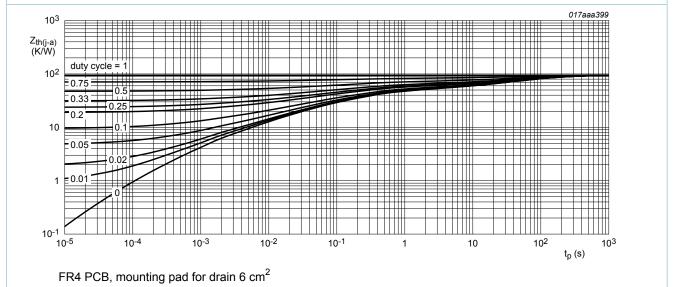


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

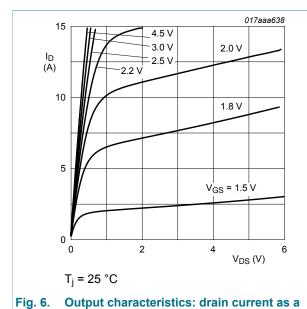
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static characteristics (per transistor)							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μ A; V_{GS} = 0 V; T_j = 25 °C		20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 μ A; V_{DS} = V_{GS} ; T_j = 25 °C		0.4	0.65	0.9	V
I _{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	μA
		V _{DS} = 20 V; V _{GS} = 0 V; T _j = 150 °C		-	-	11	μA
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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{GSS}	gate leakage current	V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	V_{GS} = 4.5 V; I_D = 3 A; T_j = 25 °C	-	32	40	mΩ
	resistance	V _{GS} = 4.5 V; I _D = 3 A; T _j = 150 °C	-	55	69	mΩ
		V _{GS} = 2.5 V; I _D = 1.4 A; T _j = 25 °C	-	40	53	mΩ
		V _{GS} = 1.8 V; I _D = 1.4 A; T _j = 25 °C	-	60	75	mΩ
9fs	forward transconductance	$V_{DS} = 5 \text{ V}; I_{D} = 3 \text{ A}; T_{j} = 25 ^{\circ}\text{C}$	-	12	-	S
Dynamic cl	haracteristics (per transist	or)		-		
Q _{G(tot)}	total gate charge	V_{DS} = 10 V; I_D = 3 A; V_{GS} = 4.5 V; T_j = 25 °C	-	14.4	21.7	nC
Q _{GS}	gate-source charge		-	1.1	-	nC
Q_{GD}	gate-drain charge	-	-	1.5	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V;	-	660	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	87	-	pF
C _{rss}	reverse transfer capacitance		-	74	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 10 V; I_{D} = 3 A; V_{GS} = 4.5 V;	-	4	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	40	-	ns
t _f	fall time		-	16	-	ns
Source-dra	in diode (per transistor)					,
V _{SD}	source-drain voltage	I _S = 1.2 A; V _{GS} = 0 V; T _j = 25 °C	-	8.0	1.2	V
	The state of the s					



function of drain-source voltage; typical values

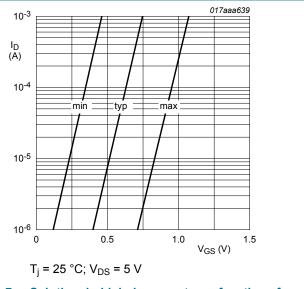


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

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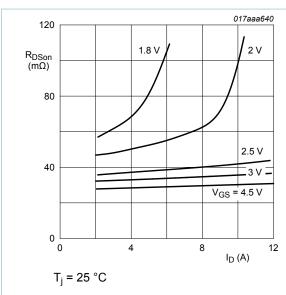


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

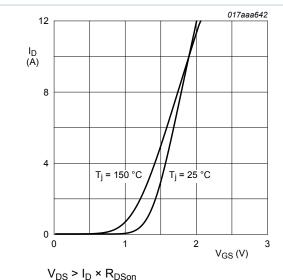


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

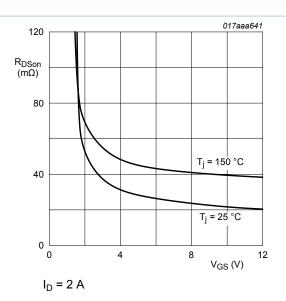


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

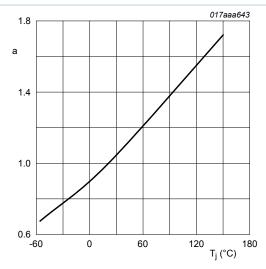


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

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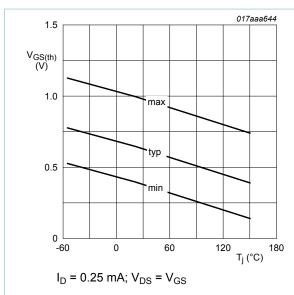


Fig. 12. Gate-source threshold voltage as a function of junction temperature

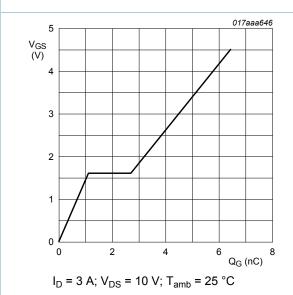


Fig. 14. Gate-source voltage as a function of gate charge; typical values

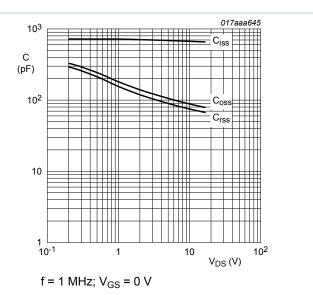


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

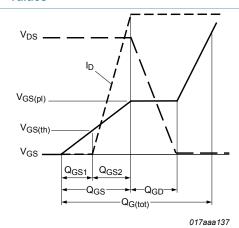
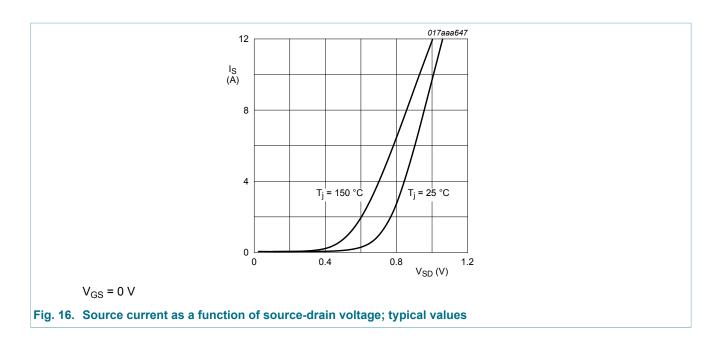
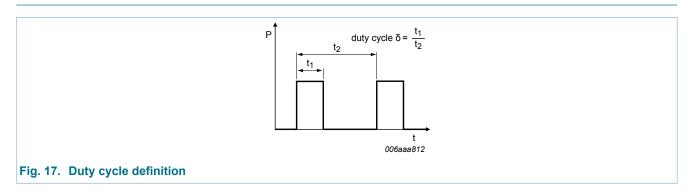


Fig. 15. Gate charge waveform definitions

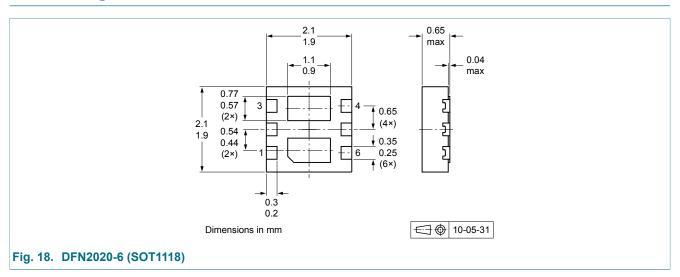
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8. Test information



9. Package outline



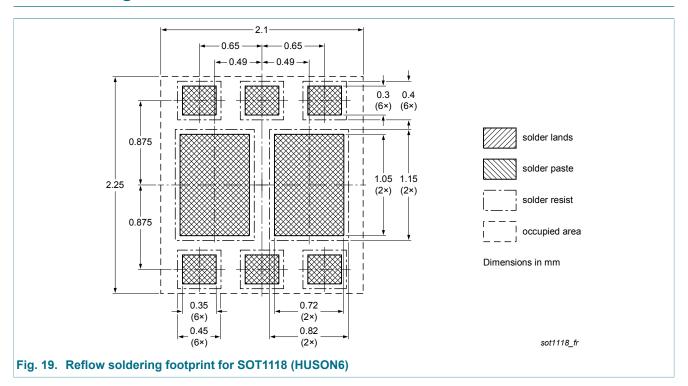
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10. Soldering



11. Revision history

Table 8. Revision history

Document ID	Release date	Document status	Change notice	Supersedes
PMDPB30XN v.1	20120706	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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