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Final

P19_0356_01_Denali_1G_Test_Report_00
Date of Approval: 2020-Nov-19

Test Report

Device Under Test		**Customer**	
Device Name	BCM89881	Order No.	P19_0356
Manufacturer	Broadcom	Name	Broadcom Corporation
Type / Version	BCM989881_CS	Address	5300 California Avenue Irvine CA, 92617 USA
Sample marking	BROADCOM BCM89881B1BFBG TN1933 9266-01 P3 W		

Number of Pages	41
Test Period	from 2020-Jun-26 until 2020-Aug-21
Test Method / Test Requirement	1000BASE-T1 Interoperability Test Suite
Performed Tests and References	1 1000BASE-T1 Interoperability Test Suite [1.3D] (May 29, 2019)
Interoperability Test Results	The Test Results refer to the delivered device and the applicable test cases.
1 1000BASE-T1 Interoperability Test Suite	**IOP Chapter (Group 1 and 2): PASS** **Advanced Feature Set (Group 3 and 4): PASS**

	Link Partner	
Chapter	RTL9075A	BCM89881
Group 1: Link Status	**PASS**	**PASS**
Group 2: Link-Up	**PASS**	**PASS**
Group 3: Signal Quality	**NOT APPLICABLE**[1]	**PASS**
Group 4: Cable Diagnostics	**NOT APPLICABLE**[1]	**PASS**

For detailed information see chapter Test List and Observations at the following pages.

Approved by

Christoph Wosnitza, Project Manager

Test performed by

Norwin Trautmann, Project Engineer

[1] The Advanced Feature Set tests are only conducted against one Link Partner.

Table of Content

Revision History

Old revision	New revision	Amendment Description	Editor
–	00	Initial version	NT

1 Device Under Test (detailed)

General	
Date of Sample Arrival	2020-04-16
Manufacturer	Broadcom
Sample Marking	BROADCOM BCM89881B1BFBG TN1933 9266-01 P3 W
Test performed with DUT no.	see "Test setup"

Device Specification	
Device Name	BCM89881
Type / Version	BCM989881_CS
SW-Version	C&S Driver - IOP (3E2EEBE) C&S Driver - Cable Diagnostics (1C6F7018) C&S Driver - Signal Quality (52BDC87)

Documentation	
Datasheet, Schematic	89881-DS107.pdf, BCM989881_AUTOBR_0020_100818.pdf

1.1 MDI circuit schematics

The following figures indicate components and circuitry used for the MDI interface.

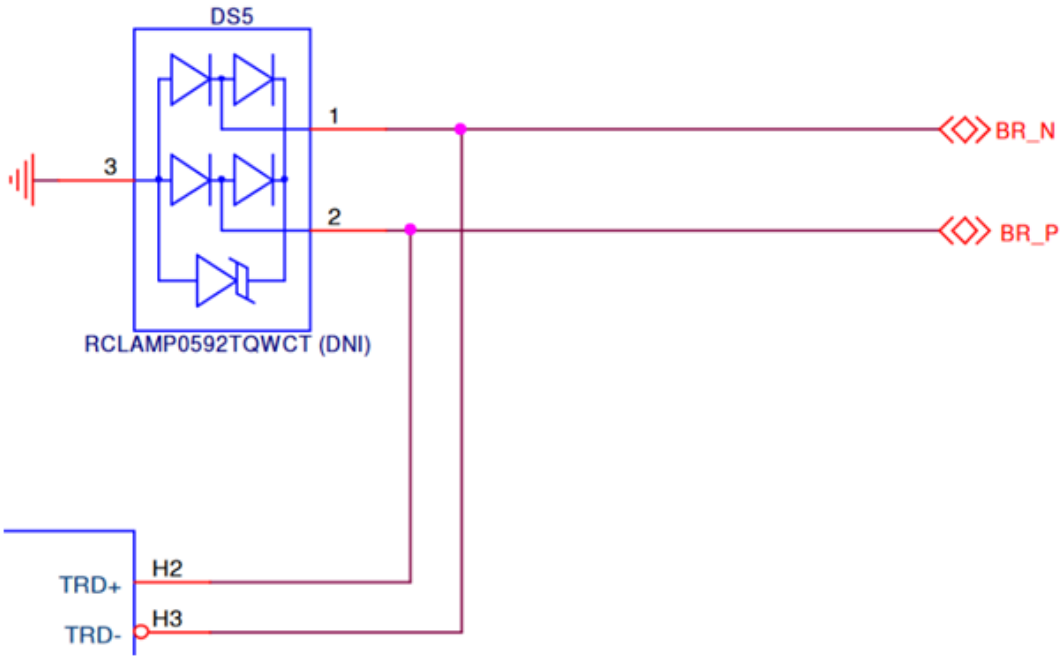

Figure 1: MDI circuit schematic part 1

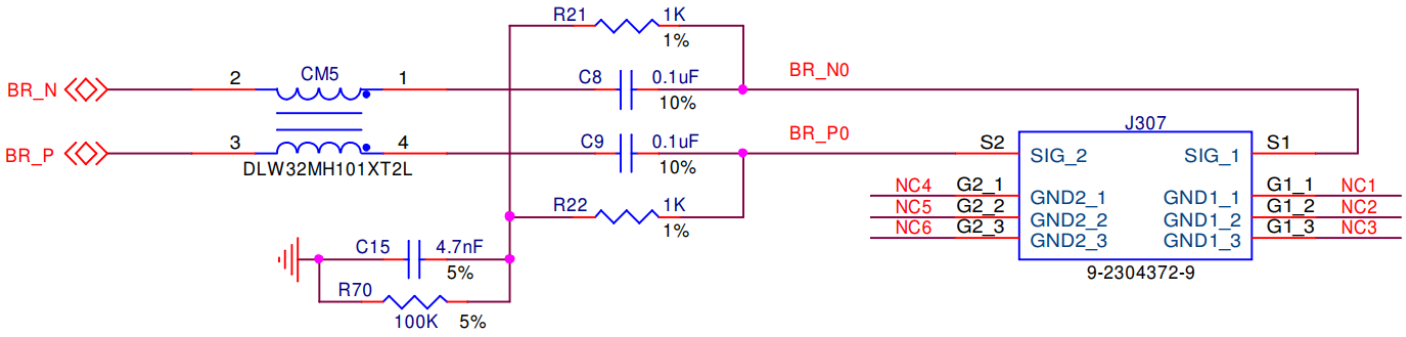

Figure 2: MDI circuit schematic part 2

2 Setup for Device Under Test

2.1 PHY Board description

The PHYs to be tested shall be supplied to the test house according to the minimum requirement detailed in this document.

The PHY board consists of three parts that work together:

- PHY host section where the PHY and all its required circuitry are allocated.
- Control section as a link between the Test System and the PHY.
- Power supply section.

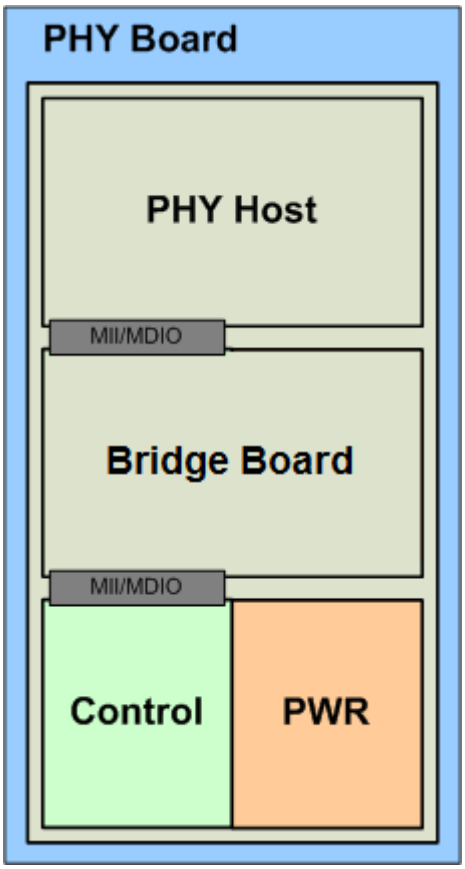

Figure 3: PHY board concept

The PHY host board shall be provided to the test house to execute the tests. In the following sections the required connectors and their pin-out are described.

2.2 PHY host board and Power Supply

In Figure 4 the PHY Host Board is depicted. This configuration is required to be implemented as shown in order to ensure the compatibility with the control board which is directly connected through the MII/MDIO Interface.

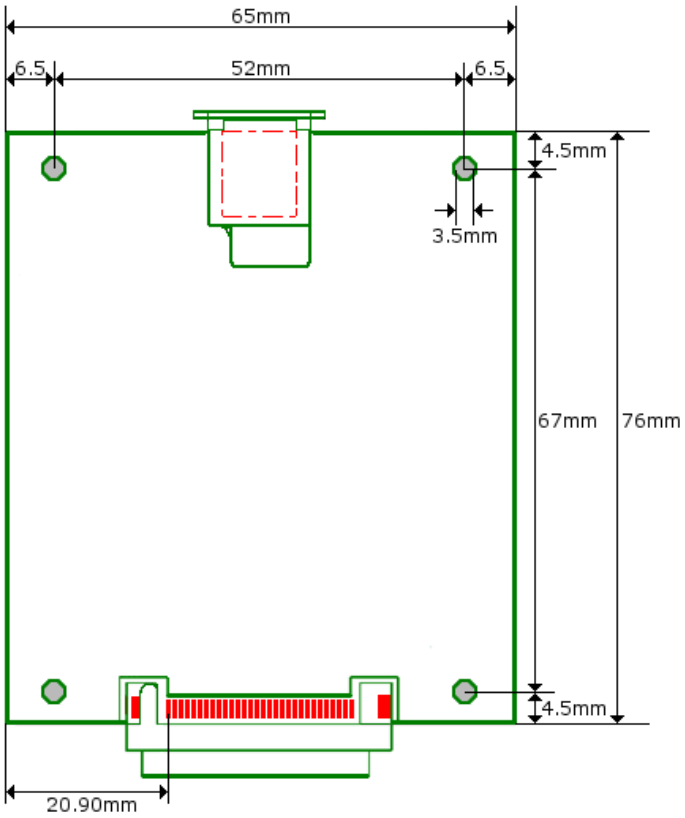

Figure 4: PHY Host board

2.3 Power Supply Requirements

The power supply shall be designed to provide a stable output when working under different temperature conditions between -40°C and +105°C.

The input voltage to the power supply module will be 12V (VBAT)

The required voltages and current outputs are listed in Table 1

Voltage [V]	Max Current [mA]	Name
3,3	1500	3V3
5	200	5V0

Table 1: Voltages and current outputs requirements

In Figure 5 it is shown a brief description of the power distribution within the PHY board.

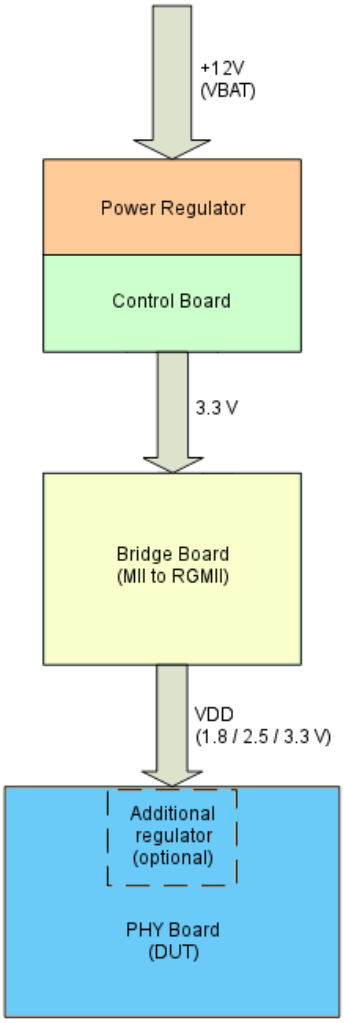

Figure 5: Power Supply Distribution

2.4 Required signals and connectors

2.4.1 MDI Connector

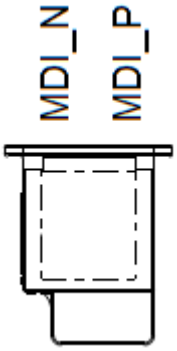

Figure 6: Power Supply Distribution

2.4.1.1 Connector description

Manufacturer:	TE Connectivity Germany GmbH
Description:	MATEnet Header
Manufacturer Part number:	9-2304372-9 1-port 90° MATEnet header, Code Z

2.4.2 RGMII / MDIO Interface

Pin	Signal	Signal	Pin
1	GND	VCC (3.3V)	2
3	GND	VCC (3.3V)	4
5	GND	GND	6
7	GND	MDC	8
9	GND	MDIO	10
11	GND	GND	12
13	GND	CRS / SPI_CS2	14
15	GND	COL / SPI_CS3	16
17	GND	GND	18
19	GND	RGMII_RXD3	20
21	GND	RGMII_RXD2	22
23	GND	RGMII_RXD1	24
25	GND	RGMII_RXD0	26
27	GND	GND	28
29	GND	RGMII_RXC	30
31	GND	RGMII_RX_CTL	32
33	GND	GND	34
35	GND	RGMII_TXC	36
37	GND	GND	38
39	GND	RGMII_TXD3	40
41	GND	RGMII_TXD2	42
43	GND	RGMII_TXD1	44
45	GND	RGMII_TXD0	46
47	GND	GND	48
49	GND	RGMII_TX_CTL	50
51	GND	GND	52
53	SPI_MOSI	TX_ER	54
55	SPI_MISO	RX_ER	56
57	SPI_CS1	GND	58
59	SPI_CLK	RESET	60
BOTTOM		**TOP**	

Table 2: RGMII / MDIO Interface

2.4.2.1 Connector description

Manufacturer: Samtec
Description: Conn Edge Rate Socket Strip SKT 60 POS 0.8mm Solder ST Edge Mount T/R
Manufacturer Part number: ERF8-030-01-L-D-EM2

3 Test Equipment

The following test equipment and test system have been used.

No.	Component	Manufacturer	Version / Type	ID
C&S Equipment				
1	Test Coordinator	C&S	Rev 1.4	-
2	Heating oven with mechanical convection	Binder	Binder FD 23	500 044
3	B 35 Cold box	Fryka	B35-50	500 065
4	Temperature Logger (heat chamber)	PCE	T390	CS140632
5	Temperature Logger (cold chamber)	PCE	T390	CS140656
Power Supplies				
6	Power Supply	Agilent	E3634A	CS140293
Noise Generator				
7	Programmable Noise Generator	Noisecom	UFX7911A	CS140790
Worst Case Channel				
8	Data cable LEONI Dacar® 647 (A.1: 15-meter length with four filter boards)	LEONI Kabel GmbH	-	-
Best Case Channel				
9	Data cable LEONI Dacar® 647 (A.3: 1.5-meter length)	LEONI Kabel GmbH	-	-

4 Technical Correspondence

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Email	n.trautmann@cs-group.de

5 Test Setup

The devices were grouped together as shown below. Each link partner was associated with one DUT, forming nine groups in total.

DUT				Link Partner			
Group	Host Board	Bridge Board	DUT ID	Host Board	Bridge Board	LP ID	LP Type
G03	CS140241	R1.1 #62	61	CS140187	R1.1 #93	46	**Realtek RTL9075A**
G04	CS140539	R1.1 #32	65	CS140196	R1.1 #05	16	
G05	CS140528	R1.1 #09	51	CS140526	R1.1 #97	38	
G06	CS140321	R1.1 #67	57	CS140198	R1.1 #65	63	**Broadcom BCM89881**
G07	CS140466	R.1.1 #86	58	CS140193	R1.1 #48	71	
G08	CS140541	R1.1 #07	49	CS140608	R1.1 #11	70	

Table 3: Description of groups used for Link Status and Link-Up

DUT				Link Partner			
Group	Host Board	Bridge Board	DUT ID	Host Board	Bridge Board	LP ID	LP Type
G04	CS140539	R1.1 #32	65	CS140196	R1.1 #05	16	**Realtek RTL9075A**
G05	CS140528	R1.1 #09	51	CS140526	R1.1 #97	38	
G07	CS140466	R.1.1 #86	58	CS140193	R1.1 #48	71	**Broadcom BCM89881**
G08	CS140541	R1.1 #07	49	CS140608	R1.1 #11	70	

Table 4: Description of groups used for Link Status and Link Up at -40°C and +105°C Temperature

DUT				Link Partner			
Group	Host Board	Bridge Board	DUT ID	Host Board	Bridge Board	LP ID	LP Type
G00	CS140328	R1.1 #32	65	CS140888	R1.1 #62	61	**Broadcom BCM89881**

Table 5: Description of groups used for Signal Quality Index and Cable Diagnostics

6 Test List

6.1 Nomenclature

The following parameters describe the test environment and if applicable the kind of stress and its location.

Reference name	Description
1000BASE-T1_IOP_XX	Test reference
SR	Soft Reset
HR	Hard Reset
O1	Open is on ETH_N or ETH_P
O2	Open on both ETH_N and ETH_P
S2	Short on both ETH_N and ETH_P
NEAR	Open/Short near to DUT
FAR	Open/Short near to LP
M	MASTER
S	SLAVE
P	Swapped Polarity
C1	Best-case Channel (A.3)
C2	Worst-case Channel (A.1)
T1	Room Temperature
T2	-40°C
T3	105°C /125°C

Table 6: Nomenclature of test environment variables

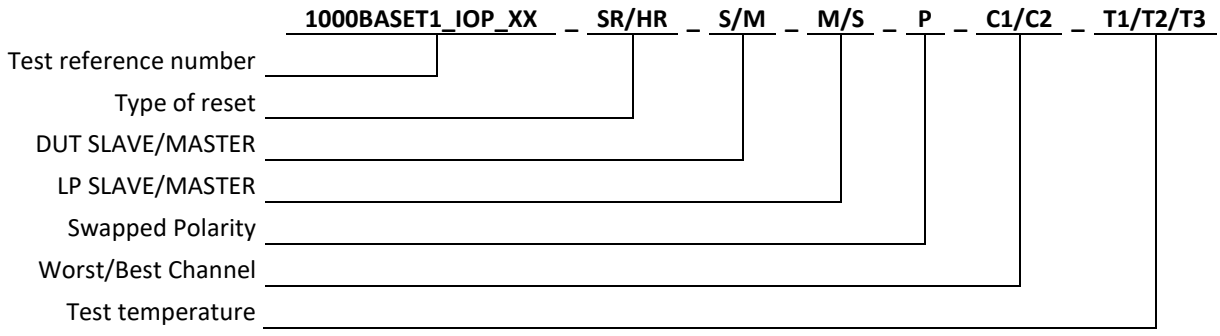

Figure 7: Test groups 1 to 3 nomenclature

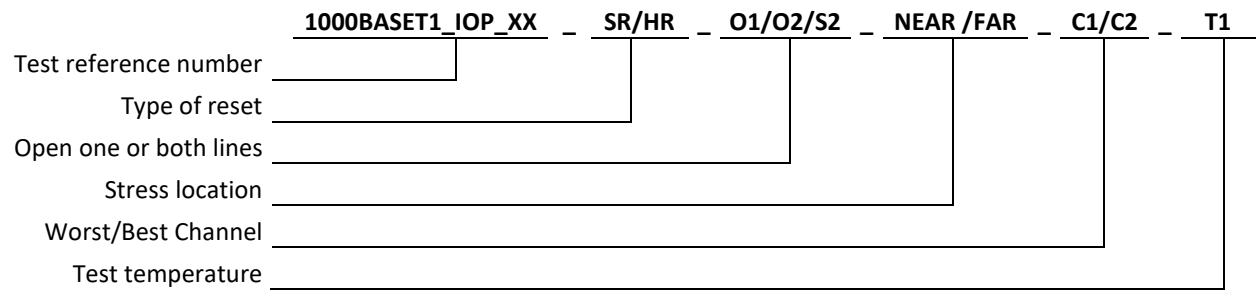

Figure 8: Test group 4 nomenclature

6.2 Test Cases

Group	Test Case	Realtek RTL9075A	Broadcom BCM89881
Group 1: Link status	IOP_16_SR_M_S_C1_T1	PASS	PASS
	IOP_16_SR_M_S_C1_T2	PASS	PASS
	IOP_16_SR_M_S_C1_T3	PASS	PASS
	IOP_16_SR_M_S_C2_T1	PASS	PASS
	IOP_16_SR_M_S_C2_T2	PASS	PASS
	IOP_16_SR_M_S_C2_T3	PASS	PASS
	IOP_16_SR_S_M_C1_T1	PASS	PASS
	IOP_16_SR_S_M_P_C1_T1	PASS	PASS
	IOP_16_SR_S_M_C1_T2	PASS	PASS
	IOP_16_SR_S_M_P_C1_T2	PASS	PASS
	IOP_16_SR_S_M_C1_T3	PASS	PASS
	IOP_16_SR_S_M_P_C1_T3	PASS	PASS
	IOP_16_SR_S_M_C2_T1	PASS	PASS
	IOP_16_SR_S_M_P_C2_T1	PASS	PASS
	IOP_16_SR_S_M_C2_T2	PASS	PASS
	IOP_16_SR_S_M_P_C2_T2	PASS	PASS
	IOP_16_SR_S_M_C2_T3	PASS	PASS
	IOP_16_SR_S_M_P_C2_T3	PASS	PASS
	IOP_17_SR_M_M_C2_T1	PASS	PASS
	IOP_17_SR_S_S_C2_T1	PASS	PASS
	IOP_19_SR_M_S_C2_T1	PASS	PASS
	IOP_19_SR_S_M_C2_T1	PASS	PASS

Group	Test Case	Realtek RTL9075A	Broadcom BCM89881
Group 2: Link up	IOP_21_HR_M_S_C1_T1	PASS	PASS
	IOP_21_HR_M_S_C1_T2	PASS	PASS
	IOP_21_HR_M_S_C1_T3	PASS	PASS
	IOP_21_HR_M_S_C2_T1	PASS	PASS
	IOP_21_HR_M_S_C2_T2	PASS	PASS
	IOP_21_HR_M_S_C2_T3	PASS	PASS
	IOP_21_HR_S_M_C1_T1	PASS	PASS
	IOP_21_HR_S_M_C1_T2	PASS	PASS
	IOP_21_HR_S_M_C1_T3	PASS	PASS
	IOP_21_HR_S_M_C2_T1	PASS	PASS
	IOP_21_HR_S_M_C2_T2	PASS	PASS
	IOP_21_HR_S_M_C2_T3	PASS	PASS
	IOP_21_HR_S_M_P_C1_T1	PASS	PASS
	IOP_21_HR_S_M_P_C1_T2	PASS	PASS
	IOP_21_HR_S_M_P_C1_T3	PASS	PASS
	IOP_21_HR_S_M_P_C2_T1	PASS	PASS
	IOP_21_HR_S_M_P_C2_T2	PASS	PASS
	IOP_21_HR_S_M_P_C2_T3	PASS	PASS
	IOP_21_SR_M_S_C1_T1	PASS	PASS
	IOP_21_SR_M_S_C1_T2	PASS	PASS
	IOP_21_SR_M_S_C1_T3	PASS	PASS
	IOP_21_SR_M_S_C2_T1	PASS	PASS
	IOP_21_SR_M_S_C2_T2	PASS	PASS
	IOP_21_SR_M_S_C2_T3	PASS	PASS
	IOP_21_SR_S_M_C1_T1	PASS	PASS
	IOP_21_SR_S_M_C1_T2	PASS	PASS
	IOP_21_SR_S_M_C1_T3	PASS	PASS
	IOP_21_SR_S_M_C2_T1	PASS	PASS
	IOP_21_SR_S_M_C2_T2	PASS	PASS
	IOP_21_SR_S_M_C2_T3	PASS	PASS
	IOP_21_SR_S_M_P_C1_T1	PASS	PASS
	IOP_21_SR_S_M_P_C1_T2	PASS	PASS
	IOP_21_SR_S_M_P_C1_T3	PASS	PASS
	IOP_21_SR_S_M_P_C2_T1	PASS	PASS
	IOP_21_SR_S_M_P_C2_T2	PASS	PASS
	IOP_21_SR_S_M_P_C2_T3	PASS	PASS

Group	Test Case	Realtek RTL9075A	Broadcom BCM89881
Group 2: Link up	IOP_22_HR_M_S_C1_T1	PASS	PASS
	IOP_22_HR_M_S_C1_T2	PASS	PASS
	IOP_22_HR_M_S_C1_T3	PASS	PASS
	IOP_22_HR_M_S_C2_T1	PASS	PASS
	IOP_22_HR_M_S_C2_T2	PASS	PASS
	IOP_22_HR_M_S_C2_T3	PASS	PASS
	IOP_22_HR_S_M_C1_T1	PASS	PASS
	IOP_22_HR_S_M_C1_T2	PASS	PASS
	IOP_22_HR_S_M_C1_T3	PASS	PASS
	IOP_22_HR_S_M_C2_T1	PASS	PASS
	IOP_22_HR_S_M_C2_T2	PASS	PASS
	IOP_22_HR_S_M_C2_T3	PASS	PASS
	IOP_22_HR_S_M_P_C1_T1	PASS	PASS
	IOP_22_HR_S_M_P_C1_T2	PASS	PASS
	IOP_22_HR_S_M_P_C1_T3	PASS	PASS
	IOP_22_HR_S_M_P_C2_T1	PASS	PASS
	IOP_22_HR_S_M_P_C2_T2	PASS	PASS
	IOP_22_HR_S_M_P_C2_T3	PASS	PASS
	IOP_22_SR_M_S_C1_T1	PASS	PASS
	IOP_22_SR_M_S_C1_T2	PASS	PASS
	IOP_22_SR_M_S_C1_T3	PASS	PASS
	IOP_22_SR_M_S_C2_T1	PASS	PASS
	IOP_22_SR_M_S_C2_T2	PASS	PASS
	IOP_22_SR_M_S_C2_T3	PASS	PASS
	IOP_22_SR_S_M_C1_T1	PASS	PASS
	IOP_22_SR_S_M_C1_T2	PASS	PASS
	IOP_22_SR_S_M_C1_T3	PASS	PASS
	IOP_22_SR_S_M_C2_T1	PASS	PASS
	IOP_22_SR_S_M_C2_T2	PASS	PASS
	IOP_22_SR_S_M_C2_T3	PASS	PASS
	IOP_22_SR_S_M_P_C1_T1	PASS	PASS
	IOP_22_SR_S_M_P_C1_T2	PASS	PASS
	IOP_22_SR_S_M_P_C1_T3	PASS	PASS
	IOP_22_SR_S_M_P_C2_T1	PASS	PASS
	IOP_22_SR_S_M_P_C2_T2	PASS	PASS
	IOP_22_SR_S_M_P_C2_T3	PASS	PASS

Group	Test Case	Realtek RTL9075A	Broadcom BCM89881
Group 3: Signal quality	IOP_24a_SR_M_S_C1_T1	NOT APPLICABLE	PASS
	IOP_24a_SR_S_M_C1_T1	NOT APPLICABLE	PASS
	IOP_24b_SR_M_S_C1_T1	NOT APPLICABLE	PASS
	IOP_24b_SR_S_M_C1_T1	NOT APPLICABLE	PASS
Group 4: Cable diagnostics	IOP_31_SR_C1_T1	NOT APPLICABLE	PASS
	IOP_31_SR_C2_T1	NOT APPLICABLE	PASS
	IOP_32_SR_O1_FAR_M_S	NOT APPLICABLE	PASS
	IOP_32_SR_O1_FAR_S_M	NOT APPLICABLE	PASS
	IOP_32_SR_O2_FAR_M_S	NOT APPLICABLE	PASS
	IOP_32_SR_O2_FAR_S_M	NOT APPLICABLE	PASS
	IOP_32_SR_O1_NEAR_M_S	NOT APPLICABLE	PASS
	IOP_32_SR_O1_NEAR_S_M	NOT APPLICABLE	PASS
	IOP_32_SR_O2_NEAR_M_S	NOT APPLICABLE	PASS
	IOP_32_SR_O2_NEAR_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_BUS_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_BUS_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_GND_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_GND_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_VBAT_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_FAR_VBAT_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_BUS_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_BUS_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_GND_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_GND_S_M	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_VBAT_M_S	NOT APPLICABLE	PASS
	IOP_33_SR_NEAR_VBAT_S_M	NOT APPLICABLE	PASS

Table 7: Test list

7 Observations

7.1 IOP_21 Link-up after PHY-reset

Test Case Description

This test case shall ensure that the PHY is able to establish a link after being reset and reconfigured within a given time limit.

1. DUT shall soft-/hard-reset and reconfigure its PHY.
2. The DUT's PHY configuration must be finished within 20ms after reset.
3. After finished configuration, the DUT shall start timer t0.
4. DUT shall wait until the PHY indicates an active link and stop timer t0.
5. DUT shall monitor whether the link status remains active for at least 750ms after initial link-up.

Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.

- DUT's PHY achieved link-up within 100ms after finished configuration (t0 <= 100ms).
- Link did not go down after test step 4.

7.1.1 Observation: Link-up times

The next figures show the link-up times distribution for every test case 21 and against each link partner:

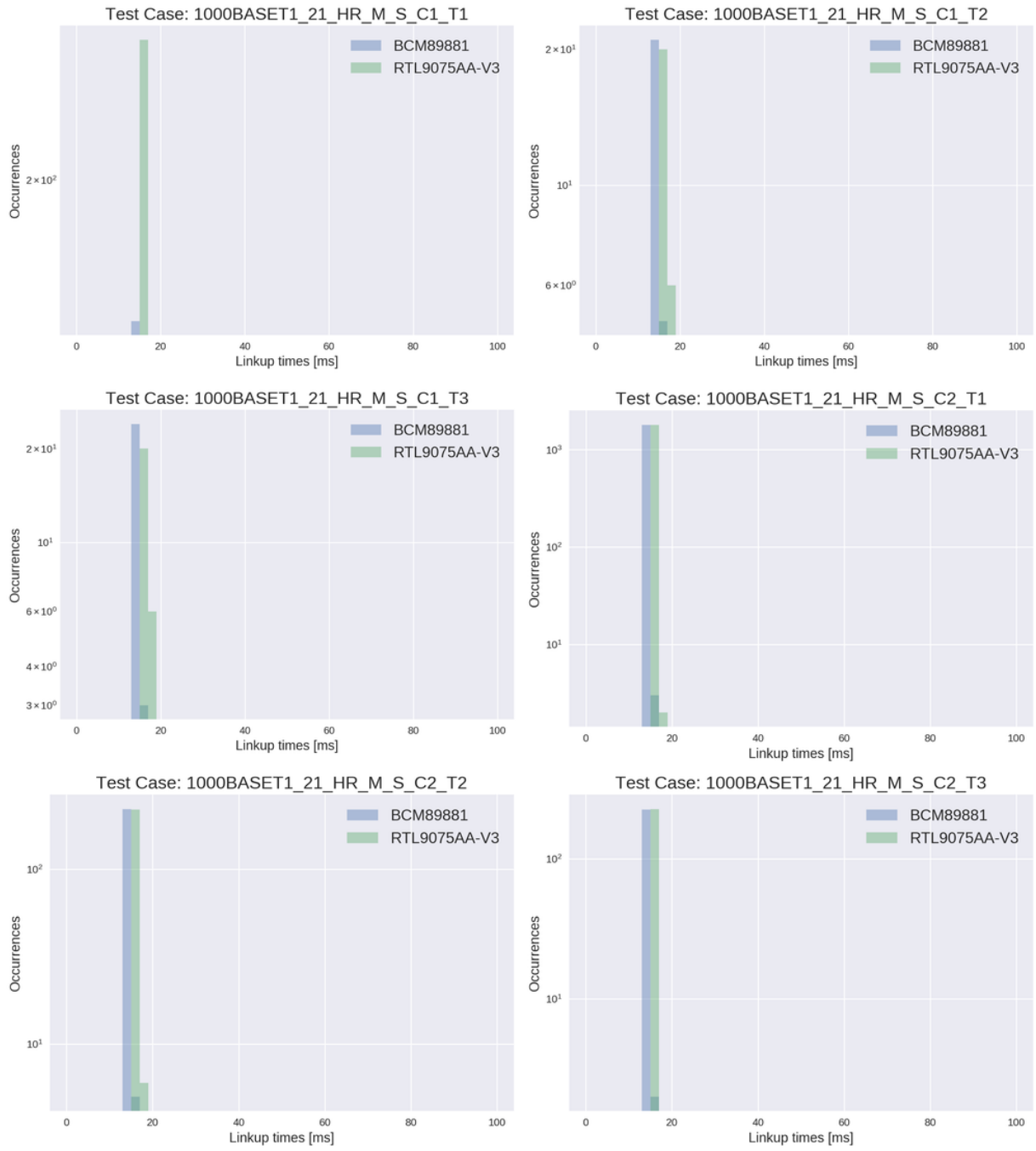

Figure 9: Link time distributions for IOP_21 with DUT as master and hard reset

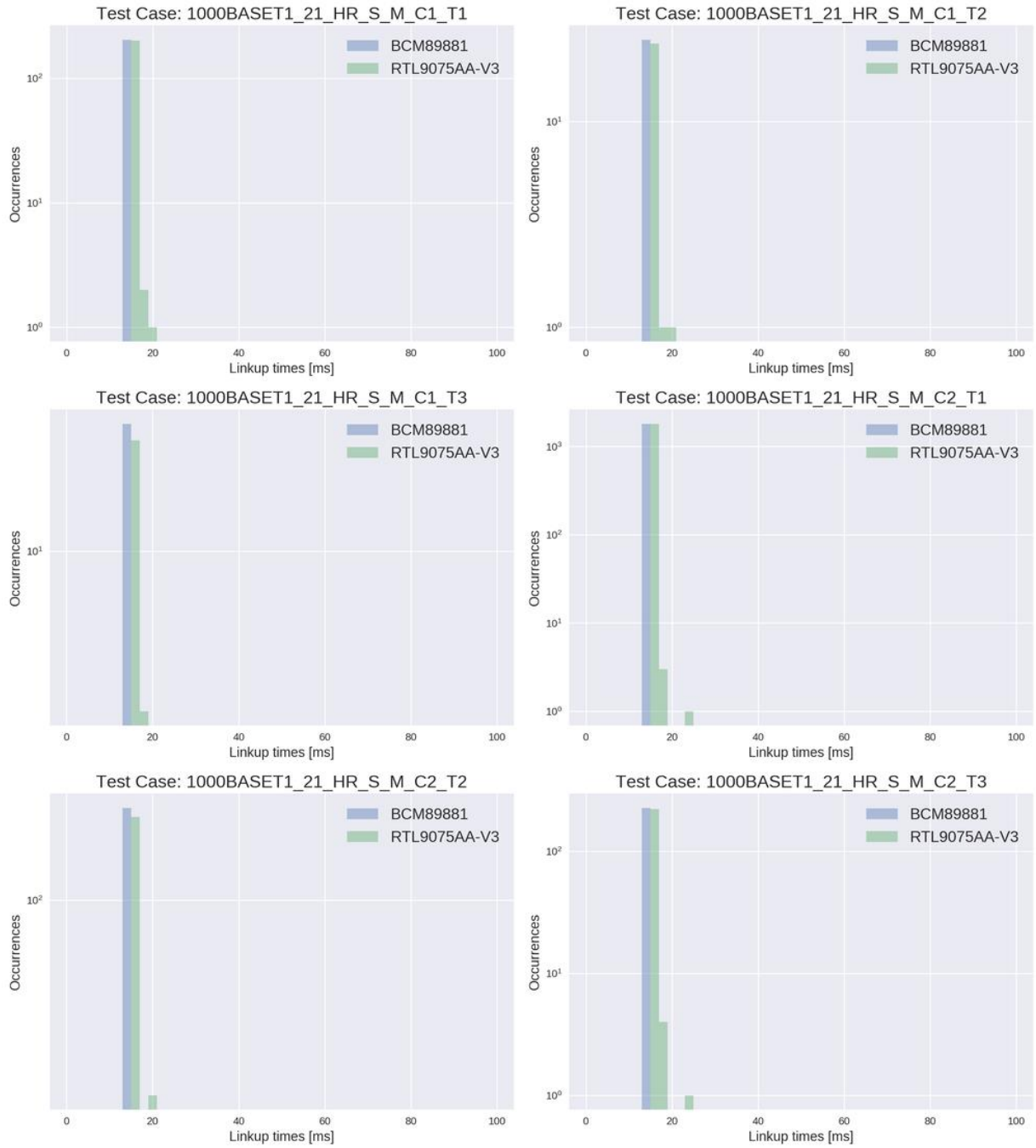

Figure 10: Link time distributions for IOP_21 with DUT as slave and hard reset

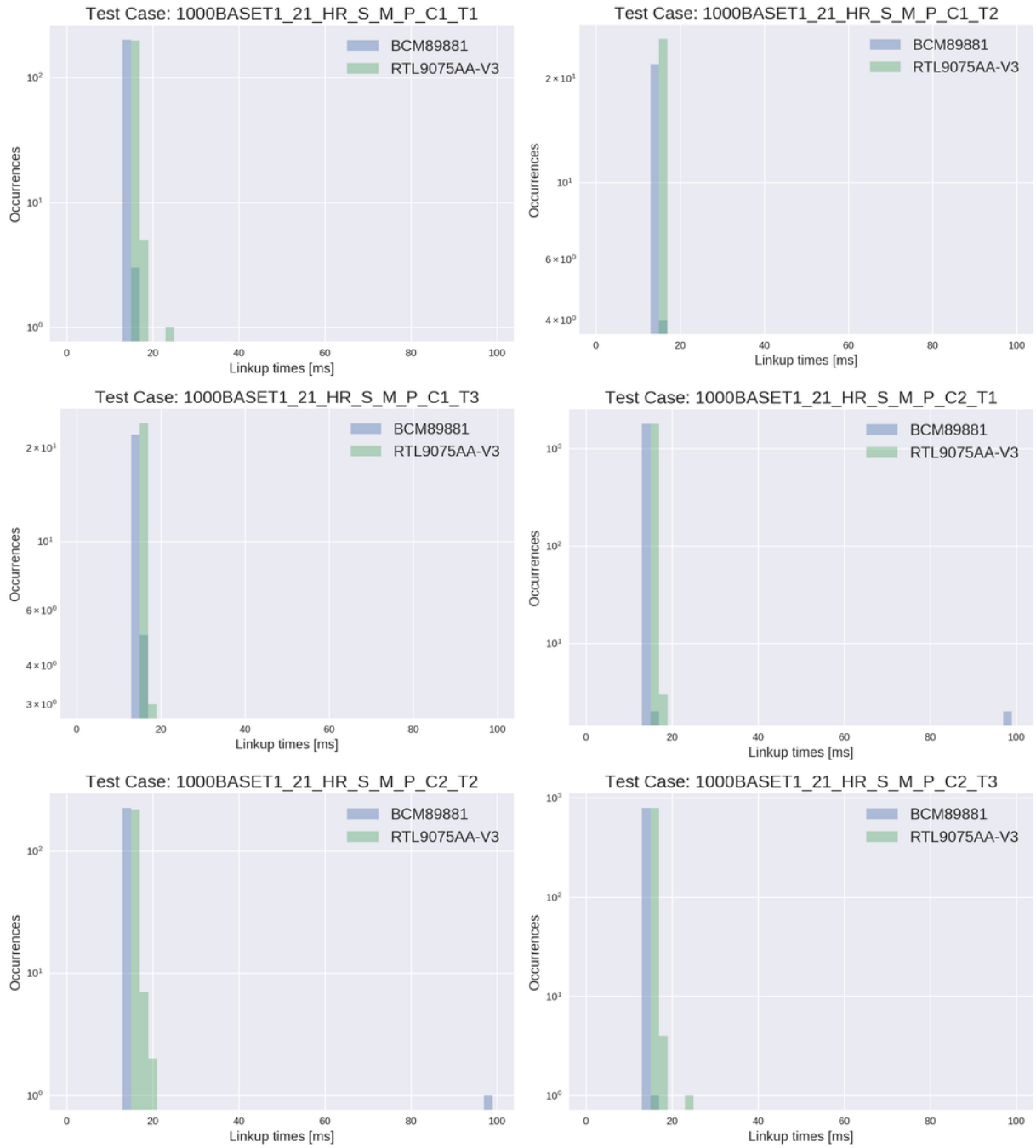

Figure 11: Link time distributions for IOP_21 with DUT as slave, swapped polarity and hard reset

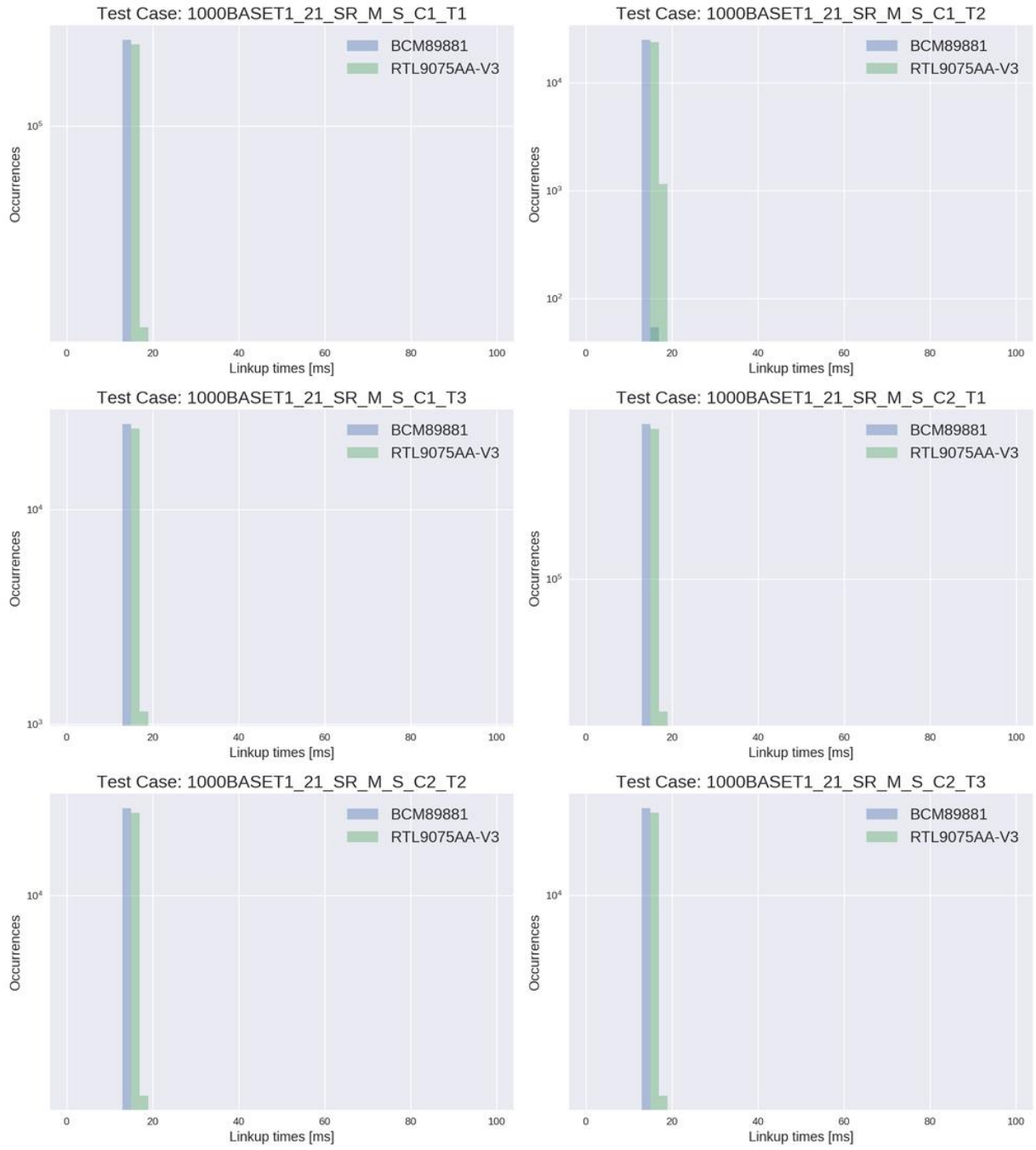

Figure 12: Link time distributions for IOP_21 with DUT as master and soft reset

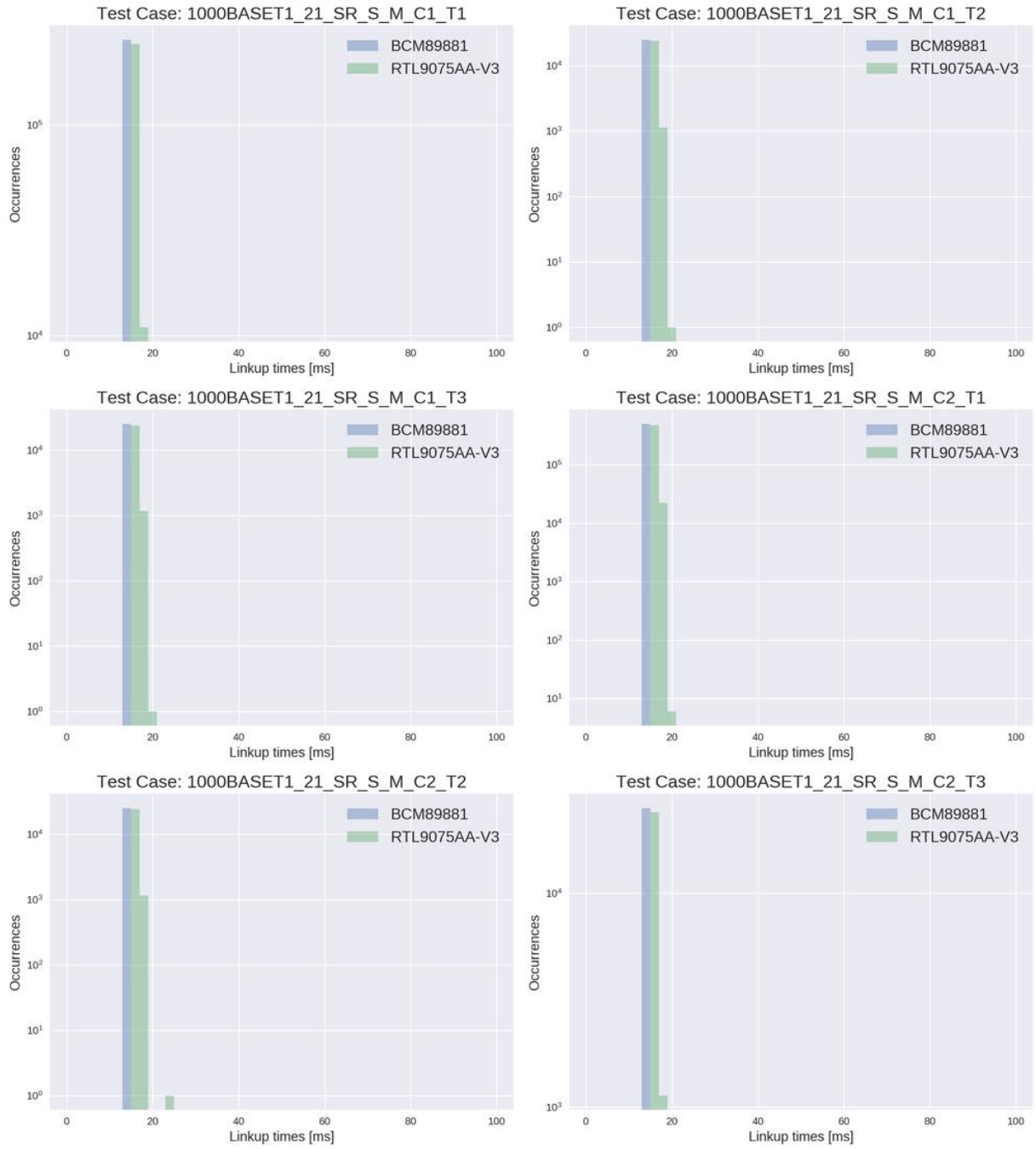

Figure 13: Link time distributions for IOP_21 with DUT as slave and soft reset

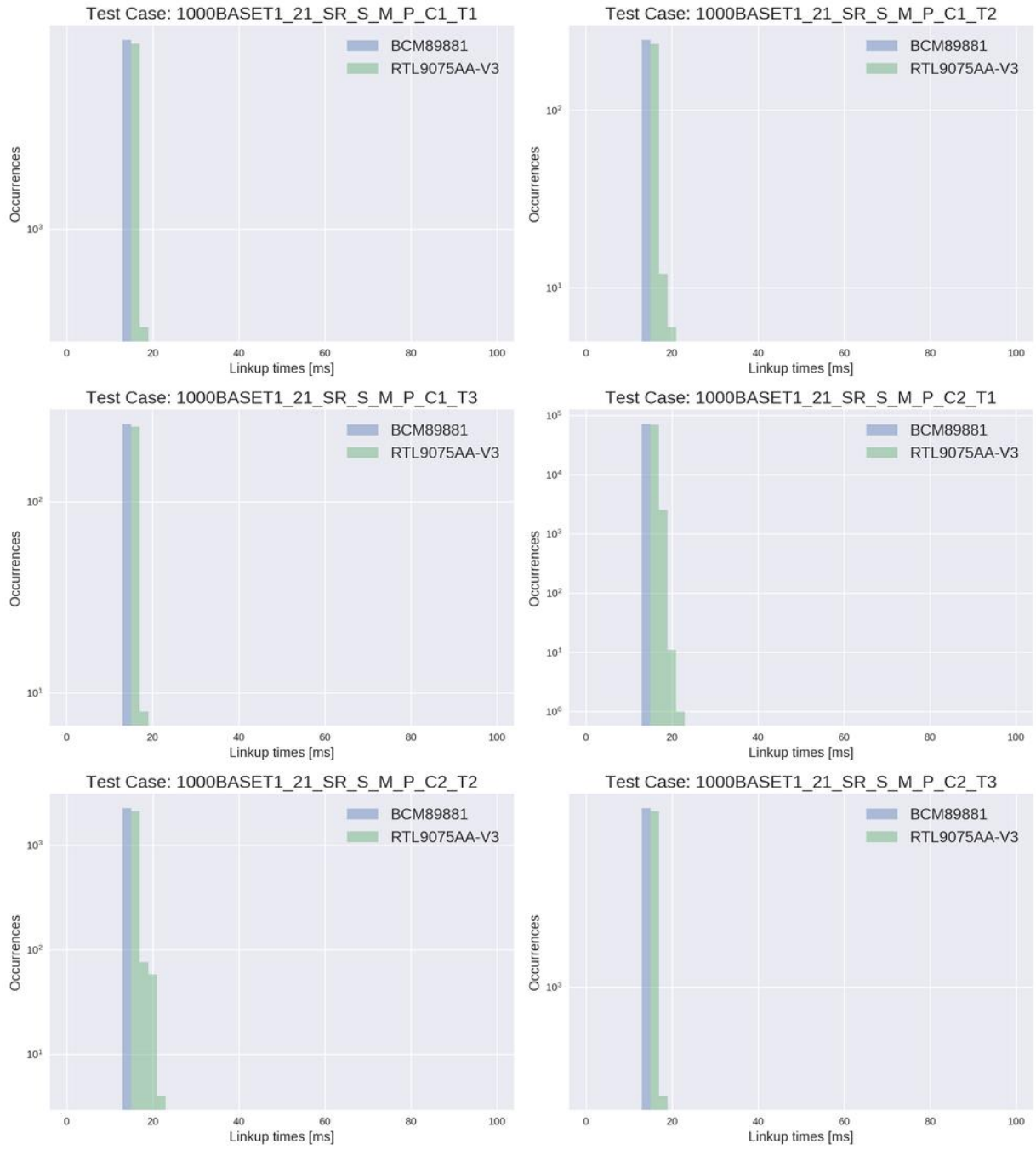

Figure 14: Link time distributions for IOP_21 with DUT as slave, swapped polarity and soft reset

7.2 IOP_22 Link-up after reset of link-partner

Test Case Description

This test case shall ensure that the PHY is able to establish a link after the link partner's PHY has been reset and reconfigured within a given time limit.

1. DUT shall wait until the PHY indicates an active link.
2. DUT shall trigger a soft-/hard-reset of the link partner's PHY or wait until the link partner has reset its PHY.
3. DUT shall start timer t0 directly after the reset of the LP's PHY.
4. The link partner must configure its PHY within 20ms after the reset.
5. DUT must ignore any indicated active links within 25ms after the reset.
6. 25ms after LP's reset: DUT shall wait until the PHY indicates an active link and stop timer t0.
7. DUT shall monitor whether the link status remains active for at least 750ms after initial link-up.

Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled:

- DUT's PHY reported link-up within 120ms after reset of the LP's PHY (t0 <= 120ms).
- Link did not go down after test step 5.

7.2.1 Observation: Link-up times

The next figures show the link-up times distribution for every test case 22 and against each link partner.

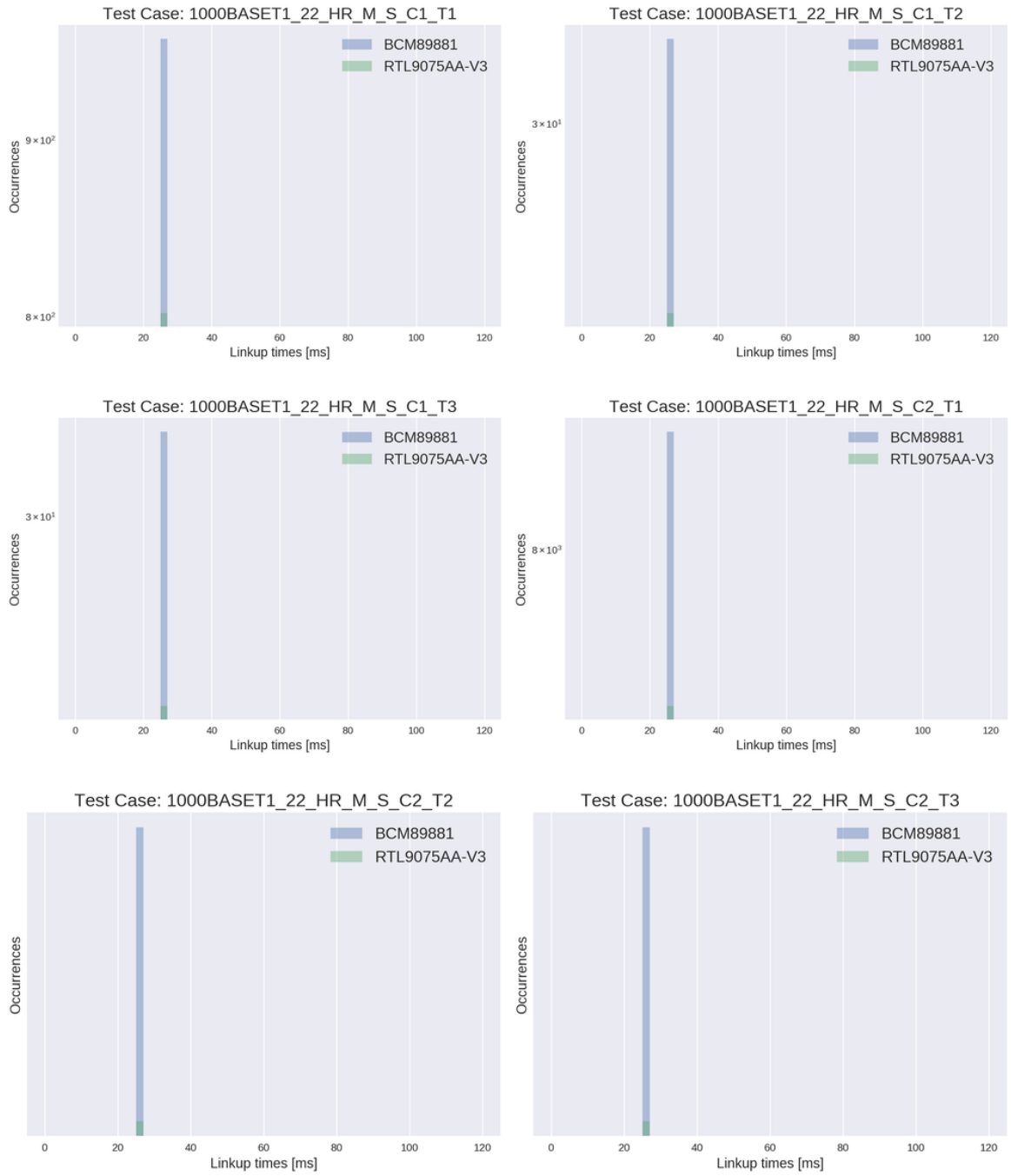

Figure 15: Link time distributions for IOP_22 with DUT as master and hard reset

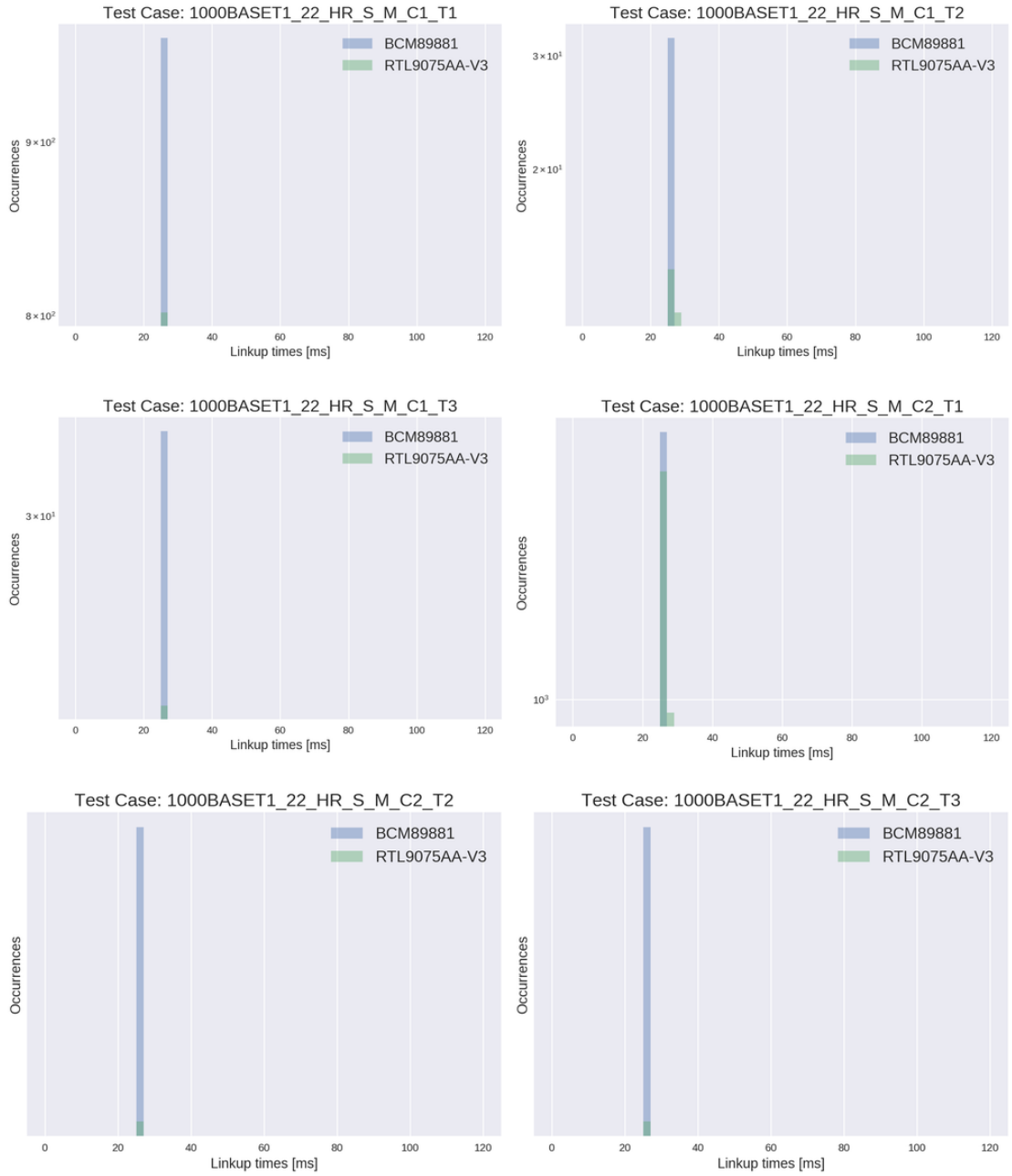

Figure 16: Link time distributions for IOP_22 with DUT as slave and hard reset

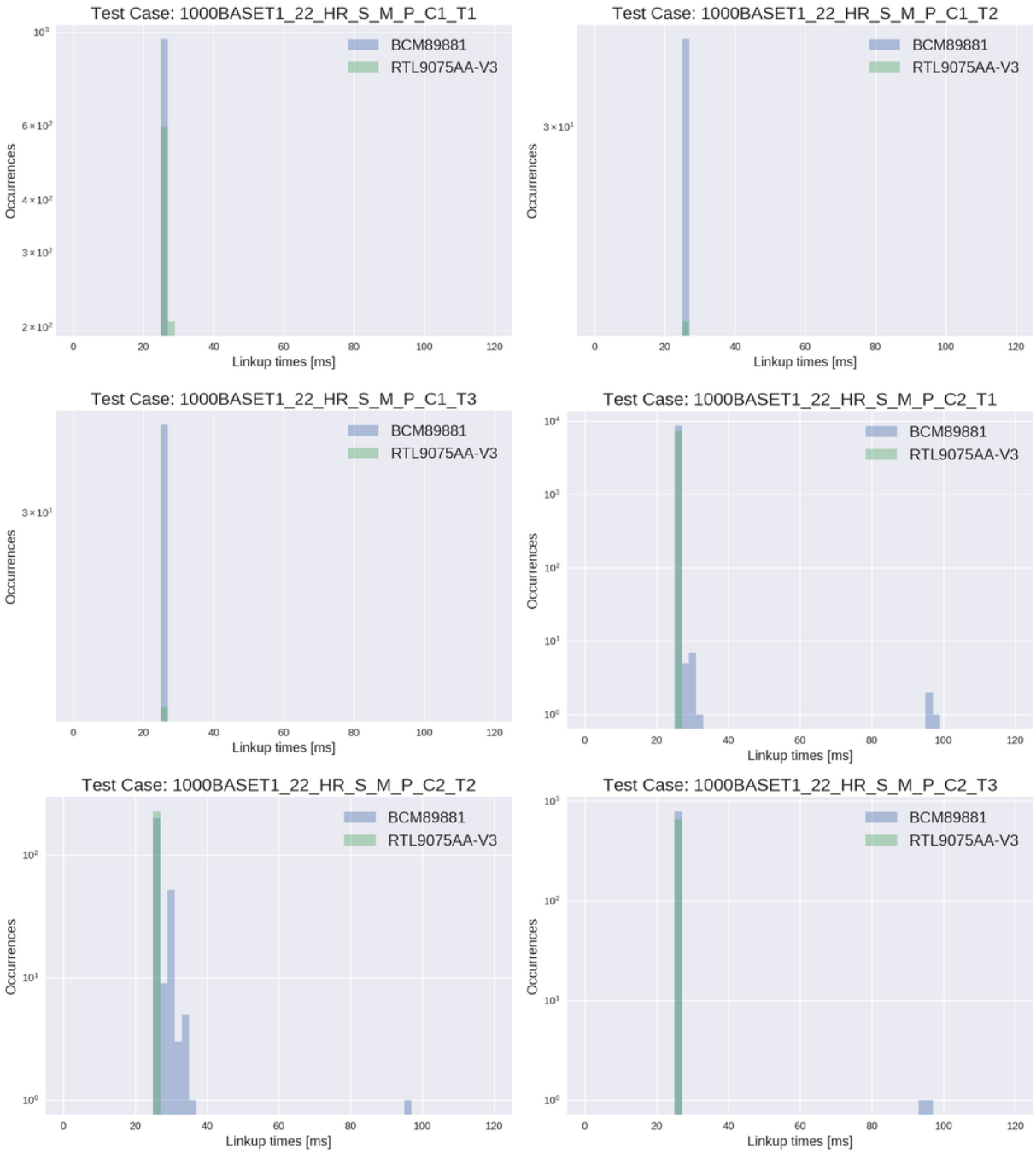

Figure 17: Link time distributions for IOP_22 with swapped polarity and hard reset

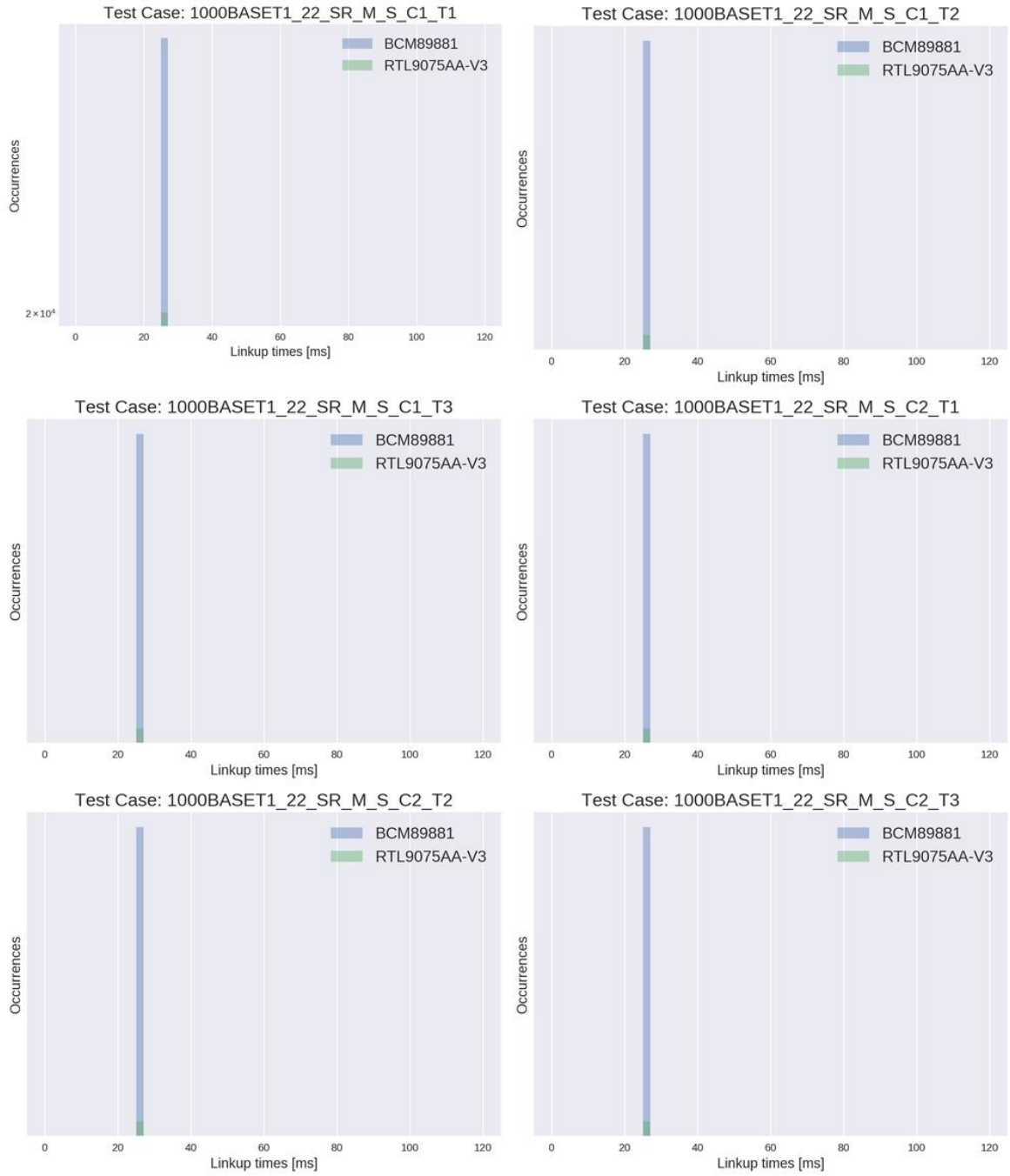

Figure 18: Link time distributions for IOP_22 with DUT as master and soft reset

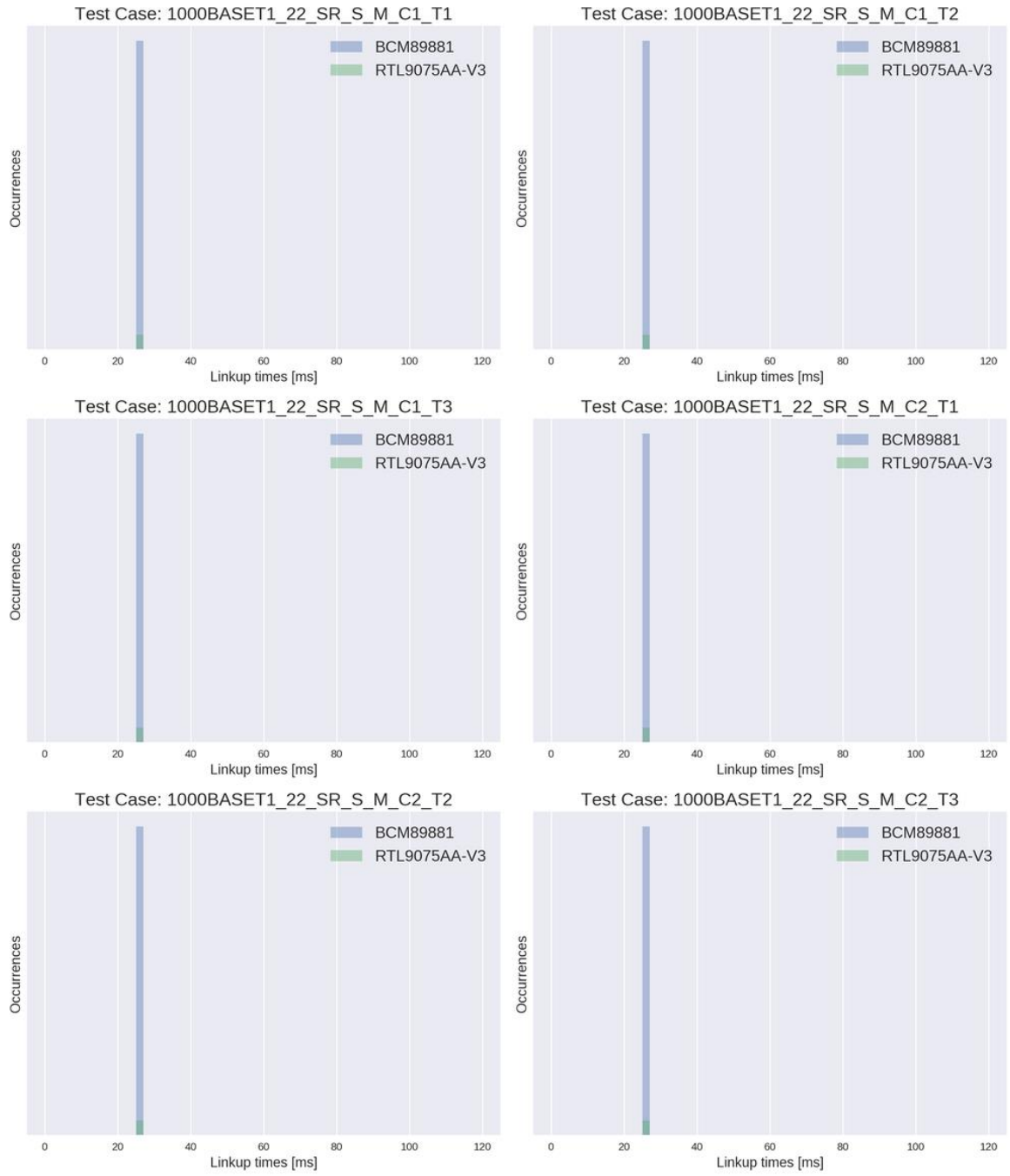

Figure 19: Link time distributions for IOP_22 with DUT as slave and soft reset

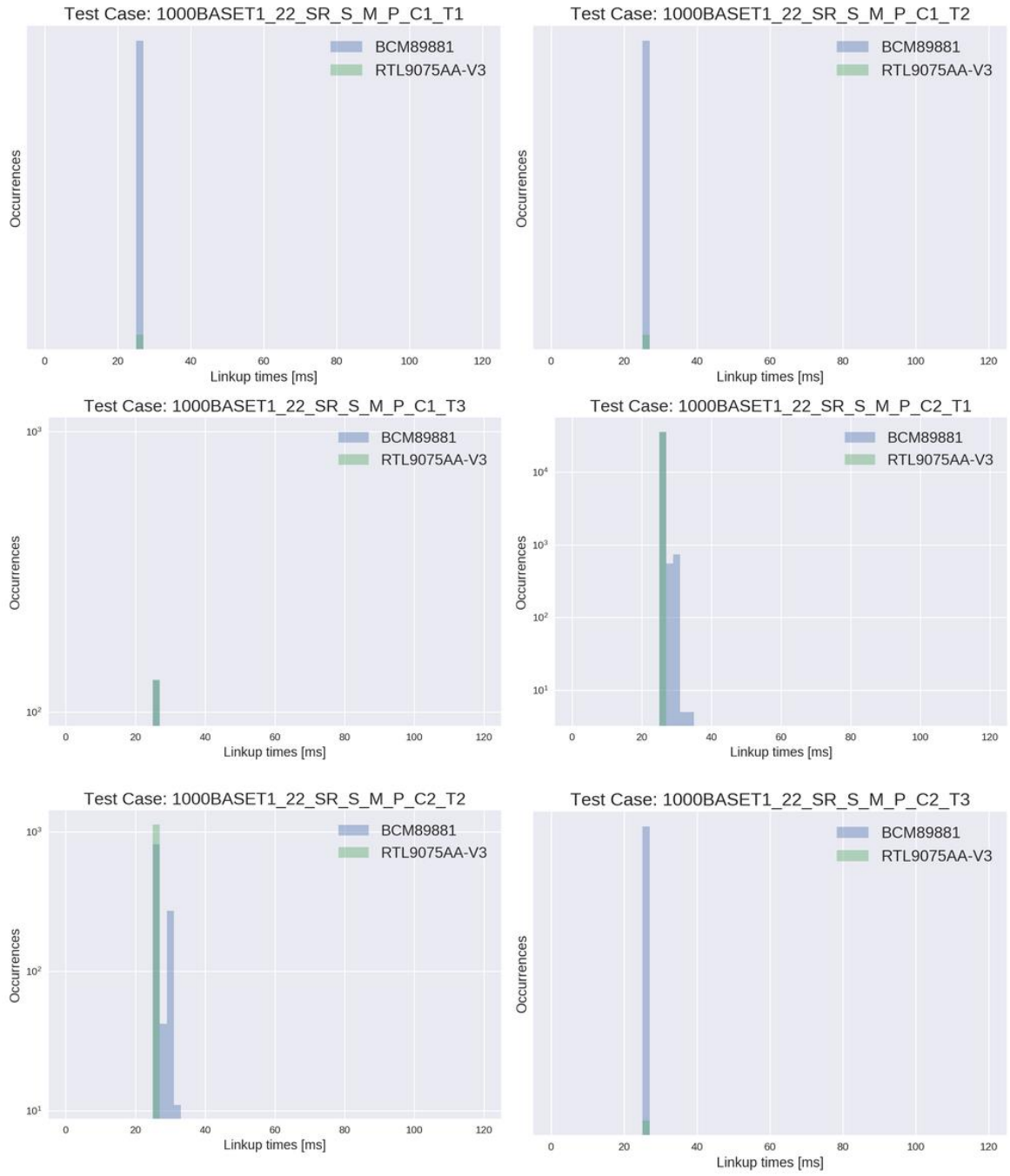

Figure 20: Link time distributions for IOP_22 with swapped polarity and soft reset

7.3 IOP_24a Indicated signal quality for channel with decreasing quality

Test Case Description

This test case shall ensure that the PHY's indicated signal quality decreases for a channel with decreasing channel quality.

1. DUT shall soft reset and reconfigure its PHY.
2. Remove any artificial channel degradation, to ensure that the highest possible signal quality is reached on both the DUT and LP.
3. Measure the PHY's SQI value for at least 100 times. Determine and store the minimum and maximum SQI read values.
4. Increase artificial noise level by one step, i.e. by 0.1dB Gaussian noise generator output.
5. Repeat steps 3 and 4 for ten additional noise levels after the PHY can no longer establish a link.

Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.

- SQI value:
  - Steadily and monotonically decreased by one step each
  - SQI values are only valid if link-up condition is present
- Link status
  - Link-up status remains for SQI values higher than 0
  - No link instabilities with intermittently link drops should be observed between SQI values higher than 0.

7.3.1 Observation: Signal quality for channel with decreasing quality

For the test cases with decreasing quality on the channel, the SQI value did steadily and monotonically decrease by one step each, leading to an overall PASS verdict.

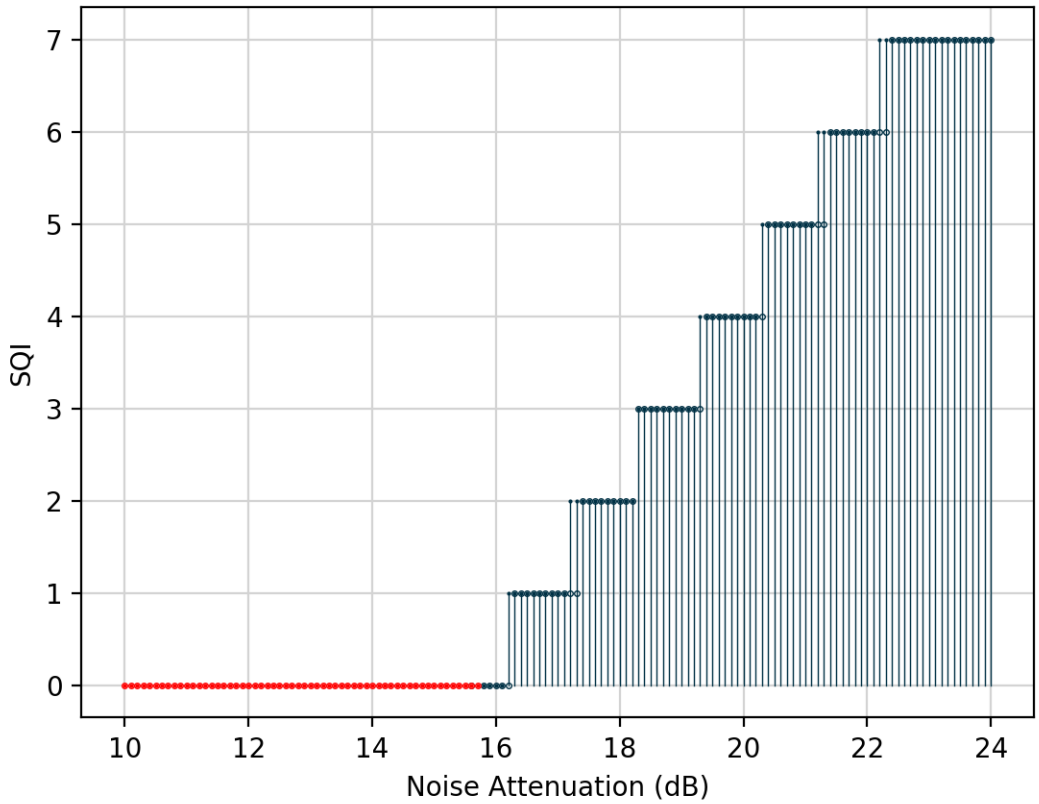

Figure 21: 1000BASET1_IOP_24a_SR_M_S_C1_T1

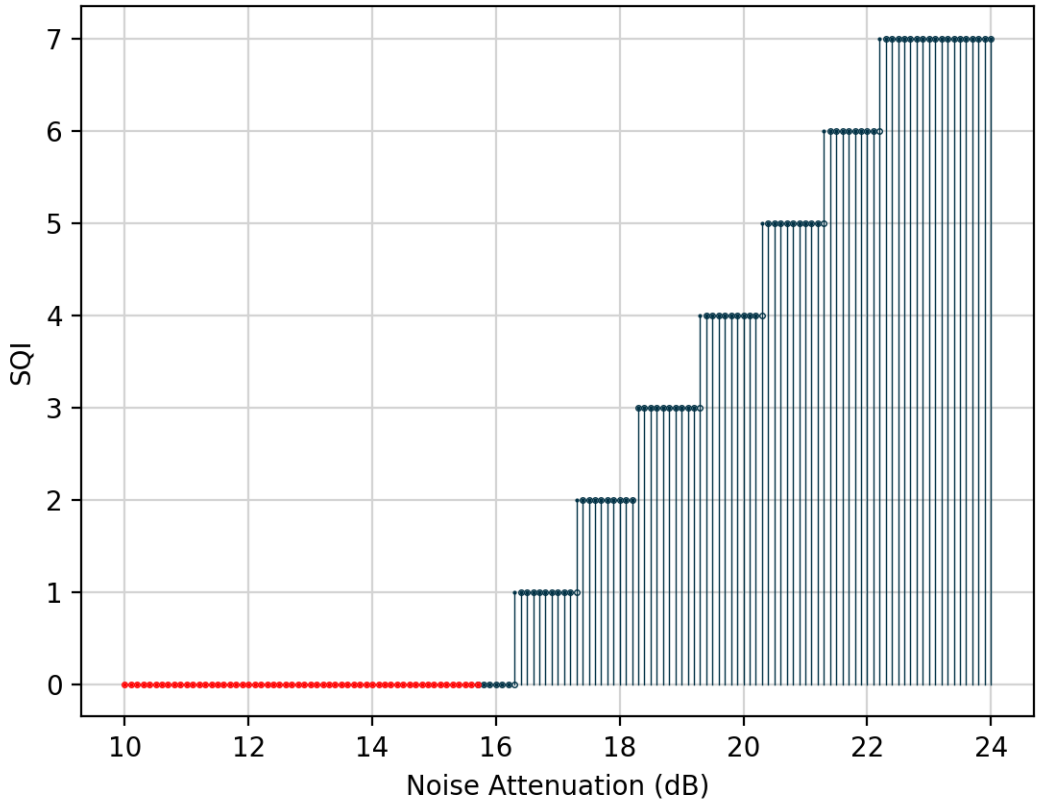

Figure 22: 1000BASET1_IOP_24a_SR_S_M_C1_T1

7.4 IOP_24b Indicated signal quality for channel with increasing quality

Test Case Description

This test case shall ensure that the PHY's indicated signal quality increases for a channel with increasing channel quality.

1. Start with the highest artificial noise channel degradation the DUT's PHY can no longer establish a link.
2. DUT shall soft reset and reconfigure its PHY.
3. Measure the PHY's SQI value for at least 100 times. Determine and store the minimum and maximum SQI read values.
4. Decrease artificial noise by one step, i.e. by 0.1 dB Gaussian noise generator output.
5. Repeat steps 3 and 4 until no artificial noise is applied.

Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.

- SQI value:
  - Steadily and monotonically increased by on step each
  - SQI values are only valid if link-up condition is present
- Link status
  - Link-up status remains for SQI values higher than 0
  - No link instabilities with intermittently link drops should be observed between SQI values higher than 0.

7.4.1 Observation: Signal quality for channel with increasing quality

For the test cases with increasing quality on the channel, the SQI value was steadily and monotonically increased by one step each, leading to an overall PASS verdict.

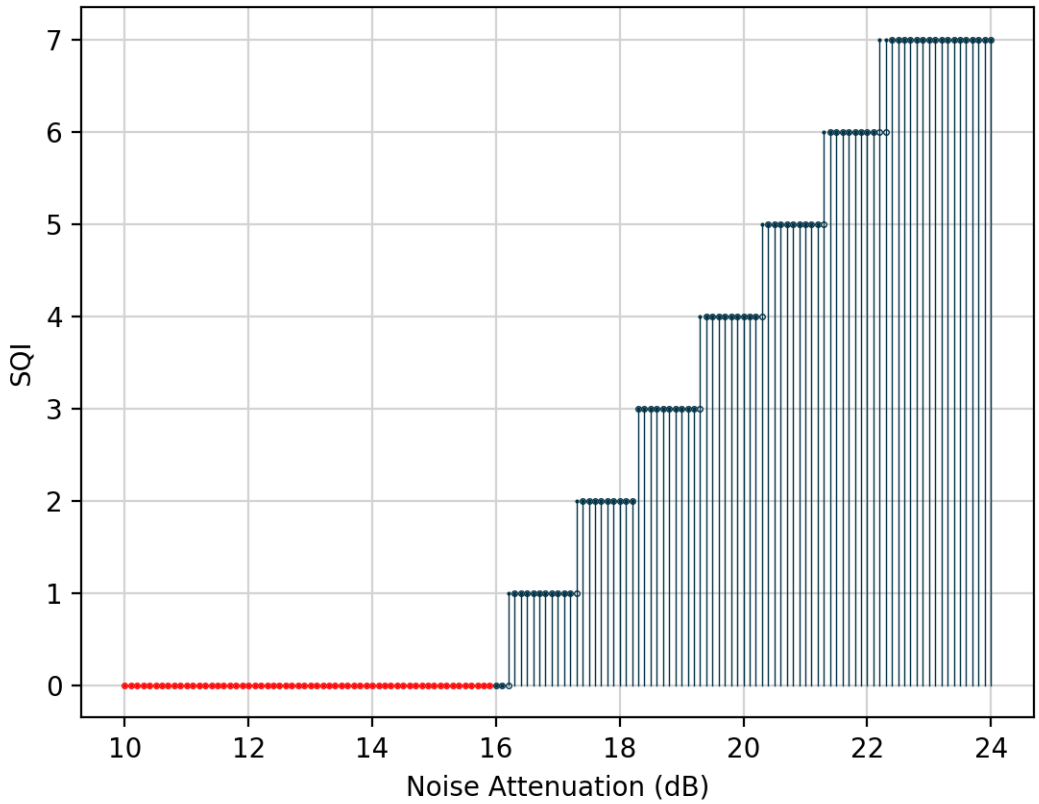

Figure 23: 1000BASE_T1_IOP_24b_SR_M_S_C1_T1

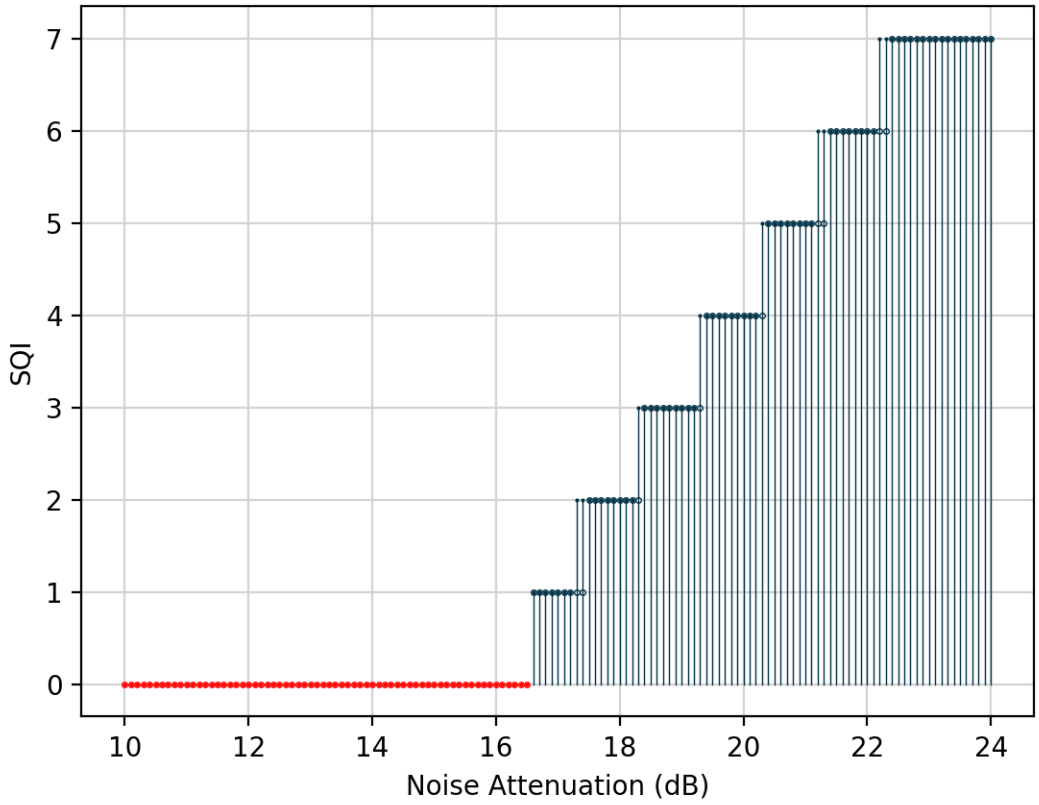

Figure 24: 1000BASE_T1_IOP_24b_SR_S_M_C1_T1

8 Annex

8.1 Result description

Result/Status	Meaning/Description
PASS	the expected results from the test specification are fulfilled
FAIL	• the expected results from the test specification are not fulfilled or **or** • the device lacks the functionality to execute the test case
PASS with remark	the expected results from the test specification are fulfilled, but observations were also made during test execution
INCONCLUSIVE	one or more results are not within the test specification with complete measurement uncertainty
IN PROGRESS	the test case has not yet been completed (*only in preliminary test reports*)
NOT APPLICABLE	this (optional) test case is not applicable to the device
NOT SUPPORTED	the optional functionality shown in this test case is not supported by the device
NOT TESTED	• not included in the order *or* • not feasible by C&S
INFO	the test case is performed in addition to the scope of the order and for informational purposes only

8.2 Configuration Script

```
void BCM_89881::init_phy()
{
    cyg_uint16 regData = 0;

    // ##########################################
    // Begin Broadcom 89881 1G specific configuration
    // ##########################################

    WriteRegister(7, 0x0200, 0x0200); // Restart auto negotiation
    WriteRegister(1, 0x932A, 0x0002); // To disable superisolate

    regData = ReadExtRegister(1, 0xA015);
    // Select RGMII 2.5V
    WriteRegister(1, 0xA015, (regData & 0xFFC7) | 0x10);

    regData = ReadExtRegister(1, 0xA010);
    // change timing degrees
    WriteRegister(1, 0xA010, (regData & 0xFFFC) | 0x1);

    // Enable and configure BCM LEDs
    WriteRegister(1, 0x931D, 0x3410); // CORE_MISC_SHD1C_0D
    WriteRegister(1, 0x931E, 0x3863); // CORE_MISC_SHD1C_0E
    WriteRegister(1, 0xA027, 0x0317); // TOP_MISC_LED_INTR_CTL
    WriteRegister(1, 0x9319, 0x2508); // CORE_MISC_SHD1C_09

    // ########################################
    // End Broadcom 89881 1G specific configuration
    // ########################################
}
```

8.3 SQI function

```
/*
 * Routine to read and compute current SQI value
 */
cyg_uint8 BCM_89881::GetSQI() {
    uint16_t sqi = 0;
    uint16_t sqi_avg = 0;

    // initialization for SQI from 2020-08-05
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_0
    WriteRegister(1, 0x8053, 0x00C3);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_1
    WriteRegister(1, 0x8054, 0x009B);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_2
    WriteRegister(1, 0x8055, 0x007B);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_3
    WriteRegister(1, 0x8056, 0x0062);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_4
    WriteRegister(1, 0x8057, 0x004E);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_5
    WriteRegister(1, 0x8058, 0x003E);
    // PHYCONTROL_TC1_DCQ_SQI_THRESHOLD_6
    WriteRegister(1, 0x8059, 0x0031);
    // initialization end

    // Read register 0x1.0x8052 bit [3:1] for SQI level.
    for(int i = 0; i < 50; i++){
        sqi = ReadExtRegister(1, 0x8052);
        sqi = (sqi >> 1) & 0x7;
        sqi_avg = sqi_avg + sqi;
    }

    sqi_avg = sqi_avg / 50;

    return sqi_avg;
}
```