Exercises for Week 6
Textbook Sections 4.1 to 4.4
Sample Solutions

Question 1

Based on Textbook Exercise 4.1 <§4.3>.

Consider the following instruction:

Instruction: `or rd,rs1,rs2`

Interpretation: `Reg[rd] = Reg[rs1] OR Reg[rs2]`

a. What are the values of control signals generated by the control in Figure 4.11 for this instruction?

The values of the signals are as follows:

RegWrite	ALUSrc	ALUop	MemRead	MemWrite	MemtoReg	PCSrc
1	0	OR	0	0	0 (ALU)	0

ALUSrc is the control signal that controls the Mux at the ALU input: 0 (Reg) selects the output of the register file and 1 (Imm) selects the immediate from the instruction word as the second input to the ALU.

MemtoReg is the control signal that controls the Mux at the Data input to the register file: 0 (ALU) selects the output of the ALU and 1 (Mem) selects the output of memory.

b. Which resources (blocks) perform a useful function for this instruction?

PC, Add (PC+4), PCSrc mux, Instruction memory, Registers, ALUSrc mux, MemtoReg mux.

c. Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

Outputs that are not used: Imm Gen, Shift left 1, Add (branch target).

No outputs: Data Memory.

Question 2

Based on Textbook Exercise 4.5 <§4.4>.

In this exercise we examine in detail how an instruction is executed in the single-cycle datapath of Figure 4.17. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word: `0x00c6ba23`.

0000 0000 1100 0110 1011 1010 0010 0011

0000000 01100 01101 011 10100 0100011
imm[11:5] rs2 rs1 funct3 imm[4:0] opcode

opcode = 0x23, funct3 = 011: sd
rs1 = x13, rs2 = x12, imm = 0x014
sd x12, 0x014(x13)

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

x0	x1	x2	x3	x4	x5	x6	x8	x12	x13	PC
0	0x06E0	0xFF30	2	4	10	6	8	42	0xFF10	0x1240

a. What are the values of the ALU control unit's inputs for this instruction?

From Figure 4.18, for sd instruction, ALUOp = 00

Instruction[30, 14-12] = 0 011, but this is not used when ALUOp = 00

b. What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

New PC value is old PC + 4 = 0x1244.

Path is from PC output to Add (PC+4) to branch mux to PC input.

c. For each mux, show the values of its data output during the execution of this instruction and these register values.

Branch mux: 0x0000000000001244

ALUSrc mux: value of Imm Gen, ie, 0x0000000000000014.

MemtoReg mux: MemtoReg is X (don't care), which means it can be 0 or 1, so output is 0x0000000000000000 (memory read data) or 0x000000000000FF24 (ALU output, result of effective address calculation).

d. What are the input values for the ALU and the two add units?

ALU inputs: value of x13 register, ie, 0x000000000000FF10; and value of ALUSrc mux, ie, 0x0000000000000014.

For Add PC+4: old PC, ie, 0x0000000000001240; and 4.

For Add branch: old PC, ie, 0x0000000000001240; and Imm Gen value shifted left 1, ie, 0x0000000000000028.

e. What are the values of all inputs for the registers unit?

Read register 1: 13 (Instruction[19-15])

Read register 2: 12 (Intruction[24-20])

Write register: 10100 (Instruction[11-7], though not used, since RegWrite is 0)

Write data: 0x0000000000000000 or 0x000000000000FF24 (output of MemtoReg mux)

Question 3

Textbook Exercise 4.7 <§4.4>.

Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I-Mem/ D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Imm Gen	Control
250ps	150ps	25ps	200ps	150ps	5ps	30ps	20ps	50ps	50ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

a. What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?

The paths for an R-type instruction are:

- Register read (PC) -> I-Mem -> Register File -> ALUSrc mux -> ALU -> MemtoReg mux -> Register Setup (Register File):
  30ps + 250ps + 150ps + 25ps + 200ps + 25ps + 20ps = 700ps
- The path from I-mem -> Control -> ALU operates in parallel with I-Mem -> Register File -> ALUSrc mux -> ALU. But Control (50ps) is shorter than Register File + ALUSrc mux, so it is not on the critical path.
- Register read (PC) -> Add -> Mux -> Register Setup (PC): 30ps + 150ps + 25ps + 20ps = 225ps.

Critical path is the longest of these: 700ps.

b. What is the latency of ld? (Check your answer carefully. Many students place extra muxes on the critical path.)

The paths for a ld instruction are:

- Register read (PC) -> I-Mem -> Register File -> ALU -> D-Mem -> MemtoReg mux -> Register Setup (Register File):
  30ps + 250ps + 150ps + 200ps + 250ps + 25ps + 20ps = 925ps
- The path from I-mem -> Imm Gen -> ALUSrc mux -> ALU operates in parallel with I-Mem -> Register File -> ALU, but Imm Gen (50ps) -> ALUSrc mux (25ps) is shorter than Register File, so it is not on the critical path.
- Path from I-mem -> Control -> ALU: as per (a).
- Path from Register read (PC) -> Add -> Mux -> Register Setup (PC): as per (a).

Critical path is the longest of these: 925ps

c. What is the latency of sd? (Check your answer carefully. Many students place extra muxes on the critical path.)

- Register read (PC) -> I-Mem -> Register File -> ALU -> D-Mem:
  30ps + 250ps + 150ps + 250ps = 680ps
- I-mem -> Imm Gen -> ALUSrc mux -> ALU: as per (b)
- Register read (PC) -> I-Mem -> Register File -> D-Mem:
  30ps + 250ps + 250ps = 530ps
- Other shorter paths as per (a).

Critical path is the longest of these: 680ps

d. What is the latency of beq?

- Register read (PC) -> I-Mem -> Register File -> ALUSrc mux -> ALU -> Gate -> Mux -> Register Setup (PC):
  30ps + 250ps + 150ps + 25ps + 200ps + 5ps + 25ps + 20ps = 705ps
- Path Imm Gen -> Shift left 1 -> Add is shorter than Register File -> Mux -> ALU -> Gate
- Path through Control is shorter as per (a).

Critical path is 705ps.

e. What is the latency of an I-type instruction?

Similar to R-type, but path through Imm Gen -> ALUSrc Mux, which is shorter than Register File. So critical path is:

- Register read (PC) -> I-Mem -> Register File -> ALU -> MemtoReg mux -> Register Setup (Register File):
  30ps + 250ps + 150ps + 200ps + 25ps + 20ps = 675ps

f. What is the minimum clock period for this CPU?

Clock period must be long enough for the longest instruction, namely, a ld instruction (925ps). So that is the minimum clock period.