Exercises for Week 6
Textbook Sections 4.1 to 4.4

Question 1

Based on Textbook Exercise 4.1 <§4.3>.

Consider the following instruction:

Instruction: `or rd,rs1,rs2`

Interpretation: `Reg[rd] = Reg[rs1] OR Reg[rs2]`

a. What are the values of control signals generated by the control in Figure 4.11 for this instruction?

b. Which resources (blocks) perform a useful function for this instruction?

c. Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

Question 2

Based on Textbook Exercise 4.5 <§4.4>.

In this exercise we examine in detail how an instruction is executed in the single-cycle datapath of Figure 4.17. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word: `0x00c6ba23`.

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

x0	x1	x2	x3	x4	x5	x6	x8	x12	x13	PC
0	0x06E0	0xFF30	2	4	10	6	8	42	0xFF10	0x1240

a. What are the values of the ALU control unit's inputs for this instruction?

b. What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

c. For each mux, show the values of its data output during the execution of this instruction and these register values.

d. What are the input values for the ALU and the two add units?

e. What are the values of all inputs for the registers unit?

Question 3

Textbook Exercise 4.7 <§4.4>.

Problems in this exercise assume that the logic blocks used to implement a processor's datapath have the following latencies:

I-Mem/ D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Imm Gen	Control
250ps	150ps	25ps	200ps	150ps	5ps	30ps	20ps	50ps	50ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

a. What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?

b. What is the latency of ld? (Check your answer carefully. Many students place extra muxes on the critical path.)

c. What is the latency of sd? (Check your answer carefully. Many students place extra muxes on the critical path.)

d. What is the latency of beq?

e. What is the latency of an I-type instruction?

f. What is the minimum clock period for this CPU?