

Quantum power multiplexer

User manual

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Introduction	1
Specification	2
Circuit description	3
Slave board	3
Master board	6
Power-on state	8
Firmware and Flow chart	8
Switching sequence matrix	9
Remote operation	9
Switching pseudocode	10
Local operation	11
Installation and connections	12
Test points list	16
List of resources	17

Introduction

The multiplexer is built in a modular form, with a master board that controls slave boards and includes timing functionalities. The slave boards have a single pole and double throw (SPDT or 2-to-1), or a single pole and four throw (SPFT or 4-to-1). The user can use many of them controlled by the master, as the next figure shows.

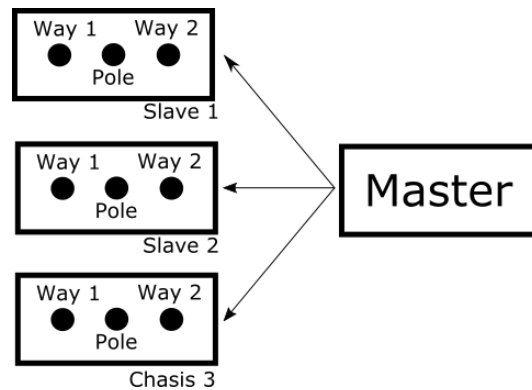


Figure 1: three slave boards SPDT controlled by a single master board.

Specification

The modular design of the multiplexer allows multiple configurations that can be selected by the user connecting the boards between them. The multiplexer uses the strategies break-before-make in order to avoid short circuits between sources and it switches synchronized with an external signal.

The signals are considered differential, so the switch commutes positive and negative terminals of the voltage source. Two slave boards have been designed, one has two throws and one pole, as the next figure shows, and the other has four throws and one pole. The slave board is reversible; the SPDT board can be considered as 2 inputs - 1 output (2-to-1) or 1 input - 2 output (1-to-2).

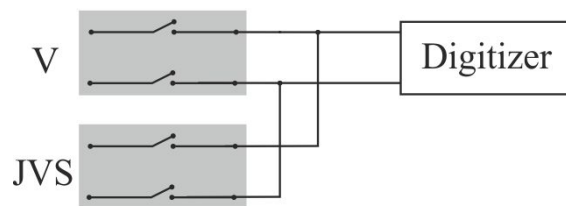


Figure 2: one slave board SPDT ready to measure a voltage source and the JVS.

Channel specification

- Maximum input voltage 60 V peak
- Turn on/off time: <3 ms
- Differential signal
- Coaxial connector for input and output signals

- Bounce-free operation
- Individual Guard connection for each signals (binding post)
- Ground connection for the multiplexer

General specification

- Trigger input (BNC connector, opto-isolated)
- USB connection to PC for configuration and control
- 9 V DC External supply

Uncertainty contribution

- 0.5 ohm On-resistance
- Off-isolation at 1 MHz < -90 dB
- Crosstalk at 1 MHz < 100 dB
- Uncertainty contribution < 0.2 ppm at power line frequency
- Maximum signal frequency 1 kHz to uncertainty lower than 1 ppm

Circuit description

Slave board

Each switch is built in T-configuration using three solid-state relays to improve the overall off-isolation. The next figure shows a simple scheme in the blue box, S1 is connected to the voltage source and its output is connected with two relays. S3 connects the signal path to ground and S2 connects the signal path to the output. The figure shows the circuit schematic, the relays U3 - U7 are the signal relay for the high terminal and the U4 - U8 for the low terminal. The relays U5 and U6 are used to tie to ground the middle point, the ground is floating and can be connected to the source ground. The capacitances and resistor networks are used to improve transition time and reduced charge injection.

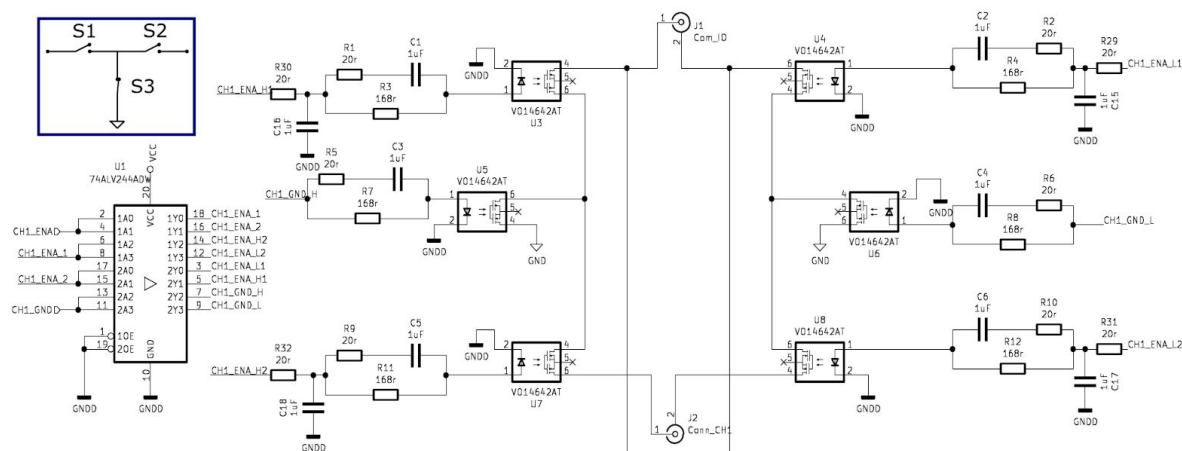


Figure 3: Circuit schematics for one differential channel, the switches are connected for each polarity in T configuration as the blue box shows.

The circuit board has a coaxial design, minimizing inductance path and stray capacitance. The figure 4 shows the top and bottom side of the slave-board, on one side are the high

terminal relays and the other side has the low terminal relays. Both sides are organized equally to minimize the area enclosed by the current path. Three guarding rings are used to reduce the stray capacitance between channels and output, they can be connected to the instrument's guards. Several test points were included to measure the digital signal, they are indicated in the top side.

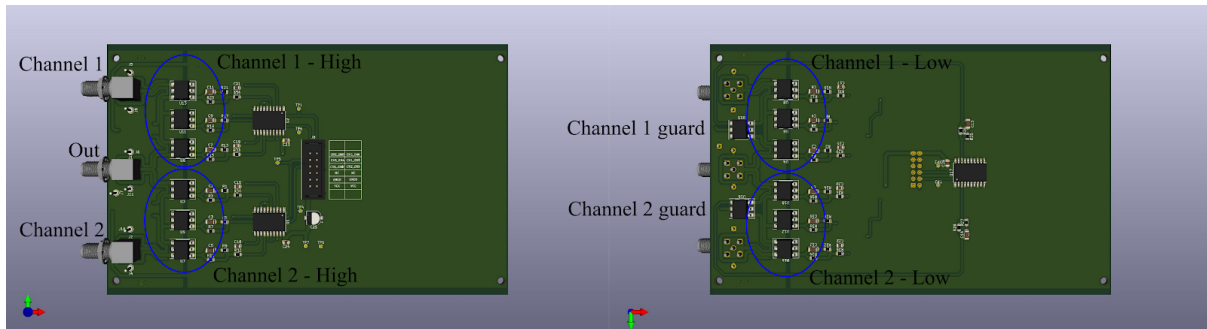


Figure 4: top and bottom of the slave 2-to1 board.

During the open or close process, the activation of each relay must be done preventing a short circuit. A break-before-make strategy is implemented: first all switches are opened and then the correct configuration is set. A secure time is included to prevent a short circuit and will be set considering the relay specifications.

Guard connection: The slave board has switches to connect the guard of each throw with the guard of the pole. The figure 5 shows the example to the slave board SPDT.

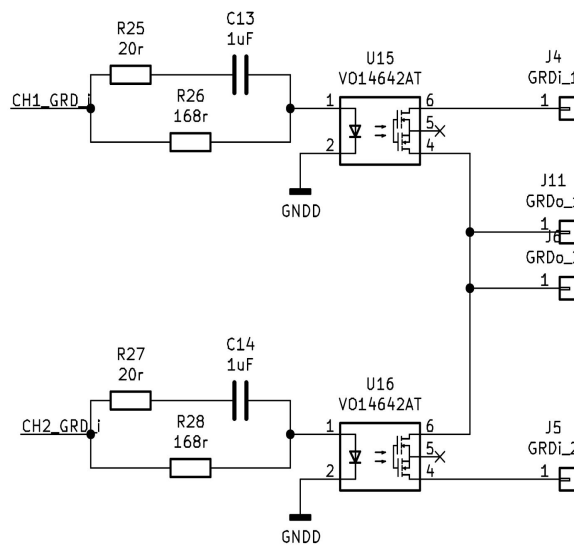


Figure 5: schematic circuit of the guard relays of the slave board SPDT.

Board connectors:**Table 1:** slave board connectors.

Identification	Connector
Control and supply	Ribbon Cable. PMOD interface.
Way 1, Way 2, Pole	SMA on board
Guard	Unipolar terminal
Ground	Unipolar terminal

Board digital pin-out: a 12-pin double-row connector (PMOD type) is used to connect the controller board and the relay board.

Table 2: slave board digital lines.

PIN	Name	Comment
1	CH02_GND	Channel 2 ground connection
2	CH02_ENA	Channel 2 enable
3	CH01_ENA	Channel 1 enable
4	CH01_GRD	Channel 1 guard connection
5	CH01_GND	Channel 1 ground connection
6	CH02_GRD	Channel 2 guard connection
7	BD	Digital line tied to GND to indicate that the board is connected.
8	No connected	No connected
9-10	GND	Digital ground
11-12	Vcc	Digital voltage supply

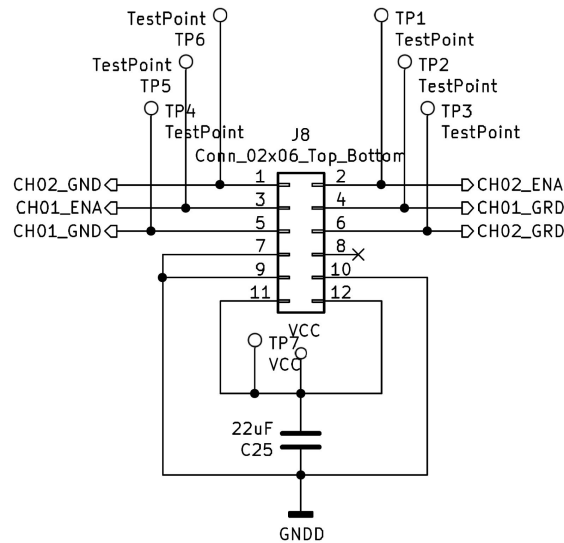


Figure 6: schematic circuit of the digital lines connector.

PhotoMos relay: the following table shows the characteristic of the relay used on the first prototype and its specification. It was selected due to its low on-resistance and availability.

Table 3: PhotoMos relay VO14642AABTR specification.

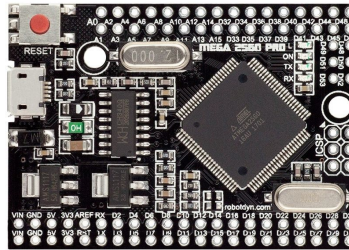
	VO14642AABTR
ON-Resistance	0.18 Ω (AC)
Max. voltage	60 V
On-time	370 μ s / 800 μ s
Off-time	50 μ s / 800 μ s
Stray capacitance	200 pF
Control current	0.5 mA to 20 mA
Family	Vishay

Other SMD relays with equivalent pinout can also be used, for example: PVG612ASPB, ASSR-1511-301E, TLP3545A, CT128/CS128, AQV252G3S, G3VM-101HR2 or PVN012APbF.

Master board

The master is built with an Arduino board and a shield board, this last one includes the connectors for 12 switches, and a voltage regulator to supply the slave boards. This voltage regulator is connected to an external supply of 12 V using a standard power connector Jack and Plug 2.1 mm x 5 mm. The arduino board and the display are supplied by the USB connector. The used display is a 16x4 liquid crystal display (LCD) with I2C Communication.

RobotDyn



38x55mm

Figure 7: Arduino board manufactured by RobotDyn,
<https://robotdyn.com/mega-2560-pro-embed-ch340g-atmega2560-16au.html>.

Table 4: master board connectors.

Identification	Connector
Control and supply for slave control	Ribbon Cable. PMOD type.
Supply	Screw terminal
Clock IN	Opto-isolated BNC
Communication to PC	USB

Table 5: master board buttons.

Identification	Button
RST	Reset the multiplexer to power-on state
LOC/REM	To select local and remote operation
ENA CH	Run the sequence step by step.
μ C RESET	Master reset. Microcontroller reset (hidden button)

Power-on state

- 1) All channels OPEN
- 2) All GRD OPEN
- 3) Local operation
- 4) Trigger Internal
- 5) Internal timer 1000 ms

Firmware and Flow chart

Switching sequence matrix

The switching sequence is transferred to the multiplexer by USB port and internally stored for further uses. The switching sequence can be considered as a matrix where each row represents the state of all the slave boards. The transition between each row will be controlled by a switching event. The user can configure the row value and in practice no more than 32 rows will be necessary. For example, if 3 slave boards are connected in a 4 step process, the matrix is:

Table 6: binary switching sequence matrix for SPDT slave boards.

Step	Slave 1 Ch1	Slave 1 Ch2	Slave 2 Ch1	Slave 2 Ch2	Slave 3 Ch1	Slave 3 Ch2	Delay time (number of external trigger)
1	1	0	1	0	1	0	10
2	0	1	0	1	0	1	15
3	0	1	0	1	0	1	15
4	1	0	1	0	1	0	10

In the binary matrix one bit indicates the state of one channel, 0 indicates open and 1 indicates close. The matrix can be built with two bytes for channel states, so a total of 16 switches can be controlled, plus an extra byte to the numbers of clocks.

Byte 1:

S4-CH2	S4-CH1	S3-CH2	S3-CH1	S2-CH2	S2-CH1	S1-CH2	S1-CH1
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Byte 2:

				S6-CH2	S6-CH1	S5-CH2	S5-CH1
--	--	--	--	--------	--------	--------	--------

Byte 3: numbers of external trigger from 0 to 255

Remote operation

A trigger tree is considered to control the switching sequence, first the master board is armed and then, the state of the multiplexer channels change synchronized with the switching event. The arm and disarm message is provided by the PC. The switching event is defined as a trigger signal at trigger BNC plus a delay time based on integer numbers of trigger pulses. The following figure presents the trigger tree.

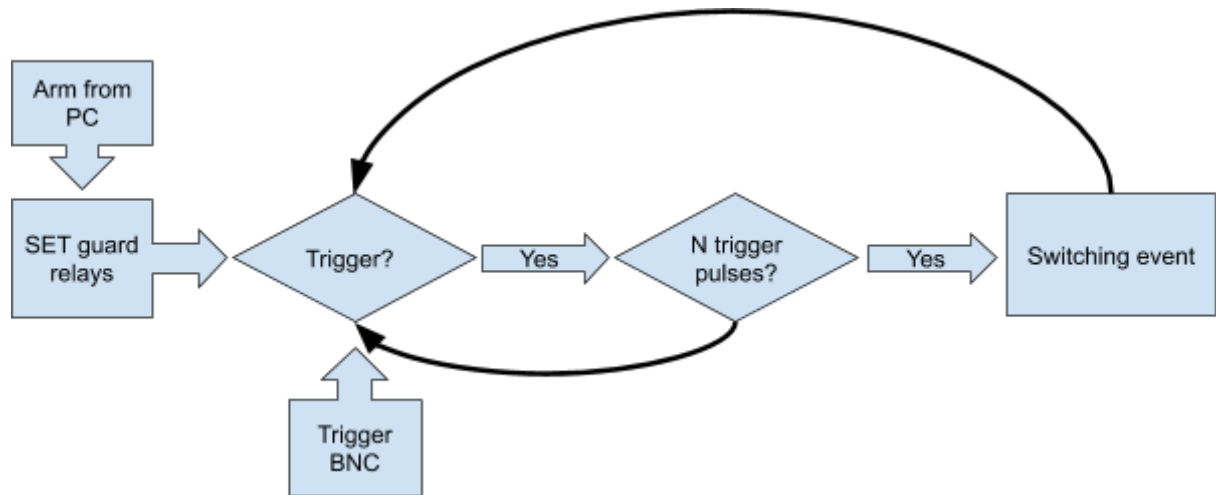


Figure 8: trigger tree, the Arm message is provided by PC and “N” is the number of external trigger pulses configured for each row in the matrix sequence.

Switching pseudocode

1. The PC configures the multiplexer and loads the switching matrix.
2. The PC arm the multiplexer.
3. The switches that connect the source guard are activated and they are not modified during the sequence.
4. The controller detects a trigger signal, the user can select positive or negative slopes.
5. The controller counts the numbers of pulses. When the configured value is reached the switching event is produced.
6. The controller writes FALSE on the “Ready for Trigger” bit.
7. Switching event (see figure 9):
 - a. All the switches are opened. (Signal relays and GND relays are opened)
 - b. An enable delay time is implemented to prevent a short circuit. The secure time is 2 times the turn-off time of the relay. It is defined as **#define ENA_DELAY** in millisecond.
 - c. The corresponding signal relays are configured based on the corresponding row of the sequence matrix.
 - d. The GND switches of the OFF channels are activated to improve Off-Isolation.
 - e. A counter to indicate the following matrix row is incremented.
8. The controller returns to point 4 and writes TRUE on the “Ready for Trigger” bit.
9. If a disarm command is received the controller returns to configuration state.

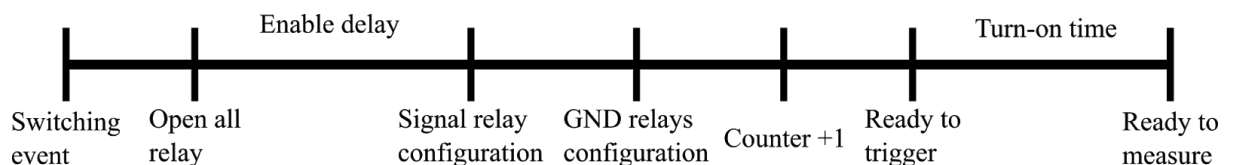


Figure 9: time diagram of the operations after switching event, items 7 a to 7 e. The Enable delay must be larger than the maximum turn-off time of the relay.

Local operation

The multiplexer can be configured on local operation. The button “ENA CH” runs the sequence step by step, each time that the user pushes the button the multiplexer changes the state following the sequence matrix, which must be previously loaded or the default sequence will be used.

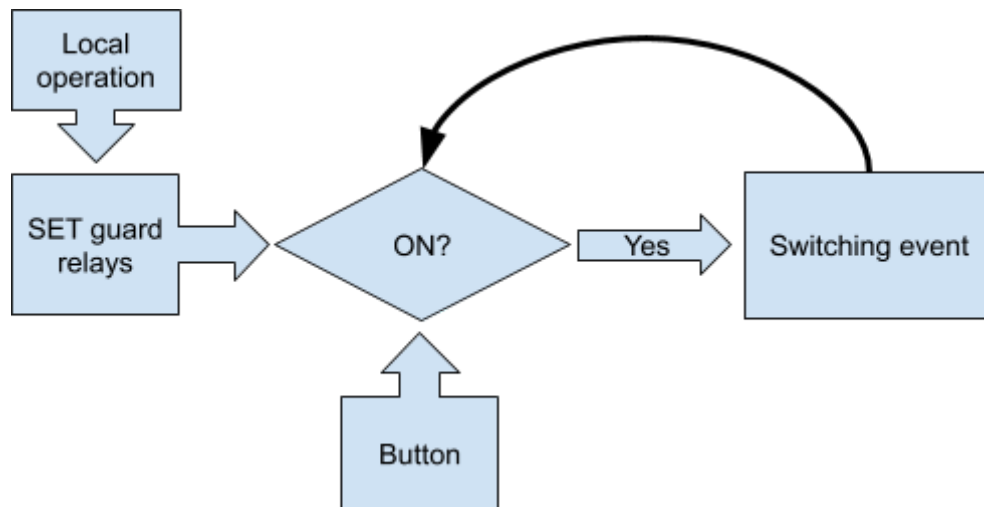


Figure 10: in local operation, the multiplexer changes between the matrix rows when the user pushes the “ENA CH” button.

Installation and connections

All the boards are designed to be fixed in a standard 19" case with a height of 3U (127 mm). The following figure shows one possible configuration with three SPDT slave boards.

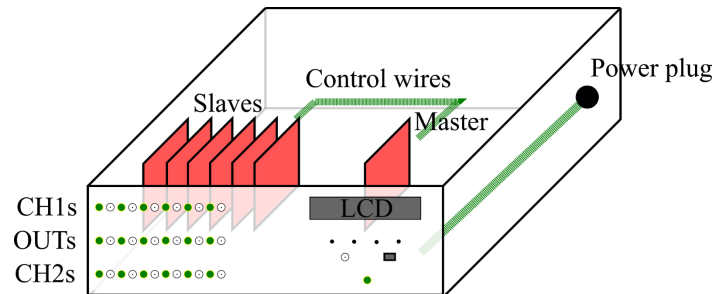


Figure 11: recommended configuration of the case for SPDT slave boards.

Each slave can be connected to the front panel by means of coaxial wire for signals and unipolar wire for guard and ground. The guard voltage provides a shield ring around the inputs and the outputs, they help to reduce the stray capacitance between signals. The ground voltage is connected to the middle point of the T-configuration during turn-off state. In order to obtain high off-isolation, the ground terminal must be the source GND and it must be connected by means of a low impedance wire.

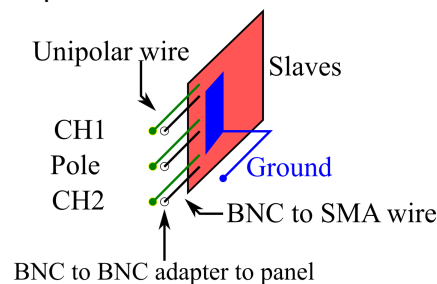


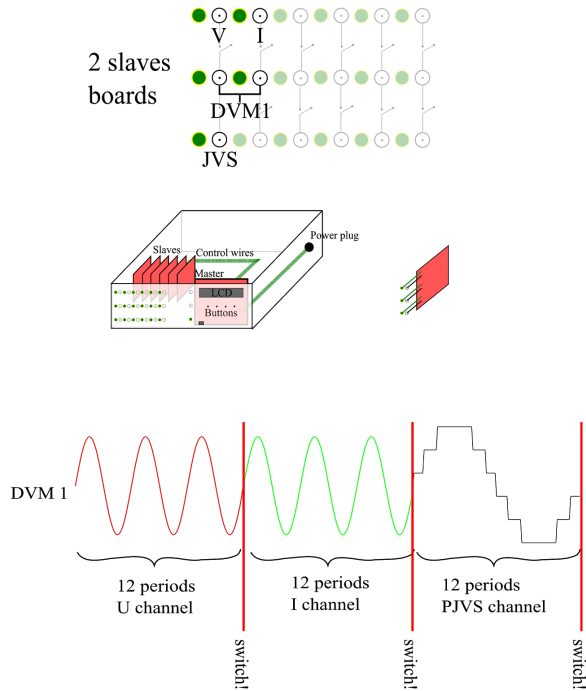
Figure 12: connection diagram of the SPDT slave board.

The following figures show possible connections for the 2-to-1 board and the 4-to-1 board, and for different cases: 1, 2 and 3 multimeters.

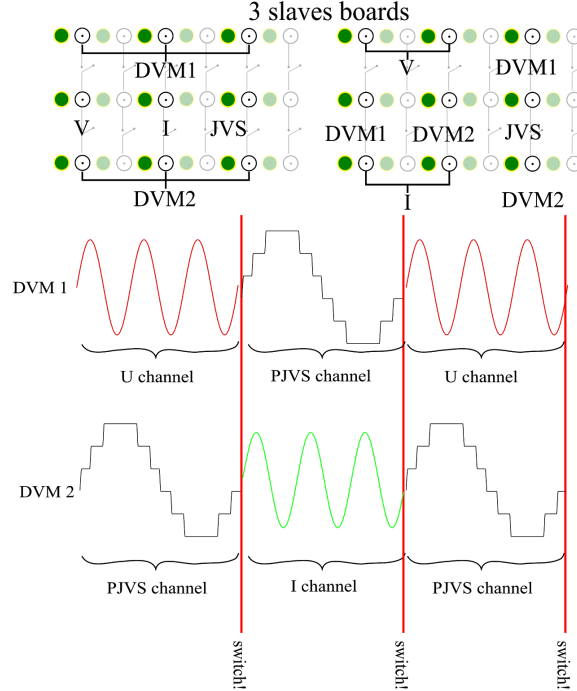
We also include the connection for the DC voltage measurement by differential method with the JVS.

In all the cases, the diagram shows all the allowed slaves boards and the shadow BNCs are not used in that connection.

1 PJVS, 1 DVM, <33% of U/I waveforms sampled



1 PJVS, 2 DVM. <50 % of U/I waveforms sampled



1 PJVS, 3 DVM. 100 % of U/I waveforms sampled

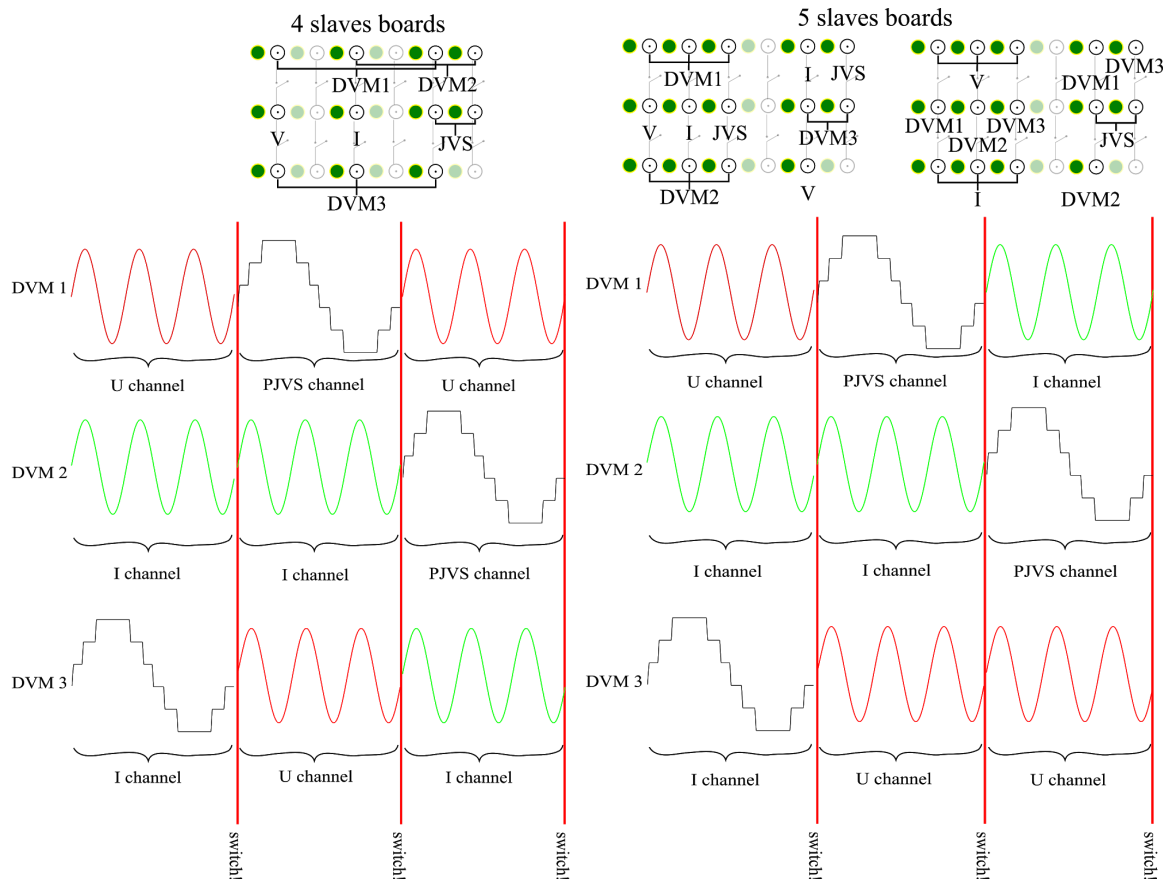


Figure 13: connection diagram for 1, 2 and 3 multimeter for SPDT (2-to-1) slaves board.

1 PJVS, 1 DVM, differential DC measurement

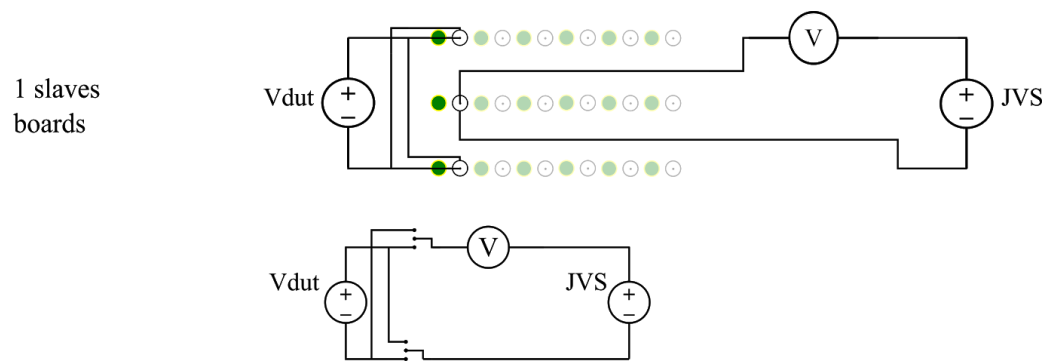


Figure 14: connection diagram for DC measurement with SPDT slave board.

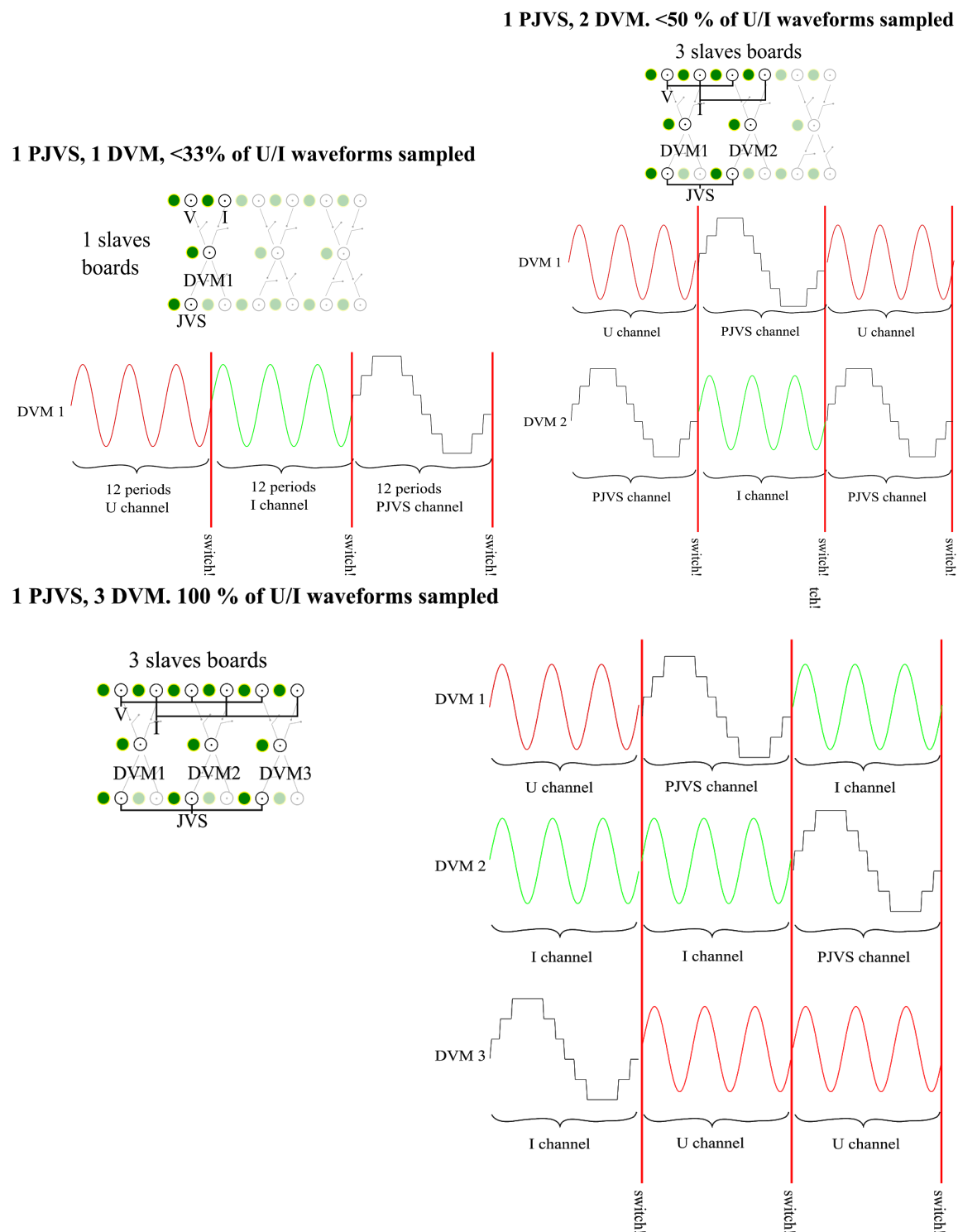


Figure 15: connection diagram for 1, 2 and 3 multimeter for SPFT (4-to-1) slaves board.

Test points list

Table 8: test points on the SPDT slave board.

Test points	Signal
0	GND Digital
1	CH02_ENA
2	CH01_GRD
3	CH02_GRD
4	CH02_GND
5	CH01_GND
6	CH01_ENA
7	VCC

List of resources

- User manual
- Schematic circuit in pdf format
- Gerber files
- List of components with RS-AMIDATA code
- Drawings/CAD of a suggested front panel
- Python test script
- Python simulator of the scanner.
File name "multiplexer_sim.py"
- Arduino firmware