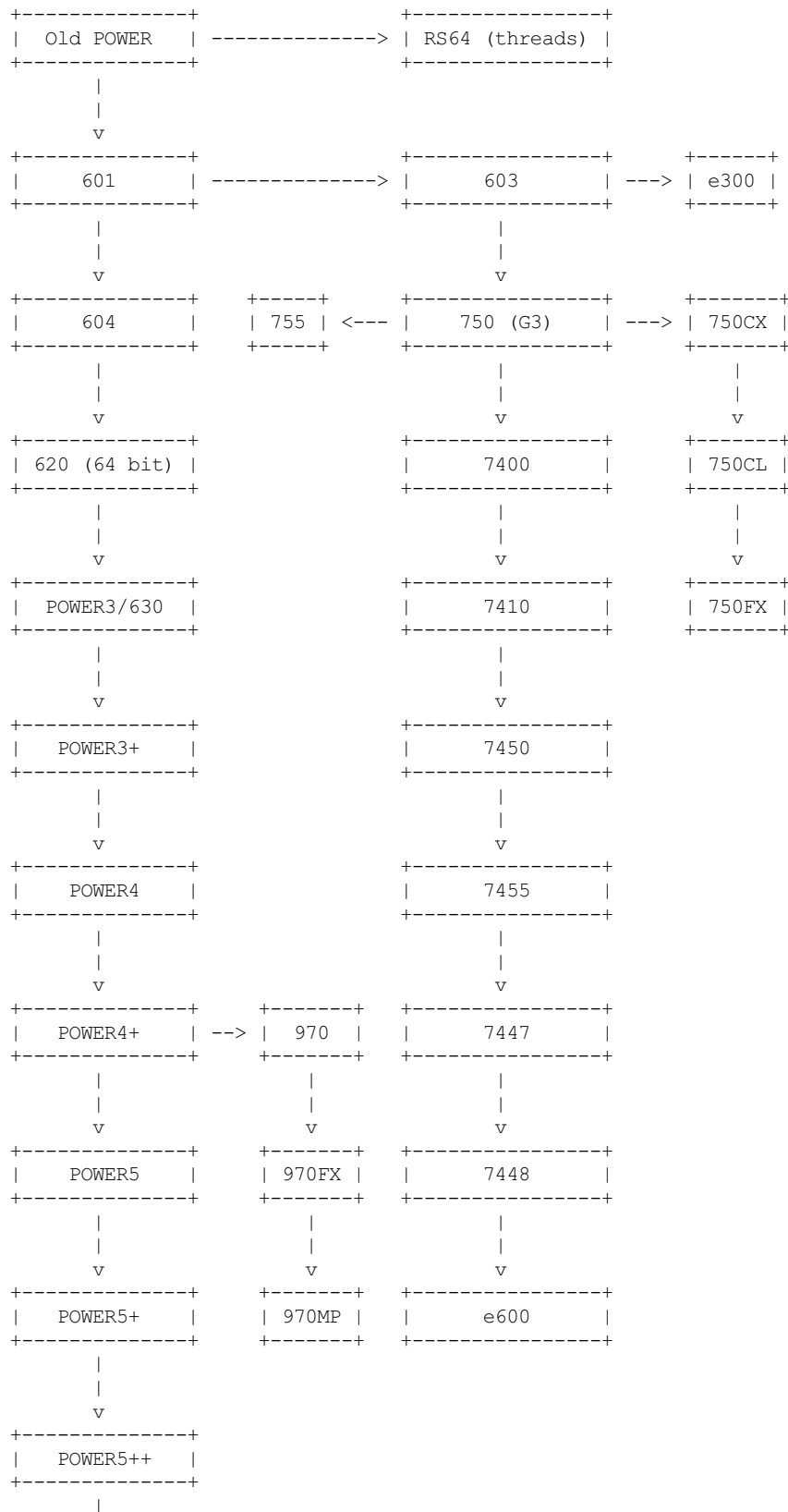


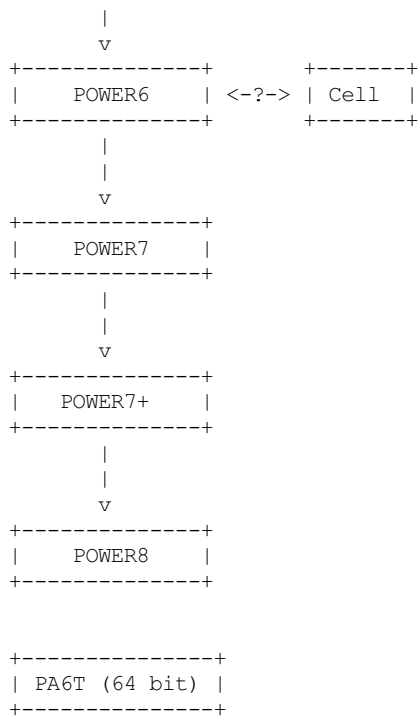
CPU Families

This document tries to summarise some of the different cpu families that exist and are supported by arch/powerpc.

Book3S (aka sPAPR)

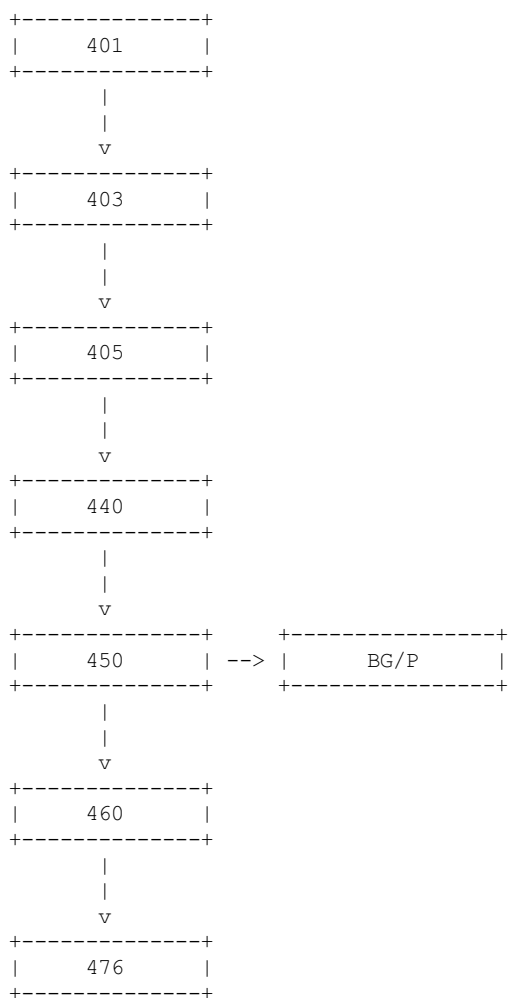
- Hash MMU (except 603 and e300)
- Software loaded TLB (603 and e300)
- Selectable Software loaded TLB in addition to hash MMU (755, 7450, e600)
- Mix of 32 & 64 bit:





IBM BookE

- Software loaded TLB.
- All 32 bit:



Motorola/Freescale 8xx

- Software loaded with hardware assist.
- All 32 bit:

```

+-----+
| MPC8xx Core |
+-----+

```

Freescal BookE

- Software loaded TLB.
- e6500 adds HW loaded indirect TLB entries.
- Mix of 32 & 64 bit:

```

+-----+
|   e200   |
+-----+

```

```

+-----+
|           e500           |
+-----+

```

```

|
|
v

```

```

+-----+
|       e500v2       |
+-----+

```

```

|
|
v

```

```

+-----+
|   e500mc (Book3e)   |
+-----+

```

```

|
|
v

```

```

+-----+
|   e5500 (64 bit)   |
+-----+

```

```

|
|
v

```

```

+-----+
| e6500 (HW TLB) (Multithreaded) |
+-----+

```

IBM A2 core

- Book3E, software loaded TLB + HW loaded indirect TLB entries.
- 64 bit:

```

+-----+ +-----+
|  A2 core  | --> |   WSP   |
+-----+ +-----+

```

```

|
|
v

```

```

+-----+
|   BG/Q   |
+-----+

```