DC Glossary

On this page, we try to keep track of acronyms related to the display component. If you do not find what you are looking for, look at the 'Documentation/gpu/amdgpu/amdgpu-glossary.rst'; if you cannot find it anywhere, consider asking in the amdgfx and update this page.

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.. glossary::

   ABM
     Adaptive Backlight Modulation

   APU
     Accelerated Processing Unit

   ASIC
     Application-Specific Integrated Circuit

   ASSR
     Alternate Scrambler Seed Reset

   AZ
     Azalia (HD audio DMA engine)

   BPC
     Bits Per Colour/Component

   BPP
     Bits Per Pixel

   Clocks
     * PCLK: Pixel Clock
     * SYMCLK: Symbol Clock
     * SOCCLK: GPU Engine Clock
     * DISPCLK: Display Clock
     * DPPCLK: DPP Clock
     * DCFCLK: Display Controller Fabric Clock
     * REFCLK: Real Time Reference Clock
     * PPLL: Pixel PLL
     * FCLK: Fabric Clock
     * MCLK: Memory Clock

   CRC
     Cyclic Redundancy Check

   CRTC
     Cathode Ray Tube Controller - commonly called "Controller" - Generates
     raw stream of pixels, clocked at pixel clock

   CVT
     Coordinated Video Timings

   DAL
     Display Abstraction layer

   DC (Software)
     Display Core

   DC (Hardware)
     Display Controller

   DCC
     Delta Colour Compression

   DCE
     Display Controller Engine

   DCHUB
     Display Controller HUB

   ARB
     Arbiter
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VTG
  Vertical Timing Generator

DCN
  Display Core Next

DCCG
  Display Clock Generator block

DDC
  Display Data Channel

DIO
  Display IO

DPP
  Display Pipes and Planes

DSC
  Display Stream Compression (Reduce the amount of bits to represent pixel
  count while at the same pixel clock)

dGPU
  discrete GPU

DMIF
  Display Memory Interface

DML
  Display Mode Library

DMCU
  Display Micro-Controller Unit

DMCUB
  Display Micro-Controller Unit, version B

DPCD
  DisplayPort Configuration Data

DPM(S)
  Display Power Management (Signaling)

DRR
  Dynamic Refresh Rate

DWB
  Display Writeback

FB
  Frame Buffer

FBC
  Frame Buffer Compression

FEC
  Forward Error Correction

FRL
  Fixed Rate Link

GCO
  Graphical Controller Object

GSL
  Global Swap Lock

iGPU
  integrated GPU

ISR
  Interrupt Service Request

ISV
  Independent Software Vendor

KMD
  Kernel Mode Driver

LB

Line Buffer

LFC
  Low Framerate Compensation

LTTPR
  Link Training Tunable Phy Repeater

LUT
  Lookup Table

MALL
  Memory Access at Last Level

MC
  Memory Controller

MPC
  Multiple pipes and plane combine

MPO
  Multi Plane Overlay

MST
  Multi Stream Transport

NBP State
  Northbridge Power State

NBIO
  North Bridge Input/Output

ODM
  Output Data Mapping

OPM
  Output Protection Manager

OPP
  Output Plane Processor

OPTC
  Output Pipe Timing Combiner

OTG
  Output Timing Generator

PCON
  Power Controller

PGFSM
  Power Gate Finite State Machine

PSR
  Panel Self Refresh

SCL
  Scaler

SDP
  Scalable Data Port

SLS
  Single Large Surface

SST
  Single Stream Transport

TMDS
  Transition-Minimized Differential Signaling

TMZ
  Trusted Memory Zone

TTU
  Time to Underflow

VRR
  Variable Refresh Rate

UVD