12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9230

FEATURES

- SNR = 64.9 dBFS @ f_{IN} up to 70 MHz @ 250 MSPS
- ENOB of 10.4 @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
- SFDR = −79 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
- Excellent linearity
  - DNL = ±0.3 LSB typical
  - INL = ±0.5 LSB typical
- LVDS at 250 MSPS (ANSI-644 levels)
- 700 MHz full power analog bandwidth
- On-chip reference, no external decoupling required
- Integrated input buffer and track-and-hold
- Low power dissipation
  - 434 mW @ 250 MSPS—LVDS SDR mode
  - 400 mW @ 250 MSPS—LVDS DDR mode
- Programmable input voltage range
  - 1.0 V to 1.5 V, 1.25 V nominal
- 1.8 V analog and digital supply operation
- Selectable output data format (offset binary, twos complement, Gray code)
- Clock duty cycle stabilizer
- Integrated data capture clock

APPLICATIONS

- Wireless and wired broadband communications
- Cable reverse path
- Communications test equipment
- Radar and satellite subsystems
- Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

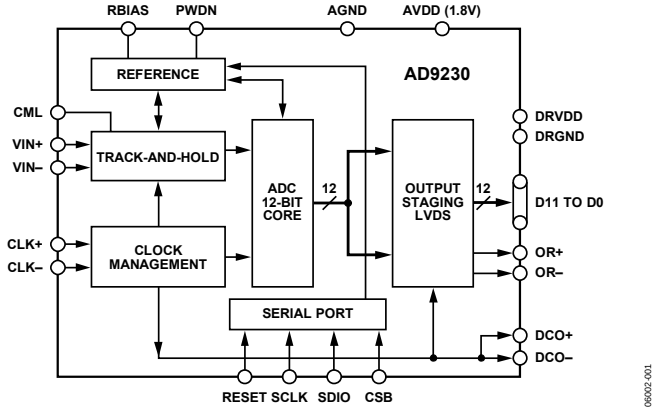

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead LFCSP, specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 434 mW @ 250 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample and hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—10-bit pin-compatible family offered as AD9211.

Rev. 0

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

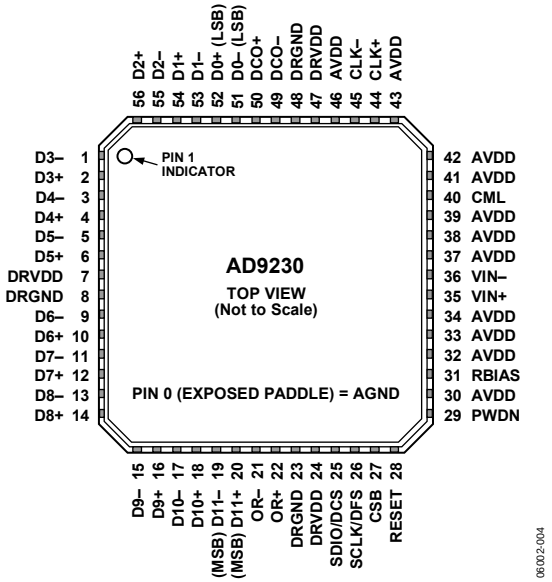

Figure 4. Single Data Rate Mode

Table 7. Single Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32 to 34, 37 to 39, 41 to 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND[1]	Analog Ground.
8, 23, 48	DRGND[1]	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI®) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0–	D0 Complement Output Bit (LSB).
52	D0+	D0 True Output Bit (LSB).
53	D1–	D1 Complement Output Bit.
54	D1+	D1 True Output Bit.
55	D2–	D2 Complement Output Bit.
56	D2+	D2 True Output Bit.
1	D3–	D3 Complement Output Bit.
2	D3+	D3 True Output Bit.
3	D4–	D4 Complement Output Bit.
4	D4+	D4 True Output Bit.