Overview

The IObundle ILA is a RISC-V-based Peripheral written in Verilog, which users can download for free, modify, simulate and implement in FPGA or ASIC. It is written in Verilog and includes a C software driver. The IObundle ILA is a very compact IP that works at high clock rates if needed. It supports full-duplex operation and a configurable baud rate. The IObundle ILA has a fixed configuration for the Start and Stop bits. More flexible licensable commercial versions are available upon request.

Features

- Supported in IObundle's RISC-V IOb-SoC open-source and free of charge template.
- IObundle's IOb-SoC native CPU interface.
- Verilog basic ILA implementation.
- Soft reset and enable functions.
- Runtime configurable
- C software driver at the bare-metal level.
- Simple Verilog testbench for the IP's *nucleus*.
- System-level Verilog testbench available when simulating the IP embedded in IOb-SoC.
- Simulation Makefile for the open-source and free of charge Icarus Verilog simulator.
- FPGA synthesis and implementation scripts for two FPGA families from two FPGA vendors.
- Automated creation of FPGA netlists
- Automated production of documentation using the open-source and free Latex framework.
- IP data automatically extracted from FPGA tool logs to include in documents.
- Makefile tree for full automation of simulation, FPGA implementation and document production.

Benefits

- Compact and simple hardware implementation
- Can fit many instances in low-cost FPGAs

Deliverables

- Verilog source code
- User documentation for easy system integration
- Example integration in IOb-SoC
- FPGA synthesis and implementation scripts

Block Diagram

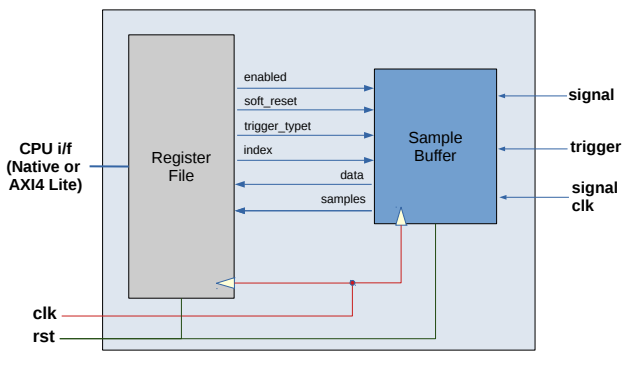

Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for two FPGA device families.

Resource	Used
LUTs	43
Registers	27
DSPs	0
BRAM	4

Resource	Used
ALM	28
FF	27
DSP	0
BRAM blocks	16
BRAM bits	131,072

Table 1: FPGA results for Kintex Ultrascale (left) and Cyclone V GT (right)

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.