Wireless Sensor Networks Environmental Monitoring

Specification V0.0

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1 Introduction

2 ADPLL

In this section the detailed specifications of the All-Digital Phase-Locked-loop (ADPLL) and its internal mixed-signal blocks are presented.

2.1 General specifications

The general specifications of the ADPLL block are given in Table 1.

	Spec	Notes
Ouput Frequency	X - X MHz	
Reference Frequency	32 MHz	
RX RMS Integrated Jitter	X ps	phase-noise integration
RX Integration Range	0.1-100 MHz	
RX Loop Bandwidth	X MHz	
TX Loop Bandwidth	X MHz	e
TX FSK error	X %	
Power Consumption	X mW	1.2 V supply
Area	X mm^2	

Table 1: General specfications.

2.2 Block diagram

The ADPLL is comprised of a digital core unit, a digital-controlled oscillator (DCO), a time-to-digital converter (TDC), and a clock retiming unit, as can be seen in Fig. 1.

Details about the TDC and the DCO blocks can be found in section 2.7 and 2.8, respectively.

The retiming unit synchronizes the DCO and adpll_ctr clock domains. This is achieved by oversampling of the FREF clock by the high-rate DCO clock. To reduce metastability issues, the retiming unit employs custom-designed flip-flops.

2.3 Interface signals

The ADPLL interface signals are shown in Table 2.

2.4 Memory mapped registers

The list of memory mapped registers is shown in Table 3.

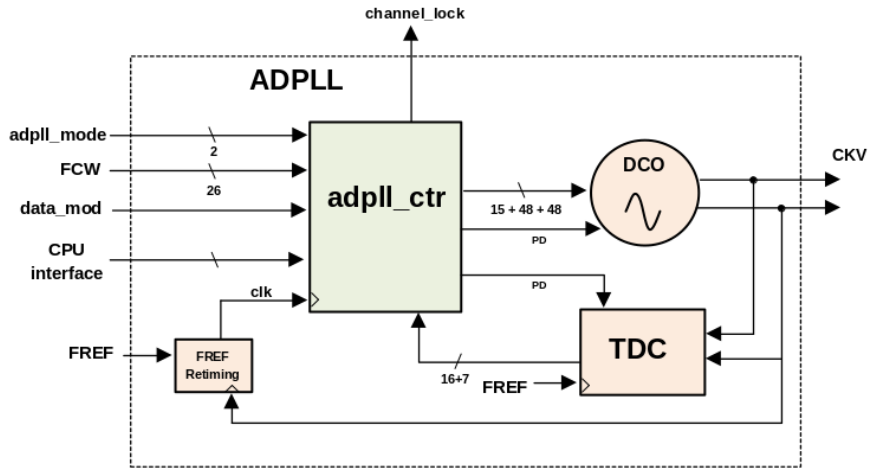

Figure 1: Diagram block

Name	Type	Direction	Width	Description
rst	digital	in	1	System reset
en	digital	in	1	System enable
clk	digital	in	1	32 MHz system clock
sel	digital	in	1	CPU interface
write	digital	in	1	CPU interface
address	digital	in	5	CPU interface
data_in	digital	in	32	CPU interface
ready	digital	out	1	CPU interface
FCW	digital	in	26	Channel frequency in MHz (Q12.14)
adpll_mode	digital	in	2	ADPLL operation mode
data_mod	digital	in	1	Data bit to modulated in TX mode
channel_lock	digital	out	1	Channel frequency locking flag
DVDD	analog		1	Digital core supply voltage
VDD_TDC	analog		1	TDC supply voltage
VDD_DCO	analog		1	DCO supply voltage
DGND	analog		1	Digital ground
GND	analog		1	Analog ground
IREF	analog		1	Analog reference current (5μA)
CKV_P	analog		1	DCO positive output
CKV_N	analog		1	DCO negative output

Table 2: Interface signals

2.5 Operation

The ADPLL performs two different tasks: RF channel frequency synthesis, and FSK modulation. While the former is required on both modes (TX and RX), the latter is only used in the TX mode. Table 4 shows all different operation modes that can be programmed according to the adpll_mode[1:0] input.

The operation of the adpll_ctr module is shown in Fig. 2, by means of its state flowchart state diagram. After the initial system reset and enable activation, the controller is in the IDLE state, remaining here if the ADPLL operation mode is PD or TEST. Otherwise, it goes to the PU state in the next CLK cycle. In the PU state, the controller successively powers up the DCO and TDC. After 32 clk cycles (3 μs), the controller enters into the

Name	Read/ Write	Address	Width	Description	Default after rst
ALPHA_L	write	0	4	Proportional gain in C_L state	14
ALPHA_M	write	1	4	Proportional gain in C_M state	8
ALPHA_S_RX	write	2	4	Proportional gain in C_S state and RX mode	7
ALPHA_S_TX	write	3	4	Proportional gain in C_L state and TX mode	4
BETA	write	4	4	Integral gain in RX mode	0
LAMBDA_RX	write	5	3	1st order IIR LPF coeficient in RX mode	2
LAMBDA_TX	write	6	3	1st order IIR LPF coeficient in TX mode	2
IIR_N_RX	write	7	2	Number of 1st order IIR LPFs in RX mode	3
IIR_N_TX	write	8	2	Number of 1st order IIR LPFs in TX mode	2
FCW_mod	write	9	5	FSK modulation freq deviation (lsb=32kHz)	9
DCO_C_L_WORD_TEST	write	10	5	DCO Large Cap bank control signed word	0
DCO_C_M_WORD_TEST	write	11	8	DCO Medium Cap bank control signed word	0
DCO_C_S_WORD_TEST	write	12	8	DCO Small Cap bank control signed word	0
DCO_PD_TEST	write	13	1	DCO power down in TEST mode	1
TDC_PD_TEST	write	14	1	TDC power down in TEST mode	1
TDC_PD_INJ_TEST	write	15	1	TDC injection-locking power down in TEST mode	1
TDC_CTR_FREQ	write	16	3	TDC ring oscillator control frequency	4
DCO_OSC_GAIN	write	17	3	DCO oscillator control gm	2
ADPLL_SOFT_RST	write	18	3	ADPLL soft reset	0

Table 3: List of meory mapped registers

adpll_mode[1:0]	Mode	Description
0	PD	Power down
1	TEST	Test mode where TDC and DCO blocks can be controlled via CPU
2	RX	Synthetizes FCW using the ADPLL receiver filtering response
3	TX	Synthetizes FCW using the ADPLL transmitter filtering response, after the channel lock flag goes high, the input data_mod bit is synthetized at 1 MHz rate

Table 4: Operation modes

C_L state. This state selects the command word of the large capacitor bank that generates the closest output frequency to the target frequency. The transition to C_M state takes place when an internal flag (lock_detect) goes up. The C_M state operates similarly to the C_L state but acting on the medium capacitor bank. Once locked, the controller goes to the C_S state. This state gives the finest resolution by acting on the small capacitor bank during 480 clk cycles (15 μs). After that, the channel_lock output flag is activated meaning that the channel tracking is completed. In the case of RX mode operation, the controller continuous the channel frequency tracking, otherwise, it performs data modulation within the channel (TX mode operation).

Fig. 3 shows the block diagram of the filters in the loop. In the RX mode, a proportional filter and integral filter, as well as a cascade of first-order LPF IIR filters, can be selected and programmed. The same filters are available in the TX mode, with the exception of the integral one.

In the case of TEST mode selection, the TDC and DCO are power-down, ready to be fully controlled by the CPU.

Note that whenever the FCW or the adpll_mode input words are changed, the ADPLL returns to the IDLE

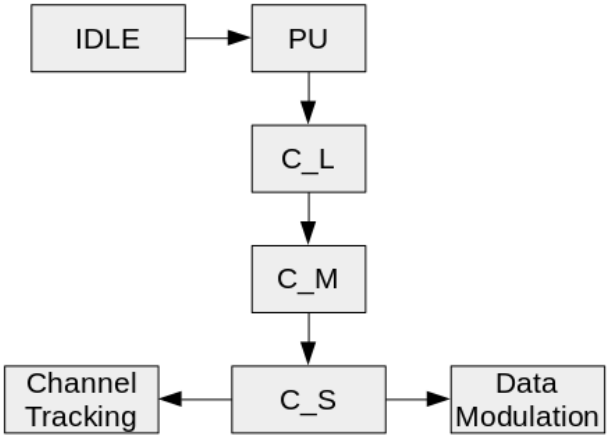

Figure 2: ADPLL state flowchart

state.

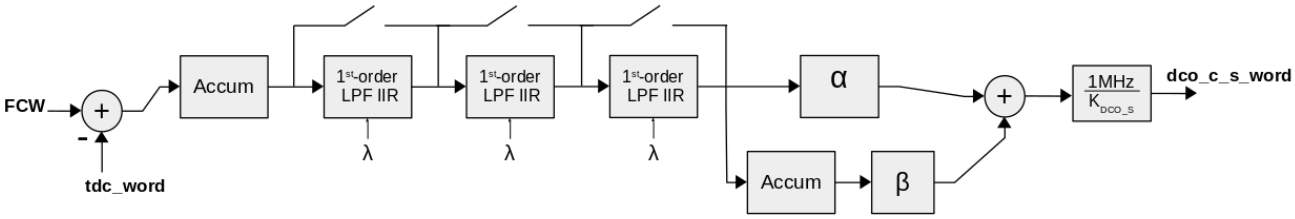

Figure 3: ADPLL filters block diagram

2.6 ADPLL Controller

2.6.1 Interface signals

The interface signals of the adpll_ctr module are shown in Table 5.

2.7 Time-to-Digital Converter

A TDC plays a major role in digital PLLs since converts the local oscillator output frequency into a digital word that is processed by the PLL unit control. This is a high-resolution TDC suitable for digital PLLs operating in the

Name	Type	Direction	Width	Description
rst	digital	in	1	System reset
en	digital	in	1	System enable
clk	digital	in	1	32 MHz system clock
sel	digital	in	1	CPU interface
write	digital	in	1	CPU interface
address	digital	in	5	CPU interface
data_in	digital	in	32	CPU interface
ready	digital	out	1	CPU interface
FCW	digital	in	26	Channel frequency in MHz (Q12.14)
adpll_mode	digital	in	2	ADPLL operation mode
data_mod	digital	in	1	Data bit to modulated in TX mode
channel_lock	digital	out	1	Channel frequency locking flag
dco_pd	digital	out	1	DCO power-down
dco_osc_gain	digital	out	2	DCO gm control
dco_c_l_rall	digital	out	5	DCO large cap bank full row control
dco_c_l_row	digital	out	5	DCO large cap bank row control
dco_c_l_col	digital	out	5	DCO large cap bank column control
dco_c_m_rall	digital	out	8	DCO medium cap bank full row control
dco_c_m_row	digital	out	8	DCO medium cap bank row control
dco_c_m_col	digital	out	8	DCO medium cap bank column control
dco_c_s_rall	digital	out	8	DCO small cap bank full row control
dco_c_s_row	digital	out	8	DCO small cap bank row control
dco_c_s_col	digital	out	8	DCO small cap bank column control
tdc_pd	digital	out	1	TDC power-down
tdc_pd_inj	digital	out	1	TDC injection-locking power-down
tdc_ctr_freq	digital	out	3	TDC ring oscillator frequency control
tdc_ripple_count	digital	in	7	RF ripple counter output
tdc_phase	digital	in	16	TDC ring oscillator phases

Table 5: Controller interface

2-3 GHz frequency band. The TDC employs a novel circuit topology that allows wide range injection-locking (more than 1 GHz) without compromise the TDC DNL.

2.7.1 Interface signals

The TDC interface signals are shown in Table 6.

The TDC employs a ring oscillator that requires an initial settling time at the time the TDC is powered up. At the worst PVT case, simulation results show an RO initial settling time of about 300 ns. Thus, it is recommended to wait for at least 300 ns before the injection of an external RF input signal. After the signal injection activation , it is recommended to wait for at least 100 ns plus five CLK cycles in order to get a valid tdc output word.

Name	Type	Direction	Width	Description
tdc_pd	digital	in	1	TDC power-down
tdc_pd_inj	digital	in	1	TDC injection-locking power-down
clk	digital	in	1	32 MHz system clock
tdc_ctr_freq	digital	in	3	TDC ring oscillator frequency control
tdc_ripple_count	digital	out	7	RF ripple counter output
tdc_phase	digital	out	16	TDC ring oscillator phases
DVDD	analog		1	Digital core supply voltage
VDD	analog		1	TDC supply voltage
DGND	analog		1	Digital ground
GND	analog		1	Analog ground
IREF	analog		1	Analog reference current (5μA)
INJ_P	analog		1	DCO positive output injector
INJ_N	analog		1	DCO negative output injector

Table 6: TDC interface signals

2.8 Digital-Controlled Oscillator

2.8.1 Interface signals

The DCO interface signals are shown in Table 7.

Name	Type	Direction	Width	Description
pd	digital	in	1	DCO power-down
dco_osc_gain	digital	in	2	DCO gm control
dco_c_l_rall	digital	in	5	DCO large cap bank full row control
dco_c_l_row	digital	in	5	DCO large cap bank row control
dco_c_l_col	digital	in	5	DCO large cap bank column control
dco_c_m_rall	digital	in	8	DCO medium cap bank full row control
dco_c_m_row	digital	in	8	DCO medium cap bank row control
dco_c_m_col	digital	in	8	DCO medium cap bank column control
dco_c_s_rall	digital	in	8	DCO small cap bank full row control
dco_c_s_row	digital	in	8	DCO small cap bank row control
dco_c_s_col	digital	in	8	DCO small cap bank column control
VDD	analog		1	DCO supply voltage
GND	analog		1	Analog ground
IREF	analog		1	Analog reference current (5μA)
CKV_P	analog		1	DCO positive output
CKV_N	analog		1	DCO negative output

Table 7: DCO interface signals

References